SSI 32D534A
Data Synchronizer/ MFM ENDEC

Preliminary Data

July, 1990

DESCRIPTION

The SSI 32D534A Data Synchronizer/MFM ENDEC is intended to provide data recovery and data encoding in storage systems which employ an MFM encoding format. Data synchronization is performed with a fully integrated high performance PLL and encoding is performed in soft/hard sector formats with optional write precompensation through the internal delay line. The SSI 32D534A has been optimized for operation as a companion device to the SSI 32C452 and the AIC 010 family of controllers. The frequency setting elements are incorporated within the SSI 32D534A for enhanced performance and reduced board space. Data rate, adjustable from 5 to 10 Mbit/s, is established with a single external programming resistor for Direct Sync operation or with two external resistors for Auto Sync operation.

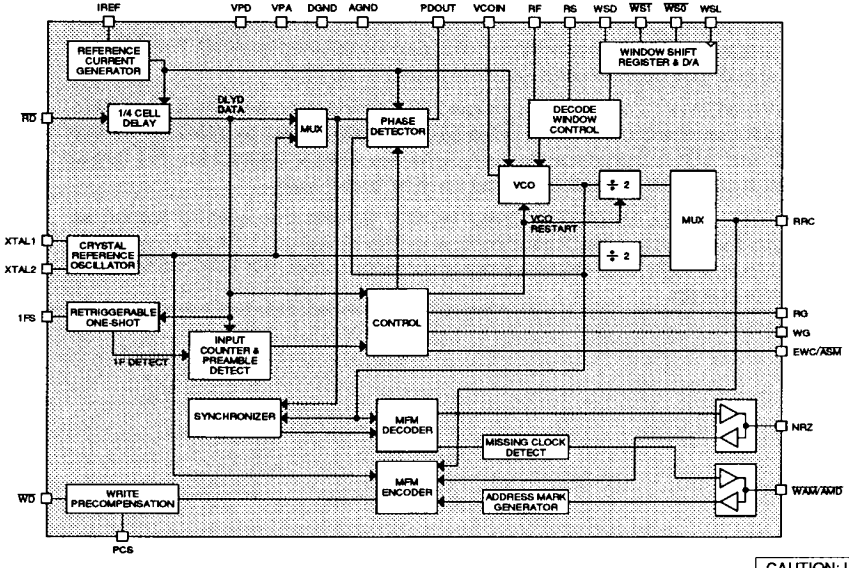
The SSI 32D534A utilizes an advanced bipolar process technology that affords precise decode window control without the requirement of an accurate 1/4 cell

(Continued)

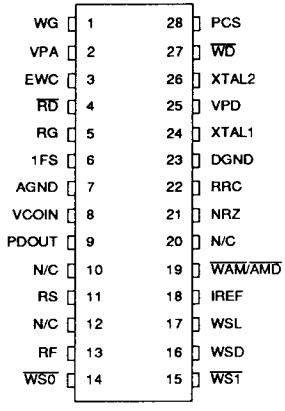
FEATURES

- **Data Synchronizer and MFM ENDEC**
- **5 to 10 Mbit/s operation programmed with a single external resistor**
- **Optimized for operation with the SSI 32C452 and AIC 010 family of controllers**
- **Programmable decode window symmetry via a µP port and/or analog pins**
- **Programmable write precompensation**
- **Fast acquisition phase locked loop - zero phase restart technique**
- **Fully integrated data separator - no external delay lines or active devices required**
- **+5V operation**
- **28-pin DIP and PLCC packages**

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (Continued)

delay or external devices. To enhance disk drive testability, decode window symmetry control is available through a digital microprocessor port and/or two analog pins. This feature can facilitate automatic calibration, systematic error cancellation, and window margin testing. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D534A requires a single +5V power supply and is available in 28-pin DIP and PLCC packages.

PIN DESCRIPTION

INPUT PINS

NAME	DESCRIPTION
$\overline{RD}$	READ DATA. MFM encoded Read Data from the disk drive read channel, active low.
RG	READ GATE. Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the $\overline{RD}$ input and enables the Read Mode/Address Mark Detection sequences. A low level selects the crystal reference oscillator. Pin RG has an internal resistor pull up.
WG	WRITE GATE. Enables the write mode. Pin WG has an internal resistor pull up. If unused, tie pin low.
WSL	WINDOW SYMMETRY LATCH. Used to latch the input window symmetry control bits WSD, $\overline{WS0}$ and $\overline{WS1}$ into an internal DAC. An active high level latches the input bits. Pin WSL has an internal resistor pull up. If unused, tie pin low.
WSD	WINDOW SYMMETRY DIRECTION. Controls the direction of the optional window symmetry shift. Pin WSD has an internal resistor pull up.
$\overline{WS0}$	WINDOW SYMMETRY CONTROL BIT. A low level introduces a window shift of 1.5% of TORC (Read Reference Clock Period) in the direction established by WSD. Pin $\overline{WS0}$ has an internal resistor pull up. If unused, leave pin open or tie high.
$\overline{WS1}$	WINDOW SYMMETRY CONTROL BIT. A low level introduces a window shift of 6% of TORC (Read Reference Clock Period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull up. If unused, leave pin open or tie pin high.
EWC/$\overline{ASM}$	ENABLE WRITE PRECOMP/AUTO SYNC MODE. Selects the synchronization sequence required in order to enter Read Mode, a low level selects the Auto Sync Mode. In the Write Mode, a high level enables write precompensation. Pin EWC/$\overline{ASM}$ has an internal resistor pull up.

PIN DESCRIPTION (Continued)

OUTPUT PINS

NAME	DESCRIPTION
$\overline{WD}$	WRITE DATA. MFM encoded write data output, active low. Precompensation is enabled with the EWC/$\overline{ASM}$ input pin.
RRC	READ/REFERENCE CLOCK. A multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.

BIDIRECTIONAL PINS

NRZ	NRZ DATA PORT. Read data output when RG is high and write data input when WG is high. In the idle mode, NRZ is in a high impedance state.
$\overline{WAM/AMD}$	WRITE ADDRESS MARK/ADDRESS MARK DETECT. In the Write Mode, used to delete clock/data pulses in the MFM encoded output stream, $\overline{WD}$, active low. In the Read Mode, a latched low level output indicates that an address mark has been detected. In idle mode, $\overline{WAM/AMD}$ is in a high impedance state.

ANALOG PINS

IREF	TIMING PROGRAM PIN. The VCO center frequency and the 1/4 cell delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected from IREF to VCC.
XTAL1, XTAL2	CRYSTAL OSCILLATOR CONNECTIONS. If a crystal oscillator is not desired, XTAL1 may be driven by a TTL signal with XTAL2 open. The frequency must be at twice the data rate.
PD OUT	PHASE DETECTOR OUTPUT. Drives the Loop Filter input.
VCO IN	VCO CONTROL INPUT. Driven by the Loop Filter output.
1FS	1F DETECT SET. Used to program the 1F detect timing with an external resistor, RT, connected from pin 1FS to ground. The 1F Detect period is the sum of the 1/4 cell delay, TQC, plus the Retriggerable One-Shot delay, TOS, which is normally set to 1 1/4 bit cell times.
RF, RS	WINDOW SYMMETRY ADJUST PINS. Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to ground will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, WS0, and WS1.
PCS	PRECOMP SET. Pin for R-C network to program write precompensation early and late times. Connect the capacitor, CPC, to VPA and the resistor, RPC, to either ground.
VPD, VPA	DIGITAL and ANALOG +5V.
DGND, AGND	DIGITAL and ANALOG GROUND.

SSI 32D534A
Data Synchronizer/
MFM ENDEC

FUNCTIONAL DESCRIPTION

The SSI 32D534A, a high performance data synchronizer and MFM ENDEC, performs data separation, data encoding with optional write precompensation, Preamble detection, and Write Address Mark/Address Mark detection. The interface electronics and the architecture of the SSI 32D534A has been optimized for use as a companion device to the SSI 32C452 or AIC 010 type Storage Controllers. It includes a zero phase restart PLL for fast acquisition, a crystal reference oscillator, the write precompensation delay line, a multiplexed Read/Reference clock output, and a bidirectional NRZ data interface.

Data rate is programmed with a single 1% external resistor, RR, connected from pin IREF to VCC, given by:

$$RR = \frac{30.67}{DR} - 0.5\ (k\Omega)$$

Where: DR = Data Rate in Mbit/s
RR = kΩ

Resistor RR establishes a reference current which controls the VCO center frequency, the phase detector gain, the 1/4 cell delay and, indirectly, the decode window shift (RF, RS).

The internal crystal reference oscillator, operating at twice the data rate, generates the standby reference input to the PLL. This minimizes the frequency step and the associated acquisition time encountered when locking the PLL onto Encoded Read Data. Additionally, in non-Read modes the RRC (Read Reference Clock) output is generated from the reference oscillator divided by two. A series resonant crystal at twice the data rate should be used. If a crystal oscillator is not desired, an external TTL compatible reference may be applied to XTAL1 with XTAL2 open.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input, a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

The SSI 32D534A provides two sync modes for controlling the PLL locking sequence, Auto Sync and Direct Sync. The Auto Sync mode provides preamble search and address mark detection while the Direct Sync mode provides direct control over the input to the PLL. These modes extend the applicability of the SSI 32D534A to a variety of controller and interface requirements. The appropriate mode should be selected for the given application, see Table 1.

TABLE 1: Mode Control

MODE	WG	RG	EWC/ $\overline{ASM}$
Idle	0	0	X
Read (Auto Sync)	0	1	0
Read (Direct Sync)	0	1	1
Write (Disable Precomp)	1	0	0
Write (Enable Precomp)	1	0	1
Illegal	1	1	X

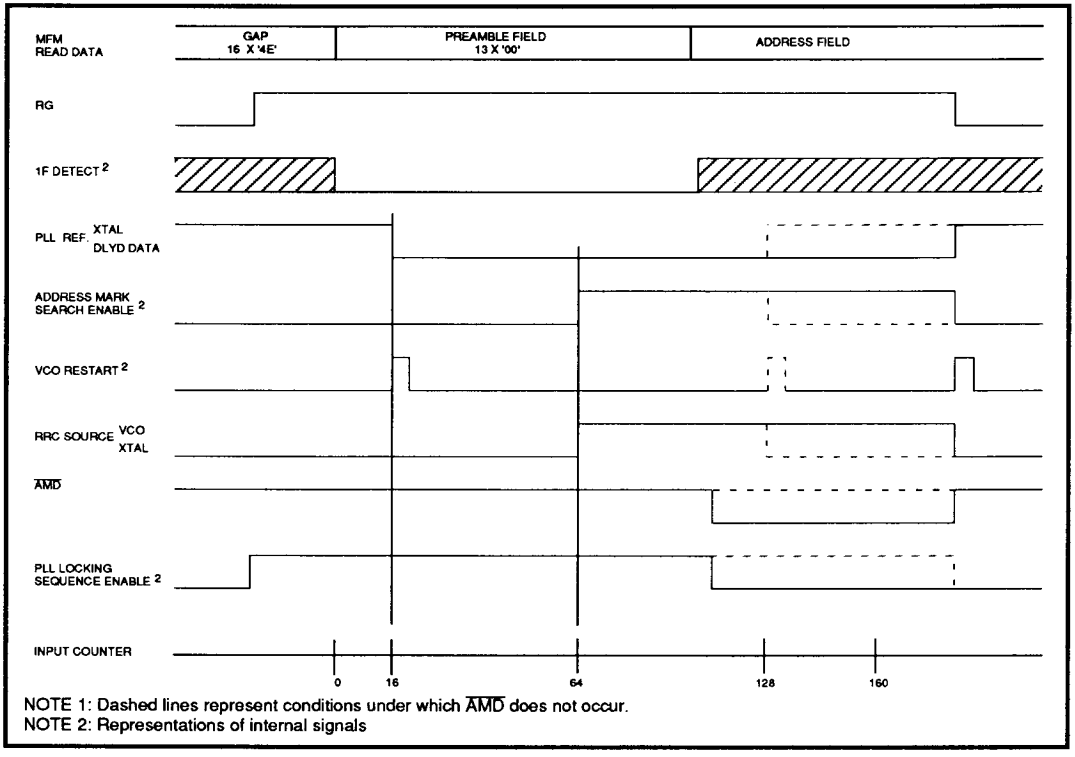
(X = Don't Care)

AUTO SYNC MODE

The Auto Sync mode, typically used for Soft Sector formats, activates the preamble search and address mark detection circuitry. As depicted in Figure 1, the SSI 32D534A requires16 continuous preamble bits before switching the reference input to the PLL, 64 preamble bits before switching the Read Reference Clock to the VCO clock divided by two, and a detected address mark prior to an additional 64 input bits in order to enter the Read Mode. This sequence repeats after 160 input bits until Read mode is successfully entered or until RG is cancelled.

When RG transitions high, the following PLL locking sequence begins:

a) PREAMBLE SEARCH: The SSI 32D534A searches for 16 continous preamble bits. The Preamble fields consist of a stream of MFM encoded 0's. The sum of the delays from the Re-



NOTE 1: Dashed lines represent conditions under which $\overline{AMD}$ does not occur.
NOTE 2: Representations of internal signals

FIGURE 1: Auto Sync Mode Waveform Diagram

triggerable One Shot, TOS, and the 1/4 Cell Delay, TQC, is set to 1 1/2 bit cell times with the external programming resistor, RT. The Preamble stream has a pulse rate of 1 bit cell time (2F frequency) which continuously resets the one-shot while a 2 bit cell period (1F frequency) allows the one-shot to time out producing a 1F detect pulse. The 1F detect pulse resets the Input counter and the search is started over.

b) PLL ACQUISITION: When 16 continuous preamble '0' bits are detected, the reference input to the PLL is switched from the crystal reference oscillator to the DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, PLL acquisition begins, and the VCO clock divider is reset. When 64 '0' preamble bits are detected, the Read Reference Clock output (RRC) is switched to the VCO clock divided by 2, and the Address Mark Detection circuitry is enabled. If a 1F detect pulse occurs before 64 preamble bits are detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, the Input Counter is reset, and the sequence is restarted. No short duration glitches will occur during this switching.

c) ADDRESS MARK DETECTION: The circuit searches for the occurrence of the Address Mark. The 1F detect circuitry remains active so that, during the search, once a 1F is detected, the Address Mark must be found within the next five counts of the Read Data input pulses. If an Address Mark is detected, prior to the Input Counter reaching count 128, the $\overline{WAM}/\overline{AMD}$ output is latched low, the PLL training sequence is terminated, and the Read Mode is entered allowing the

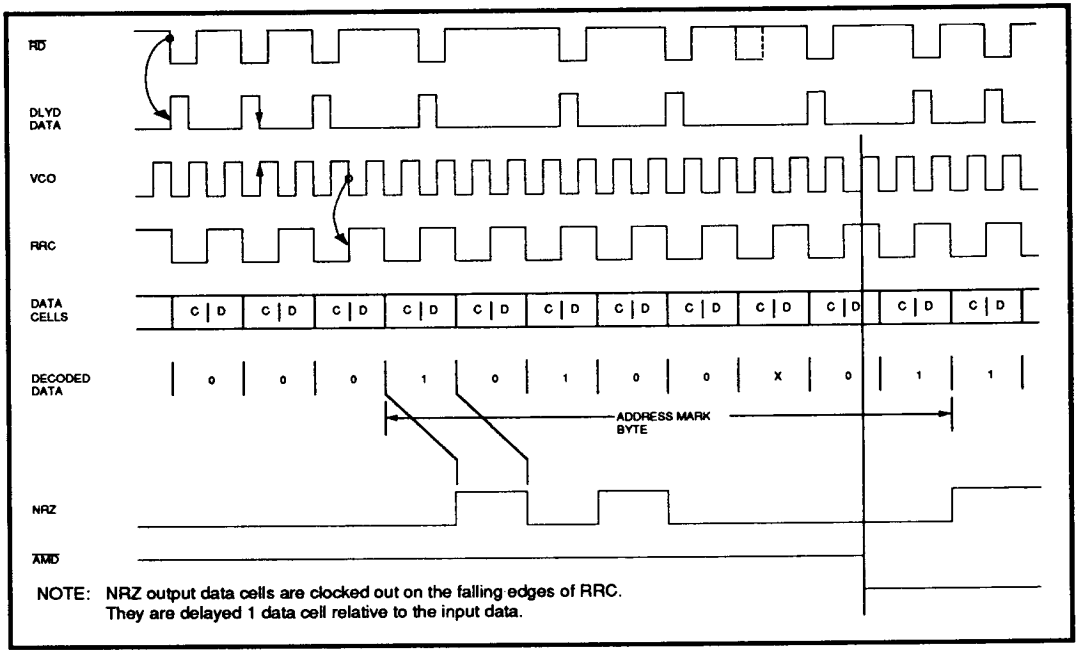


FIGURE 2: Address Mark Detection and NRZ Waveform Diagram

AUTO SYNC MODE (Continued)

data field to be read. If the input counter reaches count 128 before the Address Mark is detected, the PLL is locked back to the crystal reference oscillator, the RRC output is switched to the crystal reference oscillator divided by 2, and the PLL training sequence is restarted when the Input Counter reaches count 160. Figure 2 depicts the Address Mark detection sequence.

DIRECT SYNC MODE

Direct Sync Mode disables the preamble search and address mark detection circuitry. It allows the PLL to be controlled directly by RG, for Hard Sector format operation.

When RG transitions high, the reference input to the PLL is switched from the crystal reference oscillator to DLYD DATA, the VCO is phase reset to the next DLYD DATA pulse, PLL acquisition begins, the VCO clock divider is reset, and the RRC output is switched to the VCO clock divided by 2.

Read Gate, RG, is an asynchronous input and may be initiated or terminated at any position on the disk. Terminating RG locks the PLL to the crystal reference oscillator and switches the RRC output to the crystal reference oscillator divided by 2.

In non-Read modes the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency that is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily and then restarted in an accurate phase alignment with the next PLL reference input pulse and the VCO clock divider is reset. By minimizing the phase misalignment in this manner (phase error $\leq \pm 0.5$ rads), the acquisition time is substantially reduced.

The SSI 32D534A employs a dual mode phase detector; harmonic in Read mode and non-harmonic in Idle/Write modes. The harmonic phase detector only up-

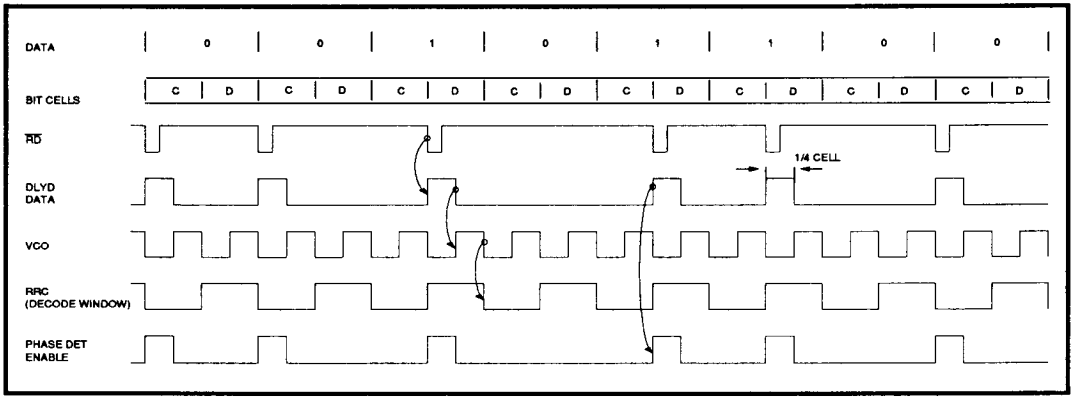
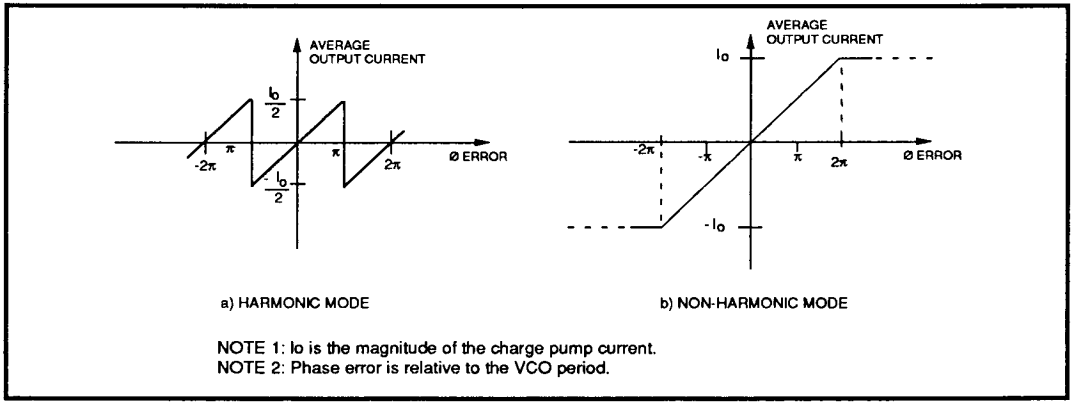


FIGURE 3: Data Synchronization Waveform Diagram

DIRECT SYNC MODE (Continued)

dates the PLL with each occurrence of a DLYD DATA pulse. This allows the PLL to remain phase locked to actual Read Data. The rising edge of DLYD DATA enables the phase detector and the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 3, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. In Idle/Write modes, both phase and frequency lock (non-harmonic) to the crystal reference oscillator is accomplished by continuously enabling the phase detector. With both phase and frequency lock to the crystal reference oscillator and the zero phase restart acquisition technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as a function of the input phase error (relative to the VCO period).



NOTE 1: Io is the magnitude of the charge pump current.
NOTE 2: Phase error is relative to the VCO period.

FIGURE 4: Phase Detector Transfer Function

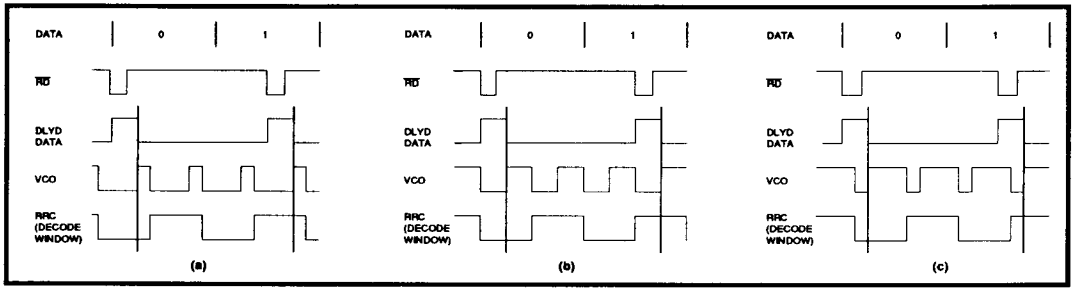


FIGURE 5: Decode Window a) Early, b) Normal, c) Late

DIRECT SYNC MODE (Continued)

An accurate and symmetrical decode window is developed from the VCO clock. The rising edges of the VCO clock are phase locked to the falling edges of DLYD DATA as shown in Figure 3. The decode window is then generated from the falling edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, the decode window is ensured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port (WSL, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2.

Window shifts in the range of ±1.5% to ±7.5% of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 5. For applications not utilizing this feature, WSL should be tied to ground, while WSD, $\overline{WS0}$ & $\overline{WS1}$ should be left floating. Additionally, for small systematic error cancellation a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, Tsa, is determined by :

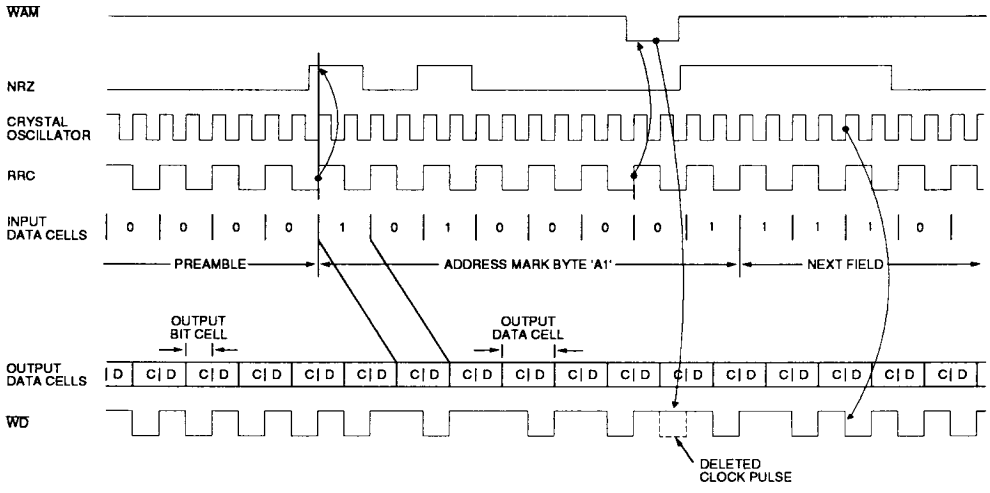
$$Tsa = \frac{(0.25)TORC}{R + 0.7}$$

Where: R is in kΩ.

Pins RF and RS are intended to be used as a trim and should be restricted to ± 1.5% window shifts. They can be used in conjunction with the digital control port.

TABLE 2: Decode Window Symetry Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
0	0	1	1
+TS1	0	1	0
+TS2	0	0	1
+TS3	0	0	0
0	1	1	1
–TS1	1	1	0
–TS2	1	0	1
–TS3	1	0	0



NOTE 1: NRZ and WAM inputs are clocked in on the rising edges of RRC (input data cell boundaries).
NOTE 2: WD output data cells are defined in terms of the falling edges of RRC. They are delayed 1 1/2 data cells relative to the input data cells.

FIGURE 6: Write Address Mark /Address Write Data Waveform Diagram

WRITE OPERATION

In the Write Mode, the SSI 32D534A converts NRZ data (from the Controller) into MFM data, for storage onto the disk. It performs write precompensation, if enabled, and inserts Address Marks as requested. Serial NRZ data is clocked into the SSI 32D534A and latched on defined data cell boundaries. NRZ data must be synchronous with the rising edges of the RRC clock output. During a Write Data Operation, the SSI 32D534A processes data and ECC fields and in a Write Format Operation, Address Marks, Preamble, ECC, Gaps, and ID fields are processed. Write Gate is an asynchronous input and may be initiated or terminated at any position on the disk. MFM encoded output write data, $\overline{WD}$, is delayed from input NRZ data by 1.5 Data Cells. For the successful completion of a write operation, Write Gate, WG, should not be terminated prior to the last output Write Data pulse.

Address Marks can be inserted into the MFM encoded data stream, $\overline{WD}$, with the pin $\overline{WAM}$ (Write Address Mark). When $\overline{WAM}$ is asserted, the data/ clock pulse in the corresponding bit cell of the MFM encoded data stream is deleted. This allows specially encoded sequences (illegal MFM patterns) to be encoded using the SSI 32D534A. $\overline{WAM}$ is synchronous with the RRC clock and is internally delayed by 0.5 data cells. To generate the missing clock A1 Address Mark pattern, $\overline{WAM}$ is asserted during the sixth data cell of the NRZ A1 data pattern. Figure 6 depicts the Address Mark generation sequence.

Write Precompensation reduces the effect of intersymbol interference caused by the proximity of magnetic transitions on the disk media. The interference is caused by specific data patterns where flux reversals are positioned closely together. Compensation consists of shifting write data pulses in time to counteract for the shifting normally exhibited in the corresponding Read Back signal. When Precompensation is enabled, see Table1, the SSI 32D534A recognizes these data patterns and appropriately shifts the write data pulses. Table 3 describes the Precompensation Algorithm relative to the current data bit, n, to be written.

WRITE OPERATION (Continued)

The SSI 32D534A utilizes an internal analog delay line to time shift the encoded write data pulses. The magnitude of the time shift, TPC, is determined by the external RC network (RPC, CPC) at pin PCS (Precomp Set) and is given by:

$$TPC = 0.15 \times RPC \times (CPC + C_s),$$
with RPC in kΩ & CPC in pF
C_s = Stray capacitance

An Early/Late compensated bit results in a pulse shifted TPC seconds before/after the nominal unshifted pulse position.

TABLE 3: Write Precompensation Algorithm

BIT n-2	BIT n-1	BIT n	BIT n+1	COMPENSATION Bit n
X	0	1	1	LATE
X	1	1	0	EARLY
1	0	0	0	LATE
0	0	0	1	EARLY

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to +150	°C
Junction Operating Temperature	0 to +130	°C
Supply Voltage, VCC	-0.5 to 7	Vdc
Voltage Applied to Logic inputs	-0.5 to VCC + 0.5	Vdc

ELECTRICAL CHARACTERISTICS

Unless otherwise specified 4.75 ≤ VCC ≤ 5.25V, 0°C ≤ TA ≤ 70°C, 5 MHz ≤ 1/TORC ≤ 10 MHz; 10 MHz ≤ 1/TVCO ≤ 20 MHz.

PARAMETER		CONDITIONS	MIN	MAX	UNIT
VIH	High Level Input Voltage		2.0		V
VIL	Low Level Input Voltage			0.8	V
IIH	High Level Input Current	VIH = 2.7V		20	µA
IIL	Low Level Input Current	VIL = 0.4V		-0.36	mA
VOH	High level Output Voltage	IOH = -400µA	2.7		V
VOL	Low Level Output Voltage	IOL = 4mA		0.5	V
ICC	Power Supply Current	All outputs open		180	mA
	Power Dissipation	Tj = 130°C		850	mW

CONTROL CHARACTERISTICS (Refer to Figure 7)

PARAMETER		CONDITIONS	MIN	MAX	UNIT
TSWS	$\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		15		ns
THWS	$\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		5		ns
TSERG	Set up time EWC to RG		10		ns
THERG	Hold time EWC from RG		0		ns
TSEWG	Set up time EWC to WG		0		ns
THEWG	Hold time EWC from WG		0		ns

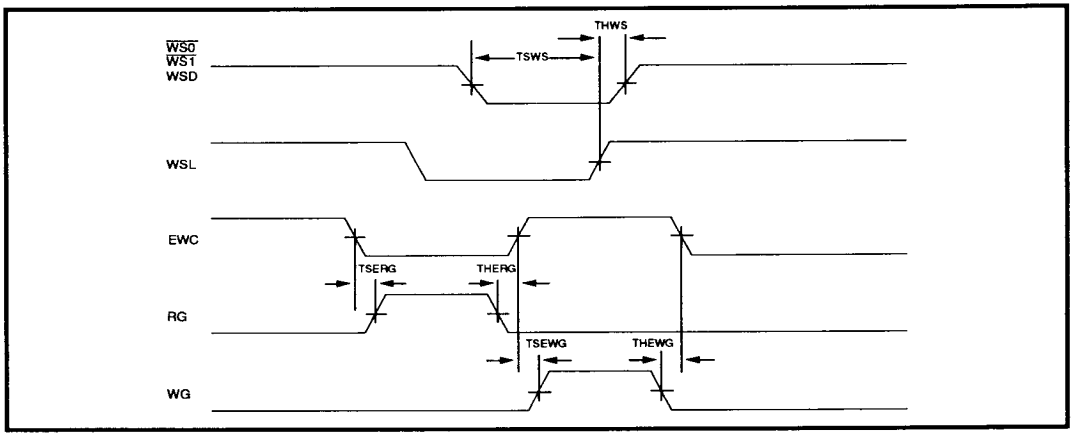


FIGURE 7: Control Timing

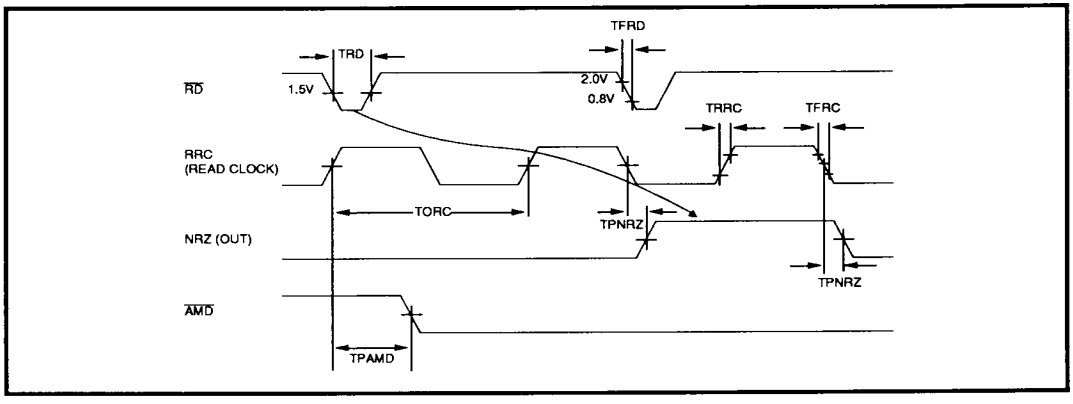


FIGURE 8: Read Timing

ENDEC CHARACTERISTICS

READ MODE (Refer to Figure 8)

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
TRD	Read Data Pulse Width		20	TORC - 40	ns
TFRD	Read Data Fall Time	2.0 to 0.8V		20	ns
TRRC	Read ClockRise Time	0.8 to 2.0V; $C_L \leq 15$ pF		10	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V; $C_L \leq 15$ pF		8	ns
TPNRZ	NRZ (out) Propagation Delay		-15	+15	ns
TPAMD	AMD Propagation Delay		$\frac{TVCO}{2} - 15$	$\frac{TVCO}{2} + 15$	ns
TQC	1/4 Cell Delay Accuracy	TQC = 0.25 TORO	0.8TQC	1.2TQC	sec
TOS	Retriggerable One-shot Delay Accuracy	TOS = RT (8.96 E-12) 12K ≤ RT ≤ 36K*	0.84TOS	1.16TOS	sec
TORC	Read Clock Period		0.8TORO	1.2TORO	ns

* Where: TOS = 1.25/Data Rate; Data Rate = Mbit/s

WRITE MODE (Refer to Figure 9)

PARAMETERS		CONDITIONS	MIN	MAX	UNIT
TWD	Write Data Pulse Width	$C_L \leq 15$ pF	$\frac{TORO}{2} - 2.4TPC - 12$	$\frac{TORO}{2} + 12$	ns
TPC	PrecompensationTime Shift Magnitude Accuracy	TPC = 0.15 (RPC)(CPC+Cs) 2K ≤ RPC ≤ 6K 15 pF ≤ CPC ≤ 36 pF Cs = Stray Capacitance	0.8TPC	1.2 TPC	sec
TFWD	Write Data Fall Time	2.0V to 0.8V; $C_L \leq 15$ pF		8	ns
TRRO	Reference Clock RiseTime	0.8 to 2.0V; $C_L \leq 15$ pF		10	ns
TFRO	Reference Clock Fall Time	2.0V to 0.8V; $C_L \leq 15$ pF		8	ns
TSNRZ	NRZ(in) Set Up Time		20		ns
THNRZ	NRZ(in) Hold Time		7		ns
TSWAM	$\overline{WAM}$ Set-up Time		20		ns
THWAM	$\overline{WAM}$ Hold Time		7		ns

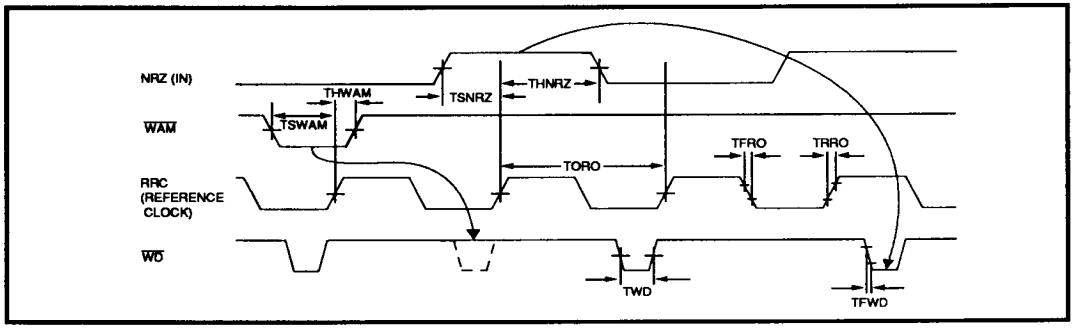


FIGURE 9: Write Timing

DATA SYNCHRONIZATION CHARACTERISTICS

PARAMETERS		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCOIN = 2.7V, TO = 1.63E - 11(RR+500) VCC = 5.0V, 2400 ≤ RR ≤ 6000Ω	0.78TO		1.22TO	sec
	VCO Frequency Dynamic Range	VCC = 5.0V, 1V≤VCOIN ≤ VCC-0.6V	±27		±40	%
KVCO	VCO Control Gain	1V ≤ VCOIN ≤ VCC-0.6 V, $\omega_0 = 2\pi/TO$	$0.14\omega_0$		$0.20\omega_0$	rad/s-V
KD	Phase Detector Gain	KD = 0.308/(RR+500); VCC = 5.0 V, 2400 ≤ RR ≤ 6000Ω	0.83KD		1.17KD	$\frac{A}{rad}$
*	KVCO x KD Product Accuracy	2400 ≤ RR ≤ 6000Ω, VCC = 5.0V	-28		+28	%
*	VCO Phase Restart Error			6		ns
	Decode Window Centering Accuracy				See Note	ns
	Decode Window		$\frac{TORC}{2} - 4$			ns
TS1	Decode Window Time Shift Magnitude	TS1 = 0.015TORC		TS1		ns
TS2	Decode Window Time Shift Magnitude	TS2 = 0.06TORC		TS2		ns
TS3	Decode Window Time Shift Magnitude	TS3 = 0.075TORC		TS3		ns
TSA	Decode Window Time Shift Magnitude	$TSA = \frac{(0.25)TORC}{R+0.7}$; (R in kΩ)		TSA		ns

Note: ±(0.015TORC+3)
*Not directly testable - Design Characteristic

APPLICATION

LOOP FILTER

The element in the phase lock loop which controls the loop dynamics is known as the loop filter. Acquisition time, data margin, and data tracking can be optimized by the loop filter selection. One possible loop filter configuration is shown in Figure 10, where the function of C_1 is as an integrating element. The larger the capacitance of C_1, the longer will be the lock time. If the capacitance is too small, the loop will tend to track high frequency jitter. The role of the resistor R is to reduce the phase shift induced by C_1. This is necessary since the loop will oscillate at the frequency where the gain is unity. The capacitor C_2 will suppress high frequency transients when switching occurs. This capacitor will have a minimal effect of the loop response if it is small compared to C_1 (typically, $C_2 = C_1/10$).

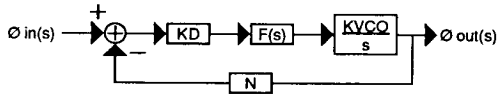
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + \frac{C_2}{C_1}\right)}$$

if $C_2 << C_1$
then,

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The phase lock loop can be described as:



where:

KD = phase detector gain [A/rad]
F(s) = Filter impedance [V/A]
$\frac{KVCO}{s}$ = oscillator transfer function [rad/s V]
N = ratio of reference input frequency to the VCO output frequency.

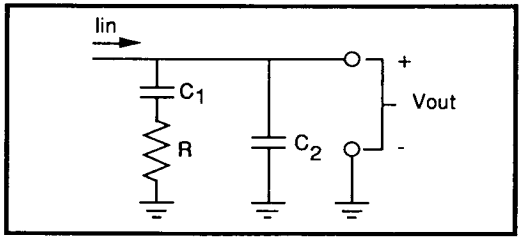


FIGURE 10: Loop Filter

Therefore, the closed loop transfer function is now:

$$T(s) = \frac{Ø\,out(s)}{Ø\,in(s)} = \frac{G(s)}{1 + G(s)H(s)} =$$

$$\frac{KD \times KVCO\left(\frac{1 + sRC_1}{C_1}\right)}{s^2 + s(N \times KD \times KVCO \times R) + \frac{N \times KD \times KVCO}{C_1}}$$

now we can put the characteristic equation (denominator) in the form:

$$S^2 + 2s\zeta\omega_n + \omega_n^2$$

$$\therefore \omega_n^2 = \frac{NxKDxKVCO}{C1} \text{ and } \zeta = \frac{NxKDxKVCOxR}{2\omega_n}$$

which results in:

$$C_1 = \frac{NxKDxKVCO}{\omega_n^2}$$

$$R = \frac{2\zeta\omega_n}{N \times KD \times KVCO} \text{ and } C_2 = \frac{C_1}{10}$$

For a $\zeta = 0.8$, the relationship between ω_n and lock time is:

$$\omega_n = \frac{4.5}{\text{lock time}}$$

Therefore, the loop filter components C_1, C_2, and R can be evaluated for a required lock time and coding scheme (N) frequency relationship to the VCO frequency.

With MFM coding:

N = 1, for Øin = reference oscillator
N = 0.5, for Øin = maximum data frequency
N = 0.25 for Øin = minimum data frequency

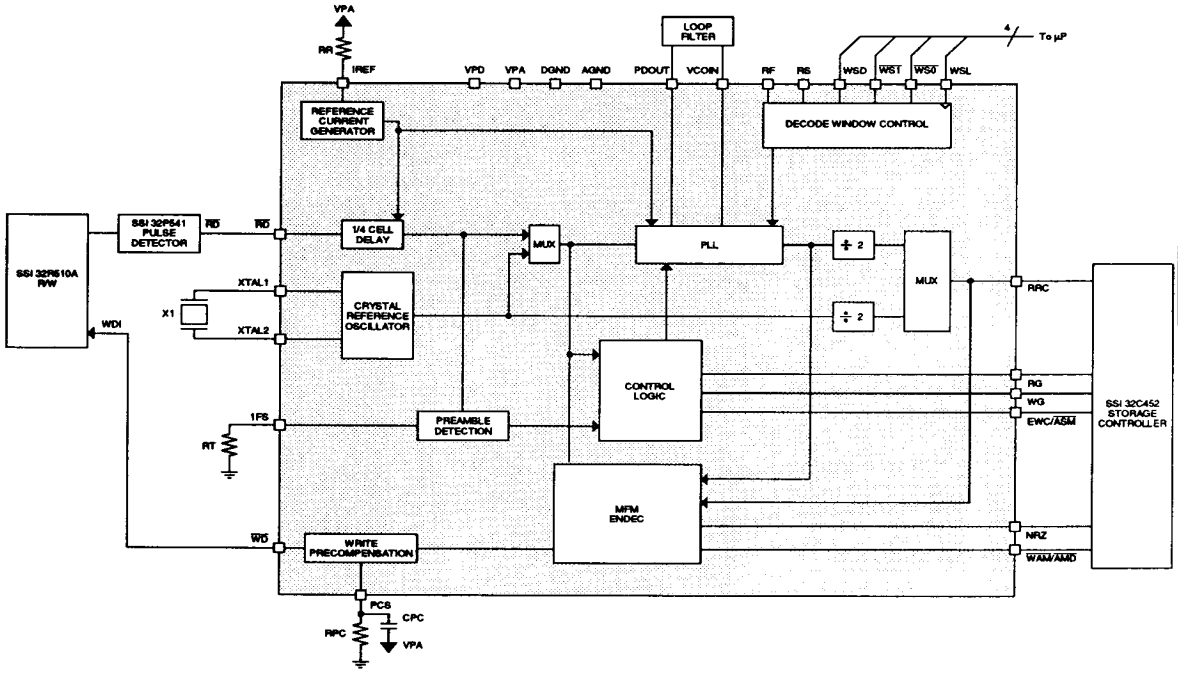


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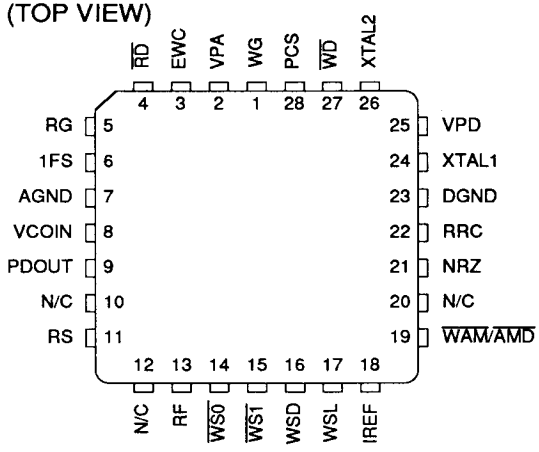
FIGURE 11: Typical Application

Typical External Component Values for a 5 Mbit/s MFM Application:

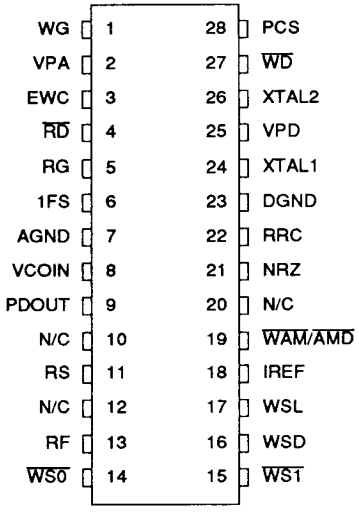
COMPONENT	CONDITIONS	VALUE	UNITS
X1	Series resonant crystal	10	MHz
RR		5.62	kΩ
RT		27.9	kΩ
RPC		2	kΩ
CPC		15	pF
Loop Filter			
R		2.8	kΩ
C_1		1200	pF
C_2		120	pF

SSI 32D534A
Data Synchronizer/
MFM ENDEC

PACKAGE PIN DESIGNATIONS
(TOP VIEW)



28-pin PLCC



28-pin DIP

THERMAL CHARACTERISTICS: Øja

28-pin PLCC	65°C/W
28-pin PDIP	55°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32D534A 28-pin PLCC	SSI 32D534A-CH	32D534A-CH
SSI 32D534A 28-pin PDIP	SSI 32D534A-CP	32D534A-CP

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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