TECHNICAL MANUAL

MICROMEMORY 3000QD

MEMORY CARD ASSEMBLY

ELECTRONIC MEMORIES & MAGNETICS CORPORATION

12621 Chadron Avenue. Hawthorne. California 90250 / Telephone: (213) 644-9881

March, 1976

TABLE OF CONTENTS

ILLUSTRATIONS

TABLES

SECTION I

GENERAL DESCRIPTION

1-1. INTRODUCTION

1-2. This manual contains information required to install, operate, and maintain the MICROMEMORY 3000QD Memory Card Assembly (figure 1-1), manufactured by Electronic Memories and Magnetics Corporation, Hawthorne, California. As part number 928637-001.

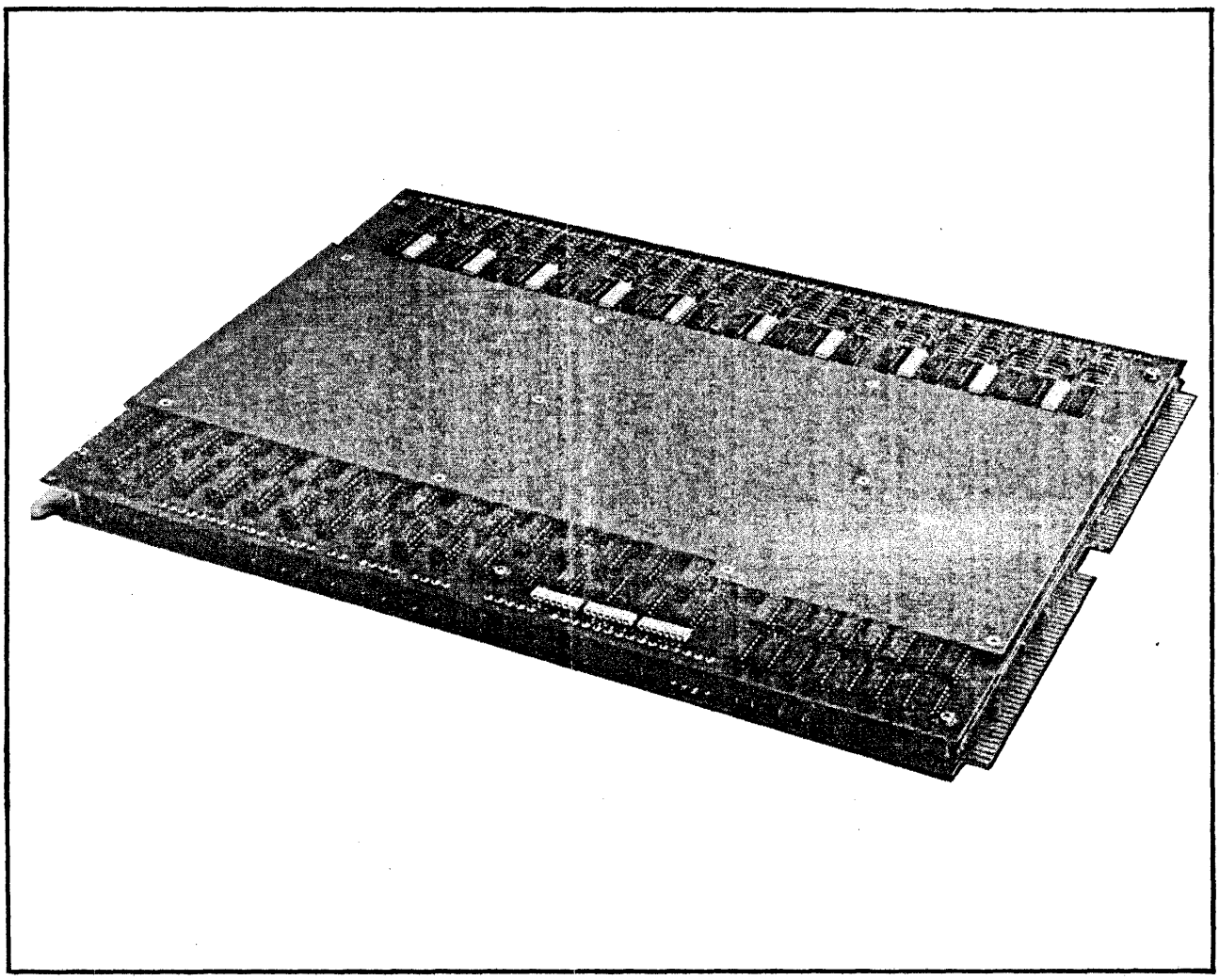


Figure 1-1. MICROMEMORY 3000QD Memory Card Assembly

* QD: Quad Density

1-3. Contents of this manual are arranged as follows:

Section I - General Description. Scope, contents and organization of the manual. General physical and electrical description, system orientation and general specifications.

Section II - Installation and Operation. Information required to install, prepare for operation, and operate the equipment.

Section III - Theory. General and detailed theory of operation including overall system theory, general block diagram description, and detailed circuit description. This section includes discussions of address decoding, core-drive system, data pattern, and system timing.

Section IV - Maintenance. Preventive and corrective maintenance procedures and troubleshooting charts.

Section V - Drawings. Circuit card schematics, assembly drawings, and parts lists.

1-4. PURPOSE OF EQUIPMENT

1-5. The MICROMEMORY 3000QD Memory Card Assembly is designed for use with central processor units as a main, directly accessible, random access storage unit. The Memory Card Assembly can be used alone; or by means of built-in address expansion circuits permitting up to eight Memory Card Assemblies to be operated together.

1-6. PHYSICAL DESCRIPTION

1-7. The MICROMEMORY 3000QD Card Assembly is a complete memory system on a single card assembly consisting of two circuit cards. The Electronics Card contains timing, control, and inhibit drivers, and the Stack Card contains the core array, diodes, and sense amplifiers. The Stack Card is pluggable into the Electronics Card.

1-8. SIZE AND MOUNTING

1-9. The memory is mounted on a 1/16-inch epoxy-glass

circuit card whose dimensions are;

Height:	11.75 inches
Length:	15.40 inches
Mounting centers:	1.00 inch

1-10. I/O CONNECTORS

1-11. The circuit card is designed to use two 80-pin edge connectors with pins on 0.125-inch centers. The recommended mating connector is **Winchester P/N HWL40D2-112-4086 or equivalent.**

1-12. FUNCTIONAL DESCRIPTION

1-13. The MICROMEMORY **3000QD Memory Card Assembly is a random-**access, coincident-current, ferrite-core memory arranged in a 3D, 3-wire configuration. Except for a dc power supply, the unit is self-sufficient, including all necessary timing and control, inhibit and sense, and stack circuitry.

1-14. MEMORY CAPACITY

1-15. Memory capacity is a function of addressing and word length within the following limits:

32,768 words by 20 bits
32,768 words by two 10-bit bytes
65,536 words by 10 bits

1-16. ZONES. Twenty-bit words can be divided into two 10-bit zones (bytes). These zones are designated Zone A (bits 0 thru 8, and 18), and Zone B (bits 9 thru 17, and 19).

1-17. MODES OF OPERATION

1-18. The memory performs in Read/Restore mode, Clear/Write mode, and Read-Modify-Write mode (Split Cycle).

1-19. GENERAL SPECIFICATIONS

1-20. Table 1-1 is a list of Memory Card Assembly general specifications.

Table 1-1. Memory Card Assembly General Specifications

ITEM	SPECIFICATION		
Type of Memory	Random access, 3-wire, 3D magnetic core		
Capacity	32,768 words by 20 bits 32,768 words by two 10-bit bytes 65,536 words by 10 bits		
Modes of operation	Read/Restore Clear/Write Read/Modify/Write (Split Cycle)		
Access Time	300ns		
Cycle Time			
Read/Restore	850ns		
Clear/Write	850ns		
Read/Modify/Write	950ns plus modify time (processor response time)		
Logic Levels:			
Input	False (ZERO) = +2.5 to +5.0 volts True (ONE) = 0 to +0.5 volt		
Output	False (ZERO) = +2.5 to +5.0 volts		
Sink/Source Capacity	See Section II		
AC Power Requirements	Non required		
DC Power Requirements, (Current in amperes - Unit operating at 850ns rate).	CURRENT		
	+15V±2%	+5V±2%	-15V±2%
Standby	0.5	3.5	0.1
All ONEs	3.8	3.8	1.2
All ZEROs	1.5	3.8	0.7

Table 1-1. Memory Card Assembly General Specifications (Cont)

ITEM	SPECIFICATION	
DC Power to Termination Resistors (Current in amperes)	CURRENT (Amps)	
	Termination Inputs Open	Termination Inputs OV
Terminations at J1 (+5V±2%)	0.14	0.34
Terminations at J2 (+5V±2%)	0.16	0.39

1-21. ENVIRONMENTAL SPECIFICATIONS

1-22. Table 1-2 is a list of environmental specifications.

1-23. EQUIPMENT SUPPLIED

1-24. Equipment supplied is the MICROMEMORY **3000QD Memory Card** Assembly.

Table 1-2. Environmental Specifications

ITEM	SPECIFICATION
Operating Conditions	
Ambient Temperature	0°C to +50°C
Thermal Shock	±10°C per hour **(max)**
Relative Humidity	95% max w/o condensation
Altitude	-1000 ft to +10,000 ft msl

SECTION II

INSTALLATION AND OPERATION

2-1. UNPACKING AND INSPECTION

2-2. Use reasonable care in unpacking the equipment. No special unpacking instructions are required. Inspect the equipment for physical damage.

2-3. INSTALLATION

2-4. The Memory Card Assembly is designed to plug into an EMM standard MICROMEMORY 3000QD Memory System chassis. Figure 2-1 illustrates card orientation and dimensions.

2-5. INTERFACE SIGNALS

2-6. All signals between the processor and the Memory Card Assembly should be carried on twisted-pair transmission lines. Termination resistors are included in each Memory Card Assembly for proper termination of the Transmission lines to minimize reflections. Connection of the termination resistors is made externally on the input/output connector receptacle and therefore is at the discretion of the user. (See figure 2-2.)

2-7. All input/output signal parameters are measured at the Memory Card Assembly input/output connectors with properly terminated processor cables attached. Times shown in timing diagram figure 2-3 are measured at the 50% point of the signal transition.

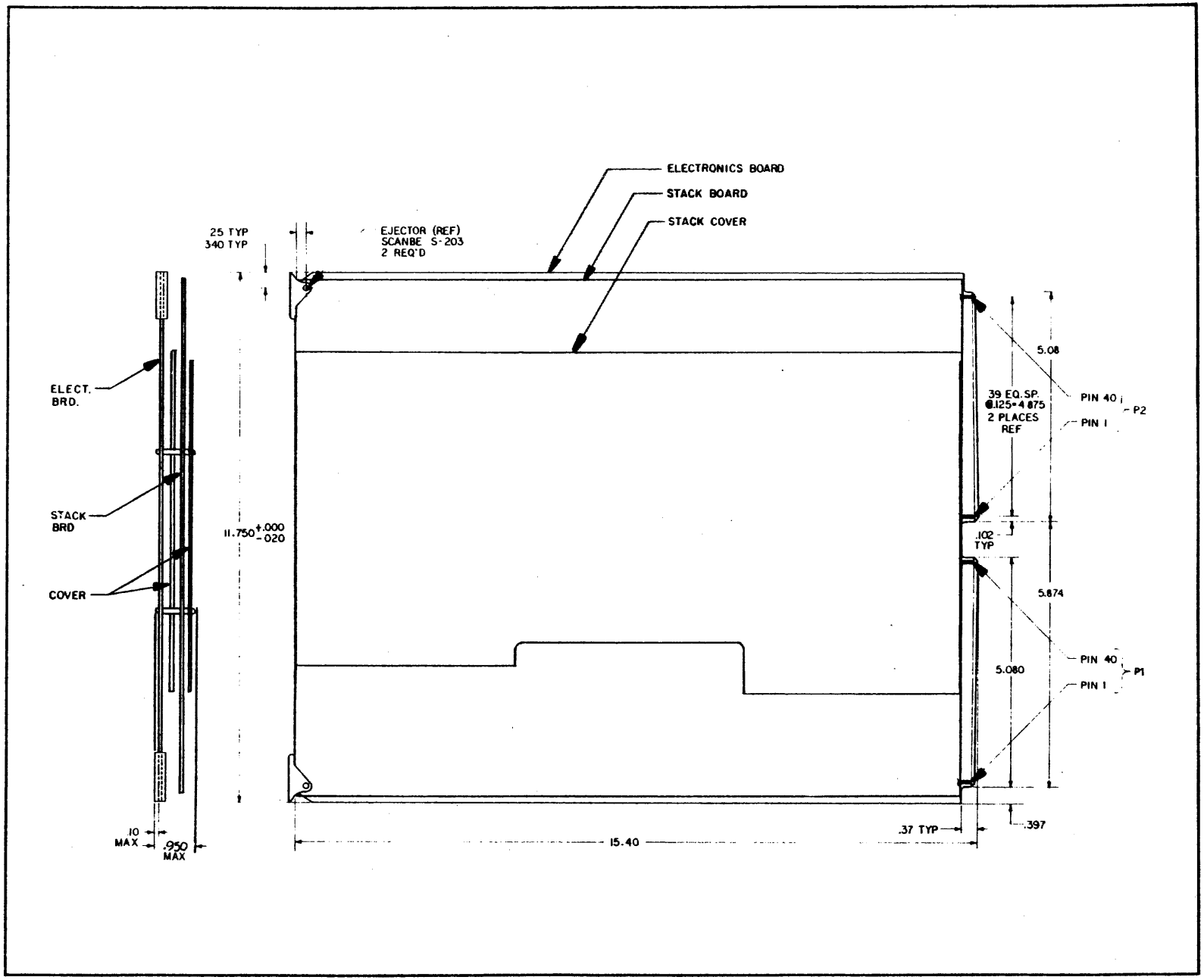
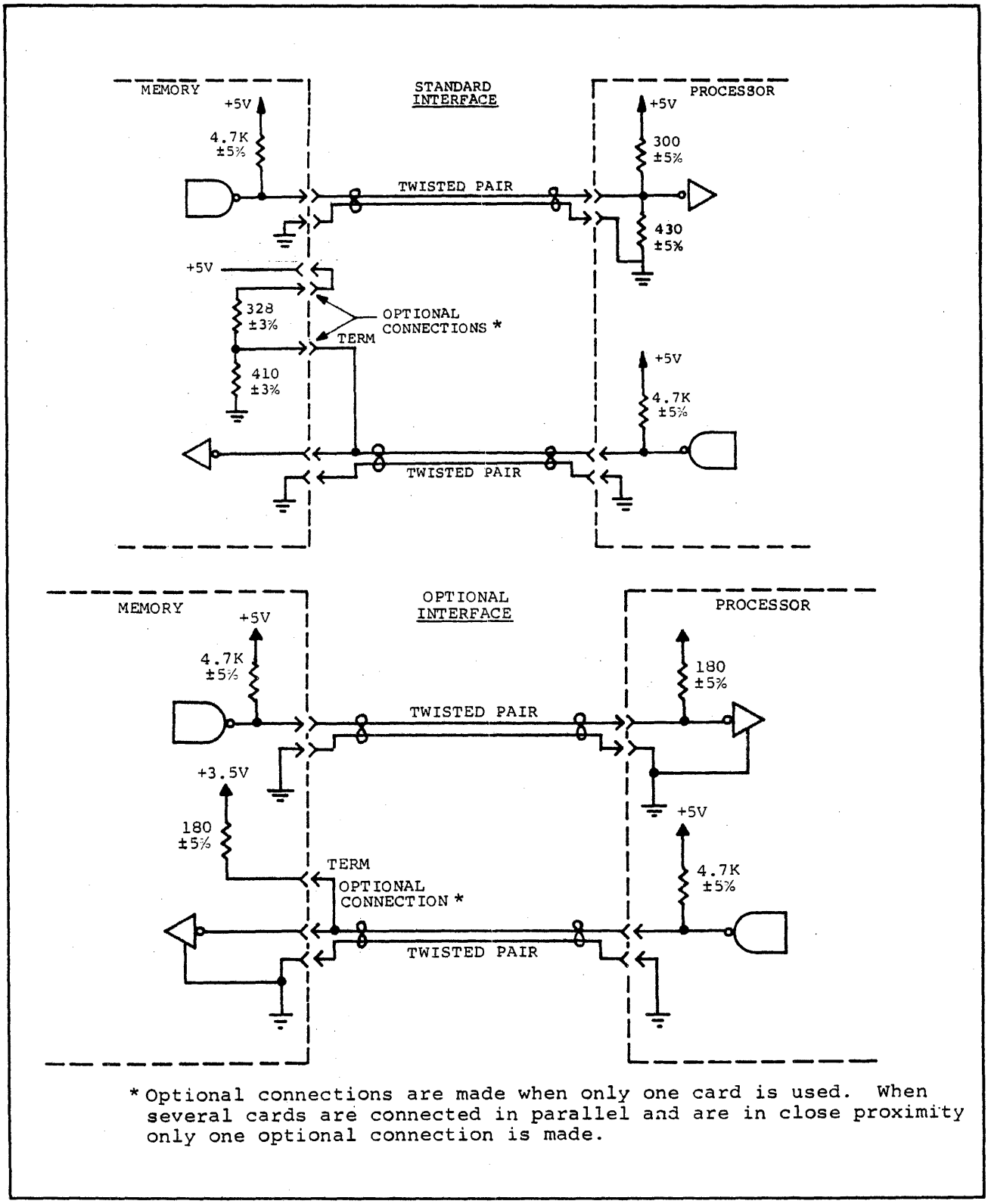
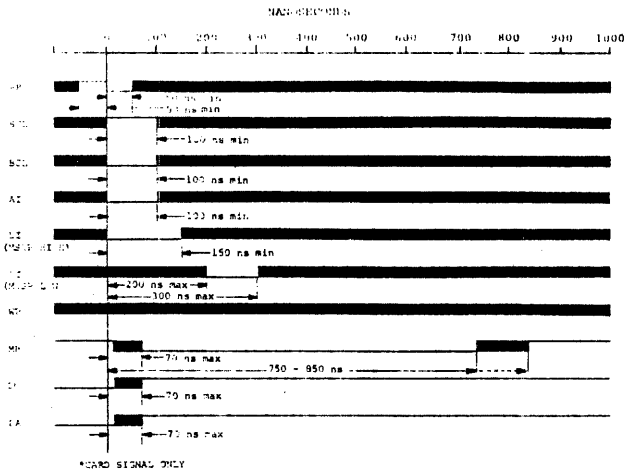


Figure 2-1. Memory Card Assembly Outline and Dimensions



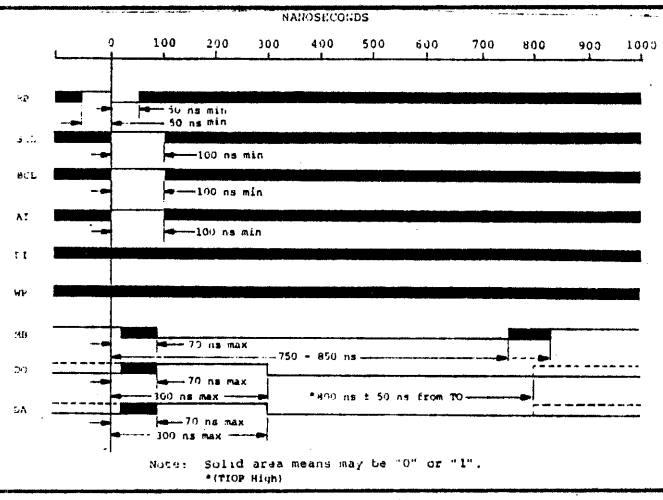
* Optional connections are made when only one card is used. When several cards are connected in parallel and are in close proximity only one optional connection is made.

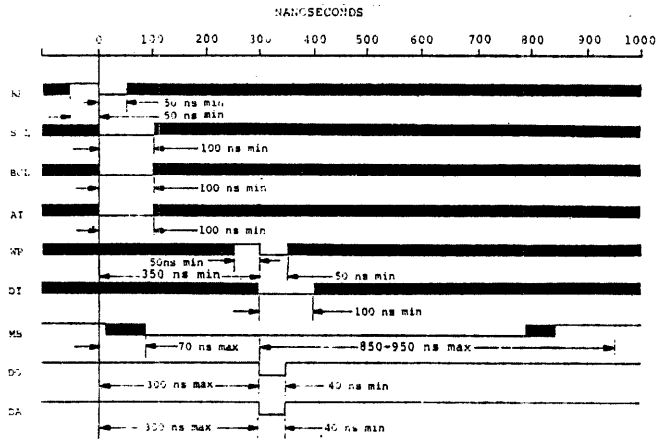
Figure 2-2. Memory Card Assembly Interface Circuit, Typical



Clear/Write Timing

Read/Restore Timing





Read/Modify/Write Timing

Note: Solid area means may be "0" or "1".

Figure 2-3. Interface Timing Diagrams

2-8. Input circuits to the memory system are TTL gates. The input drive for individual inputs is listed in table 2-1. Drive requirements are expressed in units of TTL loads where 1 TTL load = 2 ma sink from the driver in the Logic "1" (OV) state. When the termination resistors are used (externally connected), the source driver in the Logic ONE state must be capable of sinking 17 ma termination-resistor current in addition to the rated sink load for each input. No source current is required in the Logic ZERO state. Input levels required are as follows:

False (Logic ZERO) = +2.5V to +5.0V
True (Logic ONE) = OV to +0.5V

Table 2-1. Memory Card Assembly Interface Signals

SIGNAL NAME	ABBR	FUNCTION/ LOAD	DESCRIPTION
Initiate Pulse	*$\overline{RP}$	Input One TTL Load	The application of an **Initiate** Pulse (RP) when the memory is available, initiates a memory cycle. The type of cycle (Read/Restore, Clear/ Write or Split-Cycle) is defined by BCL (Byte Control level) and SCL (Split-Cycle level).
Byte Control Levels	BCL1, BCL2	Input One TTL Load	The state of the two Byte Control Levels in conjunction with the Initiate Pulse (RP) determines the memory mode for each 10-bit byte. When BCL is true (low), the Initiate Pulse (RP) executes a clear/write cycle in the selected byte. When BCL is false (high), RP initiates a read/restore cycle in the selected byte. In Split Cycle mode, if BCL is true (low), new data is stored in memory; if BCL is false (high), readout data is re-stored to memory.

* External connection of the Write Pulse (WP) **to the Initiate** Pulse (RP) is possible for control by a single line.

Table 2-1. Memory Card Assembly Interface Signals (Cont)

SIGNAL NAME	ABBR	FUNCTION/ LOAD	DESCRIPTION
Split-Cycle Level	$\overline{SC}$	Input One TTL Load	When the Split-Cycle (SC) input is true (low), the Split-Cycle mode is initiated. The Initiate Pulse (RP) executes the read phase, and the Write Pulse (WP) executes the write phase.
Write Pulse	*$\overline{WP}$	Input One TTL Load	In Split Cycle mode, the memory completes the read phase, then waits. The Write Pulse (WP) then initiates the write phase of the same cycle.
Address Option	COOP AI15	Input One TTL Load	By wiring the ADOP, and AI15 inputs to the levels specified below, the memory will function accordingly as 32K X 20 or 64K X 10. CONFIGURATION INPUT — 16K X 20 — 32K X 10 COOP — Low OV — High (open) AI15 — Low OV — Most Sig. Address Bit For 64K X 10 operation it is necessary to connect data-bit lines 0 thru 8, and 18 to data-bit lines 9 thru 17, and 19 on the input and output.
Address In	AI (0-15)	Input One TTL Load AI00 thru AI14 Two TTL Loads AI15	Memory location to be accessed is established by 15 or 16 single-ended address lines; 15 lines for 32K X 20 operation, 16 lines for 64K X 10 operation.
Extended Address In	XAI1 Thru XAI3	Input One TTL Load Per Bit	There are three extended address inputs. XAI outputs fan out to 10 TTL loads per bit. Inverters are provided to accommodate additional memory cards for increasing memory capacity. When the address inverters are properly wired to the memory select

* The Write Pulse (WP) and Initiate Pulse (RP) lines can be connected together externally for single-line control.

Table 2-1. Memory Card Assembly Interface Signals (Cont)

SIGNAL NAME	ABBR	FUNCTION/ LOAD	DESCRIPTION
			inputs (MS), selection among up to eight memory cards may be made without the necessity of using external decode circuits.
Data-In Strobe Option	$\overline{\text{MSOP}}$	Input 4.5 TTL Loads	When this pin is open, timing of data input (DI) is at time T0 (per figure 2-3). When MSOP is grounded, data is strobed-in from 200 to 300 nsec after the **leading edge of Initiate Pulse RP.**
Memory Protect	$\overline{\text{MP}}$	Input 3.5 TTL Loads	The Memory Protect (MP) input protects stored data during dc power turn-on and turn-off. The MP input should be in the high state during normal memory operation. When MP goes low, the Memory completes the cycle in process (if any) and ignores further requests for operation until the Memory Protect line is again high. The Memory will complete a Split Cycle in process correctly, provided that the Write Pulse is sent 600ns maximum after Initiate Pulse. During power turn-on, MP should be held low before any dc voltage reaches 1 volt and held low until at least 20.0 µsec after all power supplies are in tolerance. During power turn-off, MP should be driven low before any dc voltage is out of tolerance and should remain low until all dc voltages are less than 1.0 volt.
Data In	DI (0-19)	Input One TTL Load Per Bit	In a Clear/Write or Split-Cycle, new data must be presented to the memory as shown in figure 2-3.
Data Out**	DO (0-19)	Output	In a Read/Restore or Split-Cycle, data readout is presented on the data output lines no later than 300ns after RP and remains valid

Table 2-1. Memory Card Assembly Interface Signals (Cont)

SIGNAL NAME	ABBR	FUNCTION/ LOAD	DESCRIPTION
			until a subsequent RP, or will reset approximately 600ns after RP, depending on the state of TIOP (Data-Output/Data-Available option).
Common Data Buss	---	Input/ Output	Gating is provided in the data input and data output circuits to allow common-line bi-directional data transmission if desired.
Data** Available	$\overline{DA}$	Output	The Data Available signal is provided by the memory to signify that data is present and stable on all output data lines. The Data Available pulse occurs no later than 300ns after cycle initiate.
Data Output/ Data Available Option	TIOP	Input One TTL Load	With TIOP held low (OV), the Data Output (DO) and Data Available (DA) are as shown in the timing diagrams, figure 2-3. With TIOP high (open) the Data Output (DO) and Data Available (DA) will pulse from 300ns after RP until 600ns after RP.
Memory Busy**	$\overline{MB}$	Output	The Memory Busy signal (low) signifies to the processor that the memory is busy and will not accept an Initiate Pulse.
Memory Select	MS (1-3)	Input	The Memory Select inputs are used with the extended address inverters to expand addressing to include additional memory cards. When MS1, MS2, and MS3 are ZERO (high) the memory is selected: thus, when not used, the MS inputs must be wired to a logic ZERO (high) source.

** Output cables from the memory are driven from an integrated circuit TTL open collector driver (SN7438). The cable driver is capable of sinking 47ma. while maintaining a logic ONE level of from +0.25 to 0.50 volts.

Table 2-1. Memory Card Assembly Interface Signals (Cont)

SIGNAL NAME	ABBR	FUNCTION/ LOAD	DESCRIPTION
General Reset	$\overline{GR}$	Input 3.5 TTL Loads	The General Reset input, when driven low, resets all registers in the memory and initializes the timing circuits. This input should be high during normal operation of the memory. The memory will accept a new input within 5 µsec after the end of GR signal. A general reset should NOT be executed while a memory cycle is in progress - loss of data could result.

2-9. INTERFACE PIN ASSIGNMENTS

2-10. The Memory Card Assembly is designed to use two 80-pin edge connectors with pins on 0.125-inch centers. The recommended mating connector is Winchester P/N HWL40D2-112-4086 or equivalent.

2-11. MEMORY CARD ASSEMBLY POWER REQUIREMENTS

2-12. The power requirements for one Memory Card Assembly are given in table 1-1.

2-13. The dc voltages can be applied in any sequence. The power connections are given in table 2-3.

Table 2-2. Interface - Memory Card Assembly

PIN NUMBER	CONNECTOR		PIN NUMBER	CONNECTOR	
	P1	P2		P1	P2
01	OV	OV	41	OV	OV
02	+5V	DI06	42	+5V	DI01
03	-15V	DI07	43	-15V	DI00
04	OV	DI05	44	OV	DI08
05	+15V	DI04	45	+15V	DI17
06	+VPU	DO06	46	AI08	DO03
07	TERM	DO07	47	AI07	DO02
08	TERM	DO05	48	AI06	DO01
09	TERM	DO04	49	AI11	DO00
10	TERM	DI03	50	AI10	DO08
11	TERM	DI02	51	OV	DO17
12	TERM	TERM	52	AI09	DI16
13	TERM	TERM	53	AI03	DO16
14	TERM	TERM	54	OV	DO15
15	TERM	TERM	55	AI04	OV
16	TERM	TERM	56	AI05	DI15
17	TERM	TERM	57	OV	DI14
18	TERM	TERM	58	AI00	DO14
19	TERM	TERM	59	AI01	DO13
20	TERM	TERM	60	OV	OV
21	TERM	TERM	61	AI02	DI13
22	TERM	TERM	62	AI12	DI12
23	TERM	TERM	63	$\overline{GR}$	DO12
24	TERM	TERM	64	AI14	OV
25	TERM	TERM	65	$\overline{WP}$	OV
26	TERM	TERM	66	OV	OV
27	$\overline{SC}$	TERM	67	OV	OV
28	MS3	TERM	68	DI18	OV
29	MS2	TERM	69	DI19	DO11
30	MS1	TERM	70	AI15	DI11
31	BCL2	TERM	71	DO18	DI10
32	COOP/ADOP	TERM	72	DO19	DO10
33	$\overline{MB}$	TERM	73	XAI1	DO09
34	AI13	TERM	74	$\overline{XAI1}$	DI09
35	BCL1	OV	75	XAI2	+VPU
36	$\overline{DA}$	+15V	76	$\overline{XAI2}$	+15V
37	TIOP	OV	77	$\overline{XAI3}$	OV
38	MP	-15V	78	XAI3	-15V
39	$\overline{MSOP}$	+5V	79	$\overline{RP}$	+5V
40	OV	OV	80	OV	OV

Table 2-3. Memory Card Assembly Power Connections

CONN	PIN	VOLTAGE	CONN	PIN	VOLTAGE
J1	02	+5V	J2	39	+5V
J1	42	+5V	J2	79	+5V
J1	03	-15V	J2	38	-15V
J1	43	-15V	J2	78	-15V
J1	05	+15V	J2	36	+15V
J1	45	+15V	J2	76	+15V
J1	01	OV	J2	01	OV
J1	40	OV	J2	40	OV
J1	41	OV	J2	41	OV
J1	80	OV	J2	80	OV

SECTION III

THEORY OF OPERATION

3-1. GENERAL

3-2. This section comprises a functional description of the Memory Card Assembly. Description is divided into general discussion and detailed circuit description, each referring to appropriate block, simplified logic, logic, schematic, and timing diagrams. **The schematic diagram is located in Section V.**

3-3. GENERAL ORGANIZATION

3-4. The MICROMEMORY **3000QD is a complete memory system on a single card-pair. The card-pair consists of the Memory Electronics Board (Electronics Board) and the Stack Board. Contents of these boards are listed in table 3-1.**

Table 3-1. Functional Content of the 3220 System

CARD	FUNCTIONAL CONTENT
Memory Electronics	Timing Generator, Timing Counter, Control Circuits, Address Register, Data Receivers, and Address Decoder, X and Y Select, Current Generators, X and Y Drive Switches, X and Y Sink Switches, Data Register, Inhibit Drivers, and Memory Select.
Stack Card	Sense Amplifiers, and Core Array.

3-5. GENERAL THEORY

3-6. Memory system functions, contained within one card-pair, consists of addressing, data control, storage, and timing and control. System organization of these functions is illustrated in figure 3-1 and described in the following sub-paragraphs.

3-7. ADDRESSING

3-8. Addressing is accomplished in three decode levels. The general addressing scheme is illustrated in figure 3-1.

3-9. FIRST-LEVEL DECODING. Address bits in groups of three are applied to one-of-eight decoders that are gated by Read and Write control signals. The composite Read- or Write-decoded address is applied to core matrix drive or sink switches. Drive- or sink-switch output signals are then applied to the core matrix.

3-10. SECOND-LEVEL DECODING. X- and Y-drive and sink-switch outputs are applied as illustrated (figure 3-1) to the core matrix. The two decode signals (RX + WY and WX + RY) represent the sharing of four one-of-eight decoders in performing the X-Read, X-Write, Y-Read, and Y-Write functions. Because in any given function (Read or Write) related to core-matrix drive, two lines are required (such as X-Read and Y-Read), the decode result of these two 1/16 decoders is the same as if there were only one 1/16 decoder that accommodates both X and Y functions. The Y-sink switches are connected as illustrated to produce the Y-Read/Write 1/8 decode. The 1/16 Y-drive decode, combined with the 1/8 Y-sink decode, forms a 1/128 Y-line-select decoder. X-sink switches are connected similarly **except that the X sink decode is 1/16. Thus, the decode system comprises a 1/256 decode scheme.**

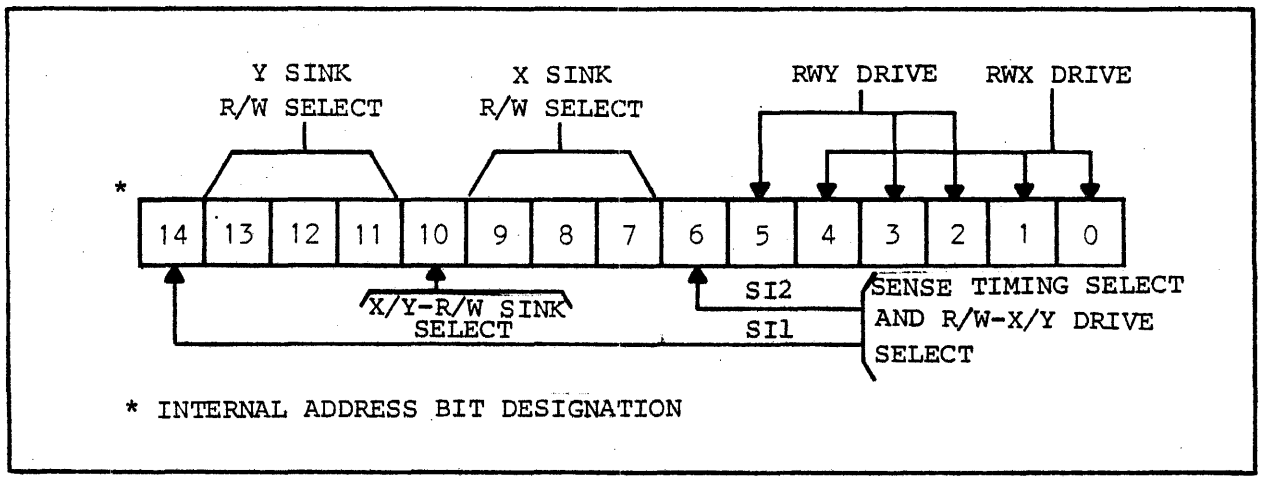
3-11. THIRD-LEVEL DECODING. Third-level decoding takes place in the matrix and consists of the selection of a single group of cores (word). The combination of X and Y lines, each representing an output from second level decoders arranged in a crosshatch, forms a core-matrix decoder. The combination of outputs from X and Y lines (1/128 Y and **1/256** X) results in a 1/**32,768** decode.

3-12. ADDRESS-DECODING DETAILS. Address decoding details are illustrated in figure 3-2. This diagram, using mnemonics and symbol details from the Memory Card schematic diagram, shows address and decode routing from the decoder inputs in the Electronics Card to the core array in the Stack Card. **The following**

diagram illustrates the functional allocation of address bits. Note that the Internal Address bits (A) differ in numerical designation (nn) from Address In (AI) bits. The address scheme described herein refers only to Internal Address bits.

EXTERNAL ADDRESS BIT	9	2	4	10	7	6	11	8	0	1	2	5	15	12	13
CONNECTOR J1 - ⟶	52	53	55	50	47	48	49	46	58	59	61	56	70	62	34
INTERNAL ADDRESS BIT	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

3-13. ADDRESS WORD. Address word configuration is illustrated as follows:



3-14. DRIVE DECODING. Internal Address bits A0 thru A5 are routed through Read/Write Address Multiplexers to Read/Write 1/8 Decoders. The R/W Address Multiplexers, controlled by Timing signal Q16, routes the appropriate Address bits to the Drive Decoders. When Q16 is high (during first phase of memory cycle), Address bits assigned to steer current for x/y Read operation are routed to the Drive Decoders; when Q16 is low (during second phase of memory cycle), Address bits assigned to steer current for x/y Write operation are routed to the Drive Decoders.

3-15. DRIVE DISCHARGE. A Drive Discharge circuit is connected to the core drive lines through isolation resistors. When activated at the proper time by Drive Discharge Time signal DDT, this circuit in effect grounds all core drive lines; thus, improving recovery time of the system.

3-16. CORE-ARRAY DRIVE SCHEME. As illustrated in figure 3-3, the entire X/Y drive system is powered by common +15V and -15V power sources.

3-17. Pulsed Current Sources

3-18. Power is applied to the drive end of the core matrix through positive and negative pulsed current sources. Pulsing of the current source is accomplished by a Read Switch-pair and Write Switch-pair controlled by Read and Write control signals.

3-19. The pulsed current source consists of eight switches (Q40 thru Q47), four current-limiting saturable transformers (T7), and a bias regulator circuit. The switches separately control the application of Read current and Write current to the X/Y drive switches. Separation of function is necessary here to allow sufficient recovery time* between Read and Write functions. Switches are triggered by Read or Write control signals.

3-20. Current-limiting transformers (T7) are biased above their saturation points so that they offer little impedance in the switch circuit when there is no current in the primary winding. When a current switch is triggered, current is in such a direction as to drive the transformer into the non-saturation region. Within this region, the transformer offers high impedance in the circuits, thus limiting the current. Circuit constants are such as to limit current to about 400 ma in any given core-matrix line.

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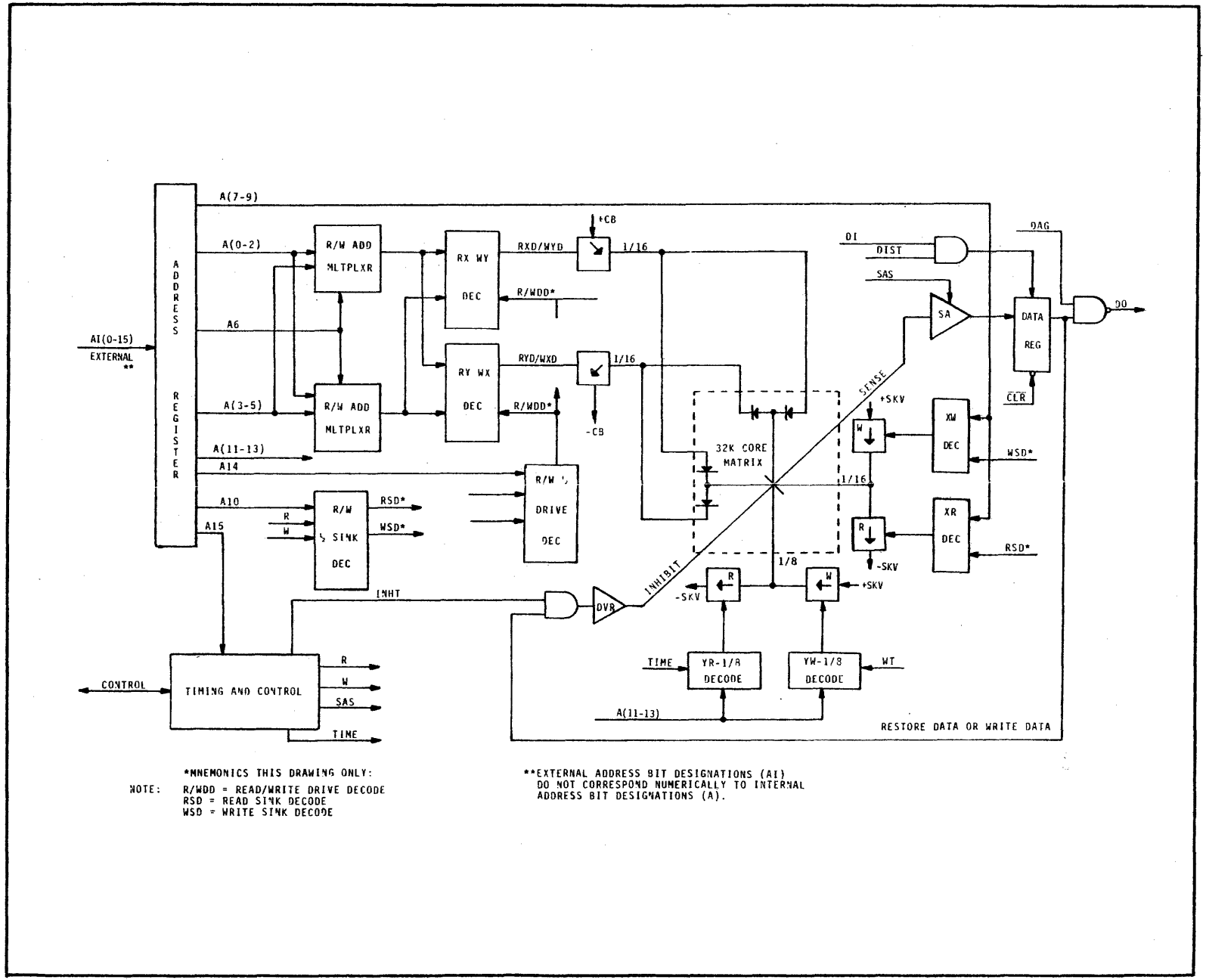
*Refers to recovery time of transformers T8 and T9.



*MNEMONICS THIS DRAWING ONLY:

NOTE: R/WDD = READ/WRITE DRIVE DECODE
RSD = READ SINK DECODE
WSD = WRITE SINK DECODE

**EXTERNAL ADDRESS BIT DESIGNATIONS (AI) DO NOT CORRESPOND NUMERICALLY TO INTERNAL ADDRESS BIT DESIGNATIONS (A).

Figure 3-1. MICROMEMORY 3000QD General Block Diagram

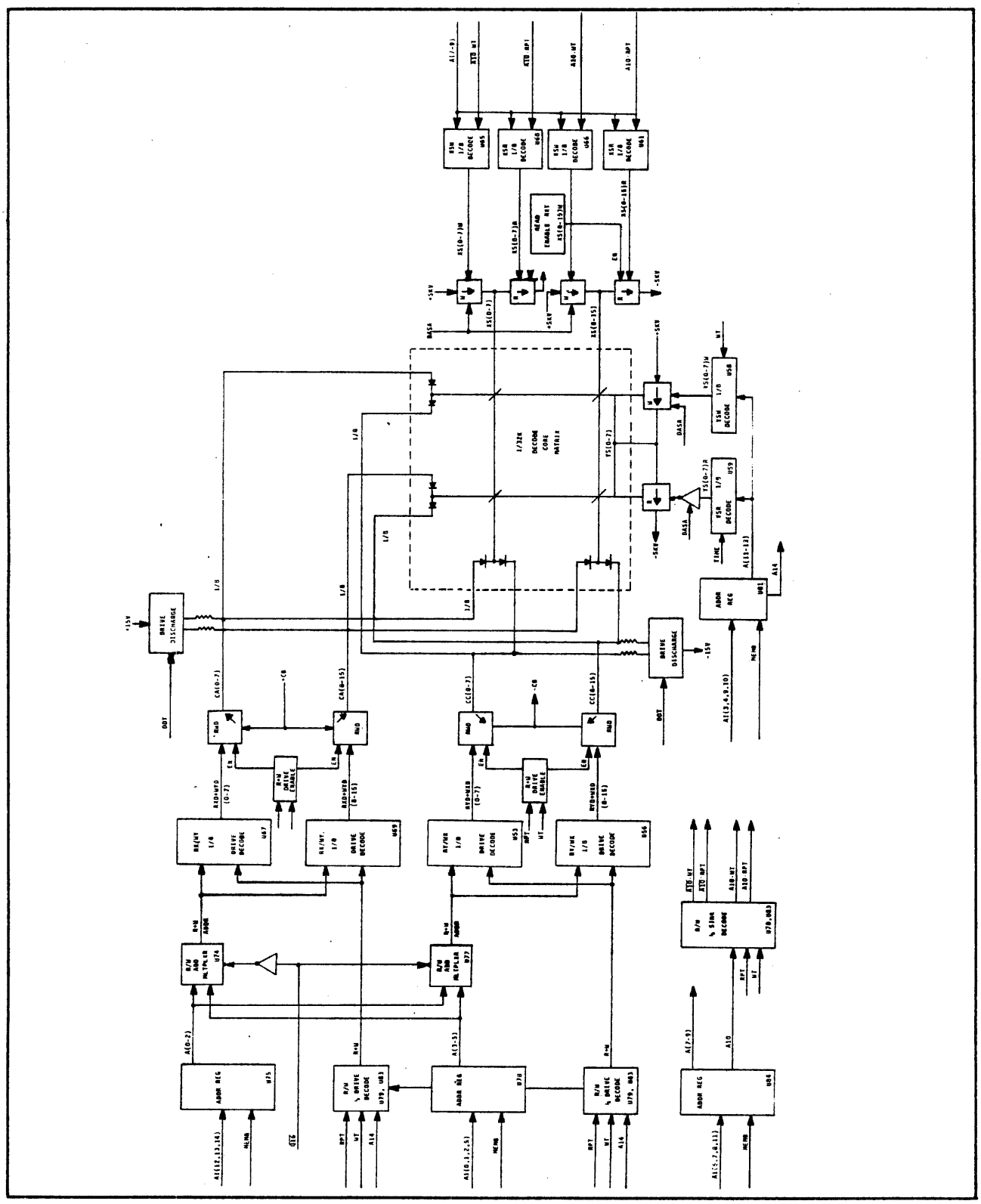


Figure 3-2. Address Decode Detailed Block Diagram

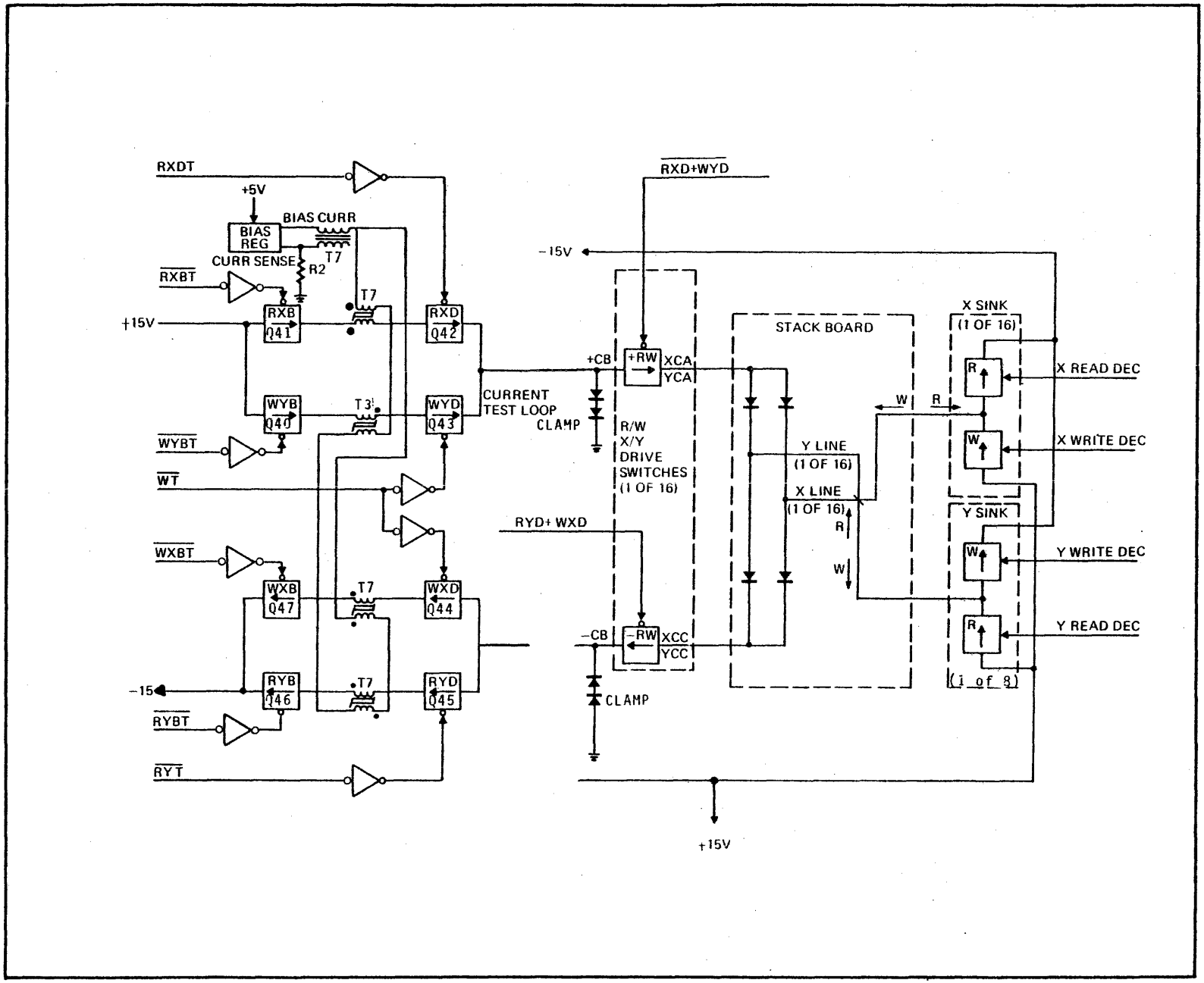


Figure 3-3. Core-Array Drive Scheme

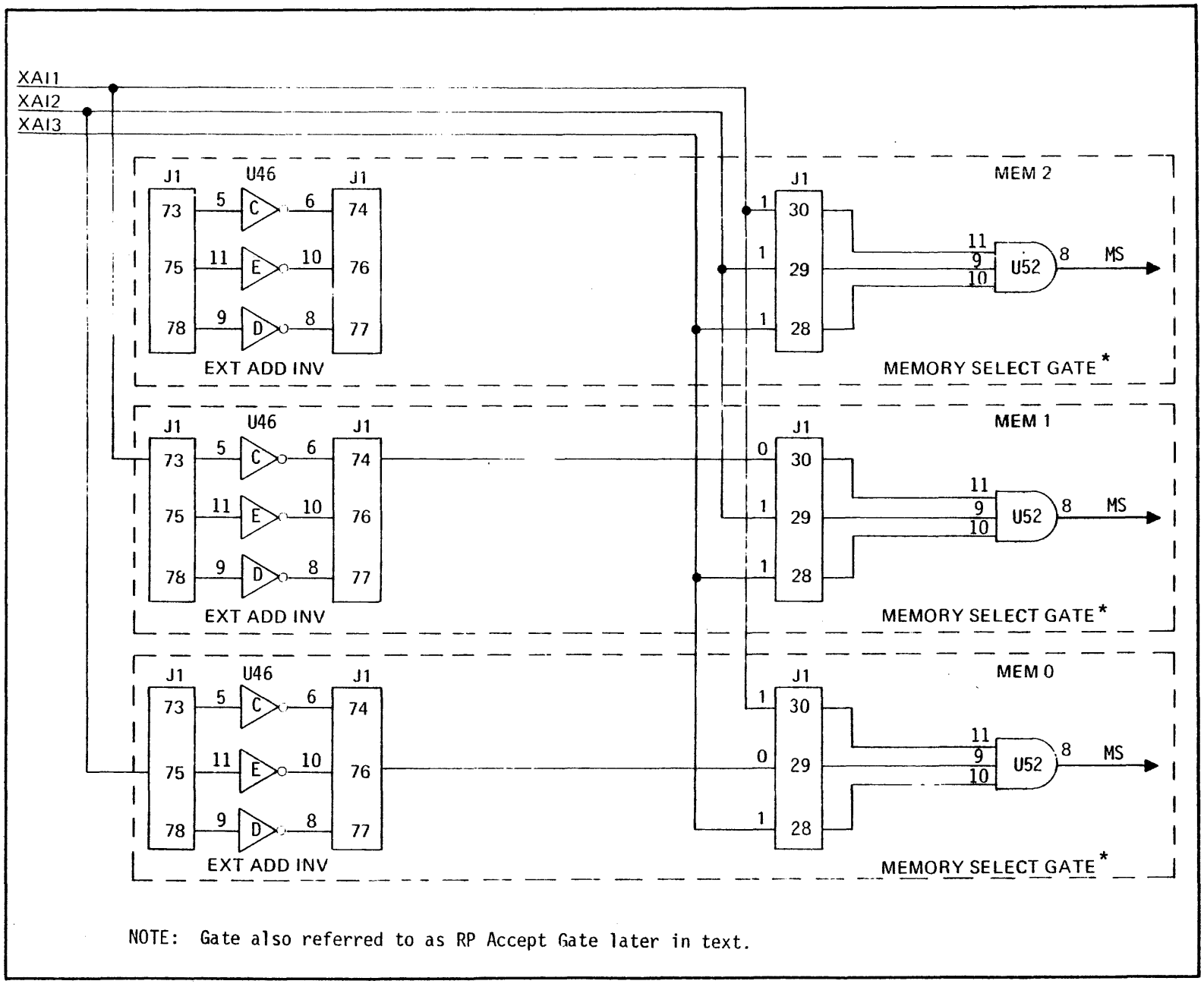


Figure 3-4. Memory Select Decode Scheme, Typical

3-21. Bias Current Regulator

3-22. The bias-current regulator consists of a voltage regulator IC (U86/RT1) and a constant-current generator (Q38/Q39). Circuit constants and the setting of (lab set) resistor R99 determine the operating current level of the current section.

3-23. In the voltage-regulator section of the circuit, thermistor RT1, located near the core matrix, changes resistance with core matrix ambient temperature. Thus, current through the core matrix changes in normal operation according to temperature.

3-24. MEMORY SELECT

3-25. When more than one Memory Card Assembly is used in a memory system, a means of selecting among the cards must be provided. This is done with the Extended Address Inverters and Memory Select Gate (figure 3-4). These inverters and gate are connected in a decoder configuration. (Note that this circuit is only typical. For exact wiring, see related system manual.)

3-26. DATA CONTROL

3-27. Data is stored or retrieved from the core matrix by use of the data-loop circuitry. Storage and retrieval actions are somewhat different; these diferences are delineated in the following subparagraphs.

3-28. GENERAL. Except for current direction in X and Y lines, addressing is the same for both Read and Write functions. Current direction, however, determines the state of the addressed cores after the operations. During Read operation, all addressed cores are cleared to (or remain cleared in) the ONE state. During Write operation, addressed cores that are not subjected to inhibit current are set to the ZERO state, those cores subjected to inhibit current remain in the ONE state*.

3-29. DATA-LOOP READ OPERATION. Prior to a Read operation, the Data register is cleared by clear signal CLR. The subsequent state

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* Set cores represent logic ZERO; cleared cores represent logic ONE.

of a given register latch depends on the state of the core addressed. Addressed cores that are in the ONE state do not affect sense circuits; thus, the Data Register for these bits remains in the ONE state (clear). Addressed cores that are in the ZERO state are cleared and the changing core flux induces a voltage pulse on the sense inhibit line. The pulse is applied to the Sense Amplifier, which is activated by Sense Amp Strobe (SAS), and then transfers the pulse to the set input of the Data Register latch. Data is routed through the output gate, which, enabled by Data Gate signals DAG, transfers ONE bits to interface lines as $\overline{\text{DOnn}}$ (low) and ZERO bits as DOnn (high).

3-30. DATA-LOOP WRITE OPERATION. A Write operation always follows a Read or Clear operation. Clear is simply a Read with no Sense Amp Strobe. In Write operation, data is gated through the input gates by Data input Strobe DIST to the set input of the previously cleared Data Register latches. A ONE bit (high) at Data Register input leaves the flip-flop in the clear state; a ZERO bit (low at Data Register input) sets the latch. Output from the Data Register is applied to the Inhibit Driver input logic.

3-31. A ZERO bit (high) from the Data Register disables the Inhibit Driver; thus, the Inhibit Drivers remain inactive, no inhibit current is applied to inhibit lines. The affected core is set to ZERO.

3-32. A ONE bit (low) from the Data Register, in conjunction with Inhibit Timing INHTn and the selected* Inhibit Select signal INHSn, activates the selected Inhibit Driver. At the same time, Inhibit Boost Drive signal INHBD momentarily activates the Boost Driver, that connects the power side of the inhibit drive transformers to +VB. The +VB voltage (about +29V) causes the inhibit current waveform to have a fast rise-time; and when the Boost Driver turns off, current is sustained by +15V applied through a diode.

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* The stack is divided into two inhibit/sense segments. Only one segment is activated at any one time. Address bit A6 $\oplus$ A14 selects the segment.

3-33. INHIBIT-DRIVER DRIVE CONTROL. Inhibit Drivers require relatively high current. To save power, the Driver input logic must be activated only when the Inhibit Drivers are needed. Drive current for these Drivers is provided by the Inhibit Timing circuit. This circuit is activated by Inhibit Timing signal INHTn.

3-34. Signal INHT is fanned out directly to all Inhibit Drivers but INHT signal is gated by exclusive ORed address bit A14 and A6 (A14 $\oplus$ A6 = SIA) to generate Inhibit Select signal INHS1 or INHS2.

3-35. The Inhibit-Driver Control circuit includes a data protection feature. This is the Data Save input. The Data Save signal, $\overline{\text{DASA}}$, is essentially a ground that is activated when a Memory Protect occurs. It is applied through isolation diodes to the resistor-buffered source voltage for the Inhibit circuit. Thus, when $\overline{\text{DASA}}$ is active, the circuit is grounded.

3-36. INHIBIT-DRIVE BOOST CONTROL. The Inhibit-Driver Boost Control circuit is a power driver that can supply the high current necessary to drive the Inhibit-Drive Boost circuit. The circuit is activated by the Inhibit Boost Timing signal INBT, and includes the data-save feature. Like the Inhibit Timing circuit, this circuit is disabled by the Data Save signal, $\overline{\text{DASA}}$, when a Memory Protect (MP) occurs. The $\overline{\text{DASA}}$ signal grounds the resistor-buffer source voltage to the circuit.

3-37. DATA SAVE. The Data Save circuit is a power driver capable of sinking several resistor-buffered voltage sources to ground. The circuit is activated by Memory Protect signal $\overline{\text{MP}}$, and when active, its output is essentially a ground ($\overline{\text{DASA}}$). Circuits that are grounded by the $\overline{\text{DASA}}$ signal are the Inhibit-Drive Control, the Inhibit-Drive Boost Control, and X and Y Core-Array Drive System (see figure 3-3).

3-38. TIMING CONTROL

3-38A. Timing Control Logic can be divided into the following functions: Clock Generator, Clock Counter, Cycle Initiate Logic, Split-cycle Control, Data-In Strobe Control, Cyte Control,

Address Configuration Control, and Data-Output/Data-Available Option Control. Because timing signals are introduced into each function, the Clock Generator and Clock Counter are discussed first.

3-39. Clock Generator

3-40. The Clock Generator is a delayed negative-feedback gate that acts as a pulse generator. When active, all inputs to the Clock Generator are high, causing a low output. This low output is routed through a delay network as negative feedback, switching off the Clock Generator Gate. Output then goes high and remains high until the positive transition propagates through the delay network - the cycle is then repeated.

3-41. Clock Counter

3-42. The Clock Counter is a cascade-type counter that, when activated, generates timing signals per figure 3-5. This Counter normally is enabled with a high input to the first flip-flop. Thus, when activated by clock signals CLK1 and CLK2 applied to alternate latches, a positive step propagates through the counter. Then, as Q16 sets, the $\overline{Q16}$ output disables the counter input gate, (U31-3) which generates a low level that propagates through the counter. In Split-Cycle mode, an output from a SC stop gate U44-8 (STOP), stops the Clock Counter at Q15 time (Split Cycle Control is described later).

3-43. Cycle-Initiate Logic

3-44. Cycle-Initiate Logic includes an Initiate Pulse ($\overline{RP}$) Input Control circuit, a Memory Busy flip-flop, the Clock Generator (already described) and a Reset Processing circuit.

3-45. Cycle Initiate

3-46. Initiate Pulse $\overline{RP}$ is routed through the RP Accept gate (U52-8) to set the flip-flop (U71/U30). Outputs from this flip-flop activate the Clock Generator and generate the Memory Busy signals,, $\overline{MB}$ and $\overline{MEMB}$. Signal $\overline{MB}$ is sent to the Processor, and $\overline{MEMB}$ is used as an enable signal for input address signals. The Memory Busy

as follows:

a. The reset signal ($\overline{GR}$ or $\overline{MP}$) goes high, and must remain high for about 4-µsec.

b. The Data Save circuit deactivates, enabling the X and Y dc sources.

c. The $\overline{RESET}$ signal goes high, enabling the MP flip-flop.

d. The high $\overline{RESET}$ signal enables the Clock Counter Gate so that when a new cycle is started, the Clock Counter will properly generate its cascade timing signals.

e. The $\overline{RES\ LOCT}$ signal goes high, allowing the RP lockout Latch to reset if the RP input is high. The next $\overline{RP}$ signal then can initiate a memory cycle.

3-55. Split-Cycle Control

3-56. Split-Cycle Control comprises the SCYL flip-flop (U49-16), WP gate (U47-8), and Split-Cycle Stop gate (U44-8). Split-Cycle signal $\overline{SC}$ is stored in the Split-Cycle flip-flop within the first 100 nanoseconds of the memory cycle. Signal SCYL enables the SC-Stop Gate (U44-8) which at Q15 time generates Split-Cycle Stop signal $\overline{SC\ STOP}$, to stop the Clock Generator. The SCYL signal also enables the WP gate (U47-8) which at time T12 admits the Write Pulse, $\overline{WP}$, to initiate the Write phase of the Split Cycle. Then, the Write Pulse, $\overline{WPUL}$, disables the SC Stop gate, allowing the Clock Generator to continue.

3-57. Data-In Strobe Control

3-58. Data-In Strobe Control logic is used to control access timing for Data-In signals. The circuit does so by determining the timing of Data-In Strobe signal DIST. This circuit accommodates the Data-In Strobe Option (MSOP). When not used, $\overline{MSOP}$ input is left open (high) and Data is strobed in at the normal time (per figure 2-3). When $\overline{MSOP}$ is active (low), Data is strobed in 200 to 300 nanoseconds later than normal. However, in Split-Cycle mode, the Data-In Strobe is dependent on the Write Pulse, $\overline{WPUL}$.

flip-flop is reset by timing signals Q15/Q16.

3-47. RP Lockout

3-48. The RP Lockout latch is connected to the RP Accept gate U52 input. This latch is activated by timing signals $\overline{Q1}$ (low) and when active applies a disabling low level to the RP Accept gate. When $\overline{Q1}$ goes high (with $\overline{RP}$ high) the RP Lockout Latch resets, discontinuing its lockout effect. The flip-flop feedback to the RP Accept gate keeps further Initiate Pulses locked out until this flip-flop resets.

3-49. Memory Select Lockout

3-50. The RP Accept gate is also used as a Memory-Select lockout element in the RP Input Control circuit. This gate, in effect is a part of a Memory-Select decoder used in a system where more than one Memory Card Assembly is included. Other elements of the decoder are the three Extended Address Inverters, U46. (Refer to paragraph 3-24).

3-51. Reset Processing (figure 3-6)

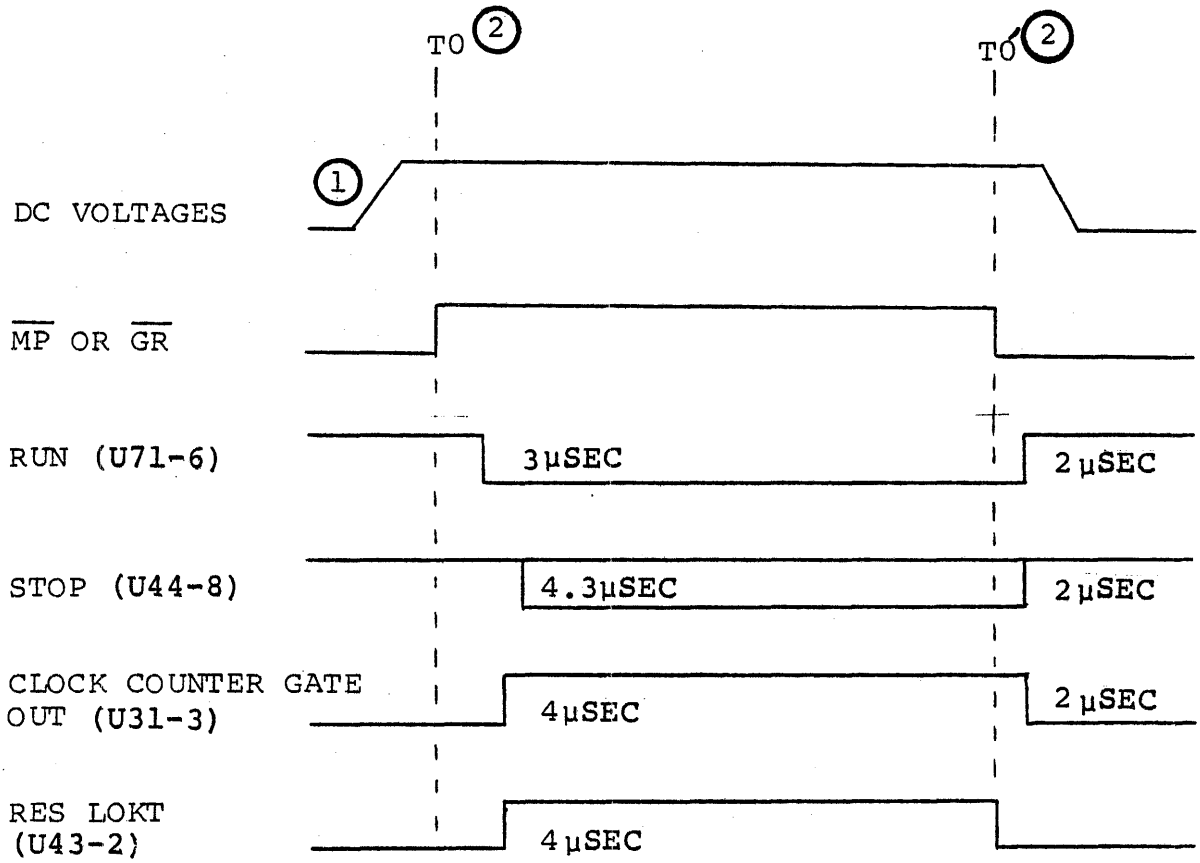
3-52. Cycle Initiate Logic circuits are reset by a General Reset signal ($\overline{GR}$) or a Memory Protect signal ($\overline{MP}$). The $\overline{GR}$ signal can occur any time; but to protect stored data, the $\overline{MP}$ signal must occur before any dc power loss.

3-53. Reset Sequence. With the reception of $\overline{GR}$ or $\overline{MP}$ signal, the following sequence occurs:

a. The RP Lockout Latch is set by the $\overline{RES\ LOKT}$ signal, preventing the RP Accept Gate from admitting any new RP signals.

b. After about a 2-µsec delay, $\overline{RESET}$ signal is generated. This signal resets the Memory Busy flip-flop. If the reset sequence is initiated by an MP signal, the Data Save circuit, after about a 5-µsec delay, generates Data Save signal $\overline{DASA}$, which disables all dc sources in the X and Y drive circuits, preventing Memory Stack currents during power up and power down.

3-54. Recovery From Reset. At the end of a reset sequence, Cycle Initiate circuitry recovers in preparation for new memory cycle



NOTE:

① DC VOLTAGES INCLUDED AS REFERENCE FOR $\overline{MP}$ ONLY.

② TIME REFERENCES FOR THIS DRAWING ONLY.

③ TIME NOTATIONS ARE WITH RESPECT TO TO AND TO. TIMES ARE APPROXIMATE.

Figure 3-6. Reset Timing Diagram

3-59. Byte Control

3-60. Byte Control logic determines mode of operation for each data byte. When Byte Control signal BCLn is high, the memory performs a Read/Restore operation on the applicable byte. When BCLn is low, the memory does a Clear/Write operation on the applicable byte. In Split-Cycle mode the memory does a Read operation on both bytes, then a restore on the byte controlled by BCLn-high, and a Write (new Data) on the byte controlled by BCLn-low. The second operation on both bytes is initiated by the Write Pulse, $\overline{WP}$.

3-61. Address Configuration Control

3-62. The Memory Card Assembly can be addressed by either of two methods: one for 32K by 20 bits and the other for 64K by 10 bits. Address Configuration Control logic is used to accommodate the Memory Card Assembly to the method used. Configurations are controlled by the state of signals COOP, and AI15. These signals are applied to the Address Configuration Control circuit (see table 3-2).

Table 3-2. Address Configuration Signals

SIGNAL	SIGNAL LEVEL FOR CONFIGURATION	
	32K x 20	64K x 10
COOP	OV (low)	Open (high)
AI15	"don't care"	Optional

3-63. The Address Configuration Control circuit affects the Byte Control circuit, the Data-In Strobe Control circuit, and the Data Gate Control circuit. For 32K x 20-bit configuration, with the COOP signal low, Byte Control output is dependent of the state of Byte Control signals BCL1 and BCL2. Also, the COOP signal (low) causes a high signal to be applied to the D inputs of the Data Gate Control flip-flops. Thus, these flip-flops set when the proper BCLn signal is routed to the C inputs. Output from either of the Data Gate Control flip-flops is routed through the Data Available latch (U35-8/6) to produce the Data Available signal,

$\overline{DA}$. The "selected" Data gate signal, however, is routed to the appropriate Data Output Gates.

3-64. For 64K x 10 bit configuration, the COOP signal is held high and both Byte Control signals are jumpered together. Under these conditions, the byte is selected by AI15 and mode by BCL1/ BCL2. Table 3-3 summarizes control-state and mode/byte relationships.

Table 3-3. Memory Address Extension Data

BCL1	BCL2	AI15	COOP	DIST 1	DIST 2	SAS1 SAS1	SAS2 SAS2	DAG1 DAG1	DAG2 DAG2	MODE/BYTE	CAPACITY
0	0	0	0	1	1	0	0	0	0	CW1/CW2	32K x 20
0	1	0	0	1	0	0	1	0	1	CW1/RR2	
1	0	0	0	0	1	1	0	1	0	RR1/CW2	
1	1	0	0	0	0	1	1	1	1	RR1/RR2	
0	0	0	1	1	0	0	1	0	0	C/W	64K x 10
		1	1	0	1	1	0	0	0		
1	1	0	1	0	0	1	1	1	0	R/R	
		1	1	0	0	1	1	0	1		

NOTE: 0 = Low
1 = High

3-65. Data-Output/Data-Available Option (TIOP)

3-66. Data Output, DOnn, and Data Available, $\overline{DA}$, signals are always generated about 300 nanoseconds after Cycle Initiate, $\overline{RP}$. Normally (without active TIOP signal) DOnn and DA signals remain on the line until the next $\overline{RP}$. However, when the TIOP signal is active (high), the DOnn and $\overline{DA}$ signals are removed from output lines 300 nanoseconds after their initial appearance.

3-67. The TIOP signal is applied to both the Data Gate Control flip-flop and Data Available gates through the timing control gates to these circuits. The Data Gate Control generates Data Gate signal DAGn, and sets the Data available latch at Sense Amp Strobe time.

When TIOP is low, the reset of Data Gate Control flip-flop and the Data Available latch depends on Read Pulse $\overline{\text{RPUL}}$ or (in Split-Cycle mode) Write Pulse $\overline{\text{WPUL}}$. When TIOP is high, the reset of these two circuits depends upon a timing signal derived from the Clock Counter. This signal occurs 500 nanoseconds after $\overline{\text{RP}}$. The TIOP signal has no effect in Clear/Write or Split-Cycle modes.

SECTION IV

MAINTENANCE

4-1. GENERAL

4-2. This section contains maintenance information for the Memory Card Assembly. Maintenance is divided into preventive and corrective tasks, and supported by tables, illustrations, and engineering drawings.

4-3. PREVENTIVE MAINTENANCE

4-4. Preventive maintenance consists of inspection and cleaning as required. However, these tasks should be done when the Memory Card Assembly MUST be removed for corrective maintenance.

4-5. INSPECTION AND CLEANING

4-6. Whenever a Memory Card Assembly MUST be removed **from its card cage for corrective maintenance, inspect and clean as follows:**

CAUTION

Circuit board containing core array should never be cleaned except as a factory maintenance procedure. Don't clean core board or expose core array to pressurized air. Memory Card Assembly must be dismantled before cleaning Electronics card. When using pressurized air at 60 psi, hold air nozzle no closer than 2 feet from surface to be cleaned.

a. Remove Memory Card Assembly from chassis.

b. **Remove screws that hold Stack Card to the** Electronics Card; separate the two subassemblies.

c. Set the Stack Card aside.

d. Spray the Memory Electronics Card with clean pressurized (60 psi max) air. Keep air nozzle beyond 2 feet from the card.

e. Reassemble Memory Card Assembly.

4-7. PCB CONNECTOR. Only when PCB MUST be removed, inspect PCB connector and clean as required:

a. Hold assembly with contacts pointed down.

b. Thoroughly saturate contacts with LPS Instant Contact Cleaner, part number ICC-16 (or equivalent).

c. Scrub contacts with soft-bristle brush.

d. Wipe contacts with soft clean cloth.

CAUTION

Contacts are gold plated and easily scratched. Never use eraser or other abrasive material to clean contacts. Also, NEVER use freon as a contact cleaner.

4-8. CORRECTIVE MAINTENANCE

4-9. Corrective maintenance consists of isolating faults within the Memory Card Assembly to the defective components. Most faults can be isolated to a small group of components by dynamic testing, using an exerciser, oscilloscope, volt/ohm/milliammeter (multimeter), digital voltmeter, and extender board. Equipment recommended for this purpose is listed in table 4-1.

Table 4-1. Recommended Test Equipment

TESTER	MANUFACTURER	MODEL
Exerciser	General Purpose	EMSE 8000
Oscilloscope	Tektronix	547
Multimeter	Simpson	260
Extender Board	EMM	926293
Digital Voltmeter	Fluke	8000A

4-10. TROUBLESHOOTING

4-11. Memory faults can be categorized as timing/control faults, data faults, and address faults. Troubleshooting in all categories

is based upon detailed knowledge of pertinent circuit operation. Theory in Section III contains circuit description to help acquire this knowledge. Refer to timing diagrams in Section III, and schematic and assembly diagrams in Section V as required. When a defective component is discovered, replace with exact replacement per parts list in Section V.

4-12. TIMING AND CONTROL FAULTS. Timing and control faults are usually characterized by complete failure to cycle in one or more modes, or failure in all or half the memory addresses or data bits. Failure to cycle is characteristic of a malfunction in the Cycle Initiate and, Mode Control circuits. Failure in all or half the address or data bits is characteristic of Inhibit, Sense-Amp Strobe, and Data-Out Gate Control circuits.

4-13. ADDRESS AND DATA FAULTS. When a fault is discovered in the address or data category, the first step is to locate the address or data bits involved. To expedite the pinpointing of address and data bits, refer to tables 4-2 and 4-3. Table 4-2 illustrates address routing and decoding from Memory Card connector input to X and Y core matrices.

WARNING

Table 4-2 also indentifies X and Y wires associated with various drive and sink decoders. This information is for troubleshooting reference use only. Do NOT attempt to repair core matrix.

4-14. TROUBLESHOOTING CHART. Table 4-3 is designed to pinpoint trouble to within a circuit area from which, with minimal effort, a defective component can be discovered using standard troubleshooting techniques. This table refers to appropriate figures, drawings, and tables which can greatly facilitate troubleshooting. The procedure in table 4-3 requires a suitable exerciser.

Table 4-2. Memory Assembly Troubleshooting Chart

PROCEDURE	INDICATIONS	PROBABLE CAUSE
A. 1. C/W (Clear/ Write) all ONEs 2. R/R (Read/ Restore).	a. All ZEROs read out at all bit positions at all addresses.	a. Faulty Inhibit Timing Control circuit (drawing 928668, sheet 3; drawing 928649).
	b. ZEROs read out at specific bit positions at all addresses.	b. Faulty Inhibit Drivers at bit positions indicated (table 4-2; drawing 928668, sheet 2 & 3; drawing 928649).
	c. ZEROs read out at random bit positions at random addresses.	c. (1) Marginal Inhibit Timing or Inhibit Boost circuit (drawing 938668, sheet 8; drawing 928649). (2) Marginal voltage: +VTH, -VA, or +VB (dwg 928668, sheet 7; dwg 928649). (3) Marginal operation of X or Y Current Source circuit (dwg 928668 sheet 7; dwg 928649)
B. 1. C/W all ZEROs 2. R/R	a. All ONEs read out at all bit positions at all addresses.	a. (1) Faulty X or Y Address Decode circuit (dwg 928668 sheets 4, 5). (2) Faulty Inhibit Timing or Inhibit Boost circuit (dwg 927393, sheet 8, dwg 928649). (3) Faulty Sense Amp Strobe Control circuit (dwg 928668 sheet 3; dwg 928649)

Table 4-2. Memory Assembly Troubleshooting Chart (cont).

PROCEDURE	INDICATIONS	PROBABLE CAUSE
	b. ONEs read out at specific bit positions at all addresses.	b. Faulty Data Loop at bit positions indicated (dwg 928668, sheet 2 & 3, dwg 928649; dwg 913999).
	c. ONEs read out at random bit position at random addresses.	c. (1) Marginal Data Control circuit: Data-In Strobe Control, Sense Amp Strobe Control, Data Gate Control (dwg 927393, sheet 6; dwg 927884) (2) Marginal voltages: +VTH, -VA, +VB (dwg 928668, sheet 7, dwg 928649).
	d. All ONEs read out at a specific small group of addresses.	d. Open diode in X or Y diode module per indicated address (table 4-2; dwg 913942; dwg 913949).
	e. All ZEROs correctly read out at a specific small group of addresses; all other addresses read out all ONEs.	e. Shorted diode in X or Y diode module per addresses operating correctly (table 4-2; dwg 913942; dwg 913949)
C. 1. C/W worst pattern 2. R/R	a. Random errors occur.	a. (1) Marginal Data Control circuit: Data-In Strobe Control, Sense Amp Strobe Control, Data Gate Control (dwg 928668, sheet 3; dwg 928649) (2) Marginal voltages: +VTH, -VA, +VB (dwg 928668, sheet 7; dwg 928649).

Table 4-2. Memory Assembly Troubelshooting Chart (cont)

PROCEDURE	INDICATIONS	PROBABLE CAUSE
D. 1. C/W Worst pattern Comp 2. R/R	a. Same as C, a.	a. Same as C, a, (1) and (2)

4-15. LOCATING DEFECTIVE CORE-STACK DIODE MODULES. Defective stack diode modules can be isolated by using information per table 4-3, item B, Symptoms d and e. To locate diodes to be checked and replaced, proceed as follows:

a. Remove screws and washers holding Stack Card in place, and gently disconnect (lift) card from Electronics card.

b. Refer to component-location drawing 913950 for location of applicable diode module.

c. Check applicable diodes with ohmmeter.

Table 5-2. Glossary of Mnemonic Terms

TERM	DEFINITION
AI (00-14)	Address In (bits 00 thru 14)
BC (1,2)	Byte Control 1,2 (flip-flop output 1 and 2)
BCL (1,2)	Byte Control Levels 1,2
BCL (1,2)F	Byte Control Levels 1,2 (flip-flop outputs 1 and 2)
CLK (1,2)	Clock 1,2
CLR (1,2)	Clear 1,2
DA	Data Available
DAG (1,2)	Data Gate 1,2
DASA	Data Save
DGC (1,2)	Data Gate Control 1,2 (flip-flop outputs 1 and 2)
DI (00-19)	Data-In 00 thru 19
DIST (1,2)	Data-In Strobe 1,2
DO (00-19	Data-Out 00 thru 19
EF (1-12)	E-tap False 1 thru 12 (clock counter false outputs)
EQ (1-12)	E-tap Q-output 1 thru 12 (clock counter true outputs)
GR	General Reset
I (0-19)A	Inhibit Drive A, 0 thru 19
I (0-19)B	Inhibit Drive B, 0 thru 19
IBD	Inhibit Boost Drive
INBT	Inhibit Boost Timing
INHS (1,2)	Inhibit Select 1 and 2
INHT	Inhibit Timing
INHT (1,2)	Inhibit Timing 1 and 2
INTA (00-14	Internal Address 00 thru 14
LOKT	Lockout
MB	Memory Busy (interface signal)
MBFF	Memory Busy Flip-Flop

SECTION V

DRAWINGS

5-1. GENERAL

5-2. This section contains assembly drawings, parts lists, and schematic diagrams for the MICROMEMORY 3000QD Memory Card Assembly. These drawings are listed in table 5-1 in assembly breakdown order, and are compiled for convenient use. Mnemonic terms used in drawing illustrations are listed in table 5-2.

Table 5-1. Engineering Drawings

TITLE	DRAWING NUMBER
Memory Assembly 32K X 20	928647-001
Memory Card Assembly	929664
Parts List	PL929664-001
Schematic	928668
Stack Assembly	913950
Parts List	PL913950-001
Schematic (sheets 2&#)	913942
Matrix Assembly, (Wired)	913949
Parts List	PL913949-001

5-3. SCHEMATIC REFERENCE CODE

5-4. Sheet tagging references on the schematics are coded by sheet number and zone, and are placed in parentheses. For example, reference (3B5) means that the signal is connected to equipment shown on sheet 3, zone B5. A reference number on sheet 3 will, in turn, refer back to the location of the first reference number.

Table 5-2. Glossary of Mnemonic Terms (Cont)

TERM	DEFINITION
MEMB	Memory Busy (internal signal)
MP	Memory Protect
MS	Memory Select
MS (1-3)	Memory Select 1 thru 3
MSOP	Memory Strobe Option (memory register strobe)
RESDLD	Reset Delayed
RES LOKT	Reset Lockout
RP	Read Pulse (cycle initate)
RPB	Read Pulse Buffered
RPUL	Read Pulse (internal cycle initiate)
RST	Read Sink Timing
RXBT	Read X Boost Timing
RXD (0-7)	Read X Drive 0 thru 7
RXD (8-15)	Read X Drive 8 thru 15
RXDT	Read X Drive Timing
RYBT	Read Y Boost Timing
RYD (0-7)	Read Y Drive 0 thru 7
RYD (8-15)	Read Y Drive 8 thru 15
RYDT	Read Y Drive Timing
SAS	Sense Amp Strobe
SAS TERM (1,2)	Sense Amp Strobe Terminations 1 and 2
SC	Split Cycle (interface signal)
SCYL	Split Cycle (internal signal)
SKV	Sink Voltage
TDEL	Timing Delayed
TNORM	Timing Normal
TIOP	Timing Option
VA	Voltage A (approximately -5V)
VB	Voltage, Boost (approximately +30V)
VTH	Voltage Threshold (sense amp threshold)
WDT	Write Drive Timing
WP	Write Pulse (finish split cycle interface signal)

Table 5-2. Glossary of Mnemonic Terms (Cont)

TERM	DEFINITION
WPB	Write Pulse Buffered
WPUL	Write Pulse (finish split cycle internal signal)
WST	Write Sink Timing
WXBT	Write X Boost Timing
WXD (0-7)	Write X Drive 0 thru 7
WXD (8-15)	Write X Drive 8 thru 15
WYBT	Write Y Boost Timing
WYD (0-7)	Write Y Drive 0 thru 7
WYD (8-15)	Write Y Drive 8 thru 15
XAI (1-3)	Extended Address In 1 thru 3
XCA (0-15)	X Common Anode 0 thru 15
XCC (0-15)	X Common Cathode 0 thru 15
XS (0-7)R	X Sink 0 thru 7 Read
XS (0-7)W	X Sink 0 thru 7 Write
XSK (0-7)	X Sink 0 thru 7
YCA	Y Common Anode 0 thru 15
YCC	Y Common Cathode 0 thru 15
YS (0-7)R	Y Sink 0 thru 7 Read
YS (0-7)W	Y Sink 0 thru 7 Write
YSK (0-7)	Y Sink 0 thru 7

5-5. REPLACEABLE PARTS

5-6. The parts lists in this section may be used for ordering Memory Card Assembly replacement or spare items. For each parts list item there is an identifying reference designation or item number. Reference designators and item numbers are also called out on corresponding assembly drawings which show the location of each item. Parts can be ordered directly from vendors and may be ordered by commercial or JEDEC numbers.

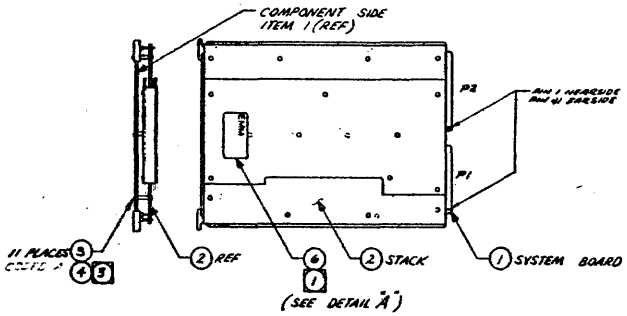
PART IDENTIFICATION
MARK PART NUMBER & PART REV. PER EMES 6-1

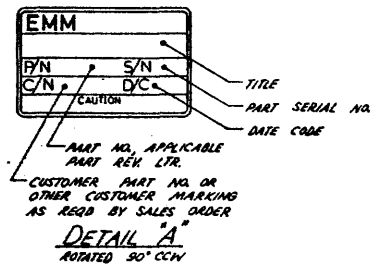
TABULATED DATA

PART NUMBER	PART REV.	SUPPORTING DOCUMENT	CONFIG.	SPECIAL FEATURE
928647-001	B	PL 928647-001	32K x 20	STD
928647-002	B	PL 928647-002	32K x 18	STD
928647-003	B	PL 928647-003	32K x 16	STD
928647-004	B	PL 928647-004	32K x 18	HI TRIP LO VOLTAGE

REVISIONS

AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
DAVE STOTT		XA	INITIAL PROTOTYPE RELEASE	7-3-75	GLF
		XB	CCA WAS 928649-XXX. ADV PART REVS	12-4-75	RB
DAVE STOTT		C	PRODUCTION RELEASE	2-24-76	RB





DETAIL "A"
ROTATED 90° CCW

3 APPLY FN 4 TO FN 3 AFTER FINAL TEST.

2. ASSEMBLE AND INSPECT PER FN 3.

1 LOCATE ITEM 6 APPROX. WHERE SHOWN AND TYPE INFORMATION AS NOTED.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO. & QTY PER ASSY

SEE PART IDENT BLOCK FOR PART MARKING REQT

FINAL

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

ITEM | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION/MATERIAL | SPEC/SOURCE | CODE IDENT NO. | FIND NO.

PARTS LIST

CONTRACT NO.

DRAWN	Daniel Mercado	7/1/75
CHECK	G. Stotter	7-2-75
ENGR	G. Stotter	7-2-75
PROJ ENGR	[illegible]	12-1-75
PROG ENGR	[illegible]	2-24-76
OTHER APPROVALS	[illegible]	8-29-96

emm MEMORY PRODUCTS GROUP
ELECTRONIC MEMORIES & MAGNETICS CORPORATION

CARD MEMORY ASSEMBLY, MICROMEMORY 3000/3220

SIZE D | CODE IDENT NO. 16224 | DWG NO. 928647

SCALE: NONE | WEIGHT | SHEET 1 of 1

DATA NO. 1016

928647

PART IDENTIFICATION MARK PART NUMBER & PART REV. PER EMMS 6-1		TABULATED DATA	
PART NUMBER	PART REV.	SUPPORT DOCUMENT	CONFIG.
929664-001	B	PL 929664-001	32K x 20
929664-002	A	AI 929664-002	32K x 18
929664-003	A	AI 929664-003	32K x 16
929664-004	A	AI 929664-004	32K x 18

JUMPER CHART		
FROM	TO	SIGNAL
E75	E4	Q0
E75	E67	Q0
E86	E3	$\overline{Q0}$
E65	E9	Q2
E7	E56	Q1
E7	E42	Q1
E62	E47	Q1
E63	E8	$\overline{Q1}$
E63	E77	$\overline{Q1}$
E8	E6	$\overline{Q1}$
E6	E49	$\overline{Q1}$
E49	E1	$\overline{Q1}$
E60	E67	Q0
E81	E10	$\overline{Q2}$
E41	E69	$\overline{Q2}$
E69	E79	$\overline{Q2}$
E40	E11	Q3
E44	E12	$\overline{Q3}$
E43	E13	Q4
E40	E17	Q6
E69	E12	$\overline{Q3}$
E45	E19	Q7
E82	E21	Q8
E32	E70	Q8
E21	E50	Q8
E66	E20	$\overline{Q8}$
E55	E24	$\overline{Q9}$
E52	E25	Q10
E51	E26	$\overline{Q10}$
E78	E27	Q11
E73	E30	$\overline{Q12}$
E62	E29	Q12
E54	E29	Q12
E46	E32	$\overline{Q13}$
E85	E31	Q13
E76	E32	$\overline{Q13}$
E76	E61	$\overline{Q13}$
E61	E57	$\overline{Q13}$
E54	E53	Q14
E53	E34	$\overline{Q14}$
E59	E35	Q15
E35	E91	Q15
E39	E37	Q16
E72	E38	$\overline{Q16}$
E5	E33	$\overline{Q16}$
E5	E84	$\overline{Q16}$
E87	E88	+V8
E67	E89	+V9
E83	E74	
E90	E91	RP short
E92	E93	DASA
E94	UVS-11	BCL2F
E95	UVS-3	BCL1F

REVISIONS					
MSTR	ZONE	LTR	DESCRIPTION	DATE	APPROVED
EM		XA	INITIAL PROTOTYPE RELEASE	10-22-74	Q
EM		XB	UNDER DEBUG CHGS: ADV PART REV TO XB	12-19-74	RB
EM		C	PRODUCTION RELEASE	2-24-75	RB

5. ASSEMBLE AND INSPECT PER EN 150.

(4) REMOVE SOLDERMASK AND LAP SOLDER TO TRACE.

(3) C187 TO BE PARALLELED WITH R72 AND FOLDED OVER R70-R71.

2. MAXIMUM COMPONENT HEIGHT NOT TO EXCEED .350 INCH.

1. POLARITY CONVENTION:

—▭— HEAVY LINE INDICATES CATHODE END OF DIODE.
\+ INDICATES POSITIVE END OF A CAPACITOR.
• INDICATES PIN 1 OF A MULTILEAD DEVICE.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST			

DASH NO. & QTY PER ASSY

SEE PART IDENT BLOCK FOR PART MARKING RECT

DO NOT SCALE DRAWING

CONTRACT NO.

DRAWN R. Lukins 10-21-74
CHECK RB
ENGR
PROJ. ENGR
PROD. CONTROL
OTHER APPROVALS Schmidt 2-25-75

EMM MEMORY PRODUCTS GROUP
ELECTRONIC MEMORIES & MAGNETICS CORPORATION

CIRCUIT CARD ASSY.
MICROMEMORY 3000/3220

SIZE D | CODE IDENT NO. 16224 | DWG NO. 929664

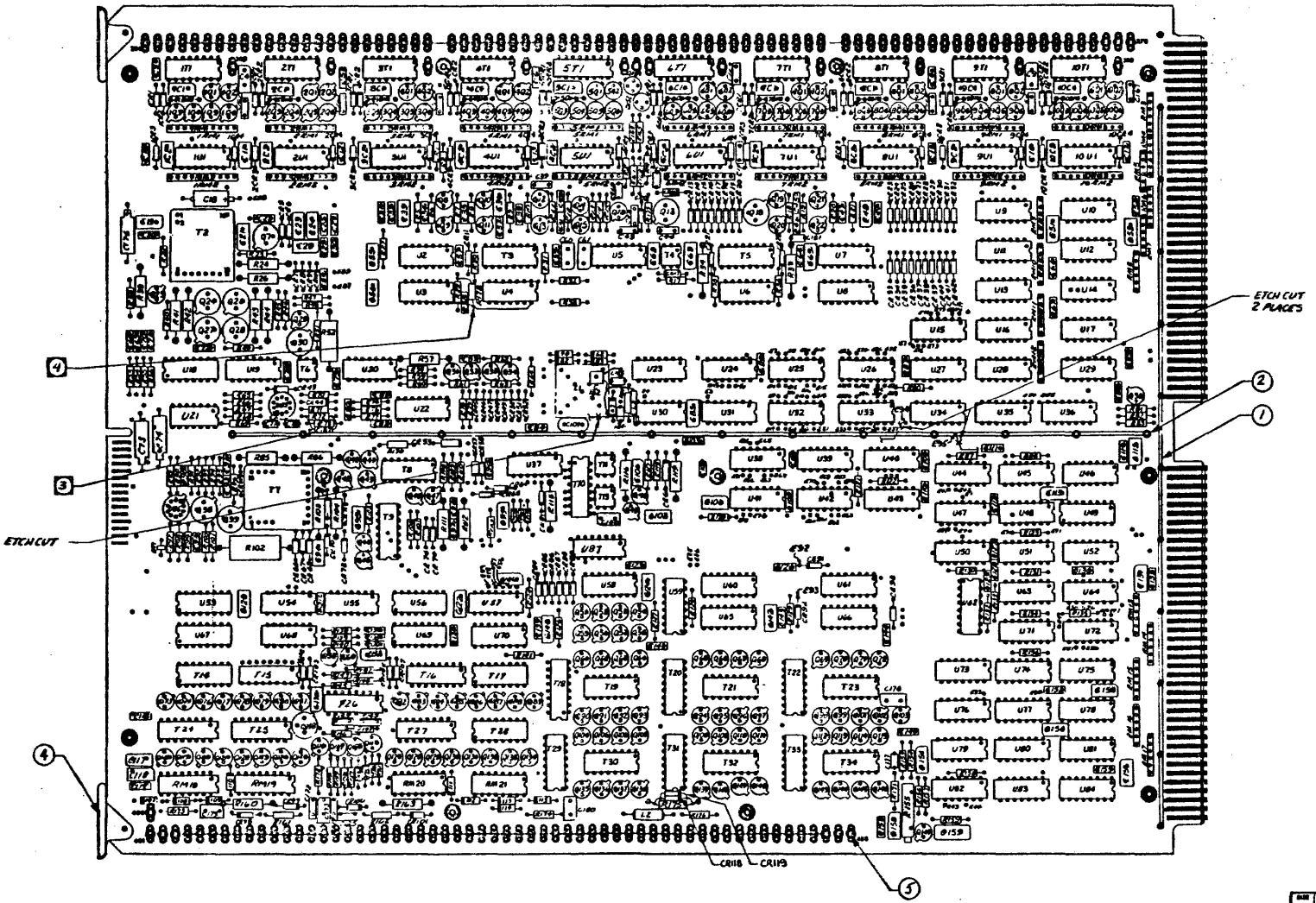
SCALE — | WEIGHT | SHEET 1 of 2

DATE NO. 10/6

C ONLY

929647	
NEXT ASSY	USED ON
APPLICATION	

REVISIONS							
LTR	DESCRIPTION	DATE	APPROVED
	SEE SHEET 1		



NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO	DWG NO
D	16224	929664
SCALE:	WEIGHT:	SHEET 2 of 2

929664

electronic memories HAWTHORNE, CALIF.
A DIVISION OF
ELECTRONIC MEMORIES & MAGNETICS CORP.

CODE IDENT NO. 16224 | PL 929664-001 | SHEET 2 | C REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	1	1	925806-001	BUSS / STIFFENER			
	2	1	925806-005	BUSS/STIFFENER			
	3	1	929665-001	PRINTED WIRING BOARD			
	4	2	984502-001	EXTRACTOR			
	5	149	984511-001	RECEPTACLE			
	6	A/R	SN63WRMA-P3	SOLDER		22-5-571	
	7						
	8						
	9						
	10						
	11	79	CK06BX103K	CAP .01 uf 200V 10%	C3,C5,6,8,10,12,13,14,15,17,20,22,26,27,29,30		
	12				31,32,33,34,43,44,46,49,52,54,57,58,64,66,67		
	13				75,76,79,80,86-89,91,92,93,96,103,105,108,110,111		
	14				112,114,116,119,121,123,125,132,135,136,138,139,141,143		
	15				144,149,152,155,157,160-167,174,124,125		
	16	2	CK06BX332K	CAP 3300pF 10%	C68,71		
	17	2	CK05BX221K	CAP 220 pf 10%	C109, C129		
	18	1	CK05BX330K	CAP 33 pf 10%	C82		
	19	1	CK06BX104K	CAP 0.1 uf 10%	C83		

electronic memories HAWTHORNE, CALIF.
A DIVISION OF
ELECTRONIC MEMORIES & MAGNETICS CORP.

CODE IDENT NO. 16224 | PL 929664-001 | SHEET 3 | C REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	20	7	CK05BX102K	CAP 1000 pf 10%	C40,C47,77,78,90,123,177		
	21	6	CK05BX101K	CAP 100 pf 10%	C34,C35,58,107,168,169		
	22	2	CK06BX152K	CAP 1500 pf 10%	C38,C45		
	23	6	CK05BX331K	CAP 330 pf 10%	C42,72,81,127,145,146		
	24	1	CM05ED750J03	CAP 75 pf 5%	C159.		
	25	1	CSR13G156KL	CAP TA 15 uf 50V 10%	C18.		
	26	12	999537-001	CAP TIM 4.7 uf 50V 10%	C28,C62,IC1-10C1		
	27	1	CM05ED470J03	CAP 47 pf 5%	C104		
	28	60	999525-011	CAP TIM 15 uf 25V	C4,9,11,16,19,21,23,24,33,36,48,51,53,55,56,60,61,63,65		
	29				85,94,95,99,100,101,102,106,113,115,117,118,120		
	30				122,124,131,137,140,142,151,153,154		
	31				156,158,IC2-10C2,170,173,178-180,186,187		
	32	3	CSR13F685KL	CAP 6.8 uF 10% 35V	C73,74,176		
	33	2	CK05BX681K	CAP 680 pF 10%	C131,181		
	34	1	CM05ED220J03	CAP 22pF 5%	C182		
	35	1	CK06BX472K	CAP 4700 pF 10%	C69		
	36	10	912206-A14	DIODE MOD 7225B TYPE	1DM1-10DM1		
	37	1	999203-003	DIODE ZENER 6.2 V IN753A	CR44		
	38	1	999208-005	DIODE ZENER 10V IN961B	CR53		

PARTS LIST

NOTE	FIND NO.	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	39	1	999203-001	DIODE ZENER IN751A	CR 61		
	40	14	999206-001	DIODE	CR 62, 63		
	41				CR 5-13, 15-18, 20-43, 45-52 54 58 59, 66-72, 74 76-79 81-105 107-119		
	42				1CR1-10CR1, 1CR2-10CR2, 1CR3-10CR3, 1CR4-10CR4		
	43						
	44						
	45						
	46	2	999101-006	I.C. SN7406	U2, U7		
	47	14	999101-007	I.C. SN7407	1U1-10U1, U9 37, 54, 68		
	48	2	999101-008	I.C SN7408	U21, U39,		
	49	5	999101-038	I.C. SN7438	U10, 12, 14, 17, 24		
	50	9	999101-045	I.C. SN7445	U53, U56, U58, U60, U61, U65, U66, U67, U69		
	51	1	999101-074	I.C. SN7474	U20		
	52	1	999101-075	I.C. SN7475	U49		
	53	1	999101-076	I.C. SN7476	U18		
	54	4	999101-150	I.C. SN74H50	U5, U57, U73, U76		
	55	10	999101-300	I.C. SN74S00	U23, U34, U38, U40, U42, U48, U55, U61, U71, U79		
	56	5	999101-304	I.C. SN74S04	U43, U46, U5 U80 U83,		
	57	-	999101-308	I.C. SN74S08	U31, U45, U72, U15		

PARTS LIST

NOTE	FIND NO.	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	58	3	999101-310	I.C. SN74S10	U30, U35, U63		
	59	3	999101-311	I.C. SN74S11	U8, U24, U36,		
	60	2	999101-320	I.C. SN74S20	U44, U47,		
	61	1	999101-330	I.C. SN74S30	U52,		
	62	11	999101-338	I.C. SN74S38	U3 4, 6, 9, 11, 13, 16, 28, 41, 50, 82		
	63	1	999101-374	I.C. SN74S74	U27,		
	64	1	999101-714	I.C. SN74S138	U59,		
	65	6	999101-395	I.C. SN74S157	U74, U75, U77, U78, U81, U84		
	66	4	999101-391	I.C. SN74S175	U25, U26, U3 U33		
	67	1	999106-004	I.C. UA711	U85		
	68	1	999110-001	I.C. UA723	U86		
	69	2	999109-001	I C UA9602	U22, U62,		
	70						
	71						
	72						
	73	1	RC07GF330J	RES. 33 1/4 W 5%	R45		
	74	6	RC07GF2R7J	RES. 2.7 1/4W 5%	R38, 148, 149, 150, 151, 176		
	75	2	RC07GF3R3J	RES. 3.3 1/4W 5%	R94, R95		
	76	2	RC07GF470J	RES. 47 1/4W 5%	R153, 172		

electronic memories HAWTHORNE, CALIF. A DIVISION OF ELECTRONIC MEMORIES & MAGNETICS CORP.		CODE IDENT NO. 16224	PL 929664-001	C
			SHEET 6	REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	77	4	RC07GF820J	RES. 82 1/4W 5%	R30, R142, R143		
	78	2	RC07GF132J	RES. 1.3K 1/4W 5%	R3, R4,		
	79	16	RC07GF101J	RES. 100 1/4W 5%	R29, R32, R36, R47, R77, R90 R93 R106, R107, R108		
	80				R109, R122, R127, R129, R146, R147		
	81	1	RC07GF121J	RES. 120 1/4W 5%	R141		
	82	9	RC07GF151J	RES. 150 1/4W 5%	R5, R146, 67, 132, 133, 139, 164, 165		
	83	11	RC07G221J	RES. 220 1/4W 5%	R11, R21, 31, 35, 96, 161, 162, 167, 169, 173, 174		
	84	5	RC07GF331J	RES. 330 1/4W 5%	R70, R101, 144, 145, 177		
	85	11	RC07GF471J	RES. 470 1/4W 5%	R9, R17, R19, R27 R51, R82, R84 R120, R156, R157, 170		
	86	18	RC07GF102J	RES. 1K 1/4W 5%	R6, R8, R10, R12, R13, R14 R15, R49, R20, 23, 33, 40, 59, 60, 62, 158, 159, 171,		
	87	5	RC07GF152J	RES. 1.5K 1/4W 5%	R53, 54, 71, 139, 140,		
	88	3	RC07GF182J	RES. 1.8K 1/4W 5%	R1, R2, R69		
	89	18	RC07GF222J	RES. 2.2K 1/4W 5%	R48, 55, 56, 61, 65, 66, 1, 74, 78, 80, 83, 88, 124, 125, 130, 135, 136		
	90	1	RC07GF302J	RES. 3K 1/4W 5%	R121,		
	91	3	RC07GF472J	RES. 4.7K 1/4W 5%	R63, R81, R1		
	92	3	RC07GF103J	RES. 10K 1/4W 5%	R58, R76, R134		
	93	2	925703-001	RES., ASSORTMENT, LAB SET	29, 9		
	94	1	RC07GF682J	RES. 6.8K 1/4W 5%	R15,		
	95						

electronic memories HAWTHORNE, CALIF. A DIVISION OF ELECTRONIC MEMORIES & MAGNETICS CORP.		CODE IDENT NO. 16224	PL 929664-001	C
			SHEET 7	REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	96	7	RC20GF1R0J	RES. 1.0 1/2W 5%	R24, 26, 39, 41, 42, 43, 44		
	97	1	RC20GF120J	RES 12 1/2 W 5%	R175		
	98	2	RC20GF271J	RES. 270 1/2W 5%	R111, R112,		
	99	2	RC20GF391J	RES. 390 1/2W 5%	R85, R104		
	100	2	RC20GF471J	RES. 470 1/2W 5%	R34, R37		
	101	1	RC20GF911J	RES. 910 1/2W 5%	R57		
	102	2	RC20GF221J	RES 220 1/2W 5%	R86, 119		
	103	1	RC32GF330J	RES. 33 1W 5%	R52		
	104	1	RL07S472G	RES. 4.7K 1/4W 2%	R98		
	105	1	RL07S331G	RES. 330 1/4W 2%	R100		
	106	1	RL07S132G	RES. 1.3K 1/4W 2%	R97		
	107	2	RL07S202G	RES. 2K 1/4W 2%	R69, R72,		
	108	1	RL07S392G	RES. 3.9K 1/4W 2%	R22,		
	109	1	RL07S512G	RES. 5.1K 1/4W 2%	R68		
	110	2	RL07S682G	RES. 6.8K 1/4W 2%	R89, R92,		
	111	1	RL07S223G	RES. 22K 1/4W 2%	R73		
	112	1	RC20GF241J	RES 240 1/2 W 5%	R103		
	113						
	114	1	999502-027	RES. WW 5.0 2W 1%	R102		

PARTS LIST

NOTE	FIND NO.	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	115						
	116	1	999545-003	RES. POT 10K	R 155		
	117	1	999605-002	RES. THERMISTOR 2 D102	RT1		
	118	4	922135-009	RES MOD 110	RM18, RM19 RM20, RM21		
	119	10	999551-001	RES. MOD 270/910/1.3K	1RM2-10RM2		
	120	10	999551-002	RES MOD 120/470	1RM1-10RM1		
	121	11	999551-005	RES. MOD 328/410	RM3, RM4, RM5, RM6, RM7, 8, 13, 14, 15, 16, 17		
	122	4	999551-007	RES. MOD 4.7K	RM9 RM10, RM11, RM12		
	123	2	RC20GF470J	RES 47 1/2W 5%	R160, 163		
	124	1	RC07GF821J	RES 820 1/4W 5%	R154		
	125						
	126						
	127	1	999415-001	XFMR - L1 SQUARE LOOPS	T7		
	128	1	999439-001	XFMR - 2L/2:1 (POWER)	T2		
	129	11	999440-001	XFMR 2:1 INHIBIT	1T1 - 10T1		
	130	24	999403-002	XFMR 2:1 BASE DRIVE	T3, 5, 8, 9 T11-25, T27-34		
	131	2	999441-002	XFMR SINGLE BALUN	T4, T6,		
	132	1	999416-009	INDUCTOR 1.0mH	L3		
	133	1	999416-011	INDUCTOR 1.5mH	L2	NYTRONICS INC.	

electronic memories HAWTHORNE, CALIF.
A DIVISION OF
ELECTRONIC MEMORIES & MAGNETICS CORP.

CODE IDENT NO. 16224

PL 929664-001 C

SHEET 9 REV

PARTS LIST

NOTE	FIND NO.	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	134	11	922114-001	TRANSISTOR TO5 50V	Q7, Q17, Q18, 24, 26, 27, 28, 30, 38, 39, 143		
	135	166	922125-001	TRANSISTOR TO18 50V	Q8, Q9, 10, 11, 16, 23, 29, 31, 32, 33, 34 Q40-Q47		
	136				Q59-Q74, Q76-Q99, Q101-Q124, Q126-Q146,		
	137				1Q1-10Q1, 1Q2-10Q2, 1Q3-10Q3, 1Q4-10Q4		
	138				1Q5-10Q5, 1Q6-10Q6, 3149, 150		
	139	12	999302-001	TRANSISTOR 2N2369A	Q12, Q13, Q14 Q15, Q19, Q20, Q21, Q22, Q36, 147, 151, 152		
	140	8	999304-001	TRANSISTOR 2N2894A PNP	Q51-Q58		
	141						
	142						
	143						
	144						
	145	A/R	922600-036	WIRE AWG 30 TEFLON			
	146						
	147						
	148	REF	EMPS 6-1	SPEC, MARKING			
	149	REF	922668	SCHEMATIC			
	150	REF	924100	WORKMANSHIP STANDARD			
	151						
	152						

REVISIONS					
AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
DWG 3168		A	PRODUCTION RELEASE	7-14-4	LB

PART IDENTIFICATION
MARK PART NUMBER & PART REV.
PSD ____

PART NUMBER	PART REV.

CONNECTOR PIN CHART P1

COMP SIDE		SOLDER SIDE	
SIGNAL	PIN	SIGNAL	PIN
0V	1	0V	41
+5V	2	+5V	42
-15V	3	-15V	43
0V	4	0V	44
+15V	5	+15V	45
+V TERM	6	AI08	46
TERM	7	AI07	47
	8	AI06	48
	9	AI11	49
	10	AI10	50
	11	0V	51
	12	AI09	52
	13	AI03	53
	14	0V	54
	15	AI04	55
	16	AI05	56
	17	0V	57
	18	AI00	58
	19	AI01	59
	20	0V	60
	21	AI02	61
	22	AI12	62
	23	GR	63
	24	AI14	64
	25	WP	65
TERM	26	0V	66
SC	27	0V	67
MS 3	28	DI18	68
MS 2	29	DI19	69
MS 1	30	AI15	70
BCL 2	31	DO18	71
COOP/ADOP	32	DO19	72
MB	33	XAI1	73
AI 3	34	XAI1	74
BCL 1	35	XAI2	75
DA	36	XAI2	76
TIOP	37	XAI3	77
MEM PROTECT	38	XAI3	78
MSOP	39	RP	79
0V	40	0V	80

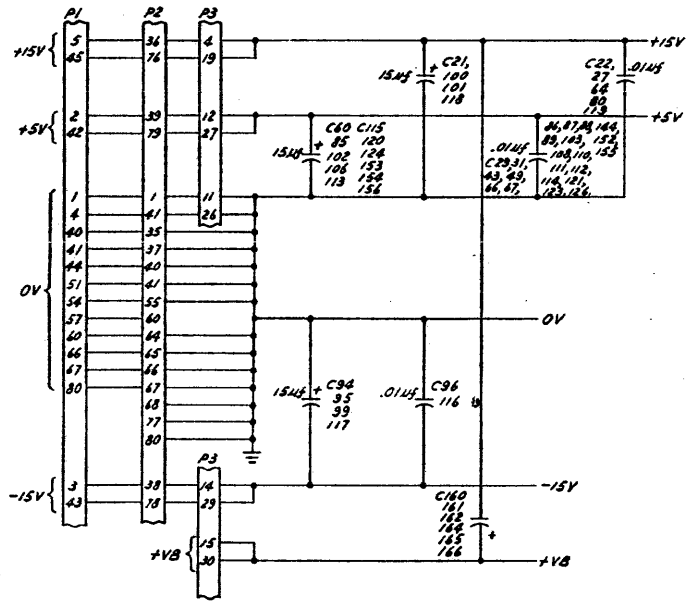
CONNECTOR PIN CHART P2

COMP SIDE		SOLDER SIDE	
SIGNAL	PIN	SIGNAL	PIN
0V	1	0V	41
DI06	2	DI01	42
DI07	3	DI00	43
DI05	4	DI08	44
DI04	5	DI17	45
DO06	6	DO03	46
DO07	7	DO02	47
DO05	8	DO01	48
DO04	9	DO00	49
DI03	10	DO08	50
DI02	11	DO17	51
TERM	12	DI16	52
	13	DO16	53
	14	DO15	54
	15	0V	55
	16	DI15	56
	17	DI14	57
	18	DO14	58
	19	DO13	59
	20	0V	60
	21	DI13	61
	22	DI12	62
	23	DO12	63
	24	0V	64
	25	0V	65
	26	0V	66
	27	0V	67
	28	0V	68
	29	DO11	69
	30	DI11	70
	31	DI10	71
	32	DO10	72
	33	DO09	73
+V TERM	34	DI09	74
0V	35	+V TERM	75
+15V	36	+15V TERM	76
0V	37	0V	77
-15V	38	-15V	78
+5V	39	+5V	79
0V	40	0V	80

CONNECTOR PIN CHART P3

COMP SIDE		SOLDER SIDE	
SIGNAL	PIN	SIGNAL	PIN
——	1	——	16
——	2	CURRENT MARGIN	17
——	3	——	18
+15V	4	+15V	19
——	5	——	20
——	6	——	21
VB MARGIN	7	——	22
-VA MARGIN	8	——	23
VTH MARGIN	9	——	24
——	10	——	25
0V	11	0V	26
+5V	12	+5V	27
-VA	13	-VA	28
-15V	14	-15V	29
+VB	15	+VB	30

LAST REF DESIG USED		REF DESIGNATION NOT USED
C	181	
CR	119	
DL		
DM	10DM1	
E	30	
L	3	
Q	152	
QM	10Q6	
R	178	
RM	21	
T	34	
U	86	
W		



2. ALL CAPACITOR VALUES ARE IN MICROFARADS.
1. ALL RESISTOR VALUES ARE IN OHMS.
NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO. & QTY PER ASSY	NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
SEE PART IDENT BLOCK FOR PART MARKING REQT			PARTS LIST			
		929664				
		928647				
NEXT ASSY	USED ON					
APPLICATION						

DO NOT SCALE DRAWING

CONTRACT NO.

DRAWN	K.M.T.	3-4-76
CHECK		
ENGR	Comerford	2-27-76
PROD. ENGR		2-27-76
PROD. DESIGN		7-14-76
OTHER APPROVALS		

MEMORY PRODUCTS GROUP
ELECTRONIC MEMORIES & MAGNETICS CORPORATION

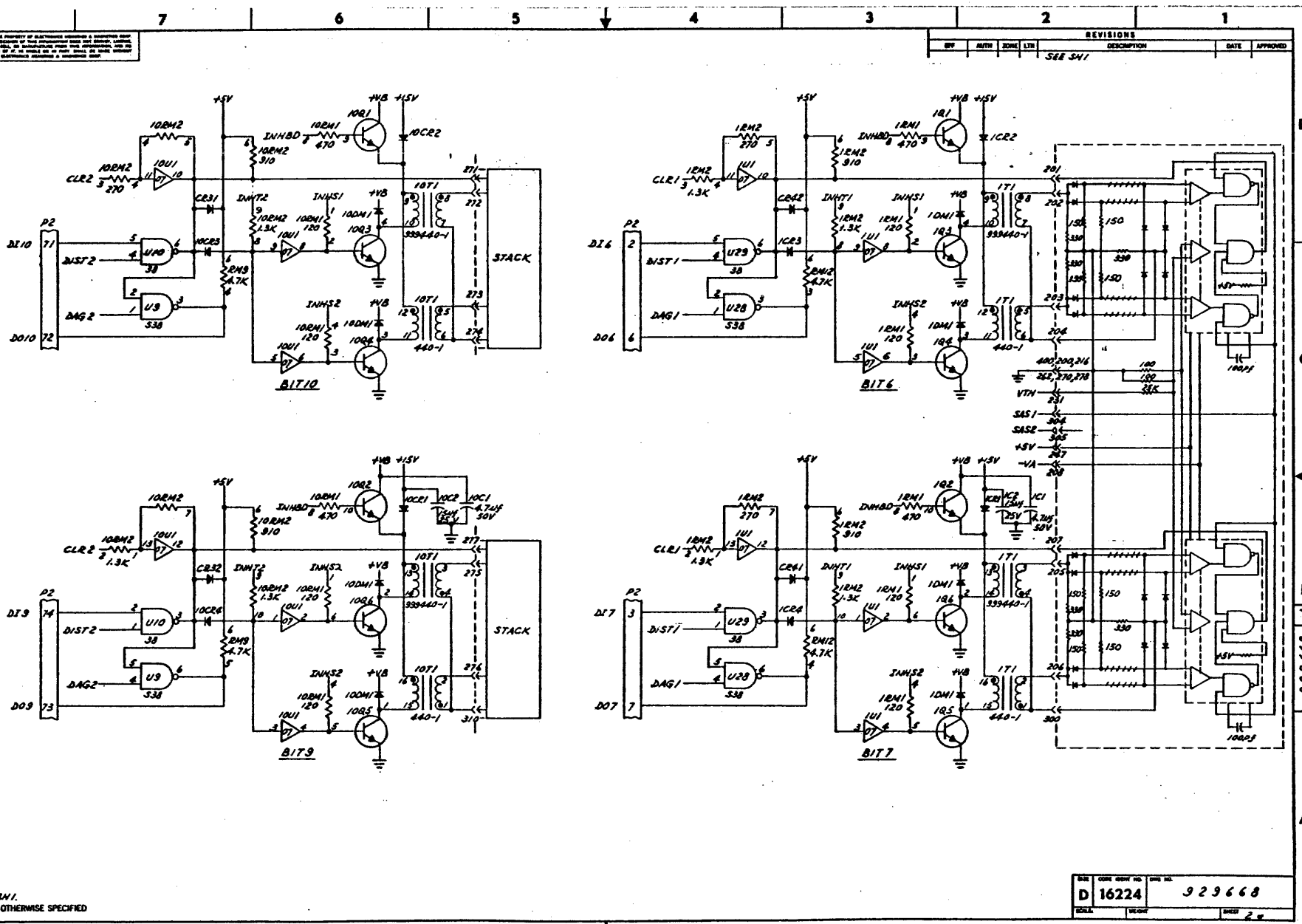
SCHEMATIC DIAGRAM, MICROMEMORY 3000/3220

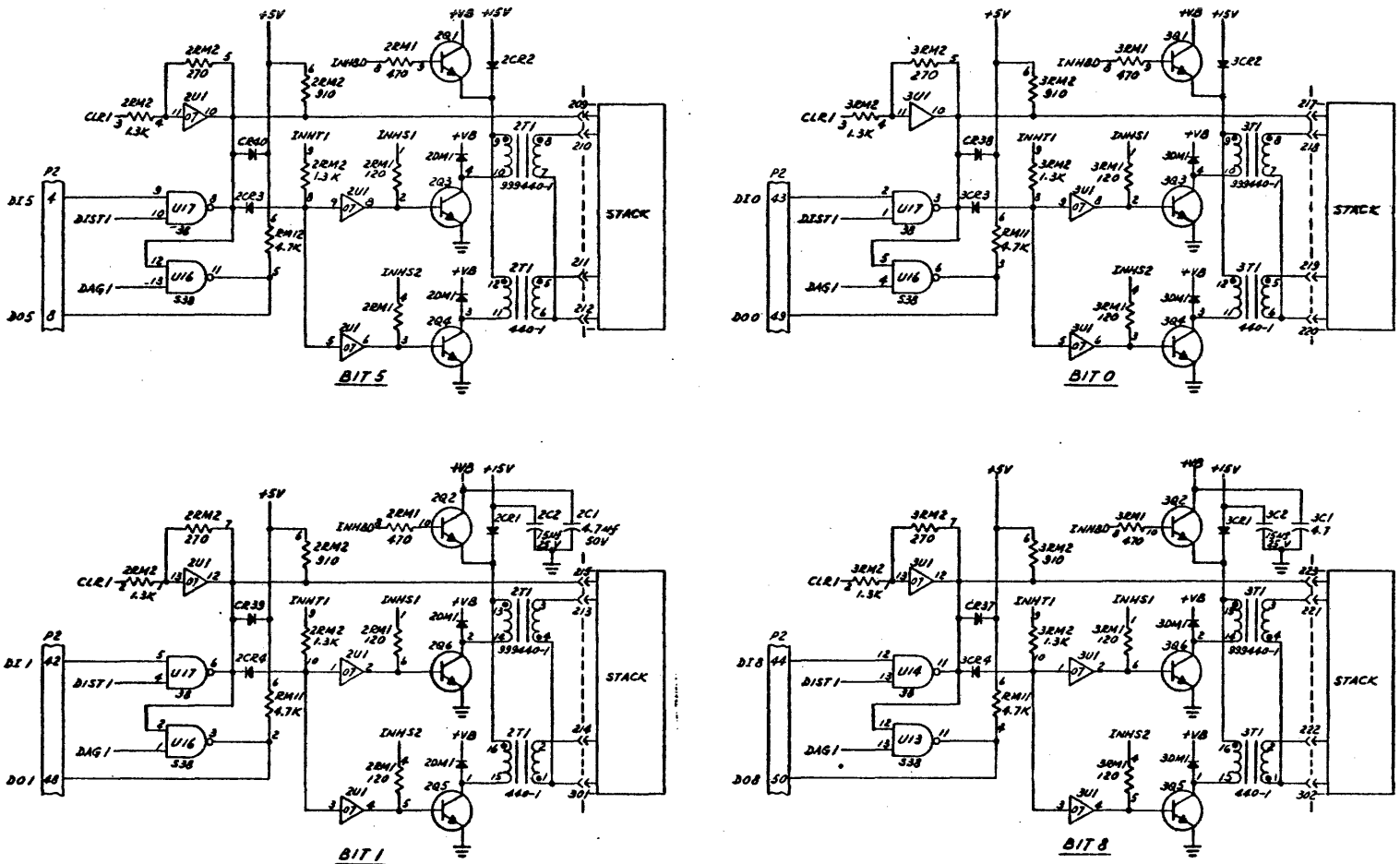
SIZE	CODE IDENT NO.	DWG NO.
D	16224	929668

SCALE NONE WEIGHT SHEET 1 OF 15

DATA NO. 1012

929668 | A | B

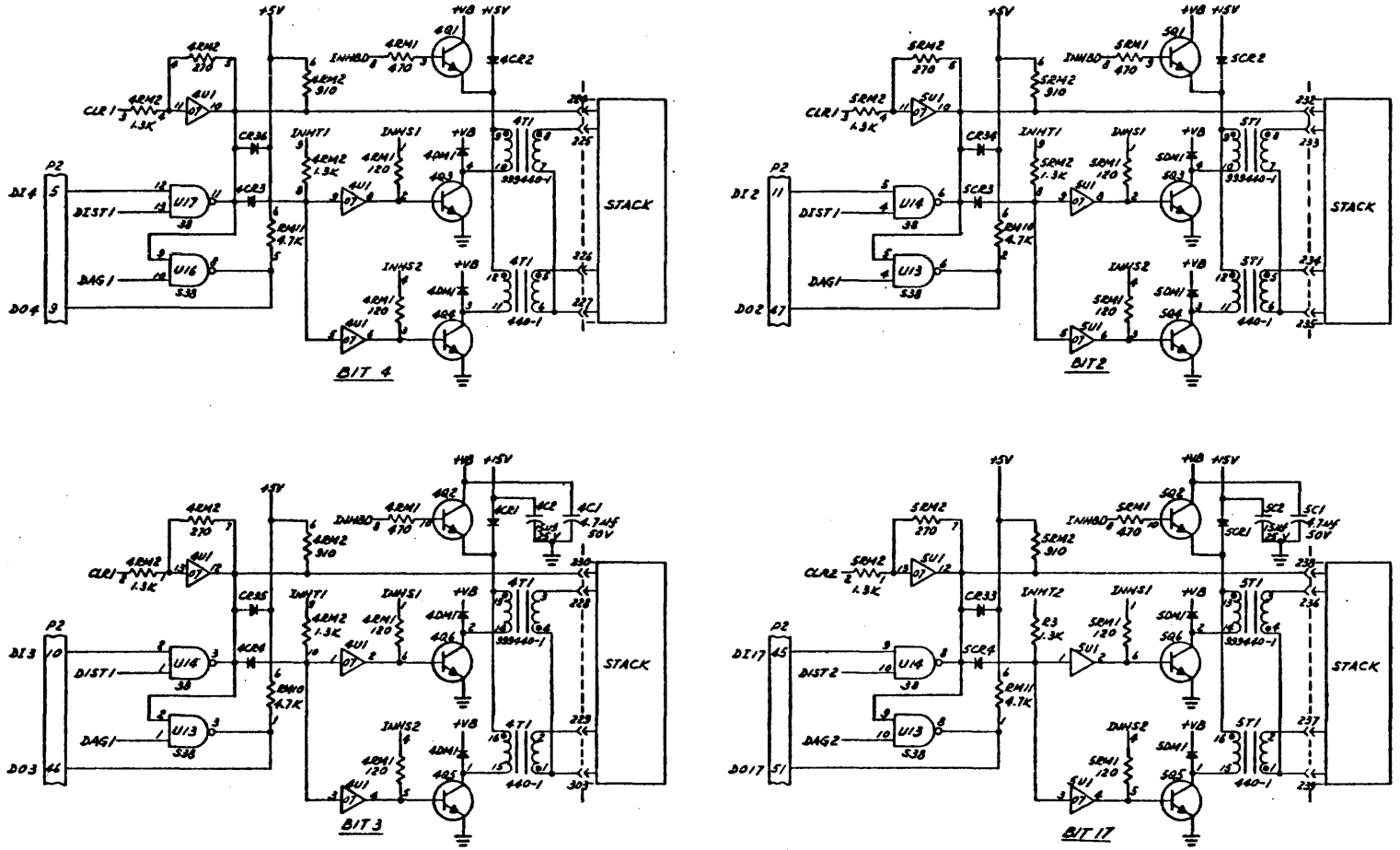

REVISIONS
SEE SH1
BIT10
BIT6
BIT9
BIT7
STACK
STACK
SEE SH1.
NOTES: UNLESS OTHERWISE SPECIFIED
D
16224
929668



REVISIONS						
ECP	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
SEE SH1						

SIZE	CODE IDENT NO.	DWG NO.
D	16224	929668
SCALE	WEIGHT	SHEET 3 of

929668

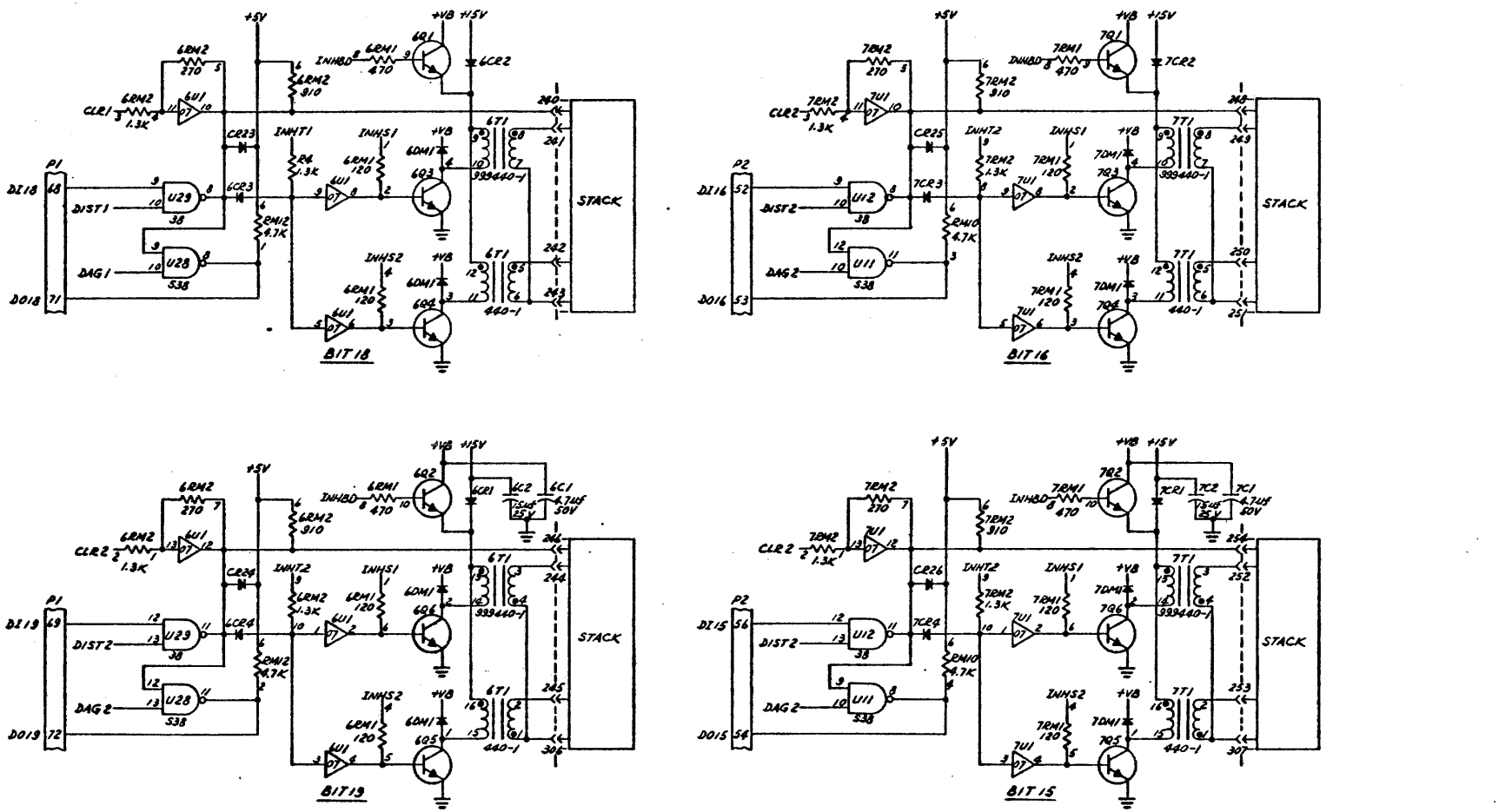


REVISIONS

DFF	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
SEE SN1						

SIZE	CODE IDENT NO.	DWG. NO.
D	16224	929668

SCALE | WEIGHT | SHEET 4 OF



REVISIONS

BY	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
				SEE SH1		

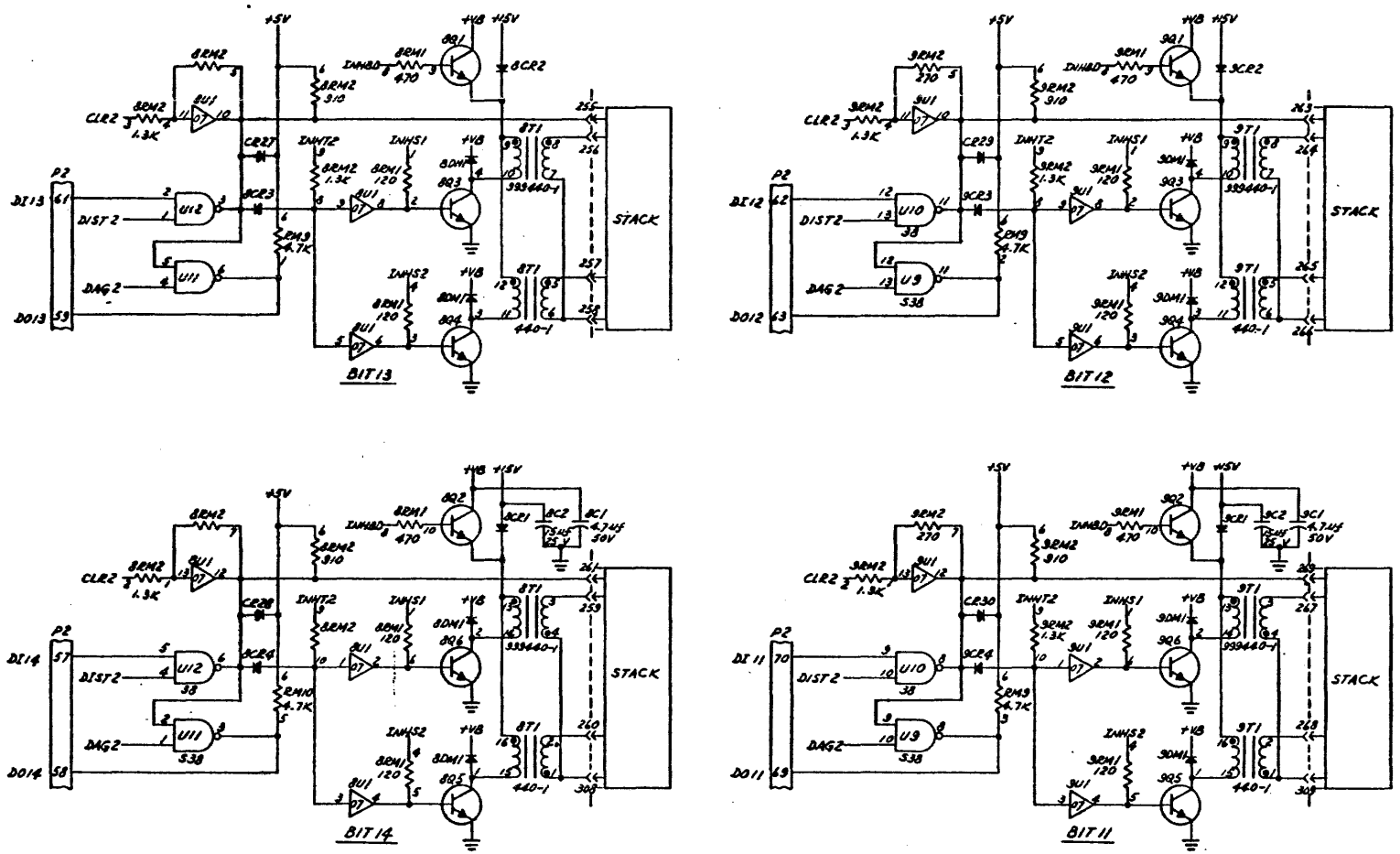
SEE SH A

NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.
D	16224	929668

SCALE: NONE WEIGHT: SHEET 5 OF

929668 A

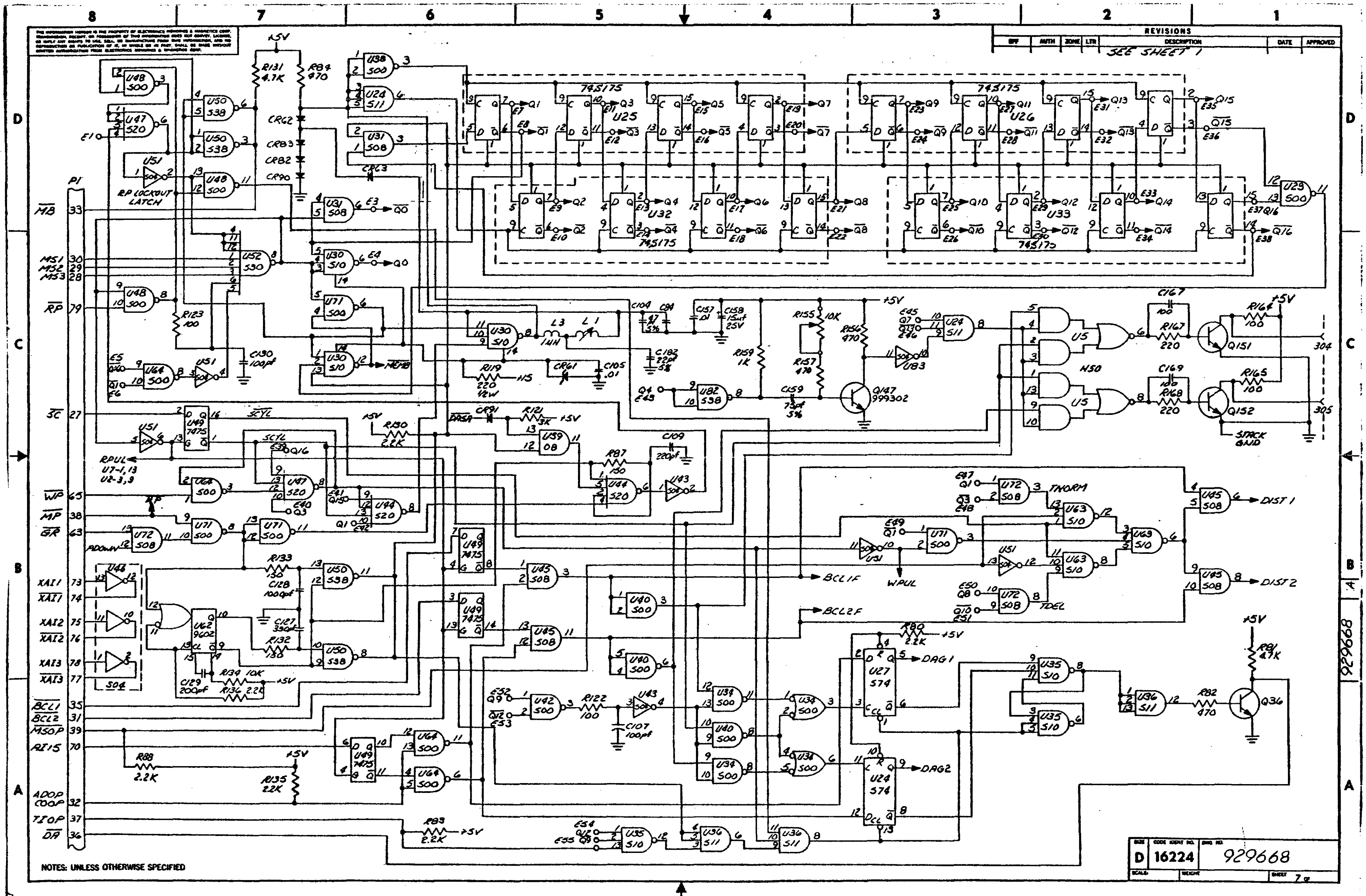


SEE SH1.
NOTES: UNLESS OTHERWISE SPECIFIED

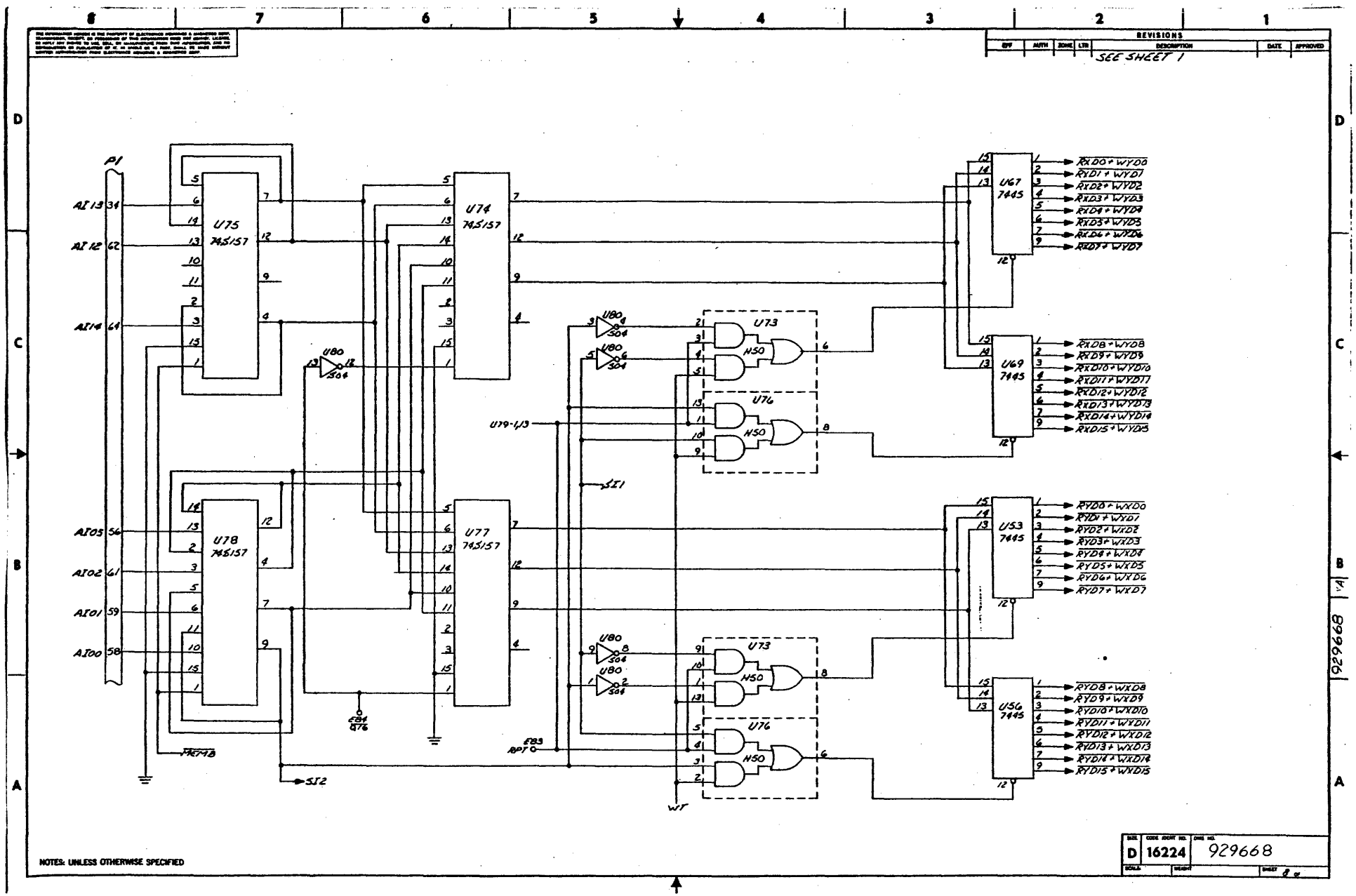
REVISIONS						
REV	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
SEE SH1						

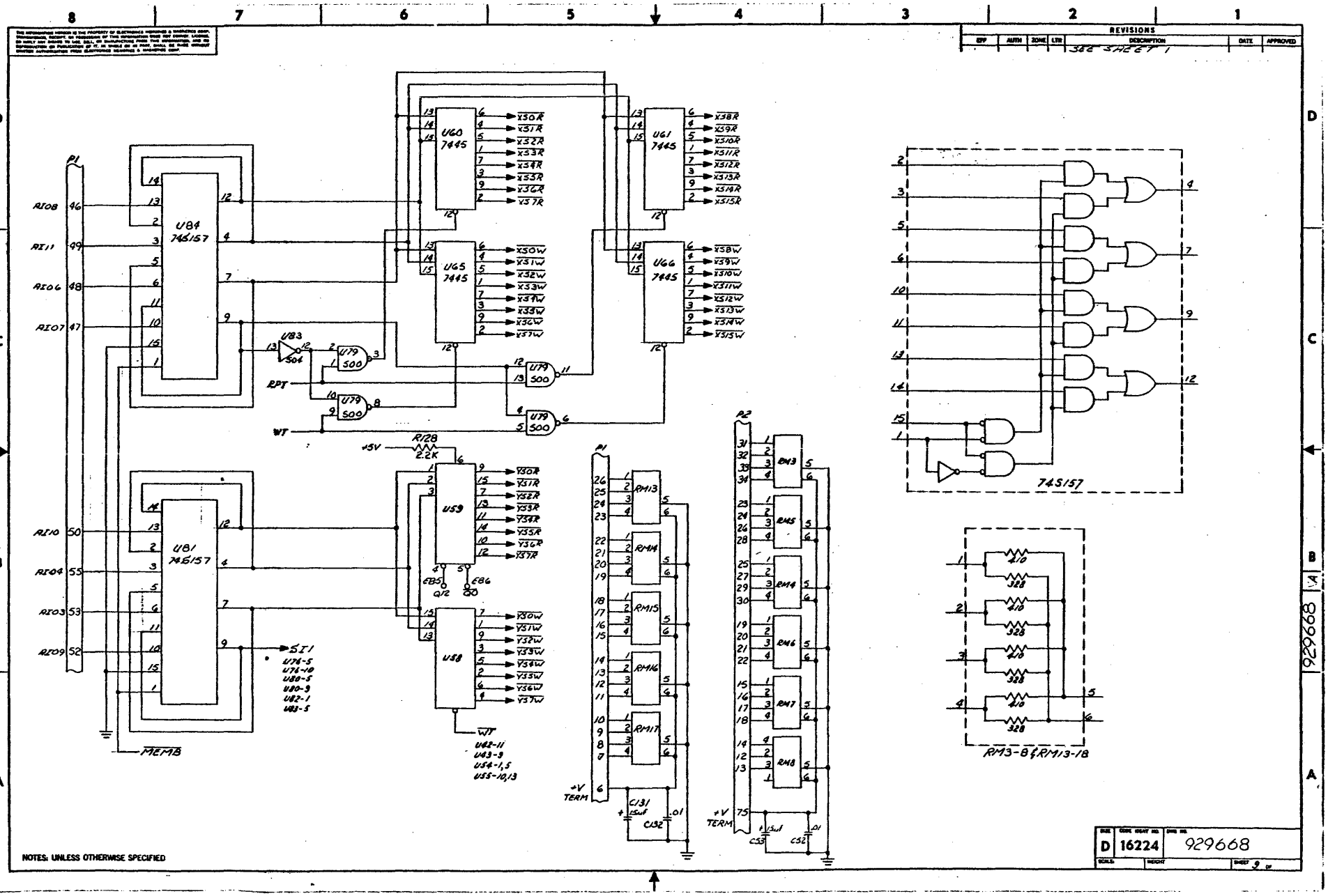
SIZE	CAGE IDENT NO.	DWG NO.
D	16224	929668
SCALE	WEIGHT	SHEET 6 of

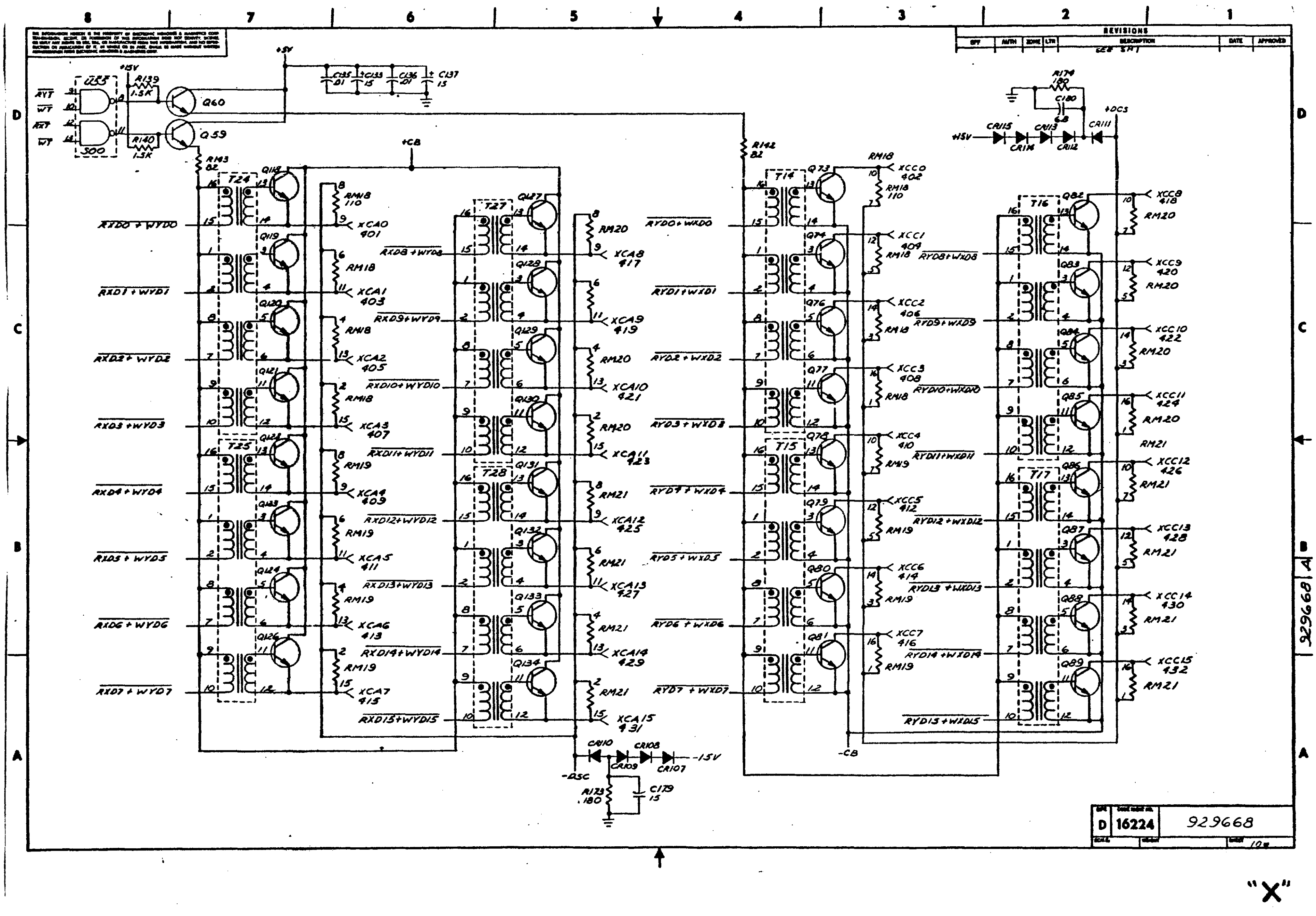
929668



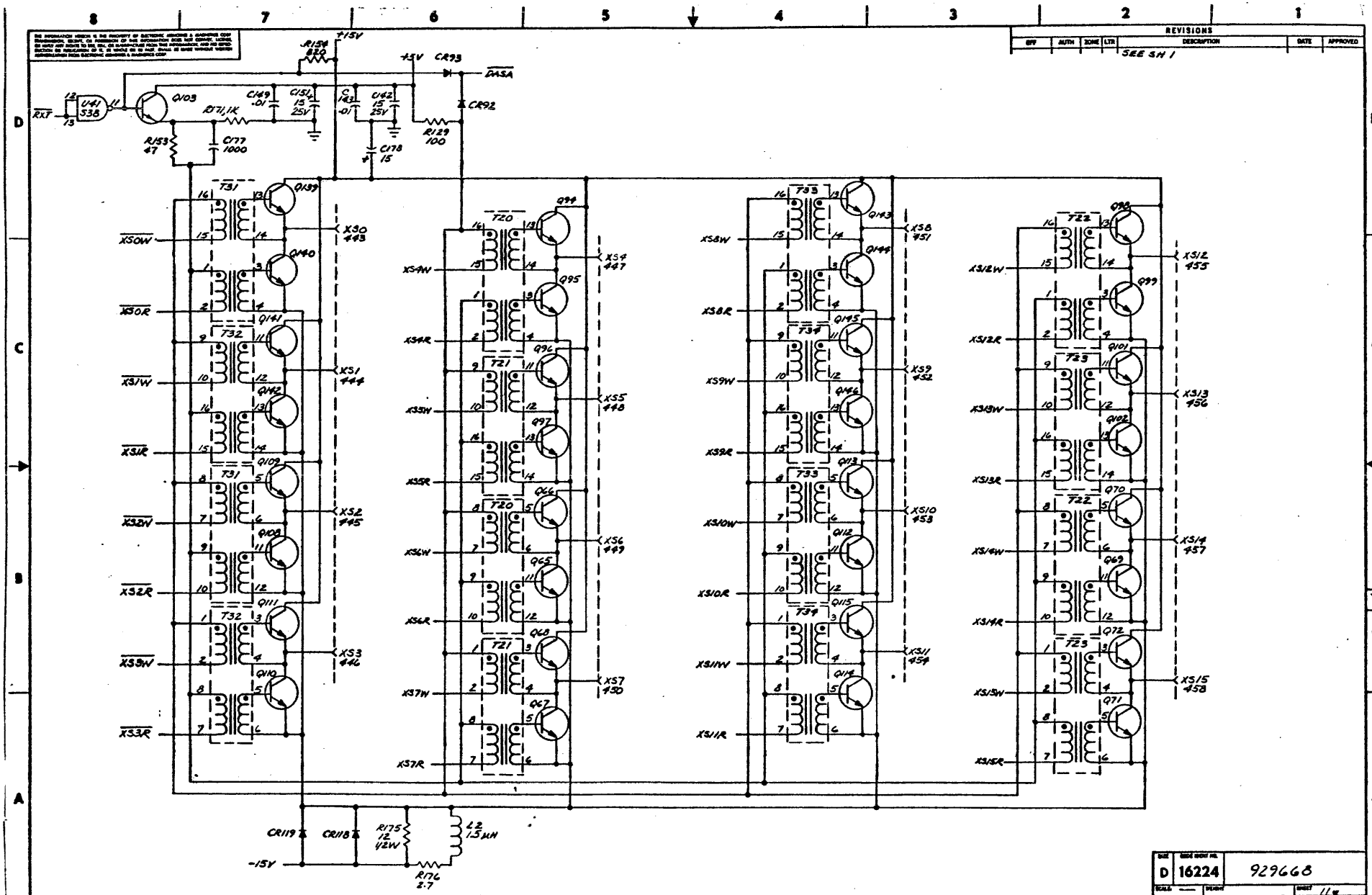
NOTES: UNLESS OTHERWISE SPECIFIED

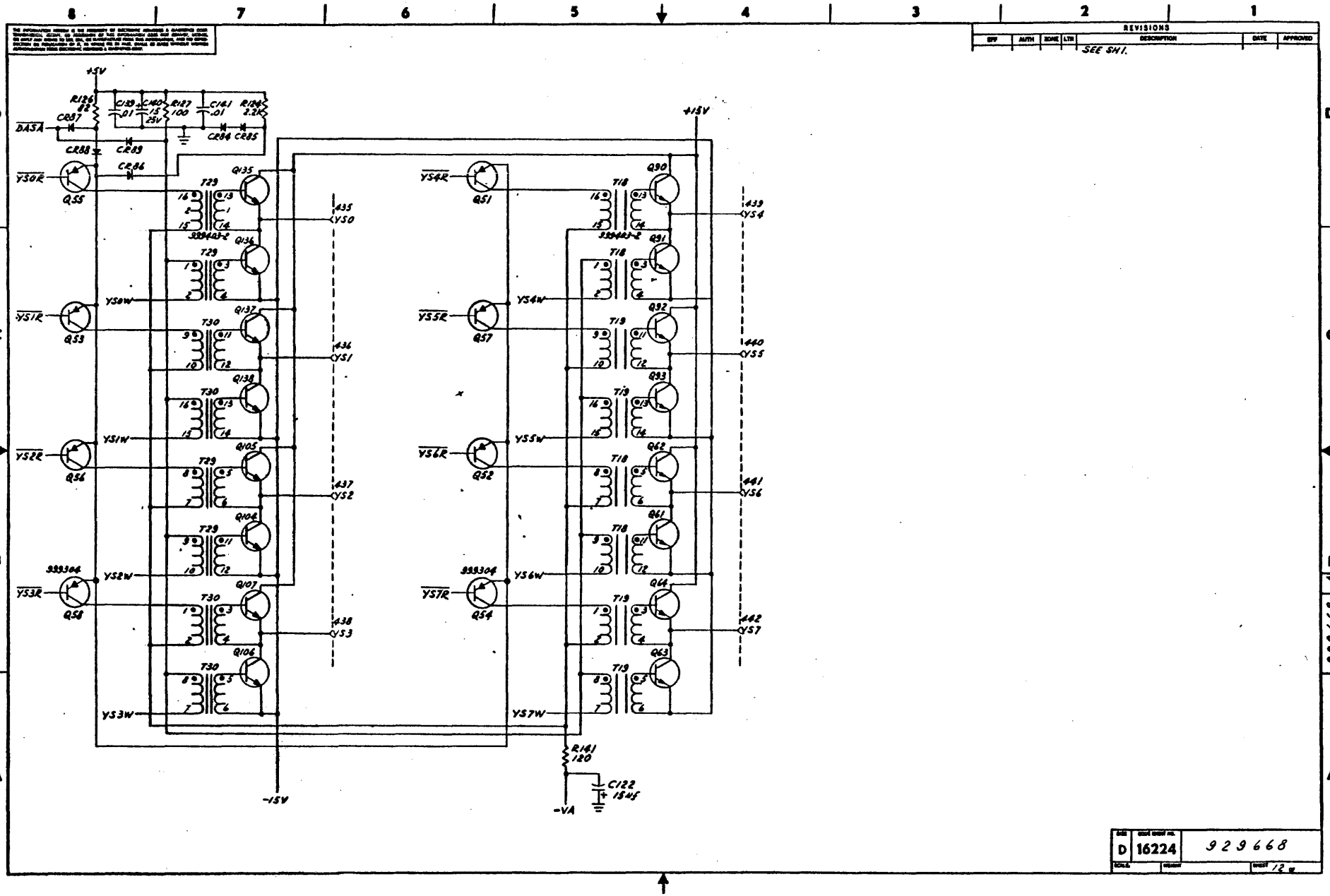

REVISIONS
SEE SHEET 1
P1
AI13 34
AI12 62
AI14 64
AI05 56
AI02 61
AI01 59
AI00 58
U75 74S157
U78 74S157
U74 74S157
U77 74S157
U80 S04
U79-1/3
U73 NSO
U76 NSO
SI1
SI2
WT
RXD0 + WYD0
RXD1 + WYD1
RXD2 + WYD2
RXD3 + WYD3
RXD4 + WYD4
RXD5 + WYD5
RXD6 + WYD6
RXD7 + WYD7
U67 7445
RXD8 + WYD8
RXD9 + WYD9
RXD10 + WYD10
RXD11 + WYD11
RXD12 + WYD12
RXD13 + WYD13
RXD14 + WYD14
RXD15 + WYD15
U69 7445
RYD0 + WXD0
RYD1 + WXD1
RYD2 + WXD2
RYD3 + WXD3
RYD4 + WXD4
RYD5 + WXD5
RYD6 + WXD6
RYD7 + WXD7
U53 7445
RYD8 + WXD8
RYD9 + WXD9
RYD10 + WXD10
RYD11 + WXD11
RYD12 + WXD12
RYD13 + WXD13
RYD14 + WXD14
RYD15 + WXD15
U56 7445
NOTES: UNLESS OTHERWISE SPECIFIED
D 16224 929668
929668 A1


REVISIONS
SEE SHEET 1
P1
A10 46
A11 49
A06 48
A07 47
A10 50
A04 55
A03 53
A09 52
U84 74S157
U81 74S157
U83 S04
U79 S00
RPT
WT
MEMB
+5V
R128 2.2K
U60 74S
U61 74S
U65 74S
U66 74S
U59
U58
X50R
X51R
X52R
X53R
X54R
X55R
X56R
X57R
X38R
X39R
X310R
X311R
X512R
X513R
X514R
X515R
X50W
X51W
X52W
X53W
X54W
X55W
X56W
X57W
X58W
X59W
X510W
X511W
X512W
X513W
X514W
X515W
SI1
U74-5
U74-10
U89-5
U89-9
U82-1
U83-5
EB5
EB6
Q12
WT
U82-11
U43-9
U54-1,5
U55-10,13
P1
RM13
RM14
RM15
RM16
RM17
+V TERM
C131
C132
P2
RM3
RM5
RM4
RM6
RM7
RM8
C53
C52
74S157
2.1Ω
328
RM3-8 & RM13-18
NOTES: UNLESS OTHERWISE SPECIFIED
D
16224
929668
SHEET 9

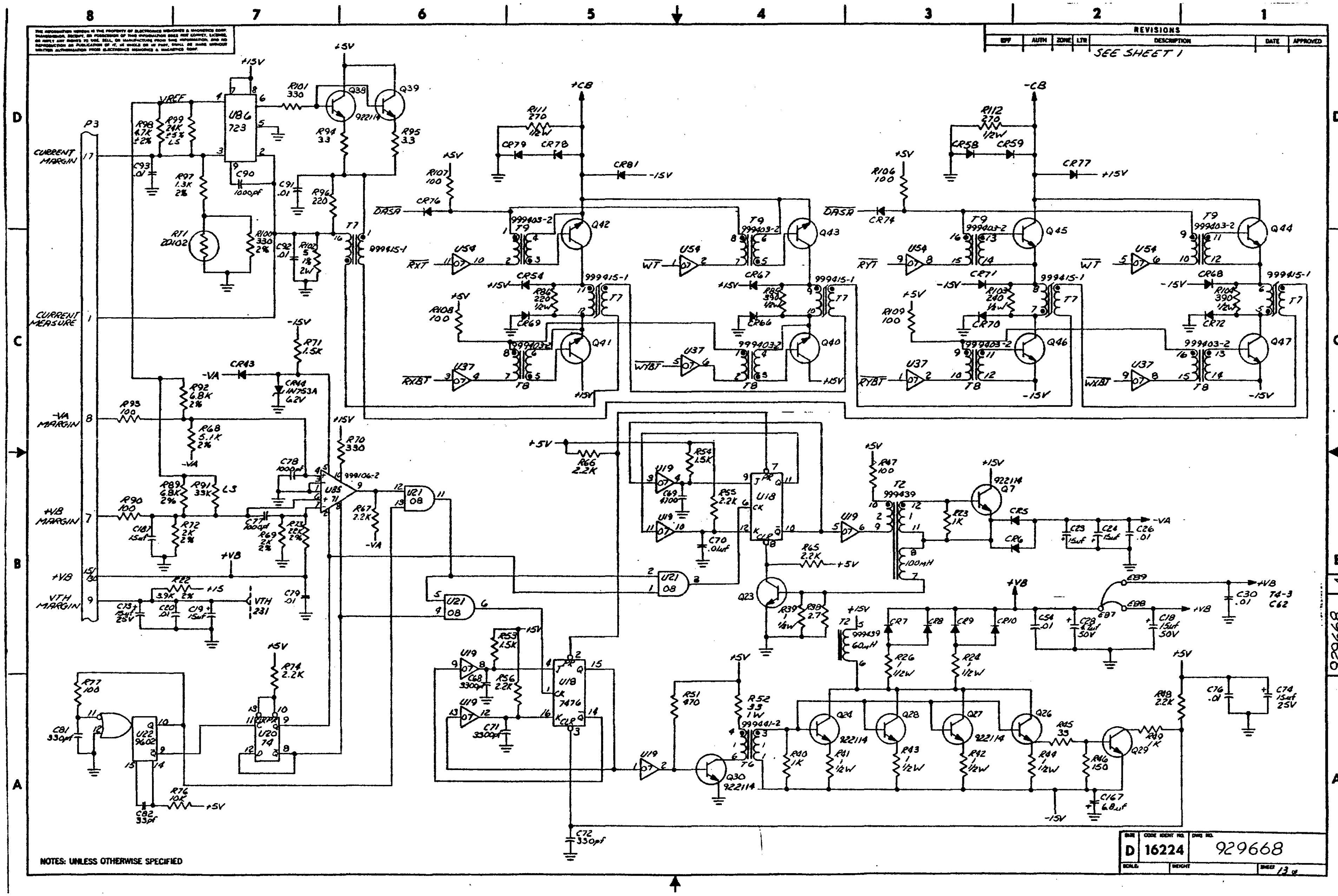


+5V
+15V
R139 1.5K
R140 1.5K
U55
500
Q60
Q59
R143 82
R142 82
C135 .01
C133 15
C136 .01
C137 15
+CB
-CB
T24
T25
T27
T28
T14
T15
T16
T17
RXD0 + WYD0
RXD1 + WYD1
RXD2 + WYD2
RXD3 + WYD3
RXD4 + WYD4
RXD5 + WYD5
RXD6 + WYD6
RXD7 + WYD7
RXD8 + WYD8
RXD9 + WYD9
RXD10 + WYD10
RXD11 + WYD11
RXD12 + WYD12
RXD13 + WYD13
RXD14 + WYD14
RXD15 + WYD15
RYD0 + WXD0
RYD1 + WXD1
RYD2 + WXD2
RYD3 + WXD3
RYD4 + WXD4
RYD5 + WXD5
RYD6 + WXD6
RYD7 + WXD7
RYD8 + WXD8
RYD9 + WXD9
RYD10 + WXD10
RYD11 + WXD11
RYD12 + WXD12
RYD13 + WXD13
RYD14 + WXD14
RYD15 + WXD15
XCA0 401
XCA1 403
XCA2 405
XCA3 407
XCA4 409
XCA5 411
XCA6 413
XCA7 415
XCA8 417
XCA9 419
XCA10 421
XCA11 423
XCA12 425
XCA13 427
XCA14 429
XCA15 431
XCC0 402
XCC1 404
XCC2 406
XCC3 408
XCC4 410
XCC5 412
XCC6 414
XCC7 416
XCC8 418
XCC9 420
XCC10 422
XCC11 424
XCC12 426
XCC13 428
XCC14 430
XCC15 432
RM18 110
RM19
RM20
RM21
R174 180
C180 6.8
+DCS
+15V
CR115
CR114
CR113
CR112
CR111
CR110
CR109
CR108
CR107
-15V
-DSC
R173 .180
C179 15
REVISIONS
SEE SH 1
D
16224
929668
929668 A
10
"X"

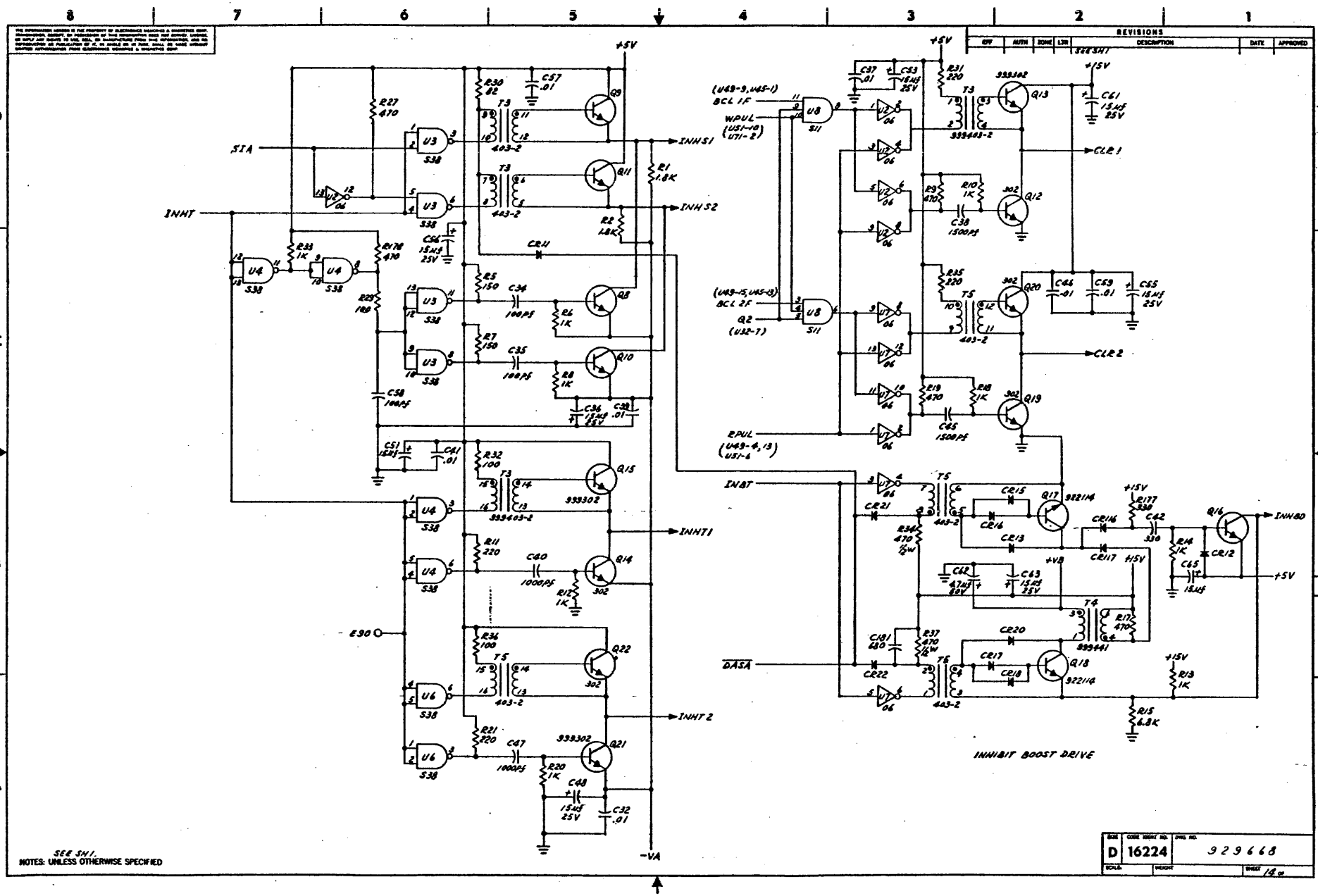

REVISIONS
SEE SH 1
+15V
-15V
+5V
CR93
DMSA
RXT
U41
S38
Q103
R154
820
R171
1K
C149
.01
C151
15
25V
C163
.01
C162
15
25V
CR92
R129
100
C178
15
R153
47
C177
1000
T31
T32
T20
T21
T33
T34
T22
T23
T30
T29
T39
T38
Q137
Q140
Q141
Q142
Q109
Q108
Q111
Q110
Q99
Q95
Q96
Q97
Q64
Q65
Q68
Q67
Q143
Q144
Q145
Q146
Q113
Q112
Q115
Q114
Q98
Q99
Q101
Q102
Q70
Q69
Q72
Q71
X50W
X50R
X51W
X51R
X52W
X52R
X53W
X53R
X30
443
X51
444
X52
445
X53
446
X54W
X54R
X55W
X55R
X56W
X56R
X57W
X57R
X54
447
X55
448
X56
449
X57
450
X58W
X58R
X59W
X59R
X510W
X510R
X511W
X511R
X58
451
X59
452
X510
453
X511
454
X512W
X512R
X513W
X513R
X514W
X514R
X515W
X515R
X512
455
X513
456
X514
457
X515
458
CR119
CR118
R175
12
1/2W
L2
1.5 μH
R176
2.7
SIZE
D
CAGE SHOT NO.
16224
929668
SCALE
DESIGN
SHEET
11 of
929668

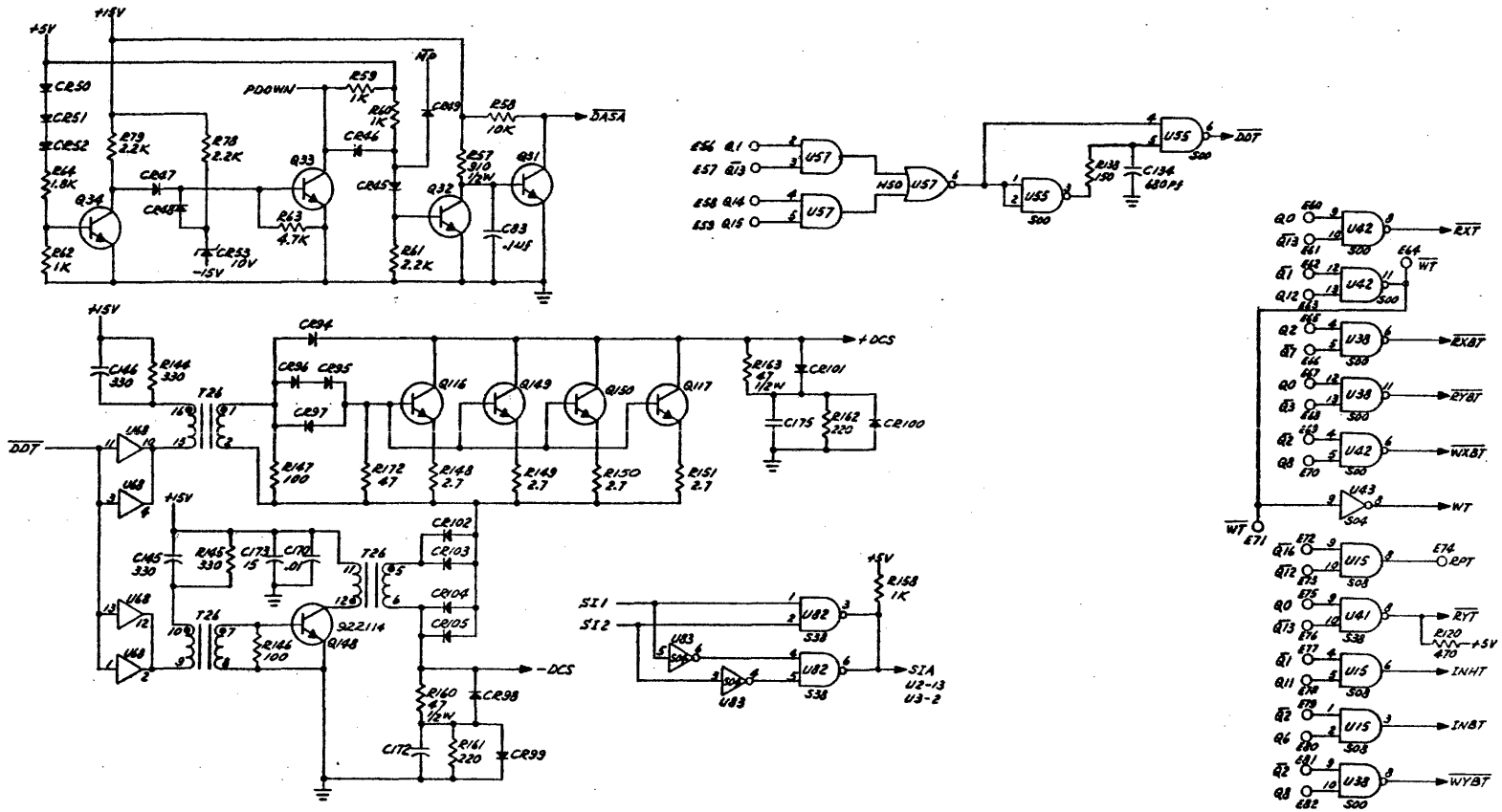

+5V
+15V
-15V
-VA
DASA
YS0R
YS1R
YS2R
YS3R
YS4R
YS5R
YS6R
YS7R
YS0W
YS1W
YS2W
YS3W
YS4W
YS5W
YS6W
YS7W
R126 82
C139 .01
C140 15 25V
R137 100
C141 .01
R138 2.2K
CR87
CR88
CR89
CR86
CR84
CR85
R141 120
C122 15uf
Q35
Q53
Q56
Q58
Q51
Q57
Q52
Q54
Q90
Q91
Q92
Q93
Q62
Q61
Q64
Q63
T29
T30
T18
T19
939483-2
999304
435 YS0
436 YS1
437 YS2
438 YS3
439 YS4
440 YS5
441 YS6
442 YS7
REVISIONS
SEE SH1.
D 16224
929668

"Y"



REVISIONS
SEE SHEET 1
CURRENT MARGIN
CURRENT MEASURE
-VA MARGIN
+VB MARGIN
+VB
VTH MARGIN
P3
VREF
U86
723
U85
999106-2
U18
7476
U22
9602
U20
74
999415-1
999403-2
999439
999441-2
922114
DASA
RXT
RXBT
WT
WXBT
RYT
RYBT
+CB
-CB
+5V
+15V
-15V
-VA
+VB
T4-3
C62
NOTES: UNLESS OTHERWISE SPECIFIED
D
16224
929668


REVISIONS
+5V
SIA
INHT
INHS1
INHS2
INHT1
INHT2
-VA
E90
INBT
DASA
(U49-9,U45-1) BCL 1F
WPUL (U51-10 U71-2)
(U49-15,U45-13) BCL 2F
Q2 (U32-7)
EPUL (U49-6,13) U51-6
CLR 1
CLR 2
+15V
+V8
INHBD
INHIBIT BOOST DRIVE
SEE SH1.
NOTES: UNLESS OTHERWISE SPECIFIED
D
16224
929668



REVISIONS

BY	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED

SEE SH1

NOTES: UNLESS OTHERWISE SPECIFIED

SEE SH1

SIZE	CODE IDENT NO.	DWG NO.
D	16224	929668

SCALE — WEIGHT — SHEET 15 OF

929668 A

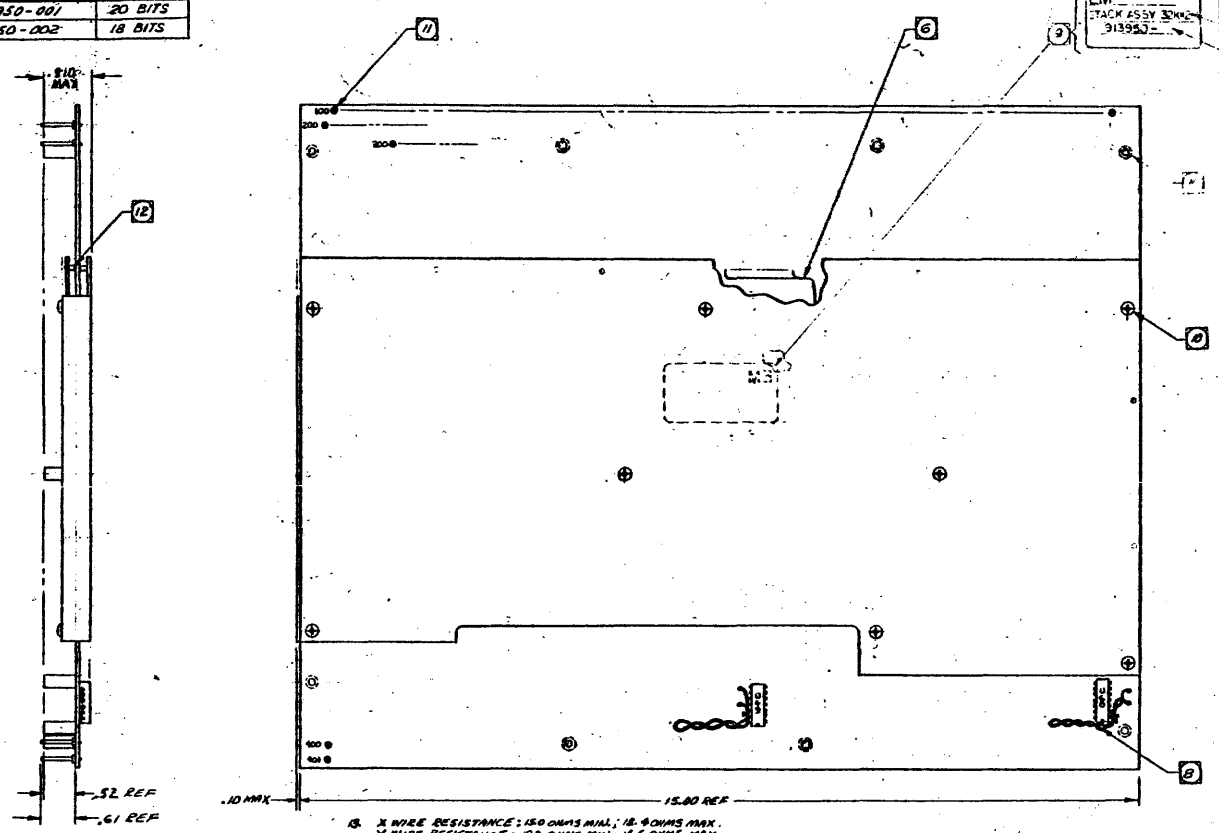
PART NUMBER	REV	TABULATED DATA	
913950-003	B	PL913950-003	16 BITS
913950-004	A	PL913950-004	20 BITS
913950-005	A	PL913950-005	18 BITS

PART IDENTIFICATION — MARK PART NUMBER & PART REV. PER CHG'S & ALL MEDIA'S — TABULATED DATA

PART NUMBER	PART REV.	SEPARATE PARTS LIST NUMBER	CAPACITY
913950-001	C	PL913950-001	20 BITS
913950-002	B	PL913950-002	18 BITS

REVISIONS

AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
DWR 3977		XA	EN RELEASE		
		XB	REVISED PER DWR		
DWR 3937		XC	ADDED VERSIONS -002 THRU -005	4-27-76	DF
		XD	DECAL & NOTE 9 REMOVED; HARDWARE REV.	7/10/76	CE
		XE	REMOVED R3 THRU R22; R23/24 WAS R23 PER ECO AND ADDED NOTE 8	8-18-76	EC
DWR 3688		F	INCORPORATED ALL EN CHANGES & INITIAL PROD RELEASED	2-27-L	KB
ECO 4041	"	G	ADVANCED -001, -002 & -003 PART REV	3-29-L	KB



5. BOND ITEM 3 TO FRONT AND BACK SIDE OF ITEM 1 USING ITEM 28.
4. INSTALL ITEM 6 IN ALL "A" CODED HOLES PRIOR TO BONDING SUBSTRATES IN PLACE. CENTRAL SPACERS WILL ACT AS GUIDES FOR POSITIONING OF WIRED MATRIX ASSEMBLY.
3. STRESS RELIEF ALL 'X' & 'Y' DRIVE TERMINATIONS.
2. POLARITY CONVENTION
   - ● INDICATES PIN 1 ON ALL MULTILEAD DEVICES.
   - ⋈ INDICATES CATHODE END OF ALL DIODES.
   - \+ INDICATES POSITIVE END OF CAPACITOR.
1. FOR SCHEMATIC SEE PARTS LIST.

NOTES: UNLESS OTHERWISE SPECIFIED

13. X WIRE RESISTANCE: 15.0 OHMS MIN.; 18.4 OHMS MAX. Y WIRE RESISTANCE: 13.0 OHMS MIN.; 14.5 OHMS MAX. S/I (1/2) RESISTANCE: 10.9 OHM 3 MIL; 12.5 OHMS MAX. HALFS TO BALANCE WITHIN .25 OHMS.
12. INSTALL ITEM 8 IN ITEM 9 PRIOR TO FASTENING IN PLACE.
11. DO NOT INSTALL AMP PINS IN ROW #100. THESE HOLES ARE USED AS TEST TERMINATION POINTS FOR SENSE WINDINGS.
10. APPLY LOCTITE ITEM 29 TO THREADS OF COVER SCREWS AFTER FINAL TEST. APPLY ITEM 29 TO THREADS AFTER INSTALLING ITEM 5.
9. ASSEMBLE AND INSPECT PER ITEM 37.
8. INSTALL WIRE LOOP ITEM 12, TWO PLACES. TWIST PORTION AS SHOWN AND SECURE TO ADJACENT COMPONENT LEADS USING ITEM 32.
7. TRIM ITEM 13 AS REQUIRED AND LAP SOLDER TO GROUND PLANE AND SUBSTRATE AS SHOWN.
6. MAINTAIN SEPERATE SENSE AND INHIBIT PAIRS AND TWIST INTO FOURS 5 TURNS PER INCH MIN. ROUTE BETWEEN MATS AND ALONG CIRCUIT ETCH AS SHOWN ON SHEETS 2 AND 3 AND SPOT BOND IN PLACE APPROX EVERY 10" USING ITEM 31. ROUTE EXCESS WIRE LENGTH WITHIN BUNDLE NEAR TERMINATION POINT.

DASH NO. & QTY PER ASSY — SEE PART IDENT BLOCK FOR PART MARKING REQT

NEXT ASSY	USED ON
APPLICATION	

DO NOT SCALE DRAWING

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST			

CONTRACT NO.

DRAWN	L. TREHER	12-17-76
CHECK		
ENGR	A.J.	2-25-76
PROJ. ENGR	B	12/1/76
PROD. DESIGN		2-25-L
OTHER APPROVALS		2-25-76

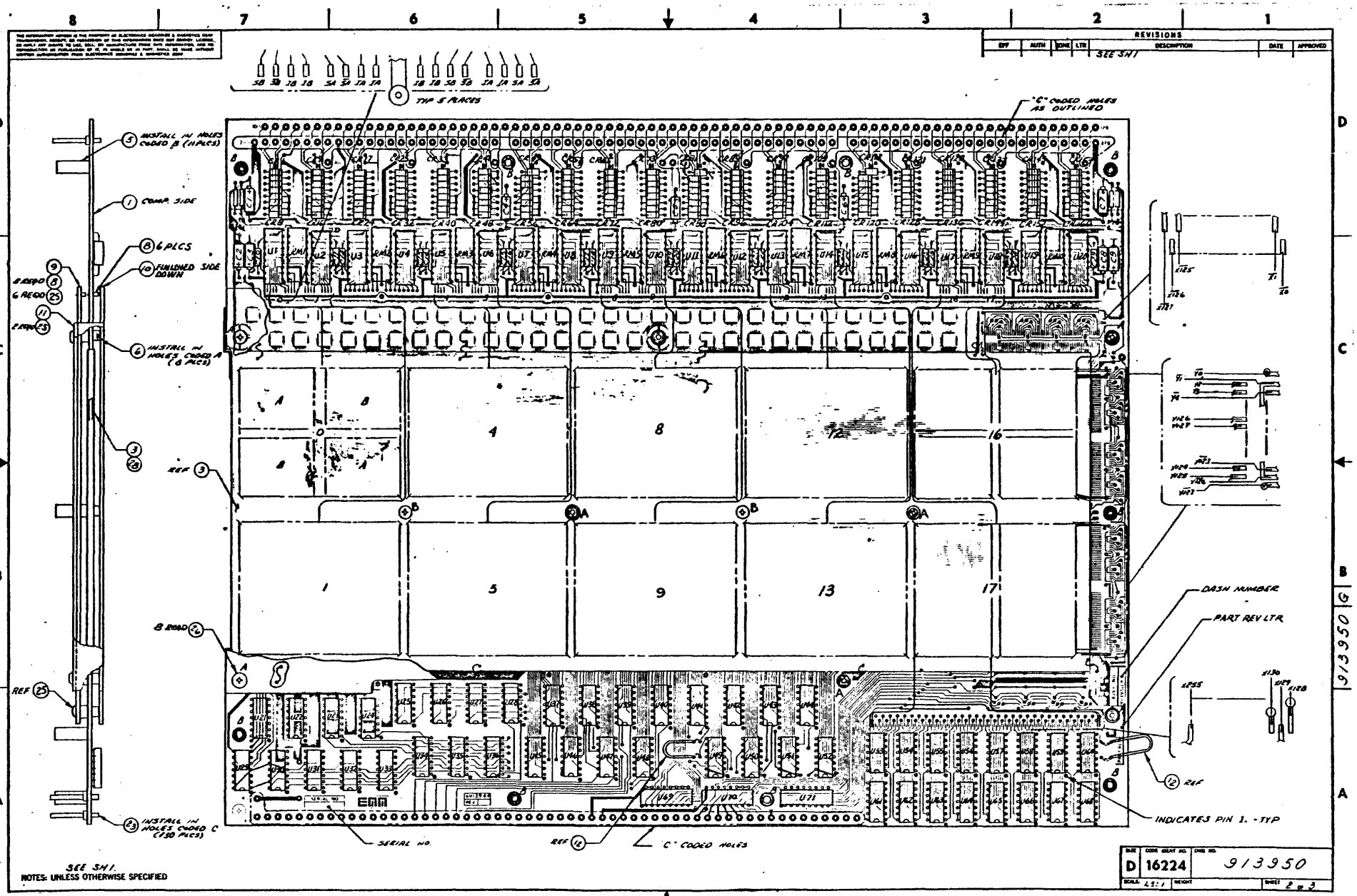
EMM MEMORY PRODUCTS GROUP
ELECTRONIC MEMORIES & MAGNETICS CORPORATION

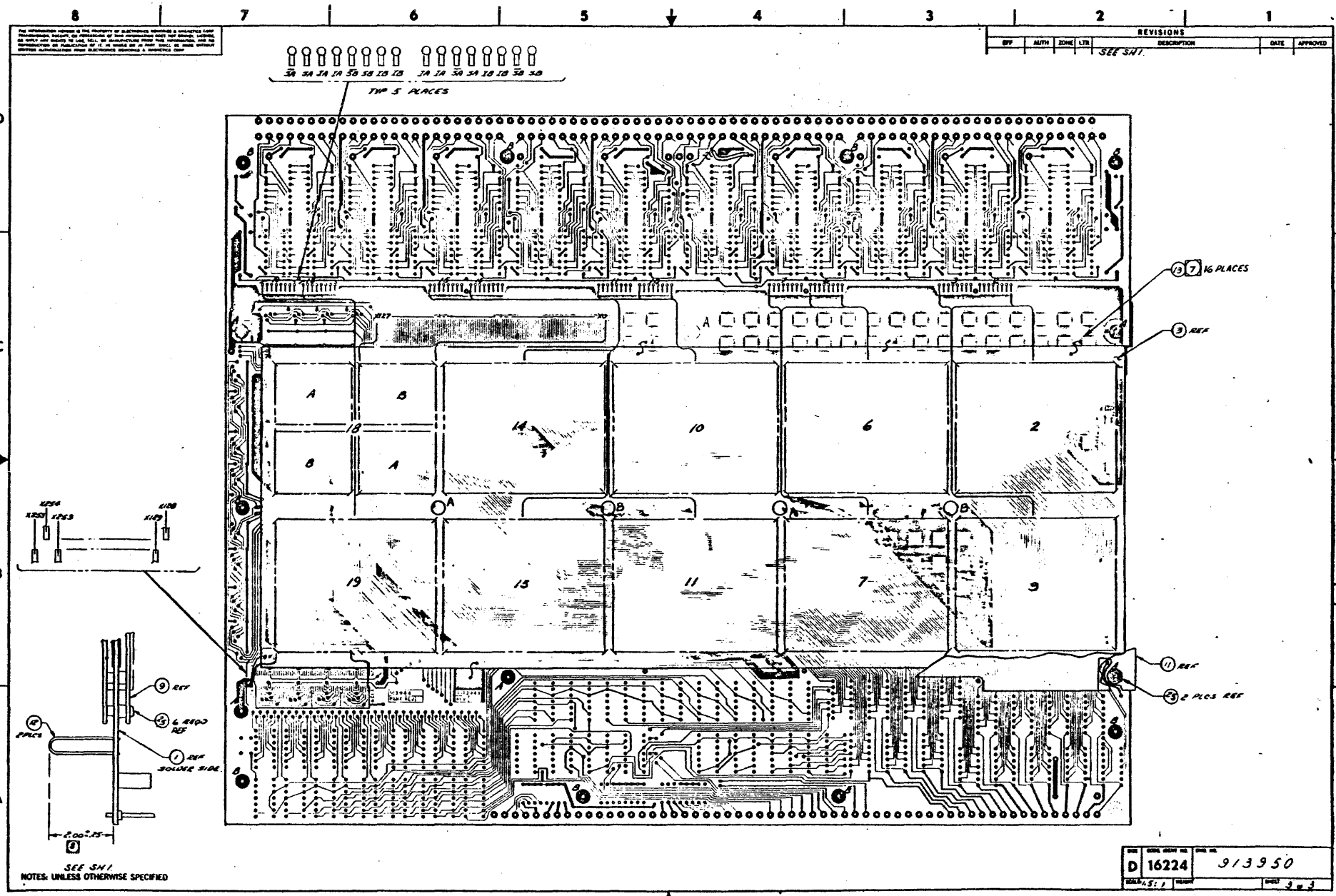
CIRCUIT STACK ASSEMBLY
STACK 32K X 20 (MAX)

SIZE D | CODE IDENT NO. 16224 | DWG NO. 913950

SCALE FULL SIZE | WEIGHT | SHEET 1 OF 3

SERIES NO. 1116


REVISIONS
SEE SH1
TYP 5 PLACES
"C" CODED HOLES AS OUTLINED
INSTALL IN HOLES CODED B (11 PLCS)
COMP. SIDE
6 PLCS
FINISHED SIDE DOWN
INSTALL IN HOLES CODED A (8 PLCS)
REF
B RIBBON
G RIBBON
INSTALL IN HOLES CODED C (150 PLCS)
DASH NUMBER
PART REV LTR
INDICATES PIN 1. - TYP
SERIAL NO.
"C" CODED HOLES
SEE SH1.
NOTES: UNLESS OTHERWISE SPECIFIED
D
16224
913950
SHEET 2 of 3


TYP 5 PLACES
16 PLACES
REF
REF
2 PLCS REF
REF
6 REQD REF
REF
SOLDER SIDE
SEE SH1
NOTES: UNLESS OTHERWISE SPECIFIED
REVISIONS
SEE SH1.
D
16224
913950
SCALE: 1
SHEET 3 of 3

electronic memories HAWTHORNE, CALIF. A DIVISION OF ELECTRONIC MEMORIES & MAGNETICS CORP.		CODE IDENT NO. 16224	PL 913950-001	J
			SHEET 2	REV

PARTS LIST

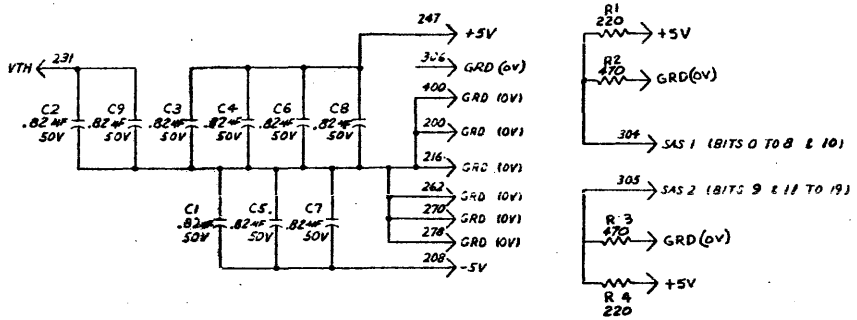
NOTE	FIND NO.	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	1	1	913944-001	PRINTED WIRING BOARD			
	2						
	3	1	913949-001	WIRED MATRIX ASSEMBLY			
	4						
	5	11	913951-001	FASTENER, MODIFIED			
	6	8	999953-001	SPACER, CAPTIVE -DOUBLE ENDED			
	7						
	8	14	913733-003	SPACER, SNAP-IN			
	9	1	913945-001	COVER, BOTTOM			
	10	1	913946-001	COVER, TOP			
	11	1	913972-001	ANGLE, COVER			
	12	AR	922600-329	WIRE, 26 AWG WHITE			
	13	AR	984512-026	WIRE, SOLID COPPER, TINNED AWG 26			
	14	160	999206-001	DIODE	CR1-CR160		
	15	48	999208-001	DIODE MODULE	U21-U68		
	16	20	921807-003	ICP, SENSE AMP	U1-U20		
	17	10	999551-015	ICP, RESISTOR NETWORK	RM1-RM10		
	18	3	999536-001	RESISTOR MODULE	U69, U70, U71		
	19						

electronic memories HAWTHORNE, CALIF. A DIVISION OF ELECTRONIC MEMORIES & MAGNETICS CORP.		CODE IDENT NO. 16224	PL 913950-001	H
			SHEET 3	REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	20	20	CK12BX101K	CAPACITOR, 100 PF, ±10%	C10-C29		
	21	9	CSR13G824KL	CAPACITOR, .82 MF, ±10%	C1-C9		
	22	2	RC07GF221J	RESISTOR, 1/4 W, 220 Ω ±5%	R1 & R4		
	23	150	1-86147-4	CONTACT, MALE POST - MOD I		AMP	
	24	2	RC07GF471J	RESISTOR, 1/4 W, 470 Ω ±5%	R2 & R3		
	25	8	MS35233-12	SCREW, MACH-PAN HD. 4-40 X 3/16" LG			
	26	8	MS24693-C1	SCREW, MACH-FLT HD. 4-40 X 3/16" LG			
	27						
	28	AR	EA9650-265	ADHESIVE			
	29	AR	984505-001	LOCTITE			
	30	AR	SN63WRMAP3	SOLDER		QQ-S-571	
	31	AR	987400	PROTECTIVE COATING MATERIAL			
	32	AR	984506-001	CORD LACING, BLK - WAXED			
	33	REF	MTP913950	MANUFACTURING TEST PROCEDURE			
	34	REF	913942	SCHEMATIC DIAGRAM			
	35						
	36						
	37	REF	984100	WORKMANSHIP STD			

REVISIONS					
SPF	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
			XA	INITIAL PROTOTYPE RELEASE	2-12-5	
			MB	X-YDRIVE DIODE REV; PIN NO'S REV; ADD W10 & W20	7-17-75	
	DWN 3693		C	INITIAL PROD RELEASED	2-27-6	MB



6. ALL RESISTORS ARE IN OHMS, ±5%, 1/8 W.
7. RESISTOR MODULES U63, U70 & U71 ARE 999526-001.
6. DIODE MODULES U21 THRU U68 ARE 999204-001.
5. ALL CAPACITORS ARE 100pf, ±10%.
4. ALL DIODES ARE 999206-001.
3. RESISTOR VALUES NOT REFERENCE DESIGNATED ARE CONTAINED IN RESISTOR MODULE 999551-014. RESISTANCE VALUES ARE IN OHMS.
[2] BIT CIRCUITS A1 THRU A10 ARE IDENTICAL WITH THE EXCEPTION OF SAS ON BIT CIRCUIT A6.
1. FOR CIRCUIT CARD ASSEMBLY SEE 913950.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO & QTY PER ASSY	03	02	01
PART REV LETTER			
NEXT ASSY	913950		
USED ON	APPLICATION		

PARTS LIST

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
					2
					1

DO NOT SCALE DRAWING

CONTRACT NO.

DRAWN	L. KELLOGG	2-12-5
CHECK		2-14-75
ENGR		2-14-75
PROJ. ENGR		2-21-76
PROD. DESIGN		2-27-6
OTHER APPROVALS		

electronic memories (HAWTHORNE, CALIF.) A DIVISION OF ELECTRONIC MEMORIES & MAGNETICS CORP.

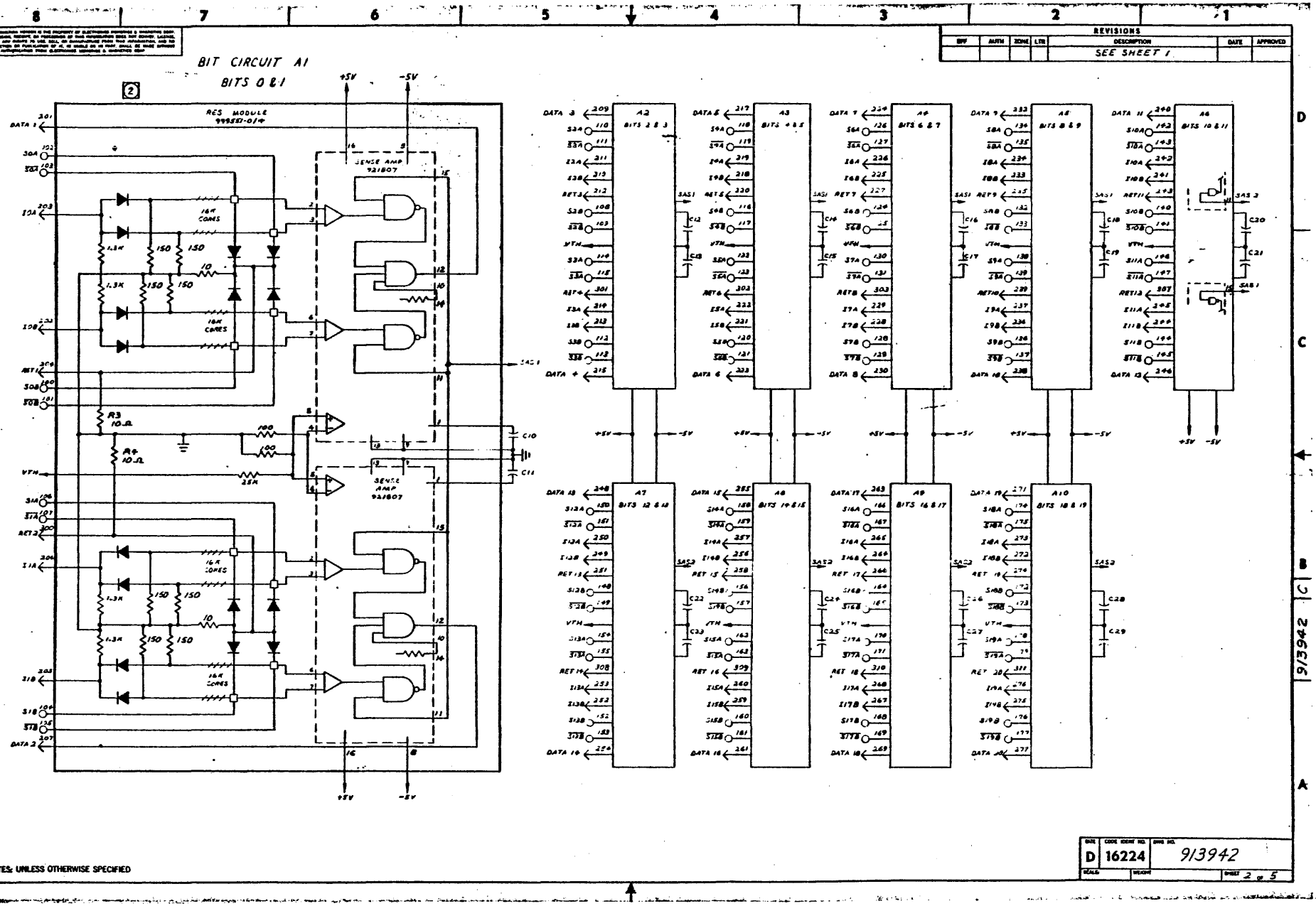
SCHEMATIC DIAGRAM
STACK ASSEMBLY, 32K x 20

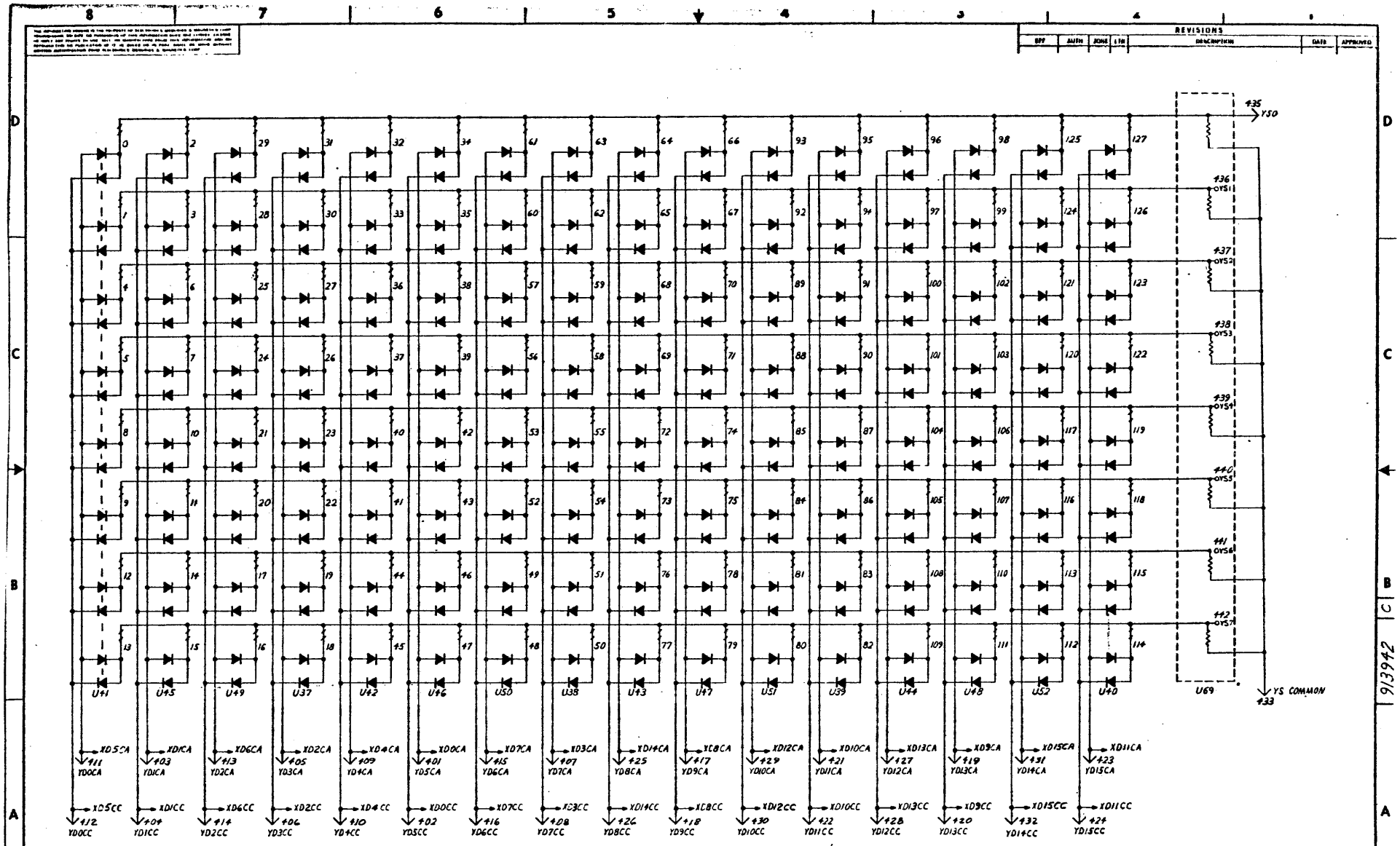
SIZE D | CODE IDENT NO. 16224 | DWG NO 913942

SCALE NONE | DESIGNER | SHEET 1 of 5

913942 C

1112


BIT CIRCUIT A1
BITS 0 & 1
REVISIONS
SEE SHEET 1
RES MODULE
SENSE AMP
16K CORES
NOTES: UNLESS OTHERWISE SPECIFIED
D 16224 9/3942
SHEET 2 of 5
9/3942

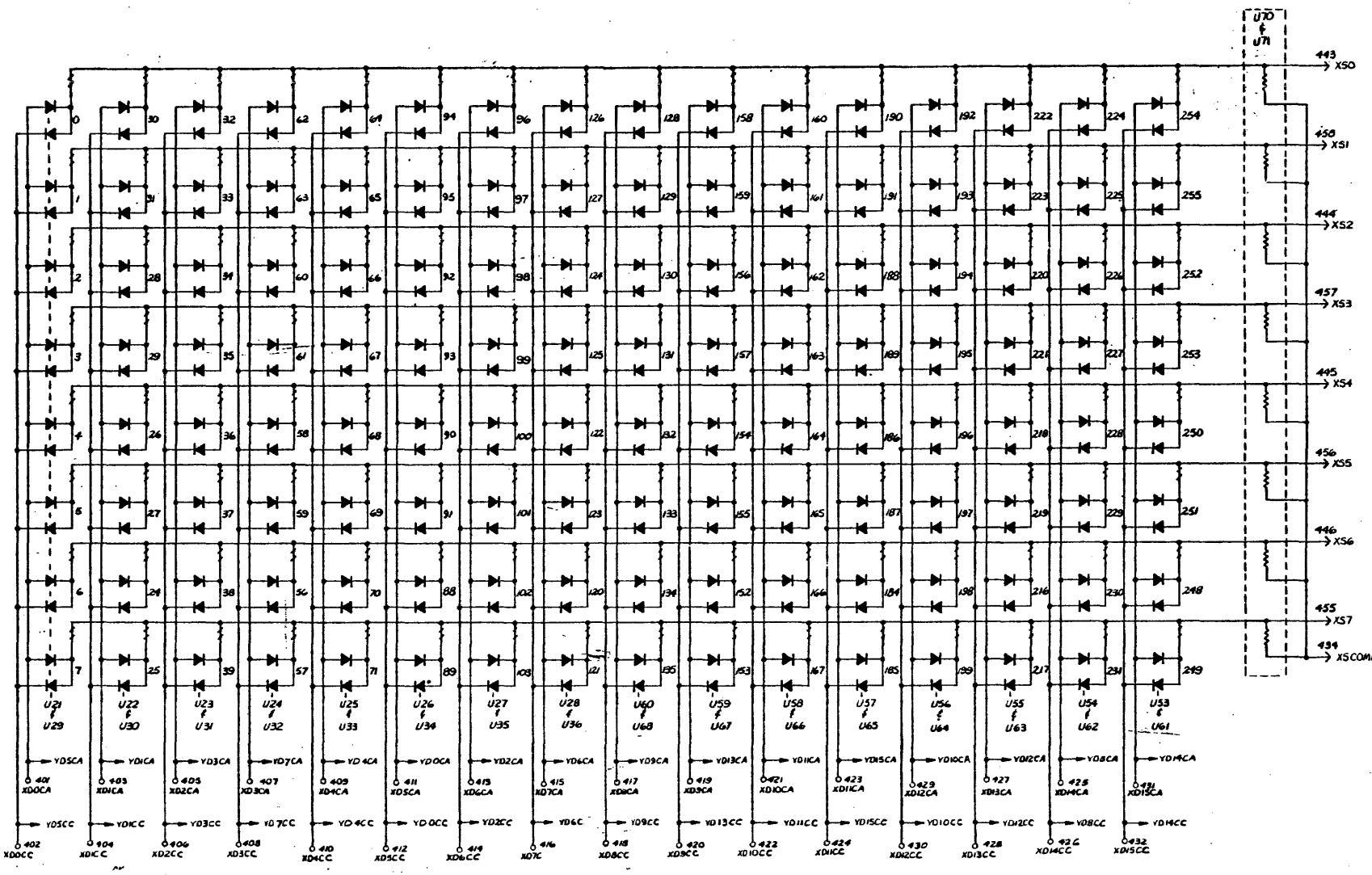


"Y" AXIS DIODE DECODE

NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO	DWG NO
D	16224	913942
SCALE	WEIGHT	SHEET 3 of 4

913942 C

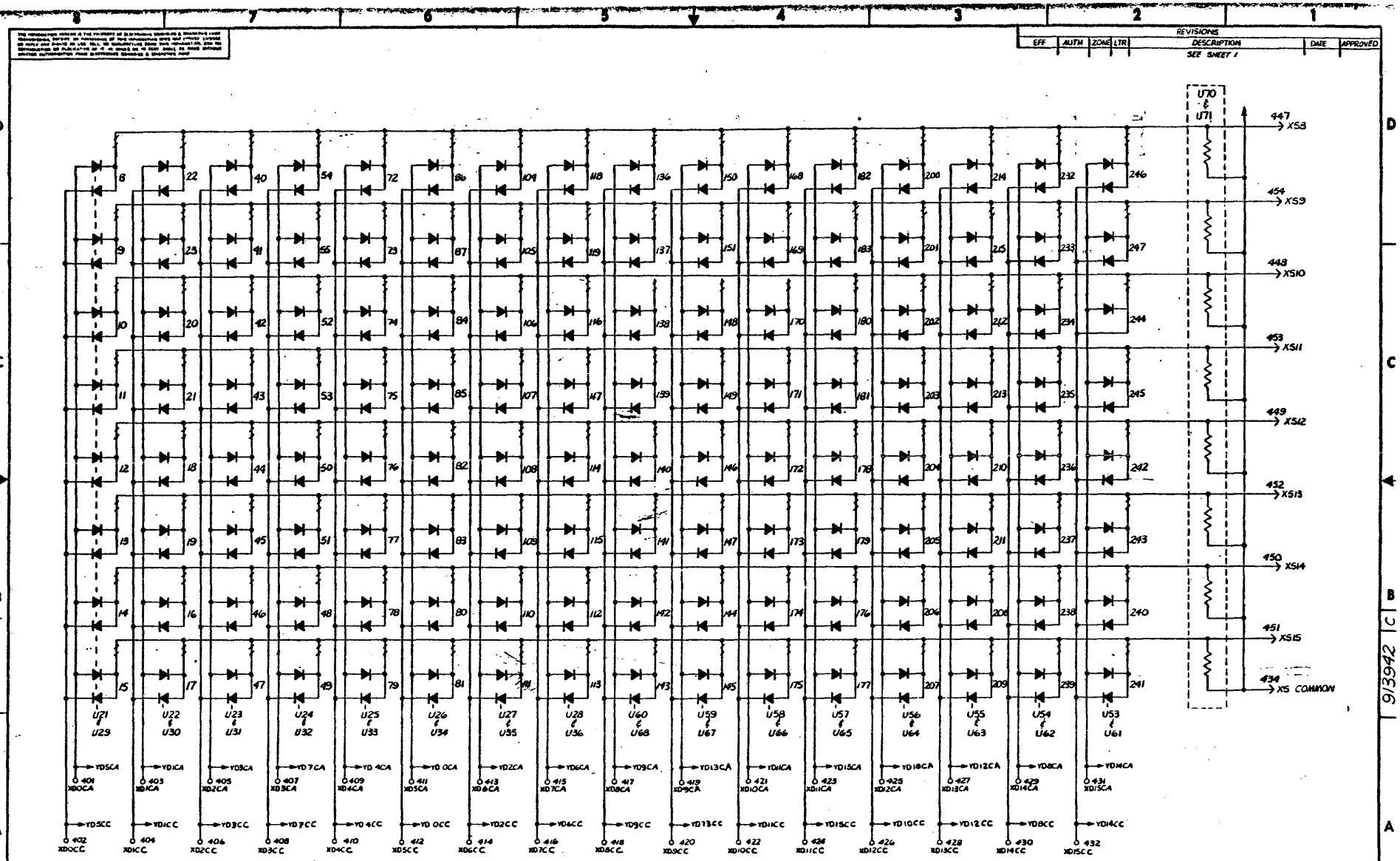


"X" AXIS DIODE DECODE

NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.
D	16224	913942
SCALE		SHEET 4 OF 5

913942 C



"X" AXIS DIODE DECODE

NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS						
EFF	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
				SEE SHEET 1		

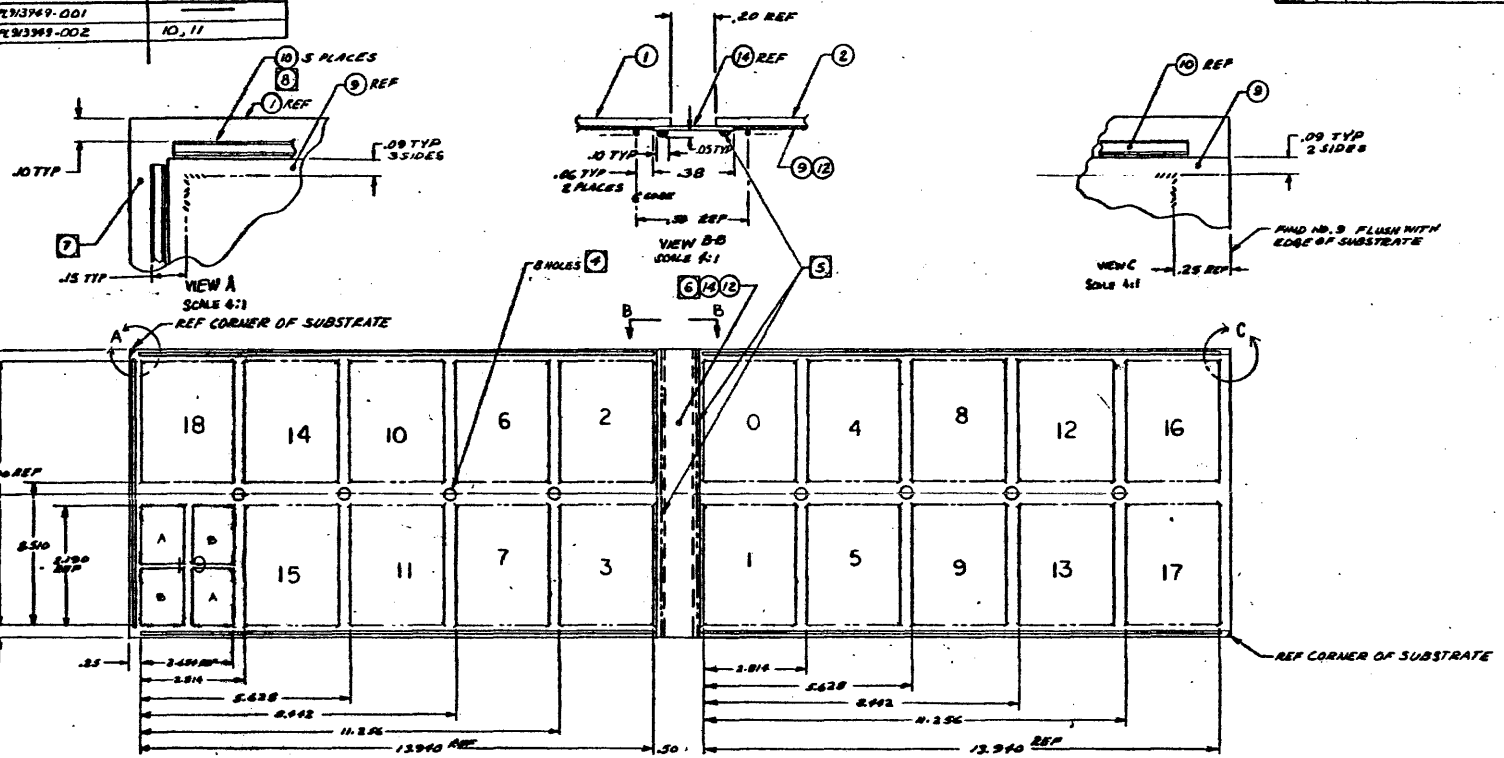
SIZE	CODE IDENT NO.	DWG NO.
D	16224	913942
SCALE	WEIGHT	SHEET 5 of 5

913942 C

PART IDENTIFICATION (SAME PART NUMBER & PART REV. FOR EMPS 6-1, 2)		TABULATED DATA
PART NUMBER	PART REV.	FOR PARTS LIST SEE	BITS NOT LOADED
913949-001	A	PL913969-001	——
913949-002	A	PL913969-002	10, 11

PART NUMBER	REV	TABULATED DATA	
913949-003	A	PL913969-003	8, 9, 10, 11
913969-004	A	PL913969-004	——
913969-005	A	PL913969-005	10, 11

REVISIONS					
AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED
3899		XA	INITIAL PROTOTYPE RELEASE		
		XB	SENSE WIRING REVISED	12-6-74	CF. L.
3927		XC	ADDED VERSIONS -002 THRU -005	6-27-75	JF.
		XD	ADDED NOTE 10	9-11-75	CP
3983		E	INITIAL PROD RELEASED	2-25-76	KB



8. BOND WIRE GUIDE, FIND NO. 10, TO SUBSTRATE USING FIND NO. 12 PER MANUFACTURING INSTRUCTION.

7. ORIENT SUBSTRATES PER MARKED CORNERS AS NOTED AND BOND SILICONE RUBBER TAPE WITH CORES TO METALLIC SIDE OF SUBSTRATES USING FN 12.

6. BOND HINGE FIND NO. 14, WITH ADHESIVE SIDE UP, TO FIND NOS 1 AND 2 USING FIND NO. 12.

5. APPLY A BEAD OF FIND NUMBER 12 ACCROSS WIRES AFTER STRINGING, APPROX WHERE SHOWN. TYP 2 PLACES. OPT: APPLY NEXT ASSY LEVEL.

4. CUT HOLES IN FIND NO. 9 (58 HOLE OPTIONAL) TO MATCH HOLES IN SUBSTRATES. MAINTAIN .25 INCH DIA CLEARANCE AROUND HOLES FOR X WIRES.

3. EIGHT (8) INCH MIN WIRE LENGTH FOR S/I LEADS AFTER TWIST.

2. SIX (6) INCH MIN. WIRE LENGTH FOR X. THREE (3) INCH MIN WIRE LENGTH FOR Y.

1. ASSEMBLE AND INSPECT PER FN 15

NOTES: UNLESS OTHERWISE SPECIFIED

10. FOR MATS NOT LOADED USE TWO (2) BEADS OF ITEM 12 ACROSS WIRES TO MAINTAIN DRESS.

9. FOR CORE PATTERN DIAGRAM SEE DWG. 913953.

NEXT ASSY	USED ON
-001 913950	43000/3220
APPLICATION	

NOTE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION/MATERIAL	SPEC/SOURCE	CODE IDENT NO.	FIND NO.
		PARTS LIST			

DO NOT SCALE DRAWING

CONTRACT NO.

DRAWN		10-4-74
CHECK		
ENGR		
PROJ. ENGR		2-25-76
PROD. DESIGN		2-25-76
OTHER APPROVALS		5-19-76

MEMORY PRODUCTS GROUP
ELECTRONIC MEMORIES & MAGNETICS CORPORATION

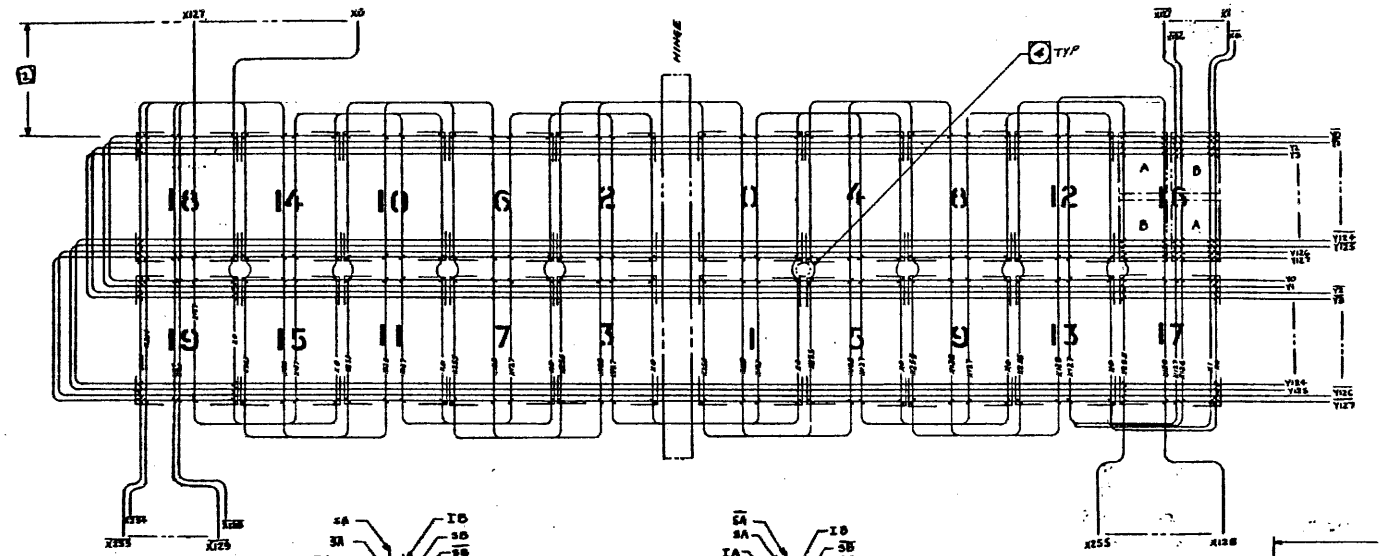
WIRED MATRIX ASSY, QUAD DENSITY — 32K X 20

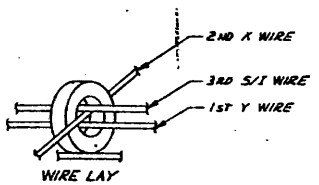
SIZE	CODE IDENT NO.	DWG NO.
D	16224	913949

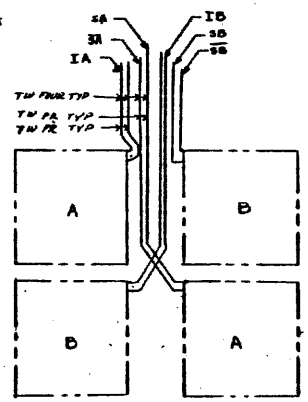
SCALE: —— WEIGHT: SHEET 1 of 2

DASH NO. 1110

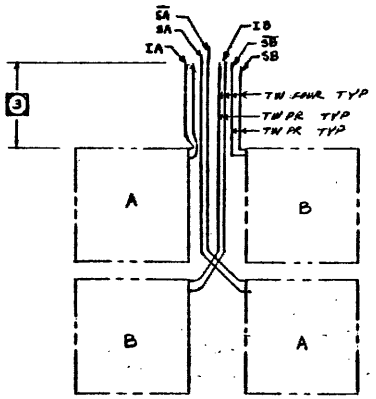
REVISIONS						
SEE SHEET 1						
REV	AUTH	ZONE	LTR	DESCRIPTION	DATE	APPROVED



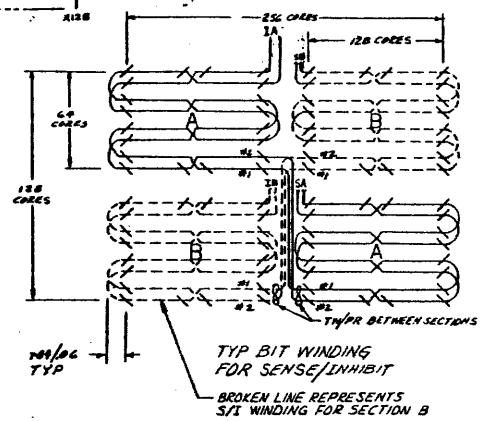




TYP BITS 1, 3, 5, 7, 9, 11, 13, 15, 17 AND 19
POLARITY IDENTIFICATION FOR
INHIBIT LEADS NOT REQUIRED



TYP BITS 0, 2, 4, 6, 8, 10, 12, 14, 16 AND 18
POLARITY IDENTIFICATION FOR
INHIBIT LEADS NOT REQUIRED



TYP BIT WINDING
FOR SENSE/INHIBIT

BROKEN LINE REPRESENTS
S/I WINDING FOR SECTION B

NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	CODE IDENT NO.	DWG NO.
D	16224	9/3949
SCALE —	WEIGHT	SHEET 2 of 2

9/3949 E

electronic memories HAWTHORNE, CALIF.
A DIVISION OF
ELECTRONIC MEMORIES & MAGNETICS CORP.

CONTRACT NO.

S.O. NO

CODE IDENT NO. 16224

PL 913949-001 C

SHEET 1 of 2 REV

DRAWN	10-4-74	DESIGN ENGR	2-20-75
CHECK		PROJ ENGR	2-25-75
OTHER APPR		OTHER APPR	2-25-75

D NO. 1110 D NO

PARTS LIST
WIRED MATRIX ASSY,
QUAD DENSITY - 32K X 20

REVISIONS

EFFECTIVITY	AUTH	LTR	DESCRIPTION	BY	DATE	APPR
DWR 3377		XA	INITIAL PROTOTYPE RELEASE	R2R		
		XB	ITEM 4 WAS 18-105 CORE	[illegible]	11-15-74	
	DWR 3693	C	INITIAL PROD RELEASED	[illegible]	2-25-75	[illegible]

REVISION	C	C																					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24

electronic memories HAWTHORNE, CALIF.
A DIVISION OF
ELECTRONIC MEMORIES & MAGNETICS CORP.

M3000/3220
QUAD DENSITY
32K X 22 STK

CODE IDENT NO. 16224

PL 913949-001 C

SHEET 2 REV

PARTS LIST

NOTE	FIND NO	QTY REQD	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	SPEC/SOURCE	CODE IDENT NO.
	1	1	913947-001	SUBSTRATE - BOTTOM			
	2	1	913948-001	SUBSTRATE - TOP			
	3	REF	913953	CORE PATTERN DIAGRAM			
	4	SEE 360	935018-103	CORE, 18 MIL			
	5						
	6	AR	9257001/44/1/1/2/2	MAGNET WIRE 44 AWG	X & Y		
	7	AR	9257001/41/1/1/2/2	MAGNET WIRE 41 AWG	S/I		
	8						
	9	AR	984513-001	TAPE, SILICONE RUBBER			
	10	AR	928386-001	STRIP, WIRE GUIDE	APPROX 63 INCHES		
	11						
	12	AR	EMMS 9-265	ADHESIVE			
	13						
	14	AR	EMMS 7-303	HINGE - TAPE, 2 1/2 GLASS CLOTH	3/8" WIDE		
	15	REF	984100	WORKMANSHIP STD			
	16						
	17						
	18						
	19						