Part Number 30028-0

MODEL DQ604
DISC CONTROLLER
INSTRUCTION MANUAL

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TABLE OF CONTENTS

Section		Page
1	DESCRIPTION	1-1
	Introduction	1-1
	Controller Characteristics	1-1
	LSI-11 Q Bus Interface	1-1
	Interrupt	1-2
	Disc Interface	1-3
	Controller Specifications	1-3
2	INSTALLATION	2-1
	Inspection	2-1
	Pre-Installation Checks	2-1
	Installation	2-1
3	OPERATION	3-1
	Introduction	3-1
	Precautions and Preoperation Checks	3-1
	Bootstrap Program, Switches and Jumpers	3-1
	Bootstrap Procedure	3-1
	Test and Format Program	3-2
	Test and Format Program Details	3-2
	Format the Disc Program Section	3-2
	Sequential Read Test Program Section	3-3
	Selected Read Test Program Section	3-3
	Random Seek/Read Test Program Section	3-3
	Random Seek, Write, Read, and Compare Test Program Section	3-4
	Alternate Cylinder Assignment	3-4
4	PROGRAMMING AND APPLICATION NOTES	4-1
	Programming Definitions	4-1
	Disc Controller Functions	4-1
	Clear Controller	4-1
	Get Status	4-1
	Seek	4-1
	Write Data	4-1
	Read Data	4-2
	Control Registers	4-2
	Control Status Register 774 400	4-4
	CS 774 440	4-4
	Bus Address Register 774 402	4-5
	Disk Address Register 774 404 During a Seek Command	4-6
	Disk Address Register 774 404 During Format Commands	4-6
	Disk Address Register 774 404 During a Get Status Command	4-7
	Multipurpose Register 774 406 During a Read Header Command	4-8
	Multipurpose Register 774 406 During Read/Write Command for Word Count	4-8
	Multipurpose Register 774 406 During a Get Status Command	4-9
5	TROUBLESHOOTING AND THEORY	5-1
	Basic System Troubleshooting	5-1
	Controller Symptoms	5-1
	Physical Layout	5-1
	Term Listing	5-1
	Adjustment Procedure for Data Separator	5-1
	Theory	5-6
	Computer Interface	5-6
	Phase-Locked Loop	5-7
	MFM Write Encoding	5-7
	MFM Read Decoding	5-11
	Controller Internal Functions	5-12
	Data Buffer	5-12
6	LOGICS	

SECTION 1
DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ604 Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to ST506 compatible Winchester disc drives. The complete controller occupies one quad module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is software compatible with DEC drivers, emulating RL01/RL02 drives.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is done automatically each time power is applied or under operator control by pressing the RESET switch. A green DIAGnostic indicator on the controller board lights if self-test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. The controller is capable of controlling up to two disc drives in various configurations up to a total on-line capacity of 40 megabytes. Figure 1-1 is a simplified diagram of a disc system.

*DEC is a registered trademark of Digital Equipment Corporation.

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q bus interface lines are listed in Table 1-1.

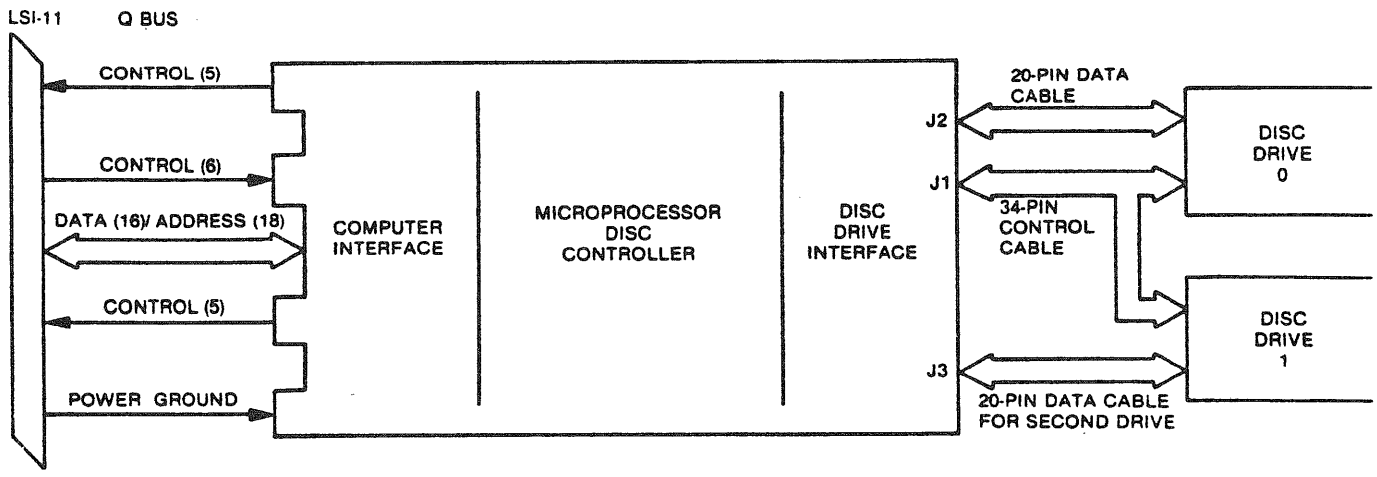


Figure 1-1. Disc Controller System Simplified Diagram

Table 1-1. Controller/Q Bus Interface Lines

BUS PIN	MNEMONIC	TO/FROM Q BUS	DESCRIPTION
AJ1, AM1, RT1	GND		Signal Ground and DC return.
AN1	BDMR L	To	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	To	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREFL	From	Memory Refresh
BA1	BDCOK H	From	DC power ok. All DC voltages are normal.
BB1	BPOK H	From	Primary power ok. When low activates power fail trap sequence.
BJ1, BM1, BT1, BC2	GND		Signal Ground and DC return.
BN1	BSACK L	To	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	To	External Event Interrupt Request.
BV1, AA2, BA2	+5	From	+5 volt system power.
AD2, BD2	+12	From	+12 volt system power.
AE2	BDOUT L	From/To	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	From/To	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	From/To	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNCL	From/To	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	From/To	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	BIRQ L	To	Interrupt Request.
AM2 AN2	BIAK1 L BIAK0 L	From/To	Serial Interrupt Acknowledge input and output lines routed from Q Bus, through devices, and back to processor to establish an interrupt priority chain.
AP2	BBS7 L	From/To	Bank 7 Select. Asserted by bus master when address in upper 4K bank (28-32K words) is placed on the bus.
AR2 AS2	BDMG1 L BDMG0 L	From/To	DMA Grant Input and Output. Serial DMA priority line from computer, through devices, and back to computer.
AT2	BINIT L	From	Initialize. Clears devices on I/O bus.
AU2, AV2	BDAL0/DAL1	From/To	Data/address lines 0 & 1, (2 of 16)
BE2, BF2, BH2 BJ2, BK2, BL2 BM2, BN2, BP2 BR2, BS2, BT2 BU2, BV2	BDAL2 through BDAL15	From/To	Data/address lines, 2-15, (14 of 16)
AC1	BDAL16	To	Extended Address Bit.
AD1	BDAL17	To	Extended Address Bit.

INTERRUPT

The interrupt vector address is factory set to address 160. The vector address is programmed in a PROM on the controller, allowing user selection.

Interrupt requests are generated under the following conditions:

1. A hard error occurs.
2. A soft error occurs. Soft errors are checksum errors (CSE).
3. The designated number of words has been transferred.
4. A selected disc drive has accepted a seek or drive reset command.
5. A seek or drive reset function has been completed.

DISK INTERFACE

The controller interfaces with one or two disc drives through 34- and 20-pin cables. If two drives are used, the 34-pin control cable is daisy chained to drive 0 and 1. The 20-pin data cables are connected separately from the controller to each drive. The maximum cable length is 20 feet. Table 1-2 lists the control interface signals. Table 1-3 lists the data interface signals.

CONTROLLER SPECIFICATIONS†

- Mechanical — the Model DQ604 is completely contained on one quad module 10.44 inches wide by 8.88 inches deep and plugs into and requires one slot in any DEC LSI-11 based system quad backplane.
- Register Addresses
  - Control Status (RLCS) 774400
  - Bus Address (RLBA) 774402
  - Disc Address (RLDA) 774404
  - Multipurpose (RLMP) 774406
- Interrupt Vector Address: 160
- Priority Level: BR4
- Data Transfer Method: DMA
- Bus Load: 1 std. unit load
- Address Range:
  - Disc Drive: 40 Megabytes
  - Computer Memory: to 128K words
- Disc Drive I/O: one 34-pin and two 20-pin flat ribbon connectors mounted on outer edge of controller module
- Signal: ST506 compatible
- Power: +5 volts @ 3.5 amps from computer power supply, +12 volts @ 100 ma.
- Environments: Operating temperature 40°F to 140°F, humidity 10-95% non-condensing
- Shipping Weight: 5 pounds including documentation and cables.

†Specifications subject to change without notice.

Table 1-2. Controller To Drive I/O Interface — "A" Cable

Signal Name (DILOG Term)	Pin	Source
Ground	1	
REDUCE WRITE CURRENT (REDUCE I)	2	Controller
Ground	3	
HEAD SELECT 3 (HESL3)	4	Controller
Ground	5	
WRITE GATE	6	Controller
Ground	7	
SEEK COMPLETE (SEEK COMP)	8	Drive
Ground	9	
TRACK 0	10	Drive
Ground	11	
WRITE FAULT (FAULT)	12	Drive
Ground	13	
HEAD SELECT 1 (HESL1)	14	Controller
Ground	15	
SELECT/NOT USED	16	Drive
Ground	17	
HEAD SELECT 2 (HESL2)	18	Controller
Ground	19	
INDEX	20	Drive
Ground	21	
READY	22	Drive
Ground	23	
STEP	24	Controller
Ground	25	
DRIVE SELECT 1 (DRSL1)	26	Controller
Ground	27	
DRIVE SELECT 2 (DRSL2)	28	Controller
Ground	29	
DRIVE SELECT 3 (DRSL3)	30	Controller
Ground	31	
NOT USED	32	
Ground	33	
DIRECTION IN	34	Controller

Table 1-3. Controller to Drive Data Cable — "B" Cable

Signal	Pin	J2 Term	J3 Term	Source
DRIVE SELECTED	1	DRIVE SELECTED UNIT 0	DRIVE SELECTED UNIT 1	Drive
Ground	2	—	—	—
Reserved	3	—	—	—
Ground	4	—	—	—
Reserved	5	—	—	—
Ground	6	—	—	—
Reserved	7	—	—	—
Ground	8	—	—	—
Reserved	9	—	—	—
Spare	10	—	—	—
Ground	11	—	—	—
Ground	12			
WRITE DATA +	13	WDAT0 +	WDAT1 +	Controller
WRITE DATA −	14	WDAT0 −	WDAT1 −	Controller
Ground	15	—	—	—
Ground	16	—	—	—
READ DATA +	17	RDAT0 +	RDAT1 +	Drive
READ DATA −	18	RDAT0 −	RDAT1 −	Drive
Ground	19	—	—	—
Ground	20	—	—	—

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and may contain cables if this option is exercised. The controller is completely contained on the quad-size printed circuit board. Disc drives, if supplied, are contained in separate shipping cartons. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

Damage to the backplane assembly may occur if the controller module is plugged in backwards.

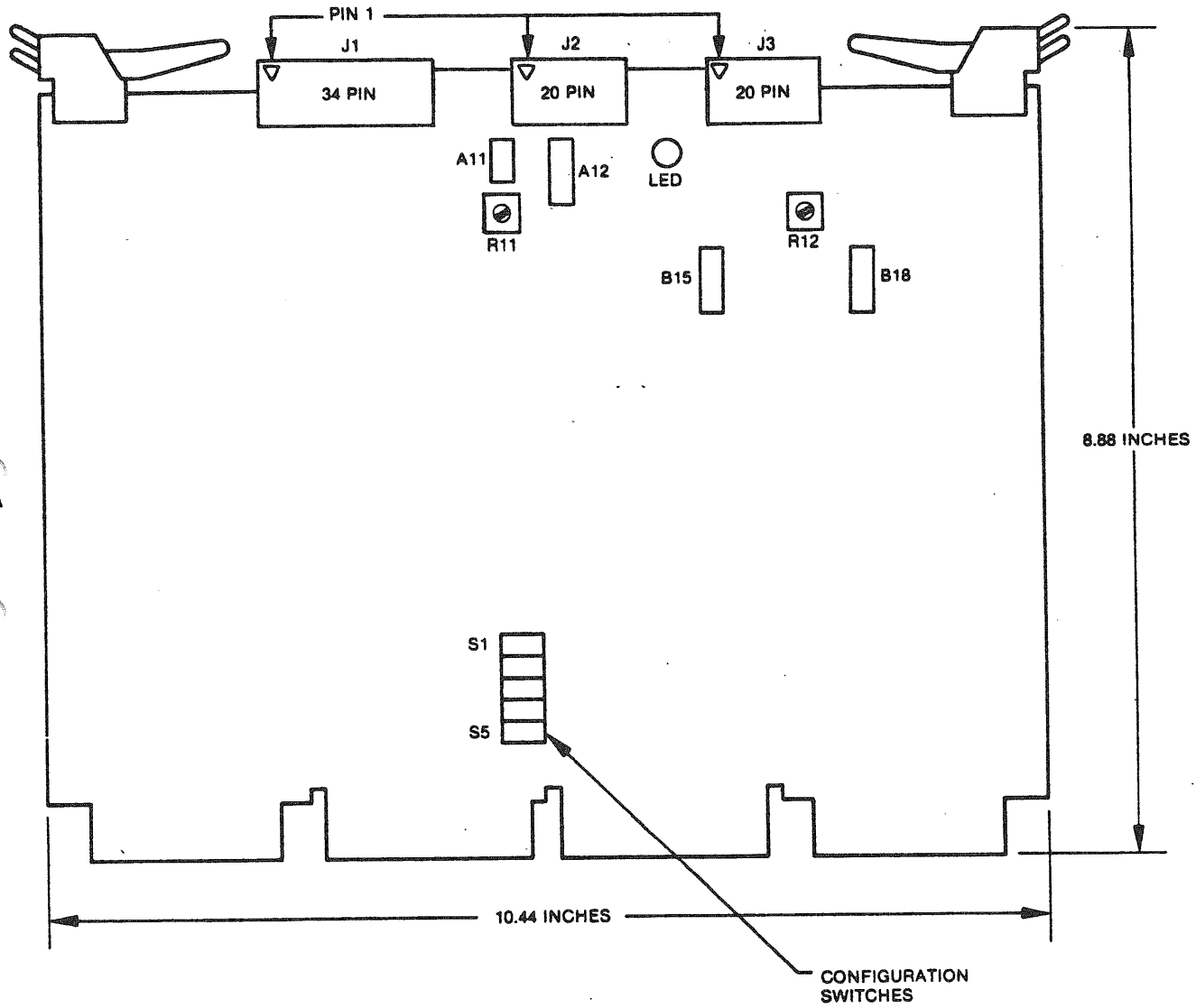
1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

   There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

   It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 x NS	C0 x M2	BIAK1/L0
C0 x S2	C0 x R2	BDMG1/L0
↑	↑	
Last Full Option Slot	Controller Slot	

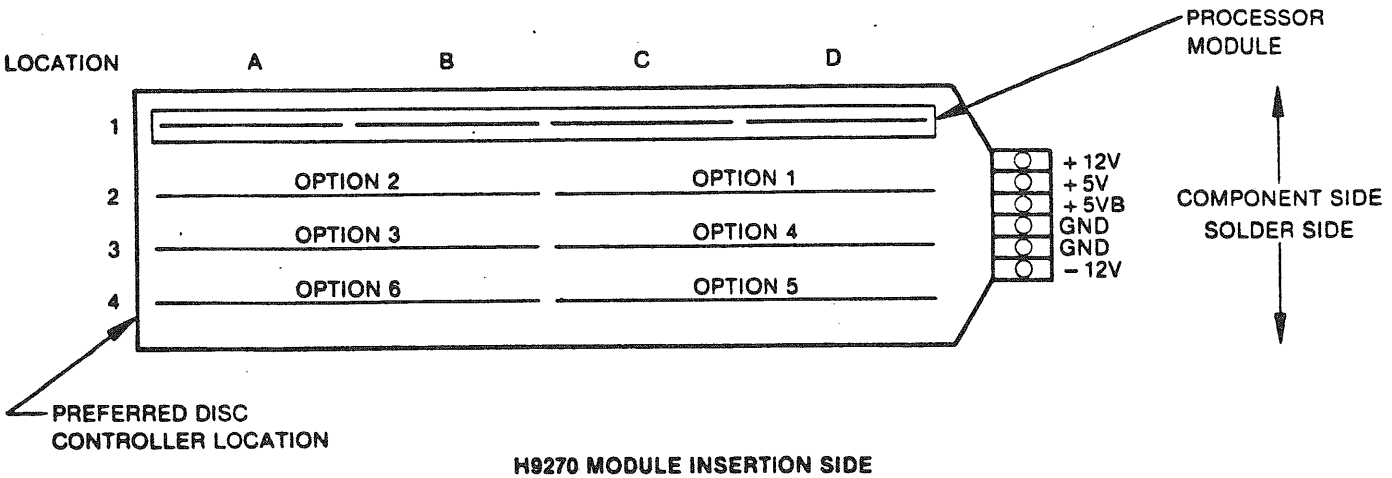
2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.



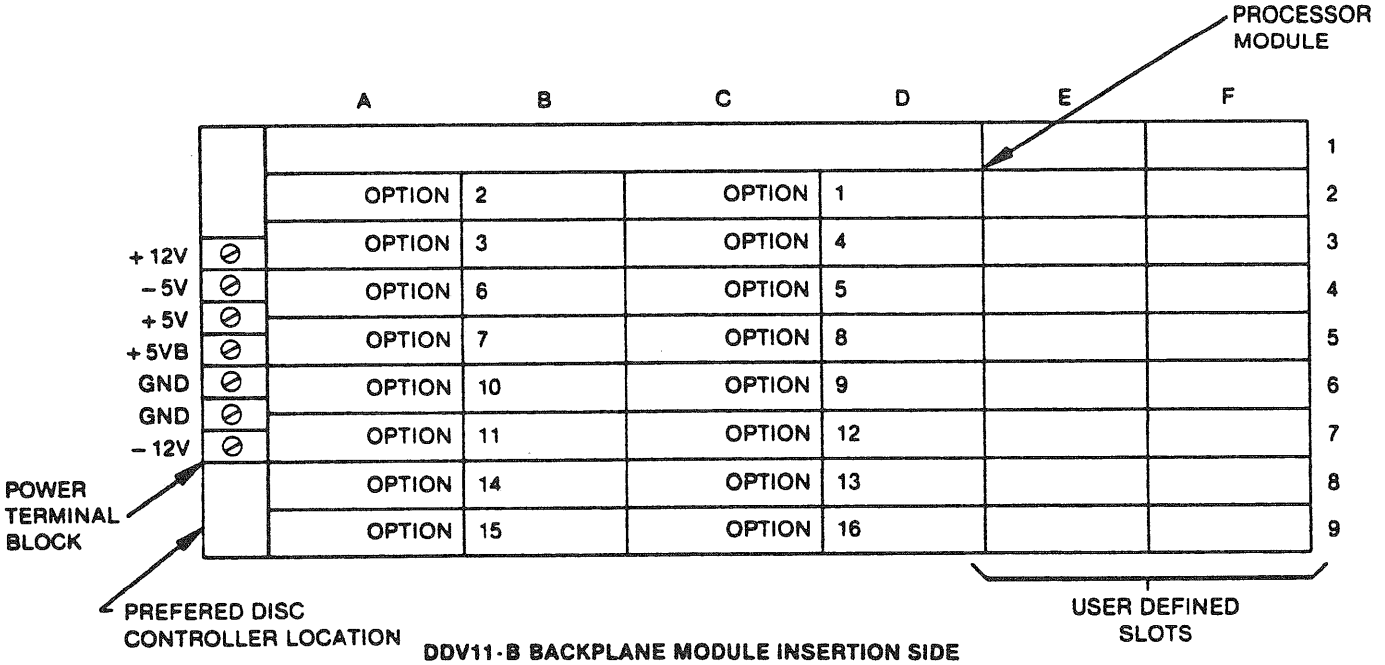
SWITCH	POSITION	DESCRIPTION
S1*	ON	RL01 STATUS
	OFF	RL02 STATUS
S2	NOT USED	
S3	ON	ENABLES CONTROLLER BOOTSTRAP
	OFF	DISABLES CONTROLLER BOOTSTRAP
S4	NOT USED	
S5	ON	ENABLES STEP BUFFER
	OFF	DISABLES STEP BUFFER

*Refer to the start-up message of the diagnotic for the implications of this status at format time. If the switch setting of S1 is changes, the drive must be reformatted.

Figure 2-1. Controller Configuration



H9270 MODULE INSERTION SIDE



DDV11-B BACKPLANE MODULE INSERTION SIDE

NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

3. Feed the module connector end of the disc I/O cables into the controller module connectors. Ensure the pins are properly aligned as shown in Figure 2-1, and install the cable connectors into the module connectors. Verify that the connectors are firmly seated.
4. Ensure the pins are properly aligned, and connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.
5. Refer to the disc manual for operating instructions and apply power to the disc drive and computer.
6. Observe that the green DIAGnostic LED on the controller board is lit.

760 000
760 010

SECTION 3
OPERATION

INTRODUCTION

This section contains procedures for operating the computer system with the controller and a disc drive or drives. An understanding of DEC operating procedures is assumed. The material here is provided for "first time users" of disc subsystems and describes procedures for bootstrapping, formatting, and diagnostic testing.

PRECAUTIONS AND PREOPERATION CHECKS

The following precautions should be observed while operating the system. Failure to observe these precautions could damage the controller, the disc cartridge, the computer, or could erase a portion or all of the stored software.

1. If the controller bootstrap is to be used, set controller switch S3 on, and disable other bootstraps that reside at that address.
2. See Figure 2-1 for proper positions of the other switches.
3. Do not remove or replace the controller board with power applied to the computer.
4. If system does not operate properly, check operating procedures and verify that the items in Section 2 have been performed.

Before operation the following checks should be made:

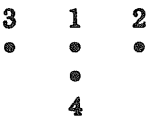
1. Verify that the controller board is firmly seated in backplane connector.
2. Verify that the cables between the controller and the disc are installed.
3. Apply power to the computer and the console device.
4. Verify that the green DIAG light on front edge of the controller board lights.
5. Be sure power is applied to disc drive.

BOOTSTRAP PROGRAM, SWITCHES AND JUMPERS

The DILOG Program will boot the system for RL01/RL02. The controller bootstrap program is disabled when Switch 3 (Figure 2-1) is OFF. In addition to Switch 3, one of three jumper wires may be inserted to select the controller bootstrap starting address. The jumper connections are located (component side) between components D22 and E22. The jumper and address configurations for selecting the bootstrap program are as follows:

Jumper	Address
1 to 2 (Standard Address)	DILOG = 173000
1 to 3 (Alternate Address)	DILOG = 171000
1 to 4 (hardware disabled)	771

The etch or jumpers are factory installed for the user's requirements, but may be changed. On the solder side of the board, the configuration resembles the following:



To change the configuration, cut the existing etch and rewire as described above.

Note

If a system has more than one device with bootstrap capabilities enabled, the bootstraps must be at different addresses.

Device address selection may also be jumper selectable. The jumper connections are located between components E18 and F18. Configurations are as follows:

Jumper	Device Address
R to P (Standard)	174400
K to R (Alternate)	175400

On the solder side of the board the configuration resembles the following:

To change the configuration cut the existing etch and rewire as described above.

BOOTSTRAP PROCEDURE

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate DEC manual for a discussion of the

Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

@ 173000G or 171000G
Depends on switch and jumper configuration above.

* DL 0 <CR>
DL if disc. Booting can be executed from logical units other than "0" shown in the example by entering the desired logical unit number, ie., 1, 2, 3....

TEST AND FORMAT PROGRAM

This DILOG supplied program tests the controller and the disc drive(s) and also formats the disc(s). During formatting, the program also verifies the disc. If there are media errors on the disc, the cylinder, and head in which the errors occur are displayed on the CRT terminal.

Note

When an error occurs during any section of the program, write down the cylinder and head (decimal) number and re-assign the alternate track in Section 8 of the program.

The test/format program contains the following sections:

1. TEST CONTROLLER
   A. Test controller registers.
   B. Test controller data buffer.
2. TEST DISC DRIVE
   A. Test is disc ready.
   B. Test of disc will restore (seek to cylinder zero).
3. FORMAT THE DISC
   This section allows the selection of logical units to be formatted. While formatting the following sequence occurs:
   A. Write headers (all data will be erased).
   B. Read headers.
   C. Write data test pattern.
   D. Read data test pattern.
4. SEQUENTIAL READ TEST
   This section reads data from all logical units starting at logical unit zero.
5. SELECTED READ TEST
   This section allows the selection of a specific logical unit to be tested (read data only).
6. RANDOM SEEK/READ TEST
   This test selects a random cylinder, logical unit, and a sector address within the cylinder. All logical units are used in this test. The terminal keyboard space (SP) character is used to exit this test.
7. RANDOM SEEK, WRITE, READ, AND COMPARE TEST
   This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows the selection of logical units to be tested. The CRT terminal keyboard space (SP) character is used to exit from this test section.
8. ALTERNATE CYLINDER ASSIGNMENT
   Alternate cylinders are assigned at this time.

Test and Format Program Details

The program format for different capacity disc drives is identical. The message content in the program introduction is as follows:

```
TEST AND FORMAT   XXXXX (e.g., DQ604)
                  DISC SYSTEM
                  (REV. X)

SWITCH INFORMATION  OPEN = OFF
                    CLOSED = ON

X (e.g., 5) ALTERNATE CYLINDERS MAY BE ASSIGNED PER UNIT.

THE INTERLACE IS X TO X (e.g., 3 to 1)
```

During execution of the first two sections of the program, drive information is displayed for the operator. The purpose of this information is to define the characteristics of the disc drive used with the system.

Parameters, such as number of logical units, bytes per logical unit, drive model, etc., will be for the specific disc drive for which the software supplied is configured.

When the last line of the introduction is displayed, sections 1 and 2 of the program will have been executed and section 3 (FORMAT THE DISC) is ready for execution.

FORMAT THE DISC PROGRAM SECTION

This program section allows the operator to either sequentially select logical units or to select one or more specific logical units to be formatted. Program messages are presented for formatting in logical unit number sequence, i.e.:

```
FORMAT RL0 (Y OR N)? Y
FORMAT RL1 (Y OR N)?
FORMAT RL2 (Y OR N)?
```

To skip over formatting logical units, respond N (no) followed by a carriage return. To format logical units, respond Y (yes) followed by a carriage return.

Before the yes response causes a logical unit to be formatted, the following message is displayed:

ARE YOU SURE?

This second-level query, which also requires a Y (yes) response to cause program execution, prevents accidentally formatting a previously-formatted logical unit (possibly destroying good data) unless specifically desired.

If for some reason the disc is not in a condition to be formatted (not ready), the system will display the following message:

PROGRAM ADDRESS XXXXXX

where the "X's" reference an address in the program listing that contains status bits identifying the problem.

As a troubleshooting aid, following the PROGRAM ADDRESS XXXXXX message are listed four controller register mnemonics, the register addresses, and the contents of the registers. Following the seven-line controller register message, a two-line message is displayed as a visual aid in isolating the specific problem. With this message as a "key" the operator can examine the contents of the registers previously displayed to isolate the exact nature of the failure to format.

The next message will be:

USE PROCEED (R) TO REPEAT TEST XXXXXX

where the "X's" are an address in the program after the program address at which the format problem occurred.

As a visual indication of the execution of the format routine, the green LED indicator on the controller board will flicker.

When a selected logical unit has been successfully formatted and verified (a four-step process), the following message will be displayed:

RLX FORMAT AND VERIFICATION COMPLETE

where the "X" is the specified logical unit number that has been formatted and verified.

After the last logical unit requested to be formatted has been formatted and verified, the following message will be displayed:

SEQUENTIAL READ (ALL CYLINDERS AND LOGICAL UNITS)?

This indicates that section 3 of the program has been completed and section 4 can now be executed.

SEQUENTIAL READ TEST PROGRAM SECTION

This section tests all cylinders and logical units of the disc(s) in the system and can be performed at any time. If the response to the section 4 message:

SEQUENTIAL READ (ALL CYLINDERS AND LOGICAL UNITS)?

is Y (yes), section 4 will be executed and the contents of the system disc will be read. If the operator response is N (no), section 4 will not be performed and a message indicating that section 5 can be executed will be displayed.

SELECTED READ TEST PROGRAM SECTION

This section of the test allows selected logical units that have been formatted to be read. The message indicating entry to this section is:

READ RLO (Y OR N)?

The message format presenting successive logical units to be read is similar to the format in section 3. A response of either N (no) or CR (carriage return) skips over the testing of logical units.

The following message indicates the exit from this test section and the entry into section 6:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND LOGICAL UNITS)?

RANDOM SEEK/READ TEST PROGRAM SECTION

This test section selects a random cylinder, random logical unit, and sector and reads 32 consecutive sectors regardless of the first sector selected by the program. If an error occurs during this test, the following message will be displayed:

PROGRAM ADDRESS = XXXXXX

where the "X's" are the program address at which the program halted. As in test section 3, register mnemonics, register addresses, and register contents are displayed followed by a summary error mesage.

The summary error message will have the following form:

READ DATA COMMAND

"the error message"

USE (R) TO REPEAT TEST (repeats section 6 only)

The keyboard space (SP) character is used to exit this test and proceed to test section 7.

RANDOM SEEK, WRITE, READ, AND COMPARE TEST PROGRAM SECTION

This test performs a write, read, and compare of data in a random cylinder and sector of a selected logical unit. The message format presents successive logical units for operator selection as in test section 3. A N (no) response skips to a successive logical unit. A Y (yes) response is followed by the message:

ARE YOU SURE?

This secondary response request attempts to prevent accidentally destroying good data. A Y (yes) response to this message initiates the test. Physical indications of test performance are the blinking of the green LED on the controller board and vibration of the disc unit (indicating random head seeking).

This test can be exited at any time by pressing the space (SP) bar on the terminal after the following message is displayed:

ALTERNATE CYLINDER ASSIGNMENT

ALTERNATE CYLINDER ASSIGNMENT

Alternate cylinders may now be assigned, the message

ASSIGN ALTERNATE CYLINDER?

will appear. The operator response to this message is either Y (yes) or N (no). This allows the operator the option of selecting alternate cylinders. Spare cylinders are always allocated. Disc manufacturers recommend that if more than seven cylinders are defective, the disc should be serviced by factory-trained personnel.

USE (R) TO REPEAT TEST

If R (REPEAT) is pressed, the entire 8-section test sequence will be repeated.

Note

After executing the test and format program, the operator must re-boot the system.

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function — The expected activity of the disc system (write, seek, read, etc.).

Command — To initiate a function (halt, clear, go, etc.)

Instruction — One or more orders executed in a prescribed sequence that causes a function to be performed.

Address — The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register — An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

DISC CONTROLLER FUNCTIONS

The disc controller performs 6 basic functions. In addition, when bit 15 of the multipurpose register is off, the function write data, becomes write format, and the function read data becomes read header. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The 6 functions performed by the controller are established by bits 01, 02 and 03 of the control status register (RLCS). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

Clear Controller

This function clears controller logic to initial conditions and terminates data transfers at the end of the sector currently being transferrred. This function is entered when the controller is initially cleared or when the function register contents equal 0. If GO is set while the contents of the function register equals zero, CLEAR CONTROLLER is generated. The CLEAR command can be executed even if the controller is in the NOT READY state.

Table 4-1. Controller Functions

Bit			Octal Code	Description
03	02	01		
0	0	0	(0)	Clear Controller
0	0	1	(2)	No Op
0	1	0	(4)	Get Status
0	1	1	(6)	Seek
1	0	0	(10)	No Op
1	0	1	(12)	Write Data*
1	1	0	(14)	Read Data**
1	1	1	(16)	Read Data (without header check)

*Write format if bit 15 is off in the Multipurpose Register — word count (774 406)

**Read format if bit 15 is off in the Multipurpose Register — word count (774 406)

Get Status

This function is used to get drive status into the multipurpose register. Bit 5 of the disc address register is used to read/write the data buffer. Bit 4 performs a restore operation.

Seek

The Seek function is responded to by the controller if the octal code 06 is loaded in the RLCS register and GO is set; all the proper responses are made to the RL01/02 handler by the controller to indicate the proper completion of this function, seek complete interrupt, etc. . . . However, the controller does not actually issue a seek command to the disc drive. This function was originally implemented when each physical disc drive was one logical unit. Now that multiple logical units are in one physical drive, the function is no longer practical. Furthermore, all Read and Write functions include automatic seeks.

Write Data

The Write Data function includes a Seek to the desired starting disc address (cylinder and track). The function is executed by loading octal code (10) into RLCS and setting GO. Causes the controller to write one or more data records on the addressed

disc. Writing starts at the drive, cylinder, head, and sector address specified by the RLDA register. The amount of data written is specified by the (RLMP) word count register. Write data transfer start from memory address specified by the RLBA register. Each data word transferred increments the Bus Address and Word Count registers. When the (RLMP) word count overflows, data transfer is completed and controller action is terminated at the end of the current disc sector. As data is written a CRCC is calculated and written as the last word of each sector. Prior to writing, the Header record is read to verify proper head positioning.

If bit 15 is off in RLMP (word count), the function performed is write format.

Read Data

Causes the controller to read one or more data records from the disc drive. The Read function includes a Seek to the starting disc address (cylinder, head, sector) and is initiated by loading octal code 14 into the RLCS register and setting GO. Data transfers from the disc are stored in memory starting with the memory address specified by the RLBA register. The amount of data read is specified by the RLMP word count register. Each data word transferred increments the Bus Address and Word Count registers. The contents of the RLMP word count at the beginning of the transfer specify the number of words to be transferred. When the RLMP word count overflows, data transfers stop.

While data is being read, the controller calculates a CRC. At the end of the sector, the calculated CRC is compared with the CRC read from the sector. If they disagree, bit 11 of RLCS is set.

Prior to reading the data record the header record is read to verify proper head position.

If bit 15 is off in RLMP (word count), the function performed is read header.

CONTROL REGISTERS

All software interaction between the disc controller, the processor, and the processor memory is accomplished by four registers which are read as eight registers in the disc controller. These registers are assigned memory addresses and can be read or written into (except as noted) by instructions that reference respective register addresses. The eight controller registers, their addresses, their mnemonics, and their bit assignments are shown in Figure 4-1.

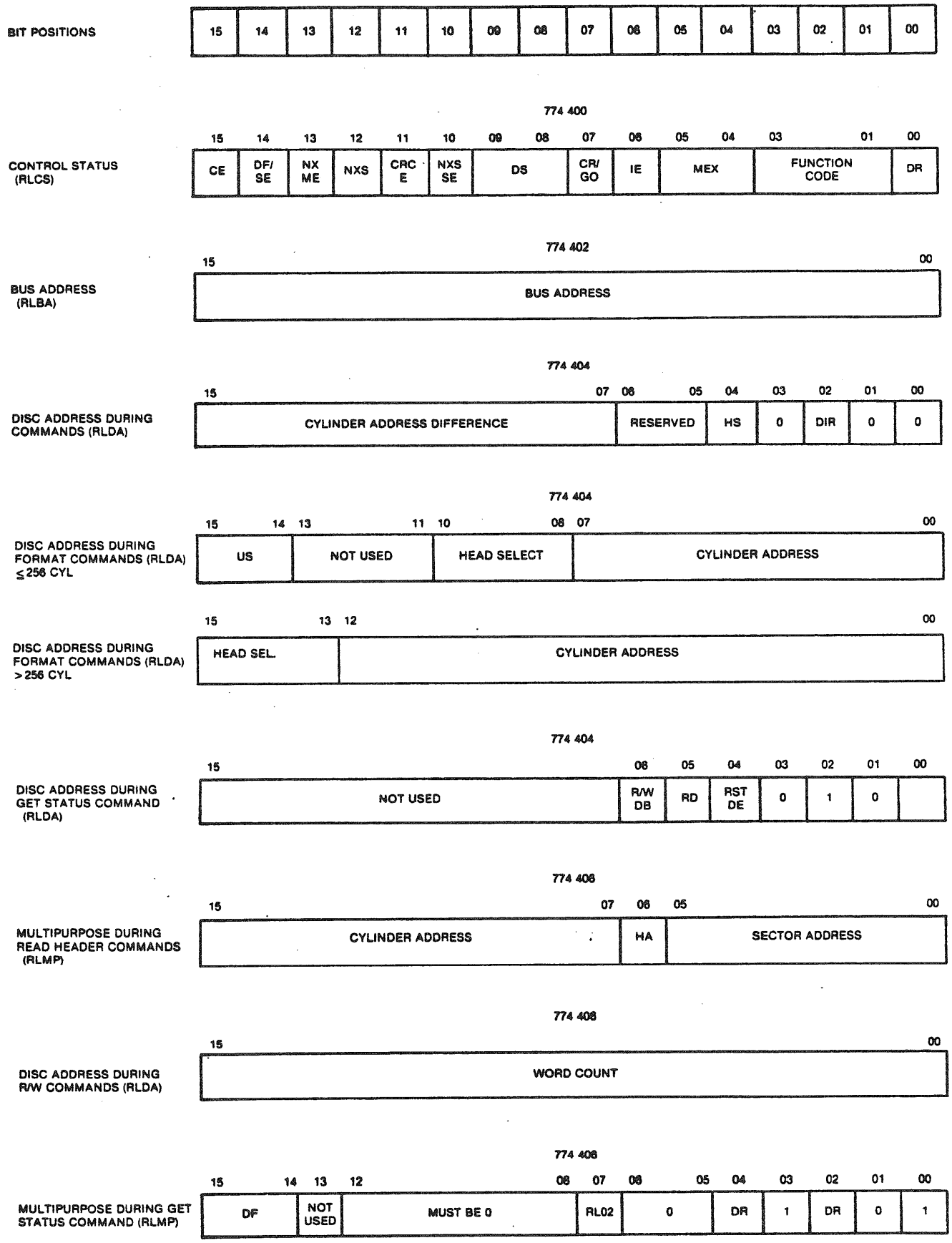
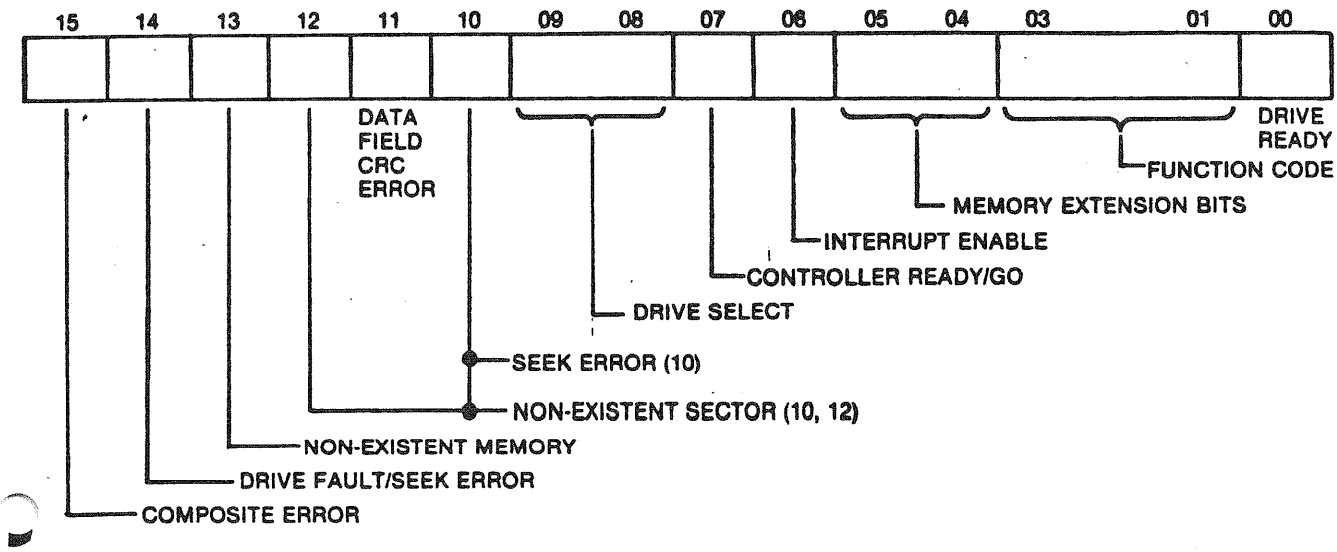


Figure 4-1. Controller Register Configurations

Control Status Register 774 400



CS 774 440

The address of RLCS is 774 400. This register indicates drive conditions; decodes drive commands; and provides overall control functions and error indications.

Bit(s)	Description
00	DRIVE READY — When set, this bit indicates that the selected drive is ready to receive a command. The bit is cleared when a function is initiated and set when the function is completed.
01-03	FUNCTION CODE — These bits are set by software to indicate the command to be executed.

They are:

Bit			Octal Code	Description
03	02	01		
0	0	0	(0)	Clear Controller
0	0	1	(2)	No Op
0	1	0	(4)	Get Status
0	1	1	(6)	Seek
1	0	0	(10)	No Op
1	0	1	(12)	Write Data*
1	1	0	(14)	Read Data**
1	1	1	(16)	Read Data (without header check)

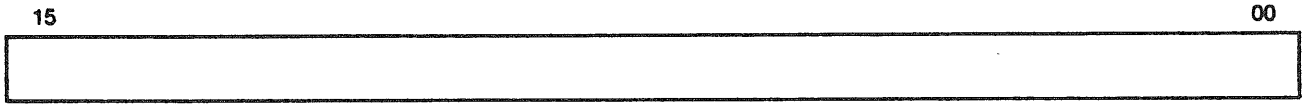
*Write format if bit 15 is off in the Multipurpose Register — word count (774 406)

**Read header if bit 15 is off in the Multipurpose Register — read header (774 406)

04-05	MEMORY EXTENDED ADDRESS — Extended bus address bits for systems with memories larger than 32K 16-bit words. Used in conjunction with the RLBA register. These bits increment each time RLBA overflows.
06	INTERRUPT ENABLE — Causes the controller to raise an interrupt request when either a disc operation is completed or if an error occurs. This read/write bit is cleared by INIT or RESET.

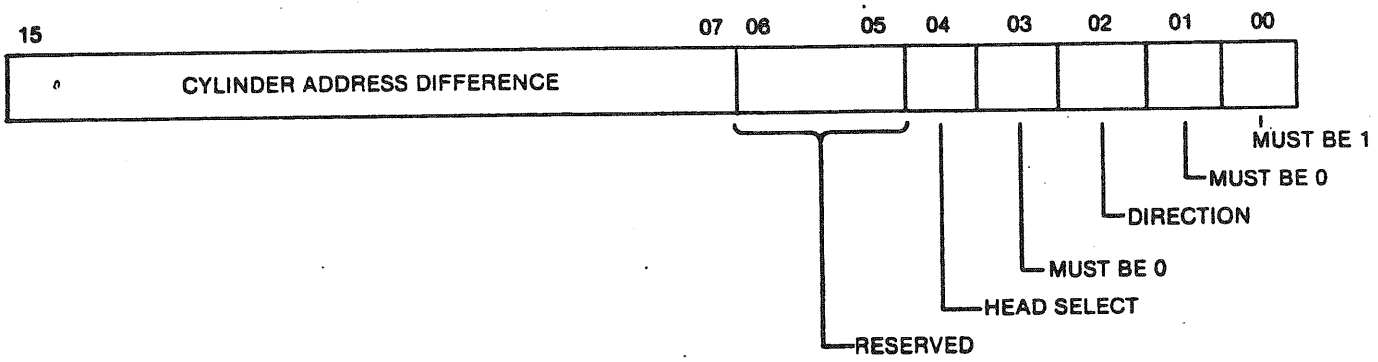
Bit(s)	Description
07	CONTROLLER READY/GO — When cleared by software, this bit indicates that the command in bits 1-3 is to be executed. When set, this bit indicates the controller is ready to accept another command.
08-09	DRIVE SELECT — These bits determine which drive will communicate with the controller via the drive bus.
10, 12	NON-EXISTENT SECTOR — Operation was attempted when the contents of the register for sector address was not within the proper range or the requested sector was not found. Reset by INIT or RESET functions.
10	SEEK ERROR — When this bit is set and bit 12 is cleared, controller unable to verify head position. Reset by INIT or RESET functions.
11	CRC ERROR — When this bit is set, a CRC error occurred in the data field during a read operation; or the error occurred in the header if a read header command was issued.
13	NON-EXISTENT MEMORY — When set, this bit indicates that BRPLY L was not received within the required time during a DMA data transfer.
14	DRIVE FAULT/SEEK ERROR — When set, this bit indicates that an error condition was detected within the drive or a seek was not completed within the required time.
15	COMPOSITE ERROR — When set, this bit indicates that one or more of the error bits is set (bits 10-14). If bit 6 is set and an error occurs, the current operation will terminate and the interrupt routine will be initiated.

Bus Address Register 774 402



The address of RLBA is 774 402. The bits of this register contain the bus address of data transferred during read or write check operations. The register is incremented by two at the end of each transfer. If the system has extended memory, the RLBA will overflow to the EX MEM bits (04, 05) of the RLCS to reflect the extended bus address. This is a read/write register cleared by INIT or RESET functions.

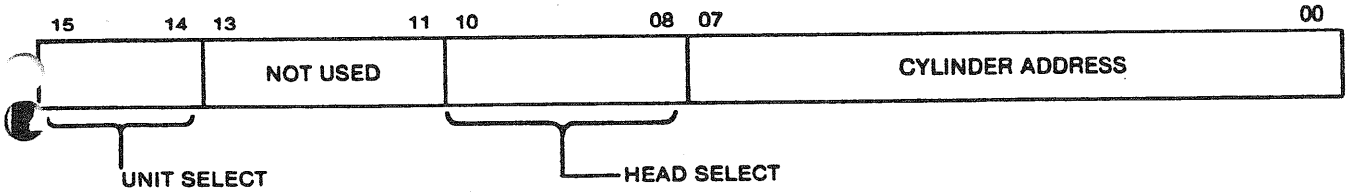
Disc Address Register 774 404 During a Seek Command



Bit(s)	Description
00	Must be 1
01	Must be 0
02	DIRECTION — This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move to a higher cylinder address. When the bit is cleared, the heads move to a lower cylinder address.
03	Must be 0.
04	HEAD SELECT — Indicates which head (disc surface) is to be selected. Set = Lower, Clear = Upper.
05-06	RESERVED
07-15	CYLINDER ADDRESS DIFFERENCE — Indicates the number of cylinders the heads are to move on a seek.

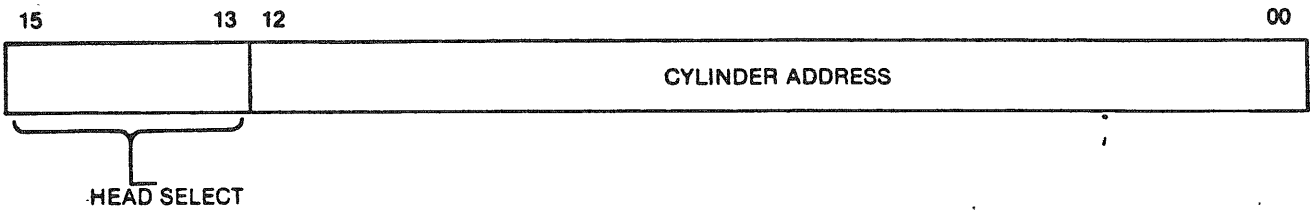
Disc Address Register 774 404 During Format Commands

On emulations where physical disc has 256 cylinders, or less:



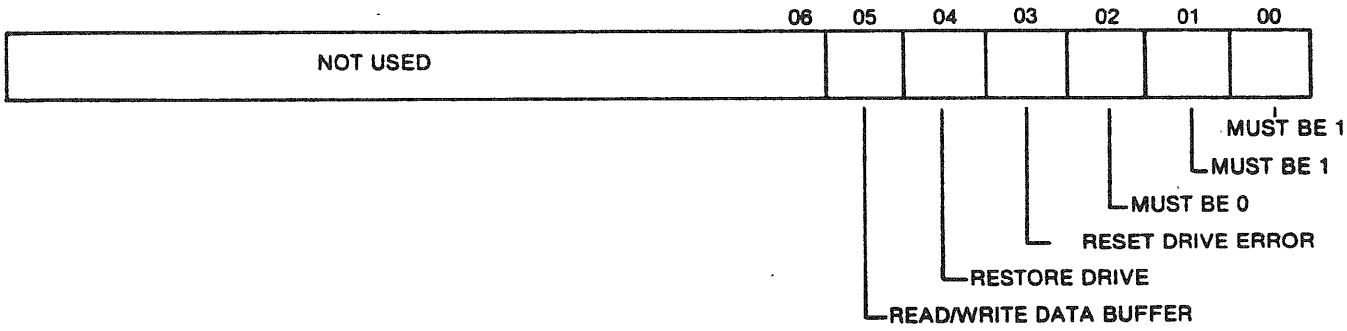
Bit(s)	Definitions
00-07	CYLINDER ADDRESS — Address of the cylinder being accessed.
08-10	HEAD SELECT — Indicates which head (disc surface) is to be selected.
11-13	NOT USED
14-15	UNIT SELECT — Indicates which logical unit is to be selected.

On emulations where physical disc has more than 256 cylinders:



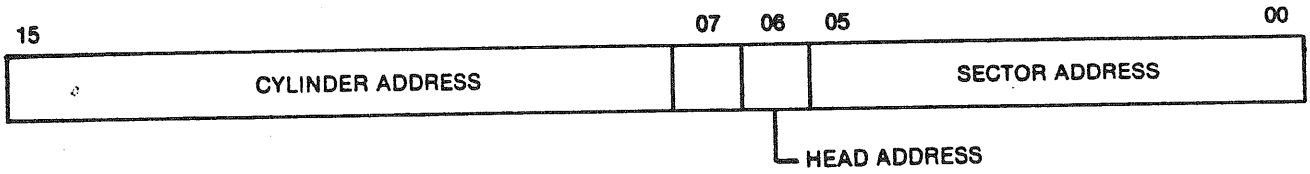
Bit(s)	Definitions
00-12	CYLINDER ADDRESS — Address of cylinder being accessed.
13-15	HEAD SELECT — Indicates which head is to be selected.

Disc Address Register 774 404 During a Get Status Command



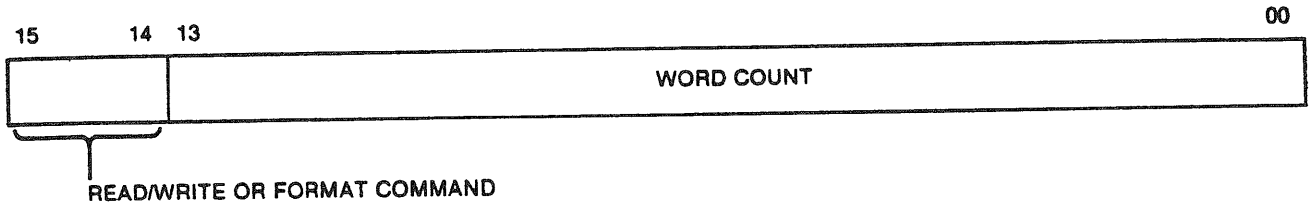
Bit(s)	Description
00-01	Must be 1
02	Must be 0
03	When this bit is set, the drive clears its error register before sending a status word to the controller.
04	RESTORE DRIVE — When set, this bit will cause the heads to return to cylinder 0.
05	READ/WRITE DATA BUFFER — When this bit is set, reading from and writing to the Multipurpose Register accesses the controller Data Buffer. Each successive access of the Multipurpose Register increments the Data Buffer address.
06-15	NOT USED — Must be 0.

Disc Address Register 774 406 During R/W Command



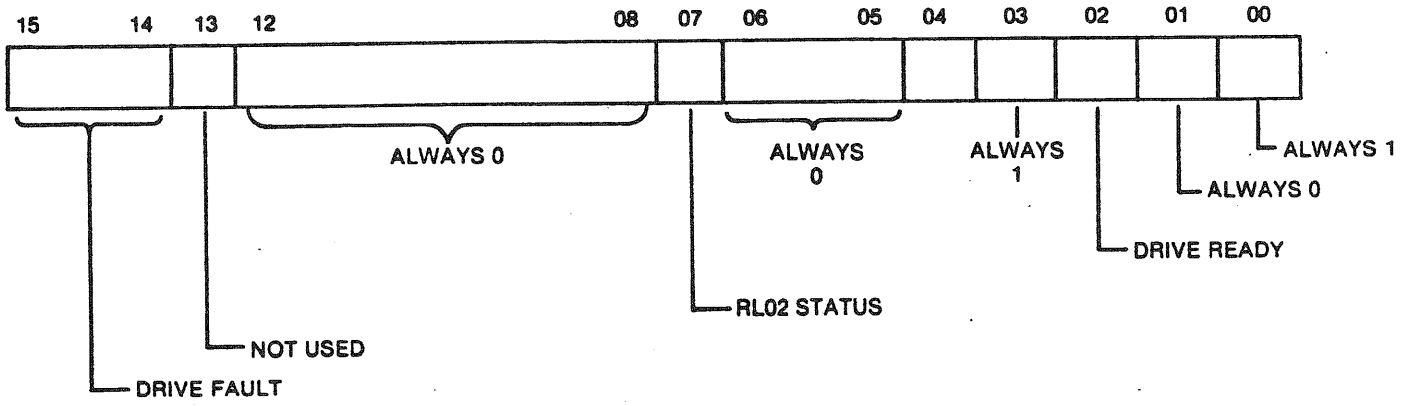
Bit(s)	Definition
00-05	SECTOR ADDRESS — Indicates addressed sector.
06	HEAD ADDRESS — Indicates addressed head. Set = lower; Clear = upper.
-15	CYLINDER ADDRESS — Indicates addressed cylinder.

ultipurpose Register 774 406 During Read/Write Command for Word Count



Bit(s)	Description
00-13	WORD COUNT — These bits are the 2's complement of the total number of words to be transferred during a read, write or write check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is completed and the controller action is terminated at the end of the current disc sector.
4-15	These bits indicate the following: 15, 14 SET; Read/write data command with mapping. 15 SET, 14 CLEAR: Read/write data command with map override. 15 CLEAR, 14 SET; Format command with seek. 15 CLEAR, 14 CLEAR; Format command with no seek.

Multipurpose Register 774 406 During a Get Status Command



RLMP is used to read/write the data buffer by using the GET STATUS command with bit 5 or RLDA.

Bit(s)	Definition
00	Always 1.
01	Always 0.
02, 04	DRIVE READY — When bits 02 and 04 are set, the drive is ready for operation.
05-06	Always 0.
07	RL02 STATUS — When set drive is RL02. When clear drive is RL01.
08-12	Always 0.
13	NOT USED
14-15	DRIVE FAULT — Sets if an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the disc drive manufacturers manual. Ensure power is off when connecting or disconnecting board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.
2. Verify that all switches are properly set as described in Sections 2 and 3.
3. Verify that all modules are properly seated in the computer and properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disc drive generate the proper responses when the system is powered up.
2. Verify that the computer panel switches are set correctly.
3. Verify that the console can be operated in the local mode. If not, the console may be defective.
4. Verify that the green diagnostic light on the controller is on.

CONTROLLER SYMPTOMS

Controller symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +12V source is shown on sheet 17, and the +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers on the logic diagrams.

ADJUSTMENT PROCEDURE FOR DATA SEPARATOR

This procedure should be performed only when a component is changed in the phase-locked loop circuitry. A two-channel oscilloscope and an extender board are required for this adjustment. A frequency counter may also be used but is not required. Component locations are shown on Figure 2-1. Proceed as follows:

1. Connect the controller to an extender board and the board to the bus.
2. Power up the computer and disc drive.
3. Connect Channel A to A12 pin 3, and adjust R11 to 2.5 volts.
4. Connect Channel A, or a frequency counter, to B18 pin 9.
5. Use a short jumper wire to connect C16 pin 3 to C16 pin 8.

Table 5-1. Controller Symptoms

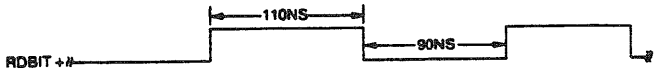
Symptom	Possible Causes	Check/Corrective Action
1. Green DIAG light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator (Sheet 3, B22) b. Short or open on board c. Bad IC d. PROMs not properly seated (Sheet 8 A1 through A7)	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901 (Sheet 7 and 9). All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitute pulses. Check +12V (Sheet 17) and +5V at various IC's. Check PROM's A1 through A7 for proper seating. Check oscillator B22.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. DEN always low (Sheet 5) b. Shorted bus tranceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal DEN for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches. Check cable connections. Controller Registers/Using ODT, examine controller register RLCS, bit 0 and 8 and 9. These bits represent DISC UNIT READY AND SELECTED and must be present for proper communication. Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from disc incorrect	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Test and Format Program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specified in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure—Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad component.

6. Observe the frequency of the VCO. The frequency should be 8.5 MHz ± 0.4 MHz (117 NS ± 5 NS).

7. Remove the jumper wire from C16.

8. Connect Channel A to B18 pin 9. Connect Channel B to B15 pin 8.

9. Adjust R12 for Channel A for 110 nanoseconds high and 90 nanoseconds low as shown:



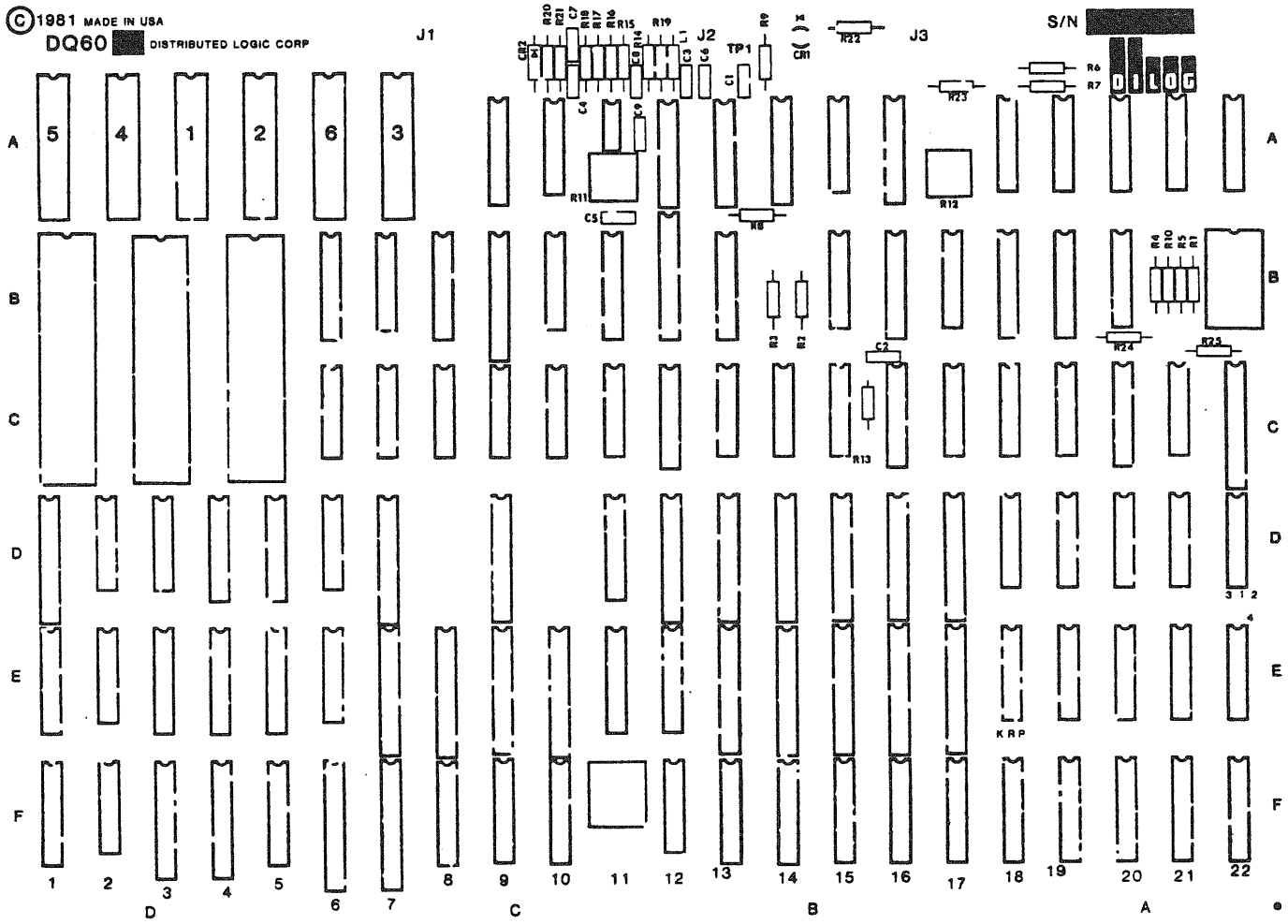
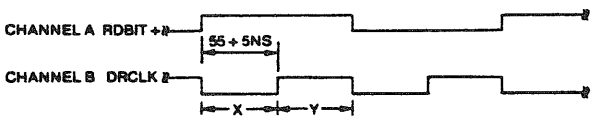


Figure 5-1. Board Layout

10. Reset the bus by pressing the computer console reset switch or by switching the computer power off and on.

11. The following relationship between Channel A and Channel B must occur:



As shown, the leading edge of the pulse on Channel A should be 55±5 nanoseconds from the leading edge of the Channel B pulse so that the X-Y transition of Channel B is approximately centered with the Channel A pulse.

12. Connect Channel B to A11 pin 1, and adjust R11 for 3.1 VDC.

13. Connect Channel B to B15 pin 8 and verify step 11.

14. Connect Channel A to A12 pin 3 and observe the voltage. The voltage should be 2.5 volts ± 0.3 volts.

15. Switch power off at the drive and computer; disconnect the extender board; and re-install the controller as previously described.

The system is now ready to operate. Refer to Section 3 for operating instructions, diagnostics and formatting.

Table 5-2. Term Listing

Term	Source	Destination	Description
AMDET+	15	12,17	Address Mark Detect
AMF+	16	15	Address Mark Found
AMSRCH	14	15, 17	Address Mark Search
BA04+	13	18	Buffer Address
BBS7+	4	2	Peripheral Address Select
BBS7L	4	BUS (AP2)	Bus Peripheral Address Select
BC4+	12	13	Bit Count Y
BDAL00L	5	BUS (AV2)	Data Bus D/R
BDAL01L	5	BUS (AV2)	Data Bus D/R
BDAL02L	5	BUS (BE2)	Data Bus D/R
BDAL03L	5	BUS (BF2)	Data Bus D/R
BDAL04L	5	BUS (BH2)	Data Bus D/R
BDAL05L	5	BUS (BJ2)	Data Bus D/R
BDAL06L	5	BUS (BK2)	Data Bus D/R
BDAL07L	5	BUS (BL2)	Data Bus D/R
BDAL08L	6	BUS (BM2)	Data Bus D/R
BDAL09L	6	BUS (BN2)	Data Bus D/R
BDAL10L	6	BUS (BP2)	Data Bus D/R
BDAL11L	6	BUS (BR2)	Data Bus D/R
BDAL12L	6	BUS (BS2)	Data Bus D/R
BDAL13L	6	BUS (BT2)	Data Bus D/R
BDAL14L	6	BUS (BU2)	Data Bus D/R
BDAL15L	6	BUS (BV2)	Data Bus D/R
BDAL16	4	BUS (AC1)	Extended Address
BDAL17	4	BUS (AD1)	Extended Address
BDCOK–	4	7, 17	DC Power OK
BDIN+	4	2, 11	Data In
BDINL	4	BUS (AH2)	Master Ready for Data
BDMGIL	4	BUS (AR2)	DMA Grant Input
BDMRL	4	BUS (AN1)	Q Bus Request
BDOUT+	4	11	Data Out
BDOUTL	4	BUS (AE2)	Valid Data From Master on Bus
BFULL–	13	11, 12, 14	Buffer Full
BFULE+	3	13	Enable Buffer Full (16)
BIAKOL	4	BUS (AN2)	Interrupt Acknowledge Output
BIAKOL	4	BUS (CN2)	Interrupt Acknowledge Output
BIAKIL	4	BUS (CM2)	Bus Acknowledge Interrupt Levels In
BIAKIL	4	BUS (AM2)	Bus Acknowledge Interrupt Levels In
BINITL	4	BUS (AT2)	Initialize-Clear Devices on I/O Bus
BIRQL	4	BUS (AL2)	Host I/O Interrupt Request
BITCK+	12	13	Byte Clock
BMBGOL	4	BUS (AS2) BUS (CS2)	DMA Grant I/O
BMBGOL	4	BUS (CS2)	DMA Grant Out
BMBGIL	4	BUS (CR2)	DMA Grant
BRPLY+	4	2, 3, 11	Reply from Slave
BRPLYL	4	BUS (AF2)	Q Bus Reply
BSACKL	4	BUS (BN1)	DMA Request Acknowledge
BSYNCL	4	BUS (AJ2)	Synchronize I/O Address

Term	Source	Destination	Description
BTSPF+	2	11	Bootstrap Flag
BWTBT+	4	11	Controller Write Byte
BWTBTL	4	BUS (AK2)	Host I/O Write Byte
CKB	16	17	20 MHz Divided by 4 Clock
CLAMP+	14	17	Reset Phase Lock Loop
COUT+	9	7	Carry Out
CORRV	17	18	Correction Voltage
CP0–	11	4	Control Decode — Reset Slave Request
CP1–	11	3	Control Decode — Set Data Out
CP2–	11	4	Control Decode — Reset Controller
CP3–	11	12	Control Decode — Reset Data Read Sync
CP4–	11	15	Control Decode — Reset Index Flop
CP5–	11	15	Control Decode — Set Index Flop
CP6–	11	2	Control Decode — Reset Q Bus Request
CP7–	11	3	Control Decode — Reset Data Out
CRCER+	11	18	CRC Error Detector
CR1-0/ CR1-2	8	7, 9	Microcode Instruction
CR1-3	8	9, 10, 14	Microcode Instruction
CR1-4/ CR1-7	8	9, 10	Microcode Instruction
CR2-0/ CR2-6	8	9	Microcode Instruction
CR2-7	8	9, 10	Microcode Instruction
CR3-0	8	7	Microcode Instruction
CR3-1/ CR3-3	8	9	Microcode Instruction
CR3-4/ CR3-7	8	10	Microcode Instruction
CR4-0/ CR4-7	8	7	Microcode Instruction
CR5-0/ CR5-7	7	8	Vector Address Register
CR5-0/ CR5-7	8	7	Microcode Instruction
CSA0+/ CSA8+	7	8	Control Store Memory Address
CYCLE–	16	17	10 MHz Clock
DAT0+/ DAT7+	13	12	Data Buffer Data Bus — Bidirectional
DAT0+/ DAT7+	12	13	Data Buffer Data Bus — Bidirectional
DA16+	3	4	Extended Data
DA17+	3	4	Extended Data
DBWS–	12	13	Data Buffer Write Strobe
DB00+/ DB07+	5	2, 11	Data Bus D/R

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
DB08 + / DB12 +	6	2, 11	Data Bus D/R
DB13 + / DB15 +	6	11	Data Bus D/R
DEN –	5	6	Enable Data
DIRECTION	14	J1	Direction of Seek
DMGI +	4	2	DMA Grant In
DRCLK	16	17	Drive Clock (10 MHz)
DRSL1	14	J1	Drive Select 1
DRSL2	14	J1	Drive Select 2
DRSL3	14	J1	Drive Select 3
DRVSEL +	18	15	Drive Selected
DR0SLT	15	18	Drive 0 Selected
DR1SLT	15	18	Drive 1 Selected
D00 + / D05 +	14	9	Switch Signals MUX
D00 + / D07 +	8	9	Source Bus Data Bits
D00 + / D07 +	10	9	Interrupt Vector Bootstrap Loader
D00 + / D07 +	11	9	Data Input MUX
D00 + / D07 +	12	9	Source Bus Data Bit
D00 + / D07 +	18	9	Status Register
D00 + / D07 +	15	9	Disk Status Register
EADD –	5	4, 6	Enable Address — Q Bus Control
EADD +	3	5, 6	Enable Address — Q Bus Control
EBITC +	3	12	Enable Bit Count
EPCOMP	14	16	Enable Precompensation of Write
GSCLK –	3	7, 8, 9, 10	Gated System Clock
HESL1	14	J1	Head Select 1
HESL2	14	J1	Head Select 2
HESL3	14	J1	Head Select 3
IAKI +	4	2	Host Interrupt Acknowledge In
IAKIG –	2	11	Interrupt Acknowledge Inverted
INIT +	4	7	Initialize
LCOUT –	7	9	Latch Carry Out
LXRA –	10	14	Drive Control (Bus 0-7)
LXRB –	10	7	Load Vector Address
LXRC –	10	3	System Control
LXRD –	10	3	Reset Data In
LXRE –	10	3	Q Bus Control
LXR0 –	10	6	Data Out Register (MSR)
LXR1 –	10	5	Data Out Register (LSB)
LXR2 –	10	6	DMA Address (MSB)
LXR3 –	10	5	DMA Address (LSB)
LXR4 –	10	13	Data Buffer Address (LSB)
LXR5 –	10	13	Data Buffer Address (MSB)
LXR6 –	10	12	Data Buffer Data
LXR7 –	10	11	Control Pulse Strobe

Term	Source	Destination	Description
LXR9 –	10	14	Drive Control (TAGS)
MRQB +	3	2	Request Q Bus
QBUSA +	2	11	Q Bus Acknowledge
RDATA +	16	12	Serial Data Input
RDBIT	17	16	Read Bit
REDUCE!	14	J1	Reduce Write Current
RESET –	4	2, 3, 7, 14	Controller Reset
RMFM +	18	17	Read Modified Frequency Modulated
RSYNC +	4	2, 11	Synchronize 2901 to Host I/O Lines
R/WCLK	17	11, 12	Read Write Clock
R/WSRE +	3	12	Shift Register Reset
SCLK –	3	7, 11, 15, 18	Controller Clock
SCLK +	3	10, 12, 13	Controller Clock
SECTOR +	15	18	Sector Pulse
SLIN +	2	7	Slave/Interrupt Acknowledge Request
SPIN0	14	J2	Not Used
SPIN1	14	J3	Not Used
STEP	14	J1	Step Pulse to Disk
TDIN +	3	4	Q Bus Data In
TDMG +	2	4	Bus Grant to D/R
TDOUT +	3	4	Q Bus Data Out
TEST	17	TEST	Test Point
TIAK +	2	4	Interrupt Acknowledge
TIRQ +	3	2, 4	Interrupt Request
TMDR +	2	4	Transmit Direct Memory Grant
TRPLY +	3	4	Q Bus Reply
TSACK –	2	4	System Acknowledge
TSACK +	2	4, 3	System Acknowledge
TSYNC +	3	4	Q Bus Sync
TWTBT +	3	4	Write Byte Q Bus Control
UNIT1	14	18	Select Drive 1
VCO +	17	16	Voltage Controlled Oscillator
VEC –	7	8	Vector Address Register Out
WDATA +	12	16	Write Data
WDAT0 –	18	J2	Write Data Drive 0
WDAT0 +	18	J2	Write Data Drive 0
WDAT1 –	18	J3	Write Data Drive 1
WDAT1 +	18	J3	Write Data Drive 1
WGT	14	18	Write Gate
WMFM	16	17	Write Modified Frequency Modulated
WREN –	12	13	Write Enable
WREN +	3	12, 13, 16, 17	Write Enable
WRITE GATE	14	J1	Write Gate Through Relay
XSD0 –	10	2	Slave Address
XSD1 –	10	11	Data Input (MSB)
XDS2 –	10	11	Data Input (LSB)
XSD3 –	10	11	Q Bus Status
XSD4 –	10	12	Data Buffer Source Decode
XSD5 –	10	15	Disk Drive Status
XSD6 –	10	18	Seek End Status

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
XSD7–	10	14	Select Bootstrap PROM
Y00+/ Y02+	9	3, 5, 6, 7, 10, 11, 12, 13, 14	Y Bus
Y03+	9	3, 5, 6, 7, 10, 12, 13, 14	Y Bus
Y04+/ Y07+	9	3, 5, 6, 7 10, 12, 13, 14	Y Bus
ZERO+	9	7	2901 Output at Zero
1K0V+	13	18	1024 Count Buffer Address
+12V	BUS (AD2)	17	12V System Power
20 MHZ	3	16	20 MHZ Clock

THEORY

The controller may be examined as three parts: computer interface, disc interface and controller internal functions. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the disc drive are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and some of the functional components. Single lines in the illustration represent serial data and the wider lines represent parallel data. A detailed block diagram of the controllers is shown on Sheet 1 of the logic drawings. The numbers in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q-Bus of the LSI-11 computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is selected by base address 774 400. The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the LSI-11 DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and used for "bus arbitration." Bus synchronization is fully controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disc controller is busy with internal functions and controller/disc data transfers.

Data bus driver/receivers F13 through F16 (Sheets 5 and 6) buffer the input data and distribute it as DB 00-15 in the controller. The DB signals are routed to data and address decode registers located on Sheets 11 and 2.

Output data from the microprocessor Y Bus (Y00-Y07) is latched by registers E13 through E16, and transferred to the Q Bus via bus driver/receivers F13 through F16.

Note that the Device Enable signal (DEN-) is active when either Address Enable (EADD) or Data Enable (EDATA) signal is active. DEN controls the operating mode of all data and address driver/receivers, under control of the firmware via the Y Bus (Sheets 5 and 6).

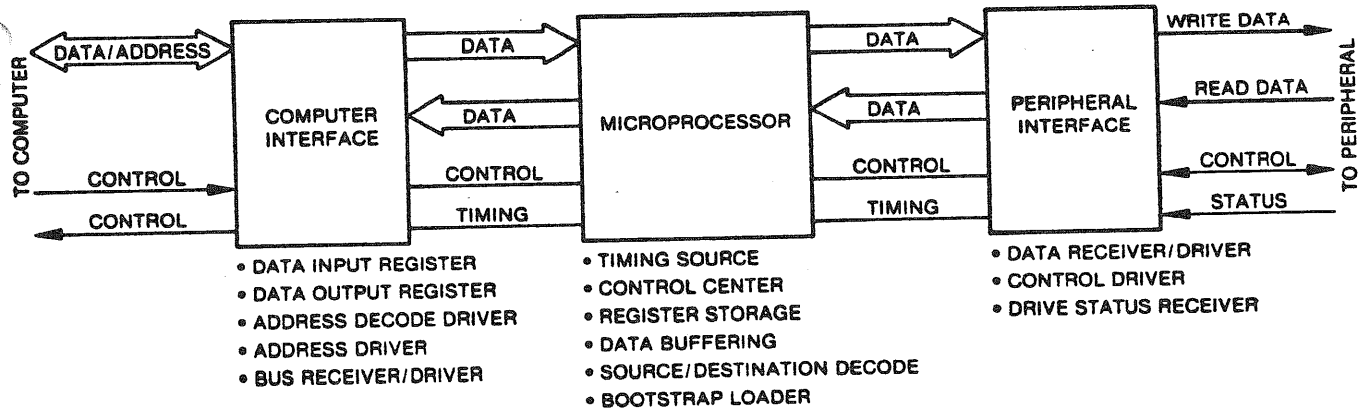


Figure 5-2. Simplified Block Diagram

Phase-Locked Loop

The purpose of the phase-locked loop circuitry, shown on Sheet 17, is to bring the timing on the controller in phase with the data from the disc. The circuit is illustrated in the simplified block diagram, Figure 5-3.

Component A10 is used at the input of the circuit as the temperature compensation reference. At the output, A10 is used for the analog conversion of phase difference. Because of temperature drift, both segments of the component change at approximately the same rate. The output of the compensation reference is transmitted to the *positive* input of the analog inverter, A11, and the output of the analog conversion is transmitted to the *negative* input of A11. The analog inverter compares the phase error and the reference and corrects the voltage for input of the voltage controlled oscillator, A12.

The timing of the circuit is shown in Figure 5-4. The term VCO− on the diagram represents the output of the voltage controlled oscillator. The term and its reciprocal (VCO+) are inputs for the VCO divider which consists of inverter C18, flip flop C15, and gate C14. The output of this circuitry is represented as REF− on the timing diagram. The relationship of VCO− and REF− is 1½ clock pulses; that is, when VCO− goes *low*, REF− goes high and remains high until VCO− goes *high* for the *second* time.

The term REF− is the clock input for the digitized phase difference flip flop, B17. This term and RDBIT+ determine the center of the phase as illustrated in Figure 5-4. If there is no phase error, the outputs of the analog conversion of phase difference, which are PLS1+ and PLS2− will be 55NS each; both will be low and high for an equal time.

As frequency of read data (RDBIT+) increases, PLS1+ remains low longer, and PLS2− remains high for a shorter time, as shown in Figure 5-5. The exaggerated phase error shown in the example occurs when both PLS1+ and PLS2− are low for 76NS and high for 34NS. Notice that the 90NS high and low times are constant in both illustrations. The 110NS segment of the cycle is also constant; the trailing edges of PLS1+ and PLS2− shift left relative to the center of this segment, whereas the leading edges of the pulses remain constant. This offset from center represents the phase error and is transmitted to the analog inverter, A11, where the voltage correction is made for the VCO. If the width of PLS2− is greater than PLS1+, RDBIT+ is slower than the reference clock and must be phase shifted in the other direction.

MFM Write Encoding

The modified frequency modulation (MFM) circuit is shown on Sheet 16. The circuit performs two major functions: encodes MFM write data to the disc drive and decodes read data from the drive. Read and write data are selected by multiplexer B18. A simplified diagram of the write data path is shown in Figure 5-6.

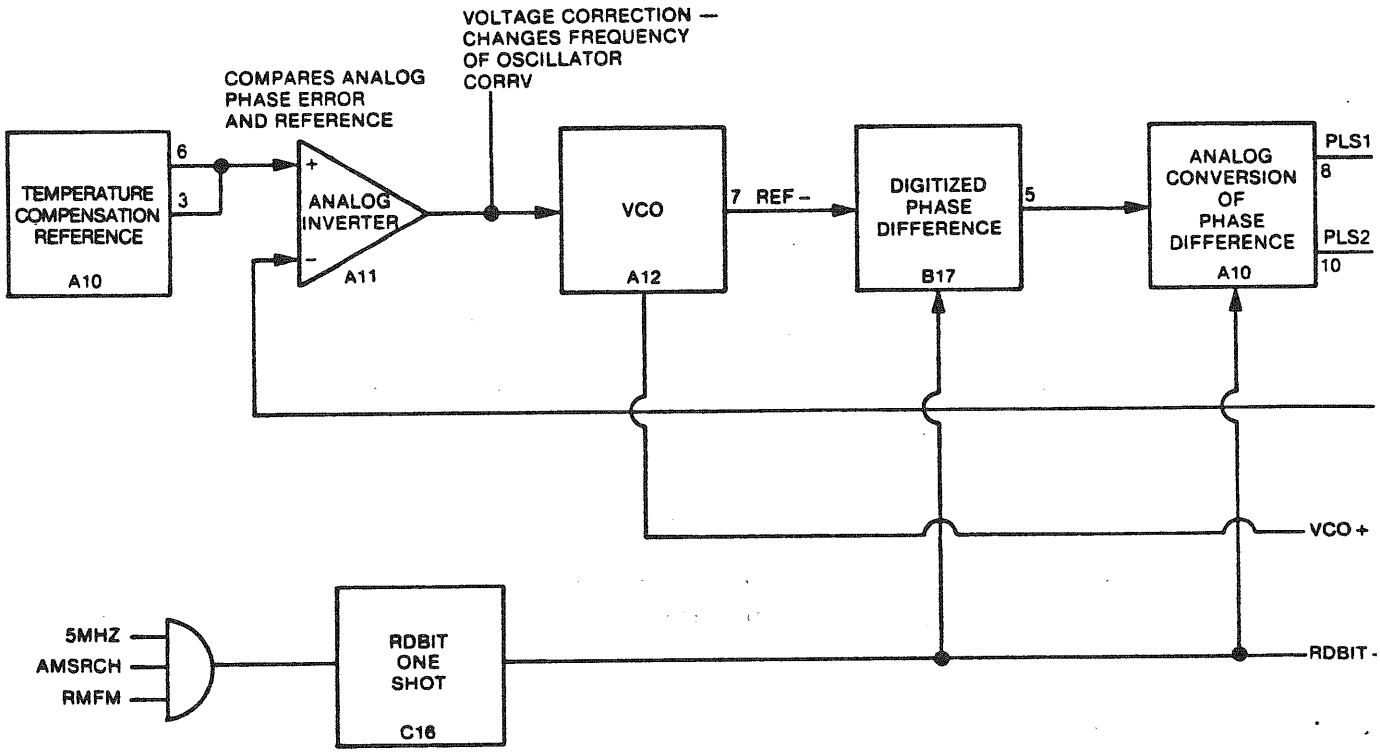


Figure 5-3. Simplified Diagram of Phase-Locked Loop

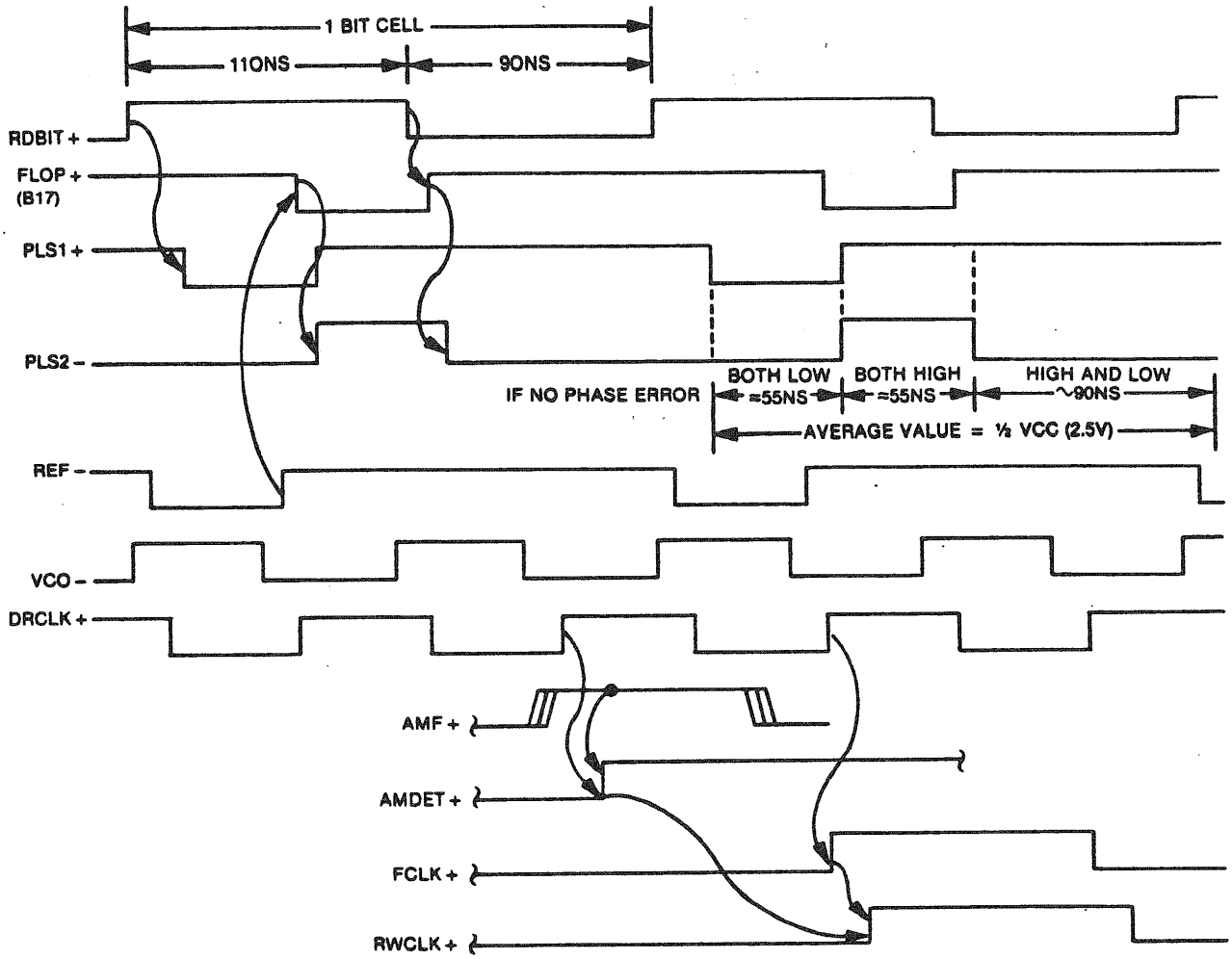


Figure 5-4. PLL Timing with No Phase Error

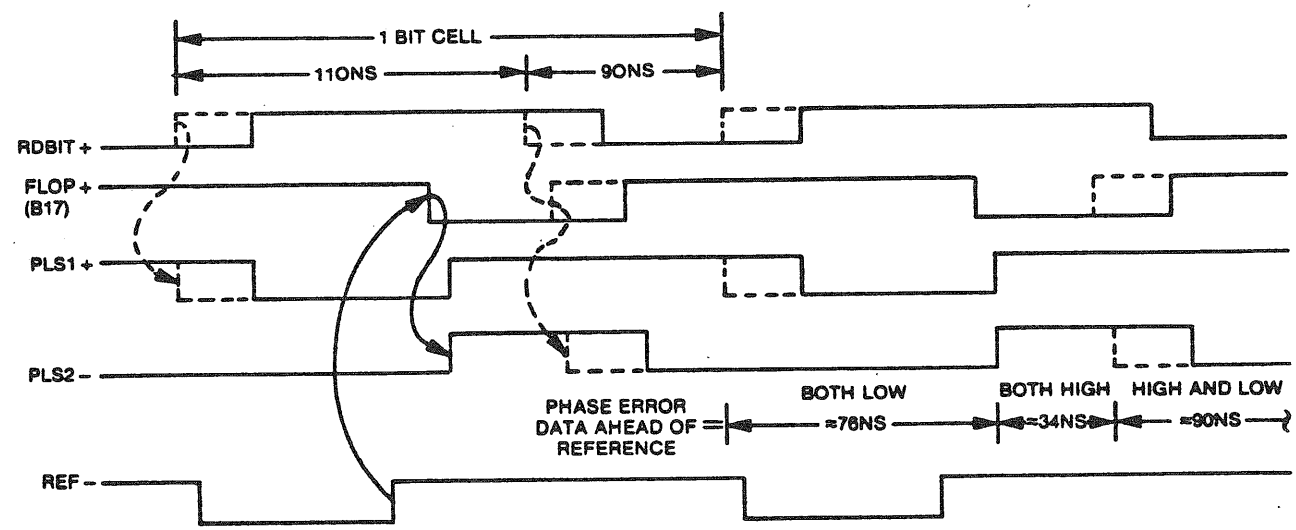


Figure 5-5. PLL Timing with Phase Error

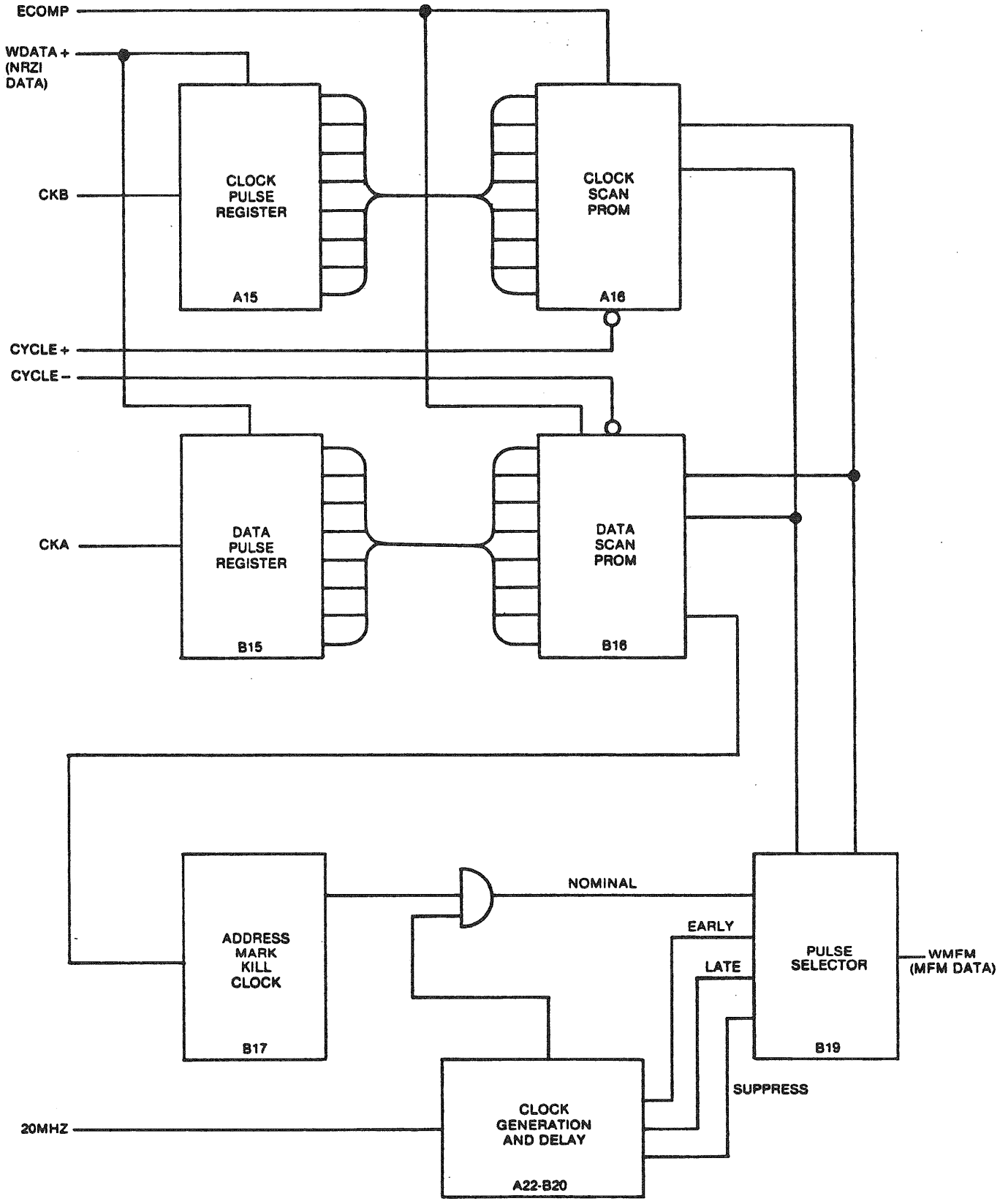


Figure 5-6. MFM Write Encode

The MFM encoding circuit basically accepts NRZI data, adds clocks, and rearranges the single output pulse stream to contain data and clock pulses. The circuit also compensates for the magnetic flux density phenomenon of peak shift; in high density packing, the pulses have a tendency to separate themselves at the point where a high frequency pulse stream meets a lower frequency pulse stream.

Write data (WDATA) is transmitted from the read/write shift register (F7, Sheet 12) to the clock and data pulse registers. The pulse stream is clocked into the registers, A15 and B15, by CKA and CKB, 5MHz clocks with a duty cycle of 25% high and 75% low. These and other regulating pulses are alternately enabled in the scan PROMs for one half cycle each by CYCLE, a 5MHz square wave. The effect is a "ping-pong" selection of the data and clock output from the PROMs. The clock PROM is selected for the first half cycle, and the data PROM is selected for the last half-cycle. The pulse selector, B19, is basically the OR gate of two independent pulse trains.

To accomplish MFM, the bit cell is divided into two domains: a clock domain and a data domain. As shown on Figure 5-7, clock pulses (CKB) transmitted to the clock pulse register are designated "0" and data pulses (CKA) are designated "1". The circuit evaluates two consecutive bit cells for arranging the pulses on the MFM train. (To simplify, ECOMP (enable compensation) and KILL (omit one pulse) are ignored at this time.) The conditions for arranging the pulses are as follows:

1. If the WMFM cell is to hold a "0" (clock), a pulse will occur at the beginning of a cell.
2. If the WMFM cell is to hold a "1" (data), a pulse will occur at the center of a cell.
3. Pulses at the beginning of a cell are suppressed if the previous cell contains a "1".
4. There is never more than one pulse, either clock or data, in any bit cell.

In the illustration, Figure 5-7, notice the input data (bit cell "0" or "1") and the arrangement of pulses as WMFM. The first clock pulse adheres to the first condition above. The next pulse is suppressed because of condition 4. This cycle is repeated, and the fifth pulse is suppressed because of conditions two and three. On the illustration, each of the pulses, adhere to the conditions above except for the KILL signal from flip flop B17. This signal strategically suppresses a pulse to create a unique pulse pattern, the address mark.

The conditions previously stated evaluate two consecutive bit cells. With the signal ECOMP,

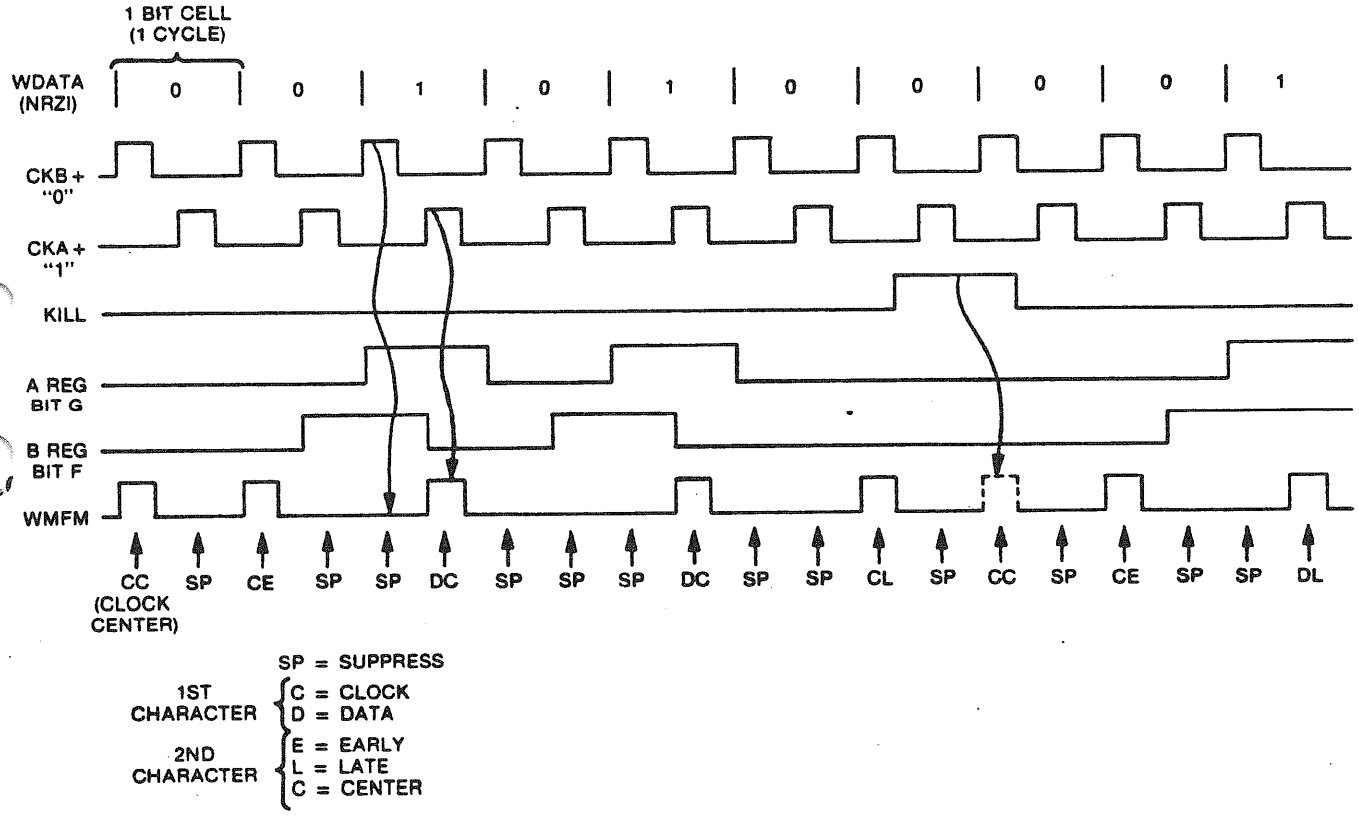


Figure 5-7. MFM Timing

enable precompensation of write, the circuit evaluates five bit cells. The purpose of ECOMP is to arrange the pulse train to compensate for peak shift. When pulses are closely packed, they tend to shift apart, and to compensate for this shift, the delay line, B20, transmits the pulse early (output of gate A19) or late (20ns delay at output of B20-6), or centered (10ns delay at the output of B20-4). The signals are transmitted to the dual, 4-input multiplexer B19. The suppress inputs to multiplexer are grounded (both pins 1). Figure 5-8 illustrates peak shift.

MFM Read Decoding

The read MFM circuit is shown on Sheet 16. A simplified diagram of the circuit is shown on Figure 5-9. The function of the circuit is to identify Address Mark Found (AMF+) and to transmit read data to the read/write shift register, F7 Sheet 12.

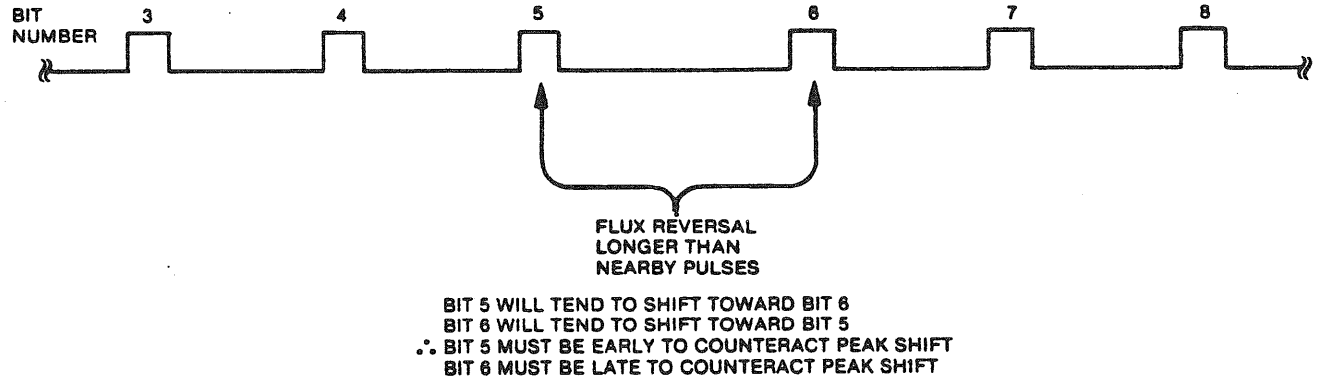


Figure 5-8. Peak Shift

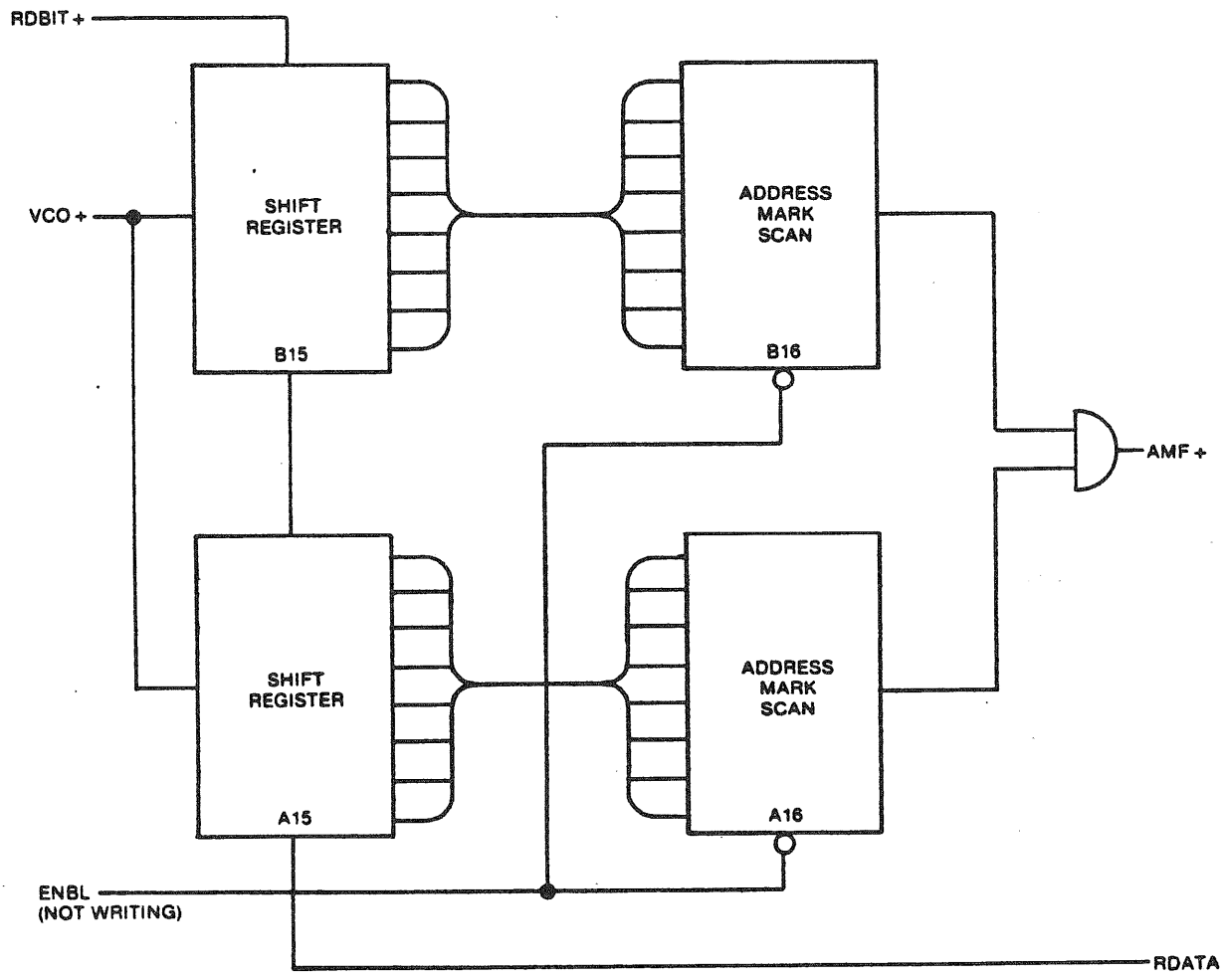


Figure 5-9. Read Decode

The data input, RDBIT from the phase-locked loop circuit, is transmitted to multiplexer B18, to shift register B15, back to the multiplexer, and to shift register A15. The input is clocked at twice the bit cell rate. The 16-bit shift register holds 8 bits of clock. Every other domain is clocked into the R/W shift register, F7; that is, one-half bit cell, the data domain. The timing is shown on Figure 5-10.

The address mark, A1, is normally 44A9; however, with the unique AMF pattern, the address is 4489 as shown on the upper part at the timing diagram. (Note the outline pulse on RMFM). The lower part of the diagram is offset to the left. The AMF+ signals on the diagram should be vertically aligned.

The start bit counter shown on the illustration holds on count 8 until the address mark is found and then proceeds to count 15 where BITCK is triggered (F2, Sheet 12).

Controller Internal Functions

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read-only memory (PROM). The instructions, called "firmware", cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the LSI-11.

Because the disc and computer transfer data at different rates, it is necessary to buffer data going to and from the disc. High-speed RAM allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disc protocol is under microprocessor control. This feature allows modification of controller operating characteristics by making only changes to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the "Y Bus". Y Bus instructions govern all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destinations decode IC's (Sheet 10).

The "D Bus" is the data input to the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/destination decode logic on Sheet 10.

The following list describes D Bus enabling signals:

Function	Term	Component Enabled	Sheet
Slave Address	XDS0	D16	2
Data Input (MSB)	XDS1	D14	11
Data Input (LSB)	XDS2	D15	11
Q-Bus Status	XDS3	D17	11
Data Buffer	XDS4	D7	12
Disc Status	XDS5	D12	15
Seek End/Unit Select	XDS6	D13	18

All data on the D Bus is under control of the firmware as decoded by PROM F8 on Sheet 10. The microprocessor selects the proper input data by enabling one of the above lines.

The Y Bus is the microprocessor output. Output of the microcode PROM A7 (Sheet 8) is decoded by F9 and F10 (Sheet 10) to select the destination of the data on the Y bus.

The following list describes Y Bus enabling signals:

Function	Term	Component Enabled	Sheet
Data Out Register (MSB)	LXR0	E13	6
Data Out Register (LSB)	LXR1	E15	5
DMA Address (MSB)	LXR2	E14	6
DMA Address (LSB)	LXR3	E16	5
Data Buffer Address (LSB)	LXR4	E3, 4	13
Data Buffer Address (MSB)	LXR5	E5	13
Data Buffer Data	XLR6	E7, C18	12
Control Pulse Strobe	LXR7	C20	11
Drive Control (UHS)	LXR9	E8	14
Drive Control (Bus 0-7)	LXRA	E10	14
Load Vector Address	LXRB	D1	7
System Control	LXRC	E17	3
Reset Data In	LXRD	E22	3
Q Bus Control	LXRE	E12, E22	3
Interrupt Vector PROM	LXRF	E9	10

With the single exception of bus reply detector D18 (Sheet 3), all data and address activity is controlled by the 15 signals shown above.

Each LXR (Load External Register) signal activates a register which, in conjunction with Y Bus data latches the appropriate data word.

Control Registers CR1 through CR5 are the outputs of the microcode PROMs (Sheet 8). These signals control the microprocessor functions and provide the data to the source/destination decode logic (Sheet 10).

Data Buffer

The data buffer and associated logic are shown on Sheets 12 and 13. Data Transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during either a read or write operation. Once loaded, the buffer

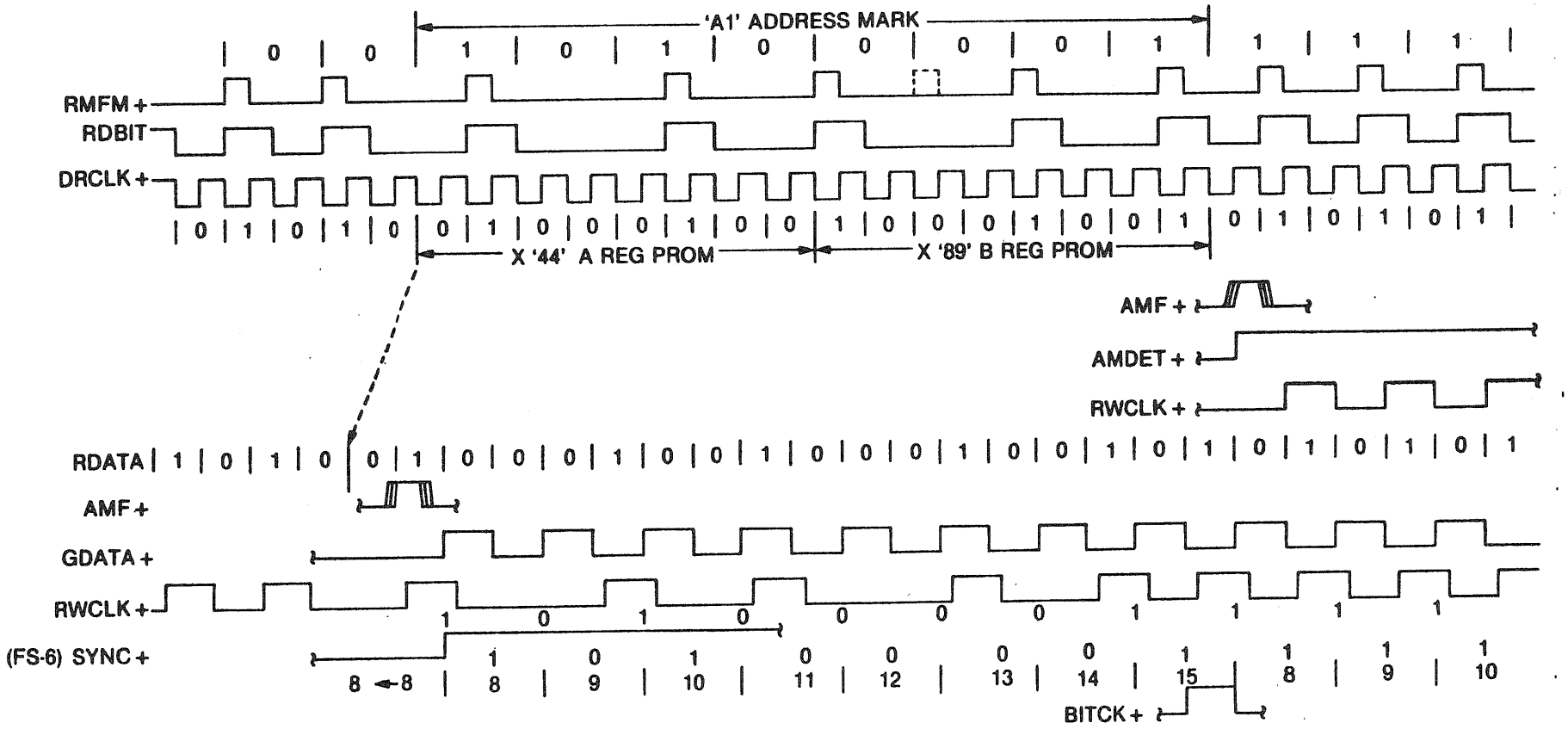


Figure 5-10. Address Mark Detector

contents are then transferred to disc or LSI-11 memory in a completely separate operation. Figure 5-11 illustrates read and write operations to and from the RAM data buffer.

During a write operation, parallel data (Y00-Y07) is transferred from LSI-11 memory via microprocessor to the storage latch E7 (Sheet 12). The data (DAT0-DAT7) is then transferred to the buffer F3 and F4 (Sheet 13). Parallel data (DAT0-DAT7) from the buffer is then transferred to shift register F7, converted to serial data (W DATA), and transferred to the data write logic.

During a read operation, serial read data (R DATA) from the data cable receivers is ANDED with Enable Bit Count (E BIT C) resulting in the signal G DATA. This signal enters the shift register F7 and is transferred as parallel data to the storage latch F6, for transfer to the data buffer while the next byte is being shifted through shift register F7. The read data from the buffer (DAT0-DAT7) is transferred to drive D7 (Sheet 12) to the microprocessor for transfer to LSI-11 memory.

The counter located at E3, E4 and E5 (Sheet 13) is used to address the location in the buffer to which data can be written into or read from. The counter has the capability of being preset to a specific starting address via the Y Bus of the microprocessor.

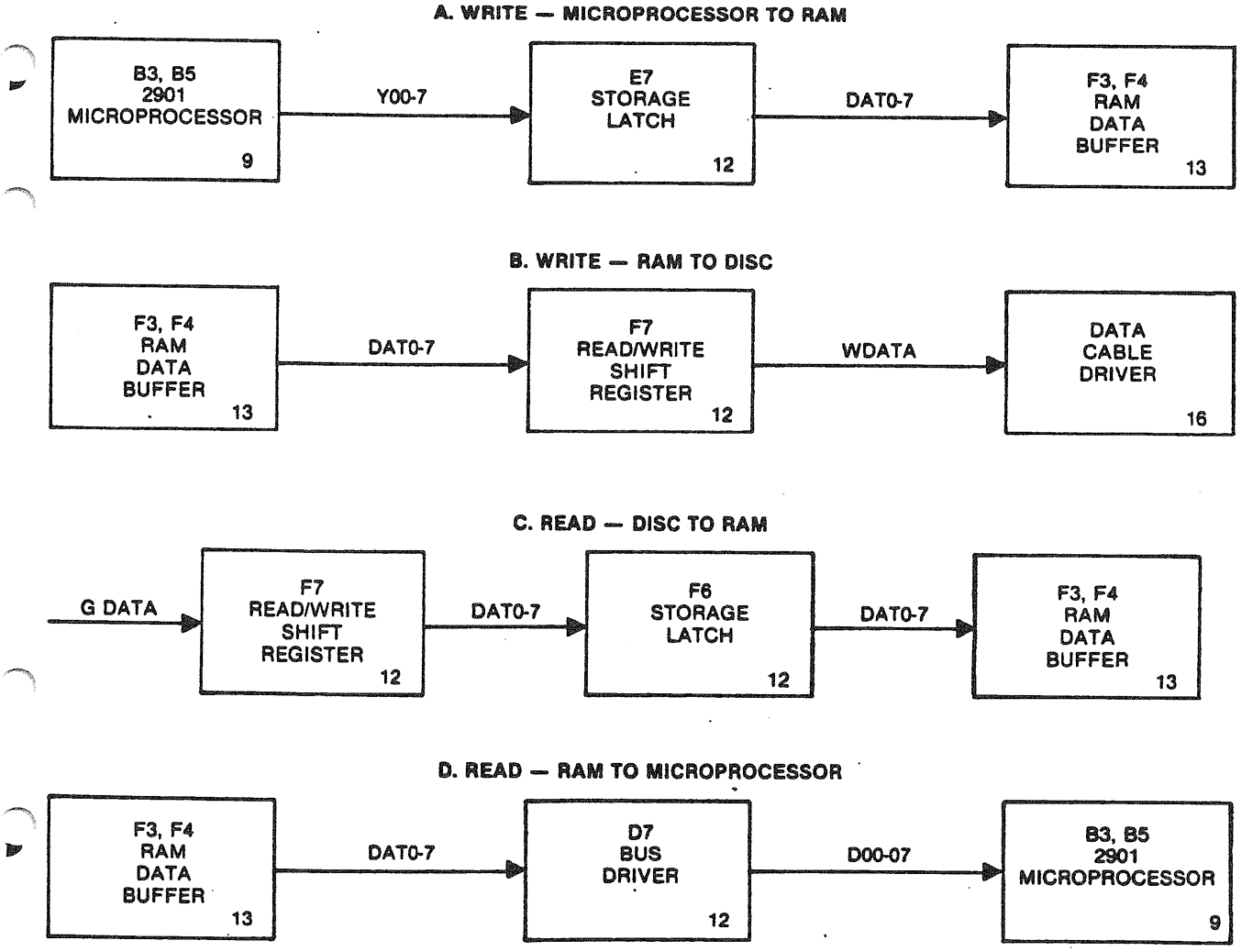
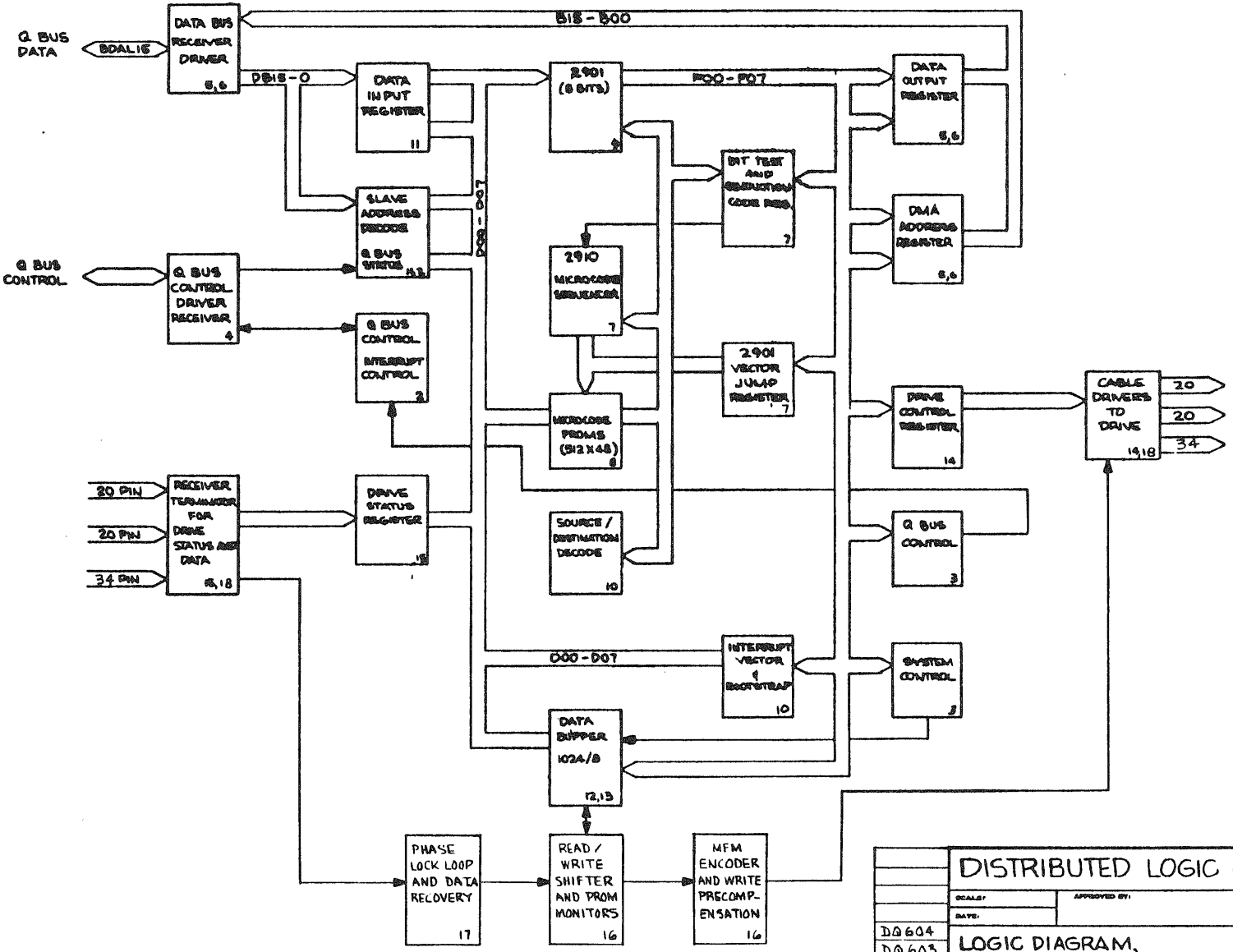
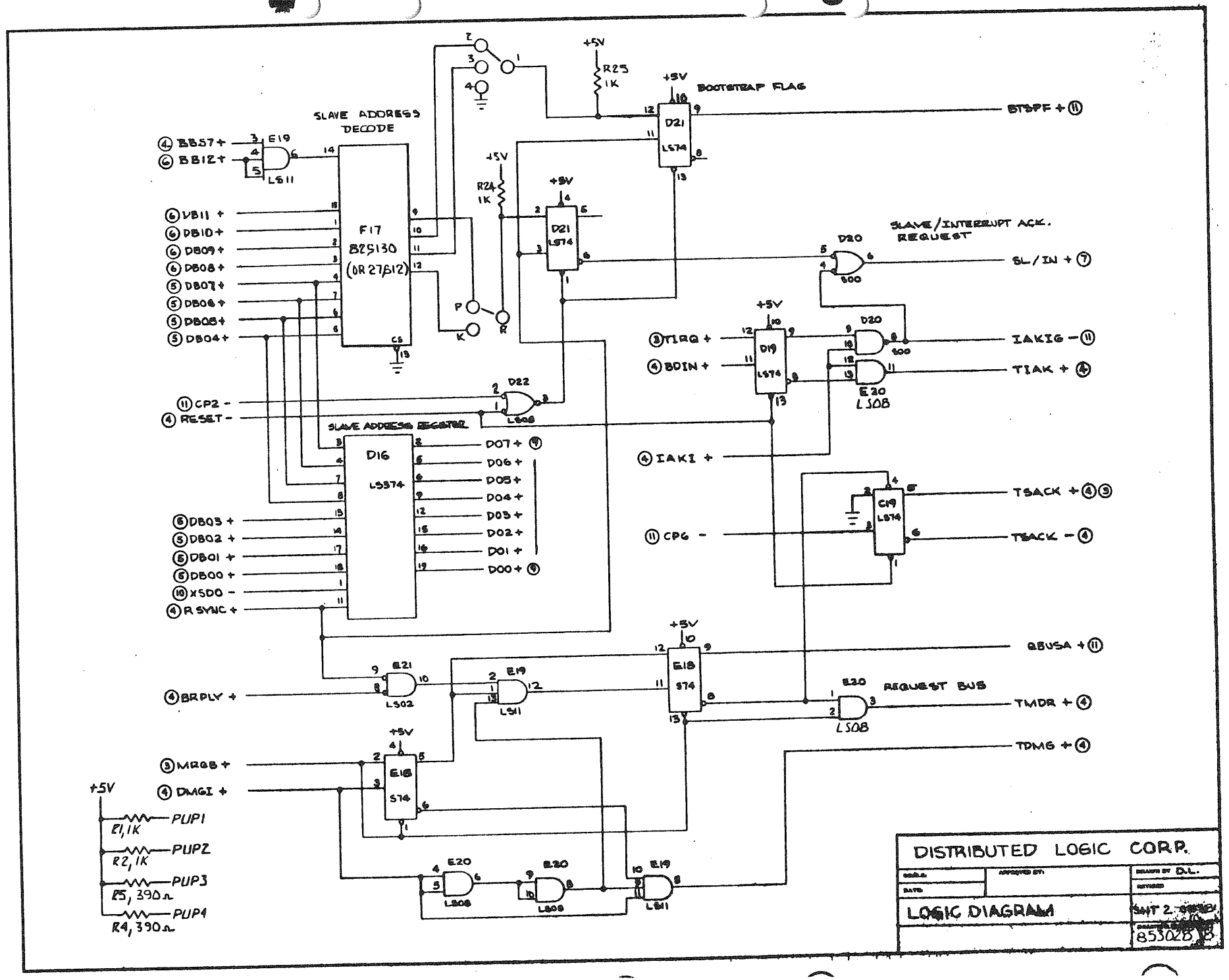
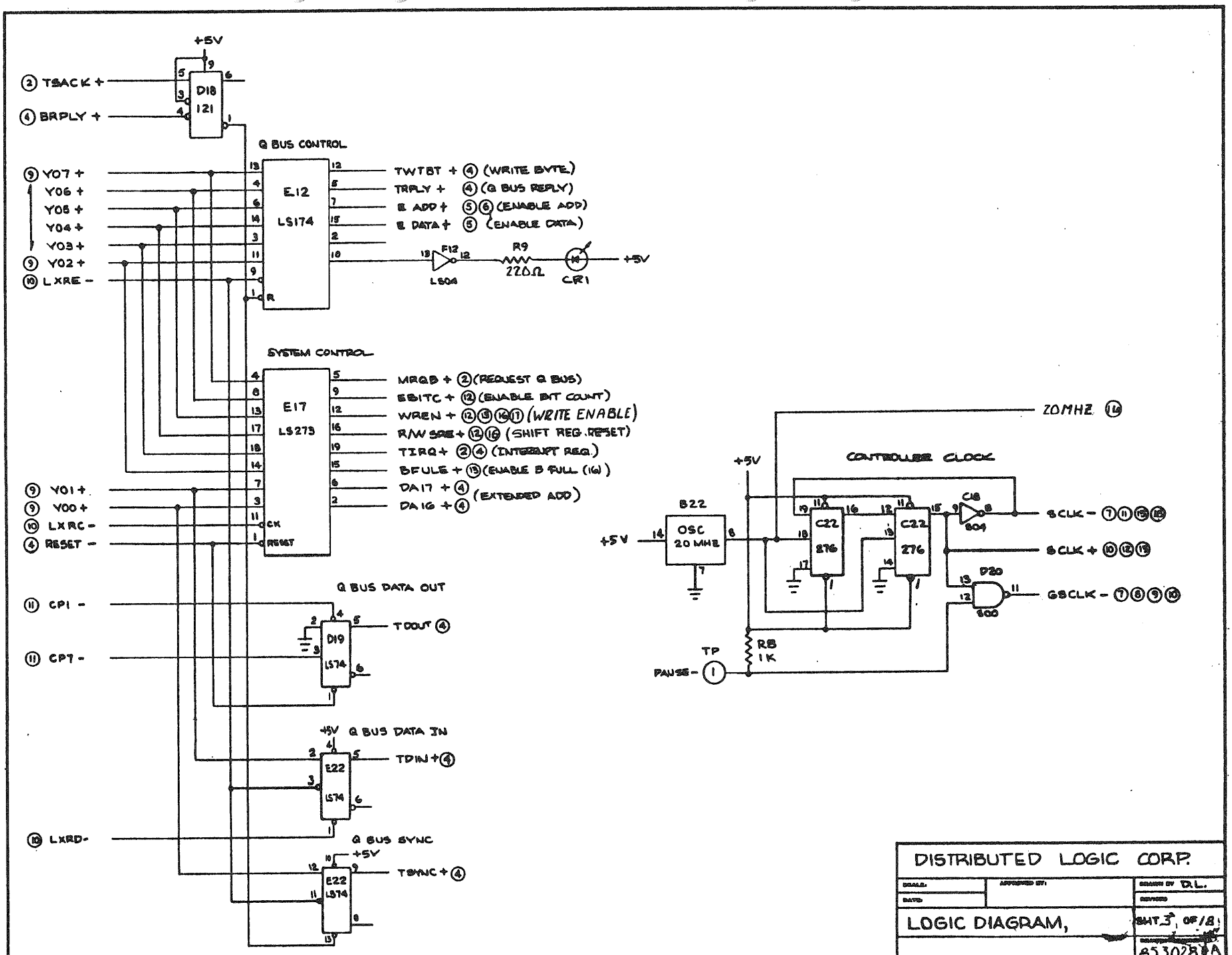


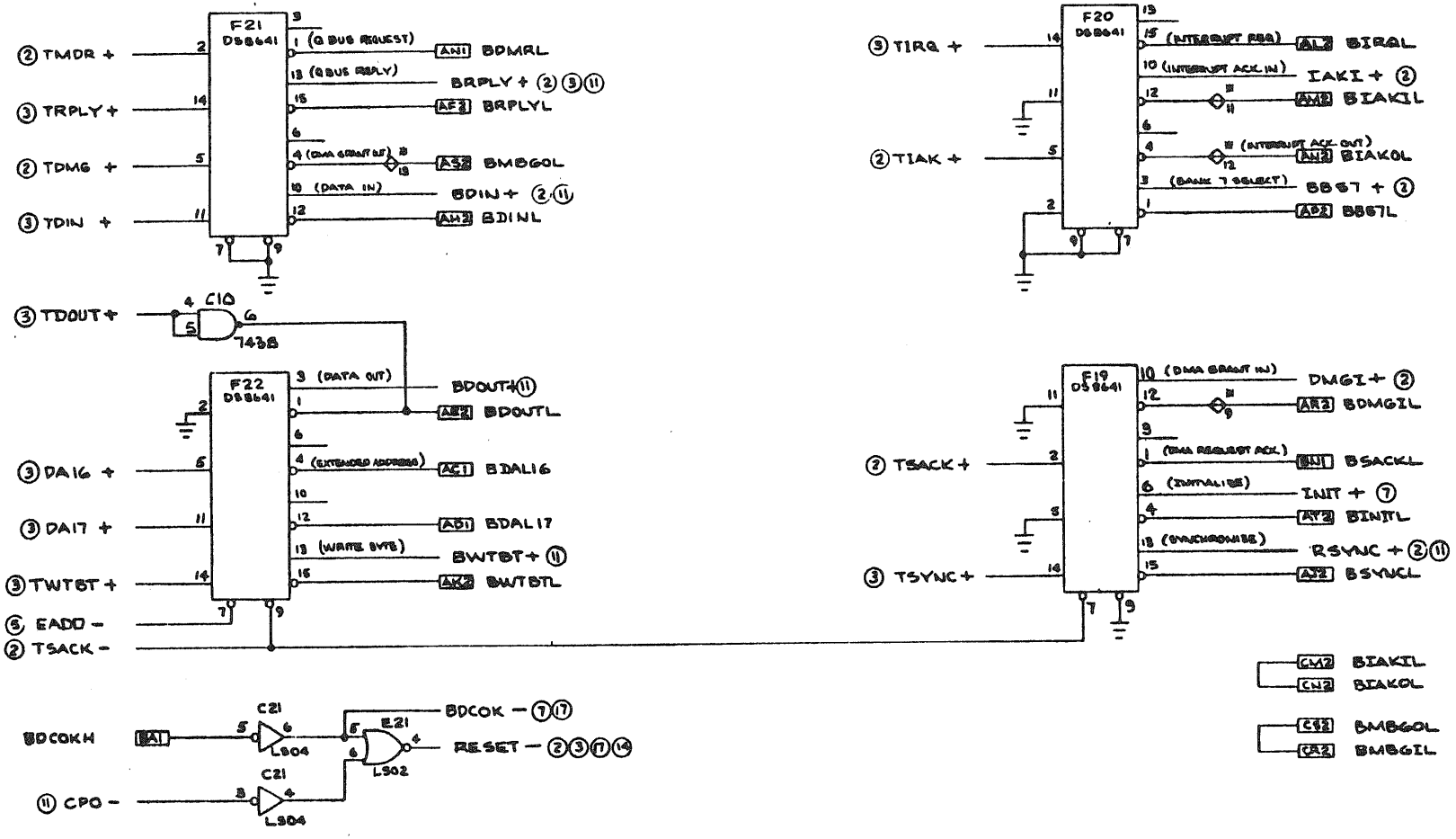
Figure 5-11. Data Paths


Q BUS DATA
BDAL16
DATA BUS RECEIVER DRIVER 5,6
B15-B00
DB15-0
DATA INPUT REGISTER 11
2901 (8 BITS) 8
F00-F07
DATA OUTPUT REGISTER 5,6
SLAVE ADDRESS DECODE
Q BUS STATUS 11
D00-D07
BIT TEST AND OPERATION CODE REG. 7
DMA ADDRESS REGISTER 5,6
Q BUS CONTROL
Q BUS CONTROL DRIVER RECEIVER 4
2910 MICROCODE SEQUENCER 7
Q BUS CONTROL INTERRUPT CONTROL 3
2901 VECTOR JUMP REGISTER 7
MICROCODE PROMS (512X48) 8
DRIVE CONTROL REGISTER 14
CABLE DRIVERS TO DRIVE 14,18
20
20
34
20 PIN
20 PIN
34 PIN
RECEIVER TERMINATOR FOR DRIVE STATUS AND DATA 15,18
DRIVE STATUS REGISTER 15
SOURCE / DESTINATION DECODE 10
Q BUS CONTROL 3
INTERRUPT VECTOR & BOOTSTRAP 10
D00-D07
SYSTEM CONTROL 3
DATA BUFFER 1024/8 12,13
PHASE LOCK LOOP AND DATA RECOVERY 17
READ / WRITE SHIFTER AND PROM MONITORS 16
MFM ENCODER AND WRITE PRECOMP-ENSATION 16
DISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY D.L.
DATE:
REVISED
DQ604
DQ603
DQ601
USED ON
LOGIC DIAGRAM,
SHT. 1 OF 18
DRAWING NUMBER
853028
A



SLAVE ADDRESS DECODE
F17
82S130
(OR 27S12)
BOOTSTRAP FLAG
D21
LS74
SLAVE/INTERRUPT ACK. REQUEST
D20
S00
SLAVE ADDRESS REGISTER
D16
LS374
D19
LS74
D22
LS08
C19
LS74
E18
S74
E19
LS11
E21
LS02
E20
LS08
REQUEST BUS
BTSPF + (11)
SL/IN + (7)
IAKIG − (11)
TIAK + (4)
TSACK + (4)(3)
TSACK − (4)
QBUSA + (11)
TMDR + (4)
TDMG + (4)
(4) BB57 +
(6) BB12 +
(6) DB11 +
(6) DB10 +
(6) DB09 +
(6) DB08 +
(5) DB07 +
(5) DB06 +
(5) DB05 +
(5) DB04 +
(11) CP2 −
(4) RESET −
(5) DB03 +
(5) DB02 +
(5) DB01 +
(5) DB00 +
(10) XSDO −
(4) R SYNC +
(4) BRPLY +
(3) MRQB +
(4) DMGI +
(3) TIRQ +
(4) BDIN +
(4) IAKI +
(11) CP6 −
+5V
R25 1K
R24 1K
R1, 1K
R2, 1K
R5, 390Ω
R4, 390Ω
PUP1
PUP2
PUP3
PUP4
DISTRIBUTED LOGIC CORP.
LOGIC DIAGRAM
D.L.
SHT 2
853028


+5V
② TSACK +
④ BRPLY +
D18
121
Q BUS CONTROL
⑨ YO7 +
YO6 +
YO5 +
YO4 +
YO3 +
⑨ YO2 +
⑩ LXRE -
E12
LS174
TWTBT + ④ (WRITE BYTE)
TRPLY + ④ (Q BUS REPLY)
E ADD + ⑤⑥ (ENABLE ADD)
E DATA + ⑤ (ENABLE DATA)
F12
LS04
R9
220Ω
CR1
+5V
SYSTEM CONTROL
E17
LS273
MRQB + ② (REQUEST Q BUS)
EBITC + ⑫ (ENABLE BIT COUNT)
WREN + ⑫⑮⑭① (WRITE ENABLE)
R/W SRE + ⑫⑯ (SHIFT REG. RESET)
TIRQ + ②④ (INTERRUPT REQ.)
BFULE + ⑮ (ENABLE B FULL (16))
DA17 + ④
DA16 + ④ (EXTENDED ADD)
⑨ YO1 +
⑨ YO0 +
⑩ LXRC -
④ RESET -
CK
RESET
Q BUS DATA OUT
⑪ CP1 -
⑪ CP7 -
D19
LS374
TDOUT ④
+5V Q BUS DATA IN
E22
LS374
TDIN + ④
⑩ LXRD -
Q BUS SYNC
+5V
E22
LS374
TSYNC + ④
20MHZ ⑭
CONTROLLER CLOCK
+5V
B22
OSC
20 MHZ
+5V
C22
276
C22
276
C18
804
SCLK - ⑦⑪⑮⑯
SCLK + ⑩⑫⑬
D20
800
GSCLK - ⑦⑧⑨⑩
TP
PAUSE - ①
R8
1K
DISTRIBUTED LOGIC CORP.
DRAWN BY D.L.
LOGIC DIAGRAM,
SHT 3 OF 18
853028 A



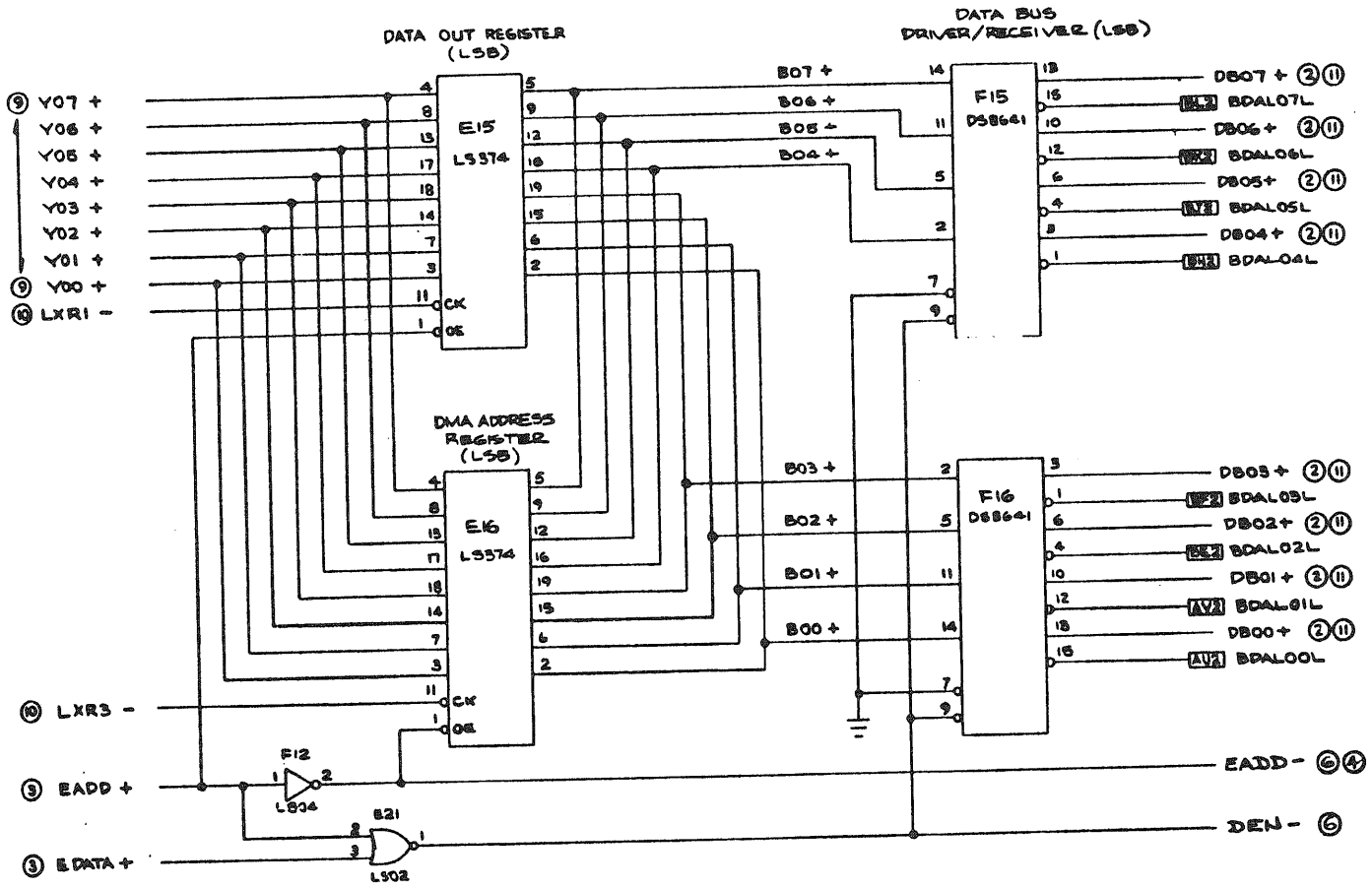
NOTE: * 12 SYMBOL INDICATES PULL-UP(180Ω)/PULL-DOWN(390Ω) RESISTORS. NUMBER SHOWN IS PIN NUMBER USED IN PACK, LOCATION F18.

DISTRIBUTED LOGIC CORP.

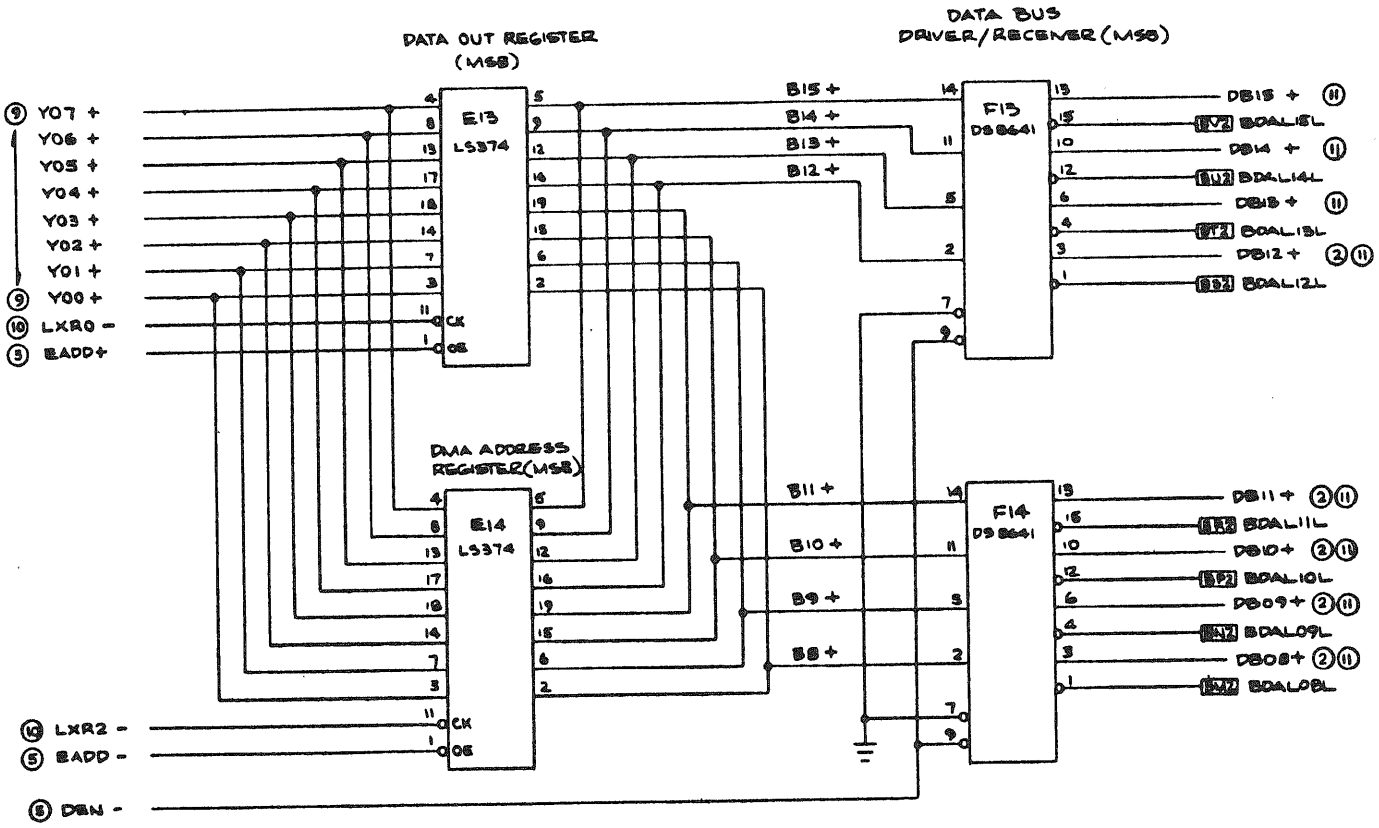
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED

LOGIC DIAGRAM, SHT 4 OF 18

DRAWING NO. 855028 B

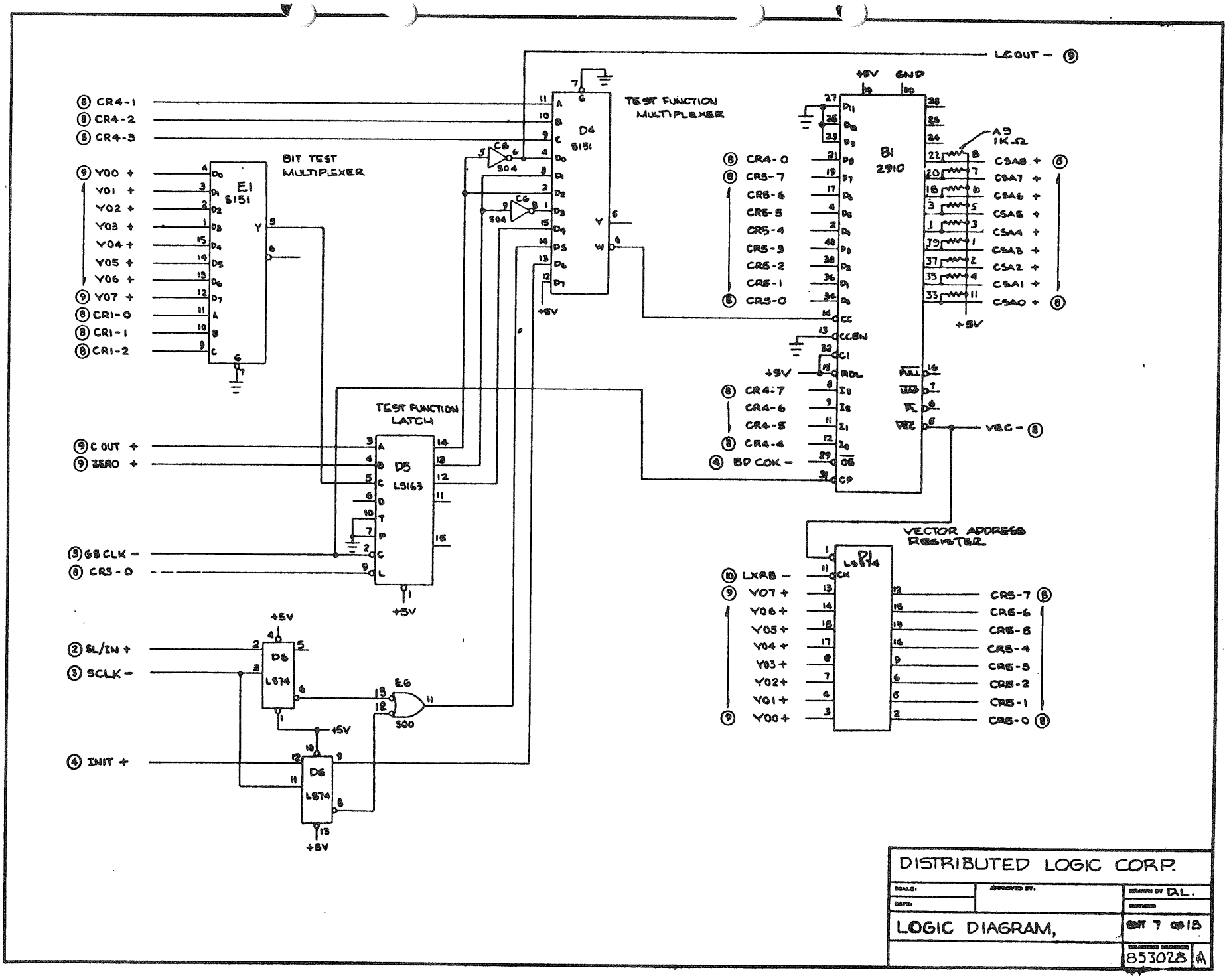


DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 5 OF 18
		DRAWING NUMBER 853028 B

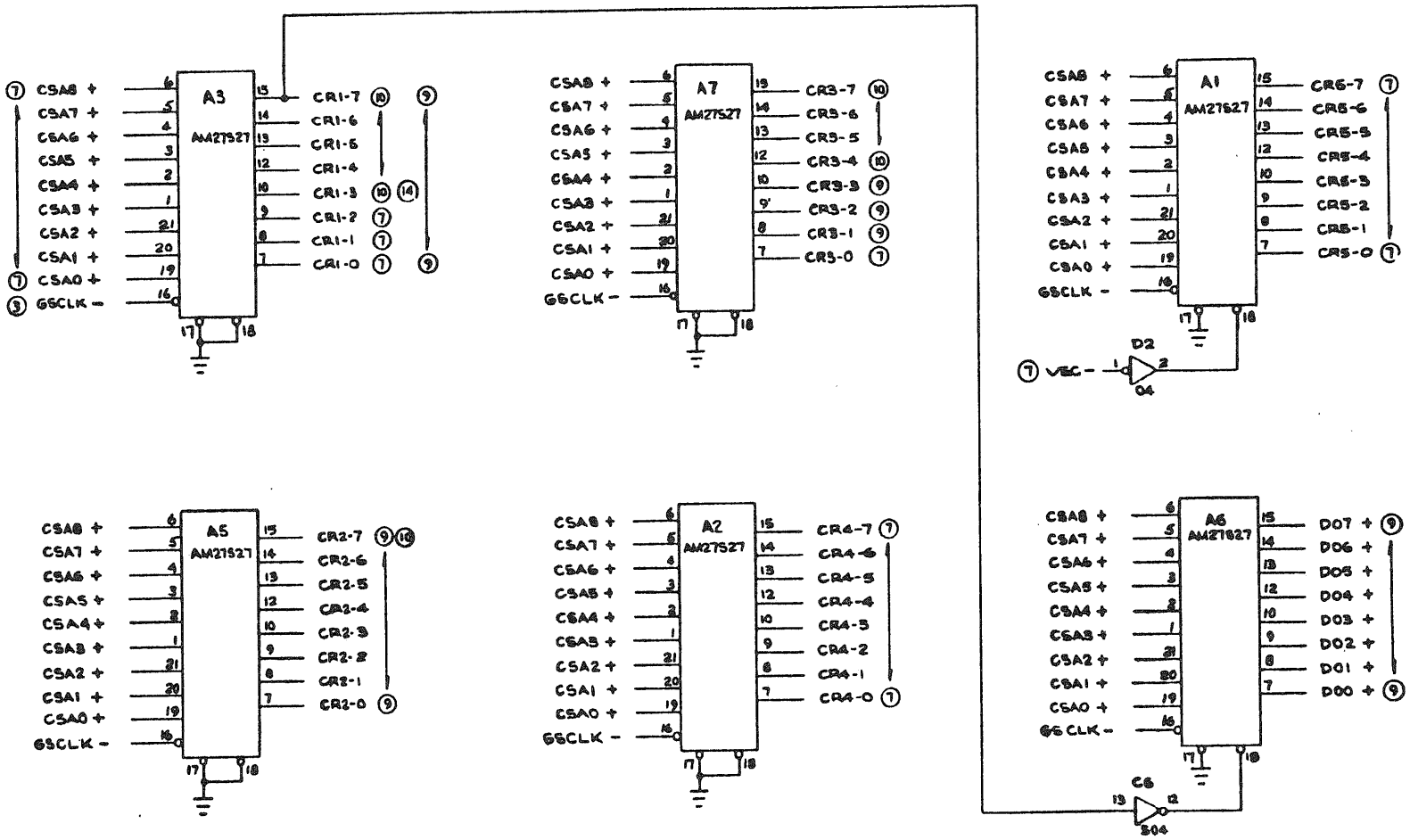


DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM		SHT 6 OF 18
		853028 A

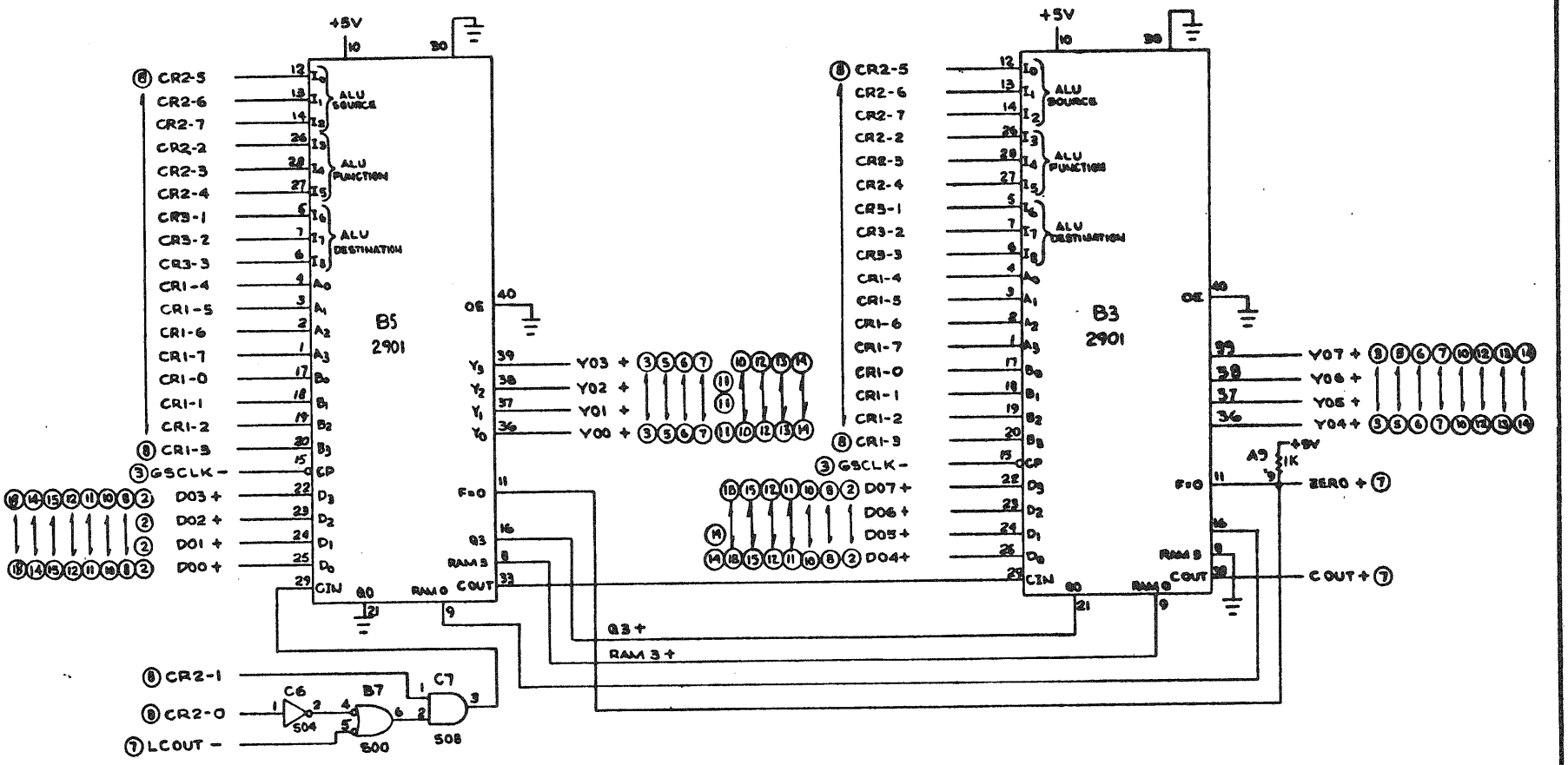


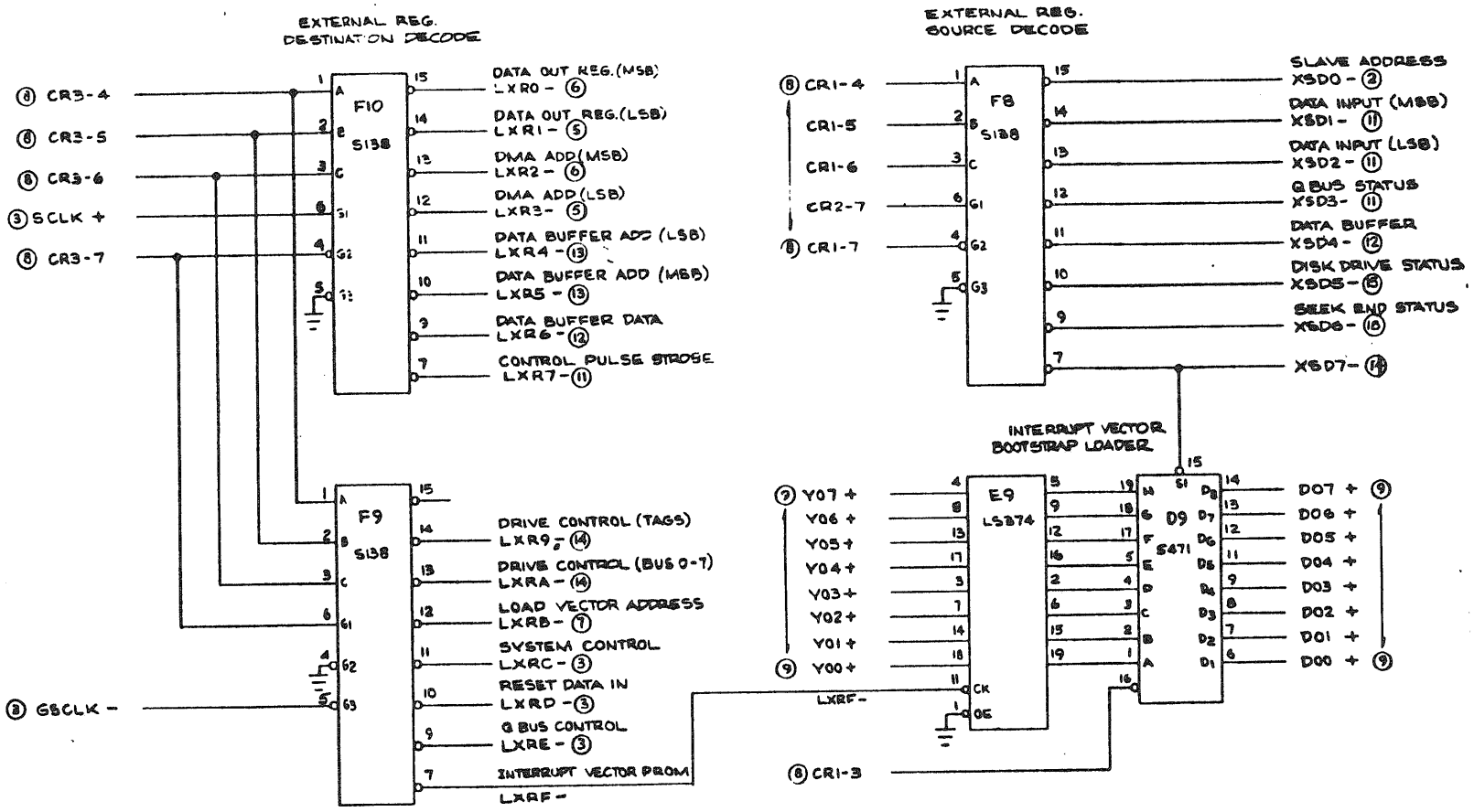
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 7 of 18
		DRAWING NUMBER 853028 A



DISTRIBUTED LOGIC CORP.

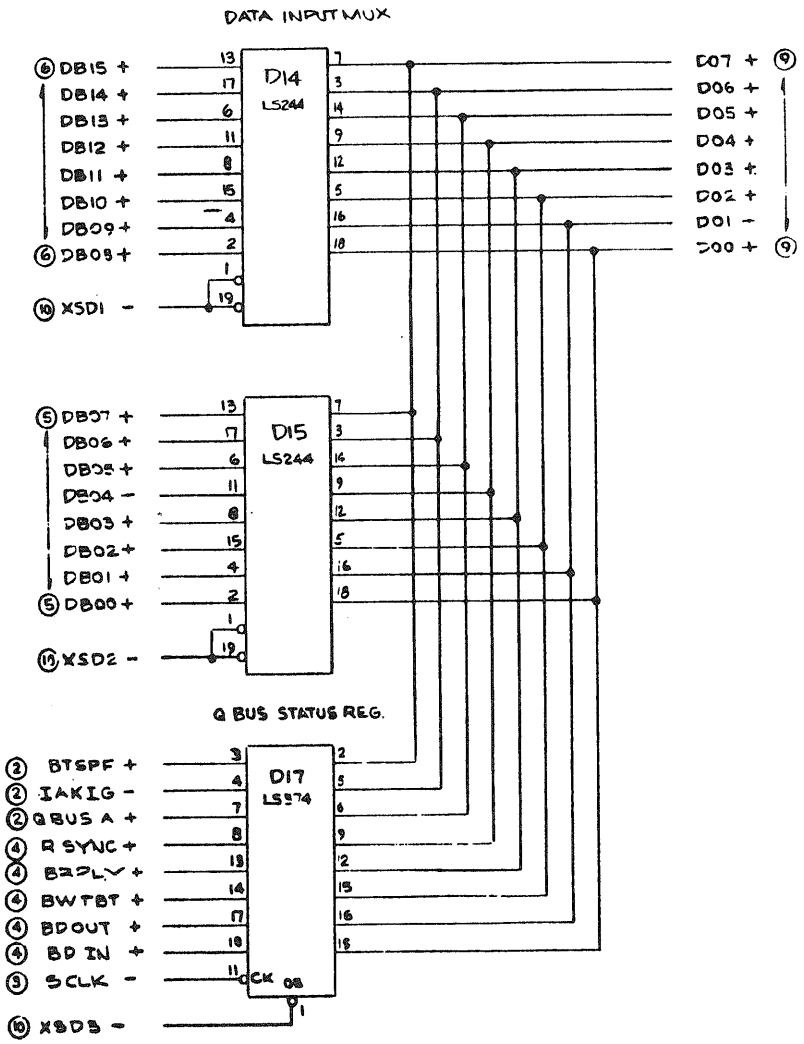
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 8 OF 18
		DRAWING NUMBER 853028 A

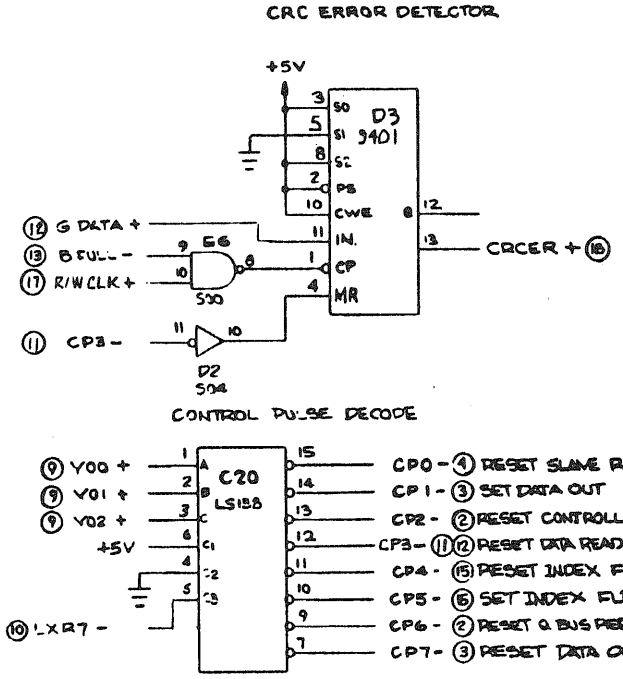

+5V
B5
2901
B3
2901
ALU SOURCE
ALU FUNCTION
ALU DESTINATION
CR2-5
CR2-6
CR2-7
CR2-2
CR2-3
CR2-4
CR3-1
CR3-2
CR3-3
CR1-4
CR1-5
CR1-6
CR1-7
CR1-0
CR1-1
CR1-2
CR1-3
GSCLK-
D03+
D02+
D01+
D00+
D07+
D06+
D05+
D04+
Y03+
Y02+
Y01+
Y00+
Y07+
Y06+
Y05+
Y04+
Q3+
RAM 3+
ZERO+7
COUT+7
CR2-1
CR2-0
LCOUT-
C6
B7
C7
S04
S00
S08
DISTRIBUTED LOGIC CORP.
LOGIC DIAGRAM,
SHT 9 OF 16
853028
B



DISTRIBUTED LOGIC CORP.

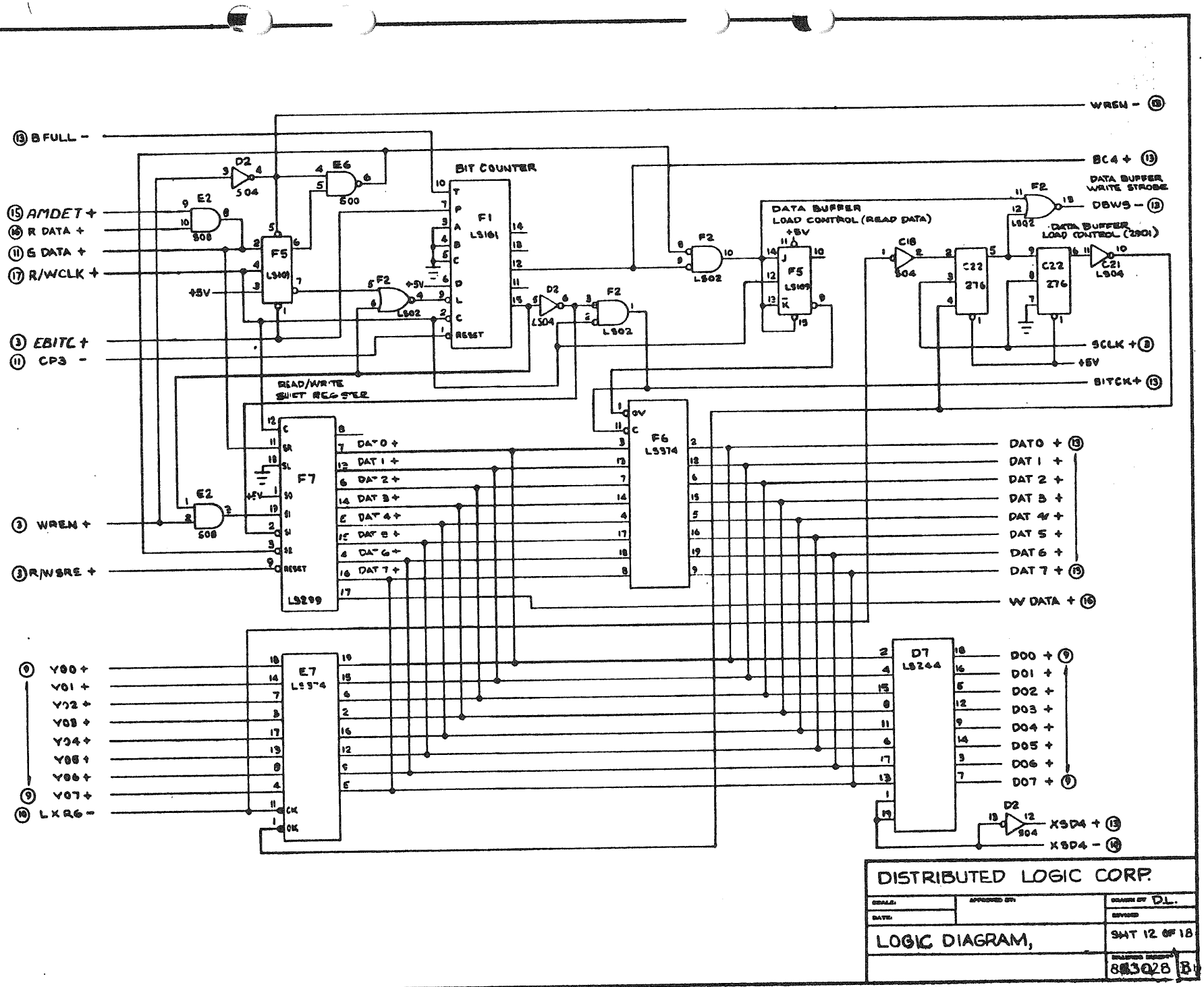
SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 10 OF 18
		DRAWING NUMBER 853028 A





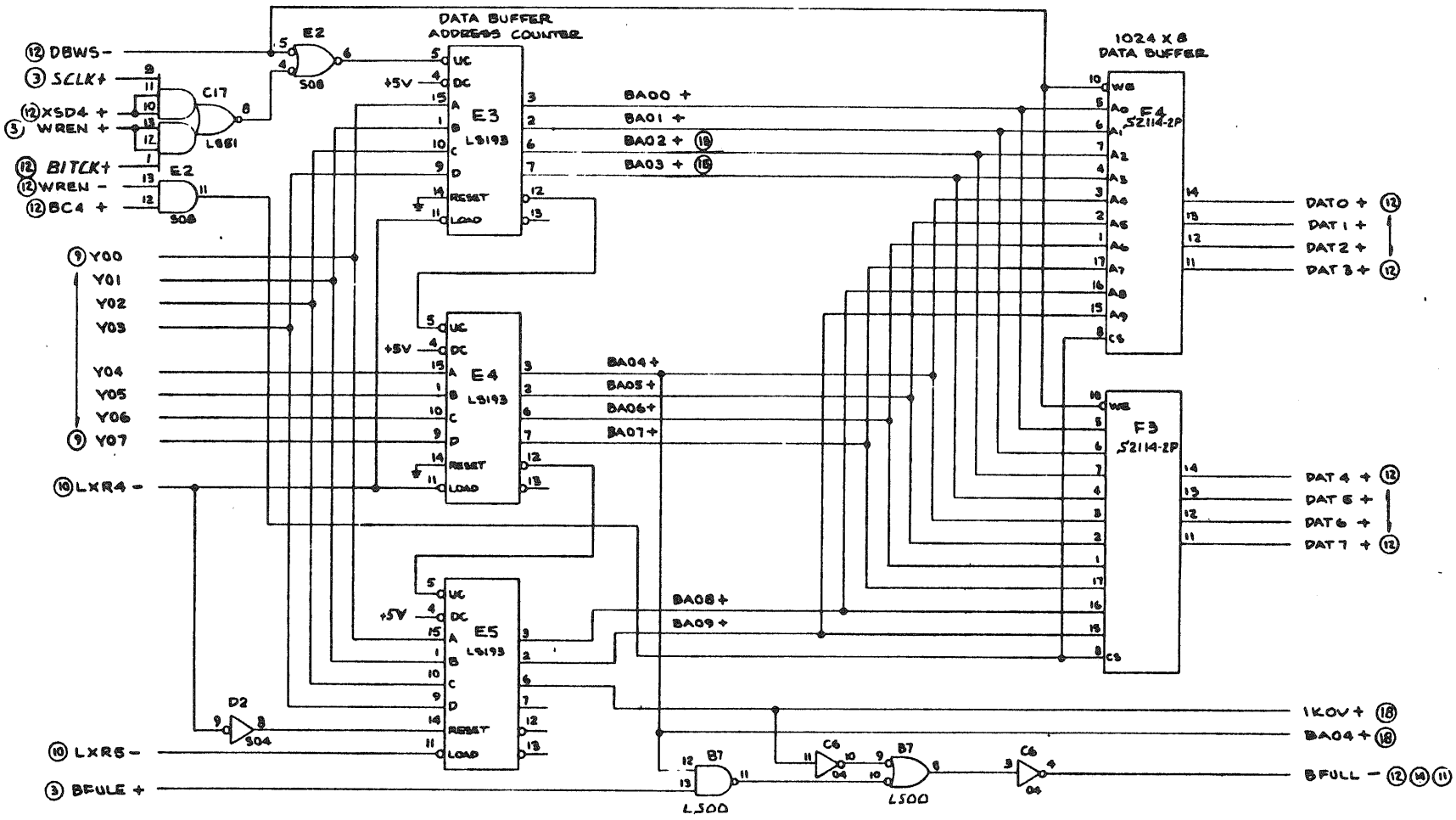
DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 11 OF 18
		DRAWING NUMBER 853028 B

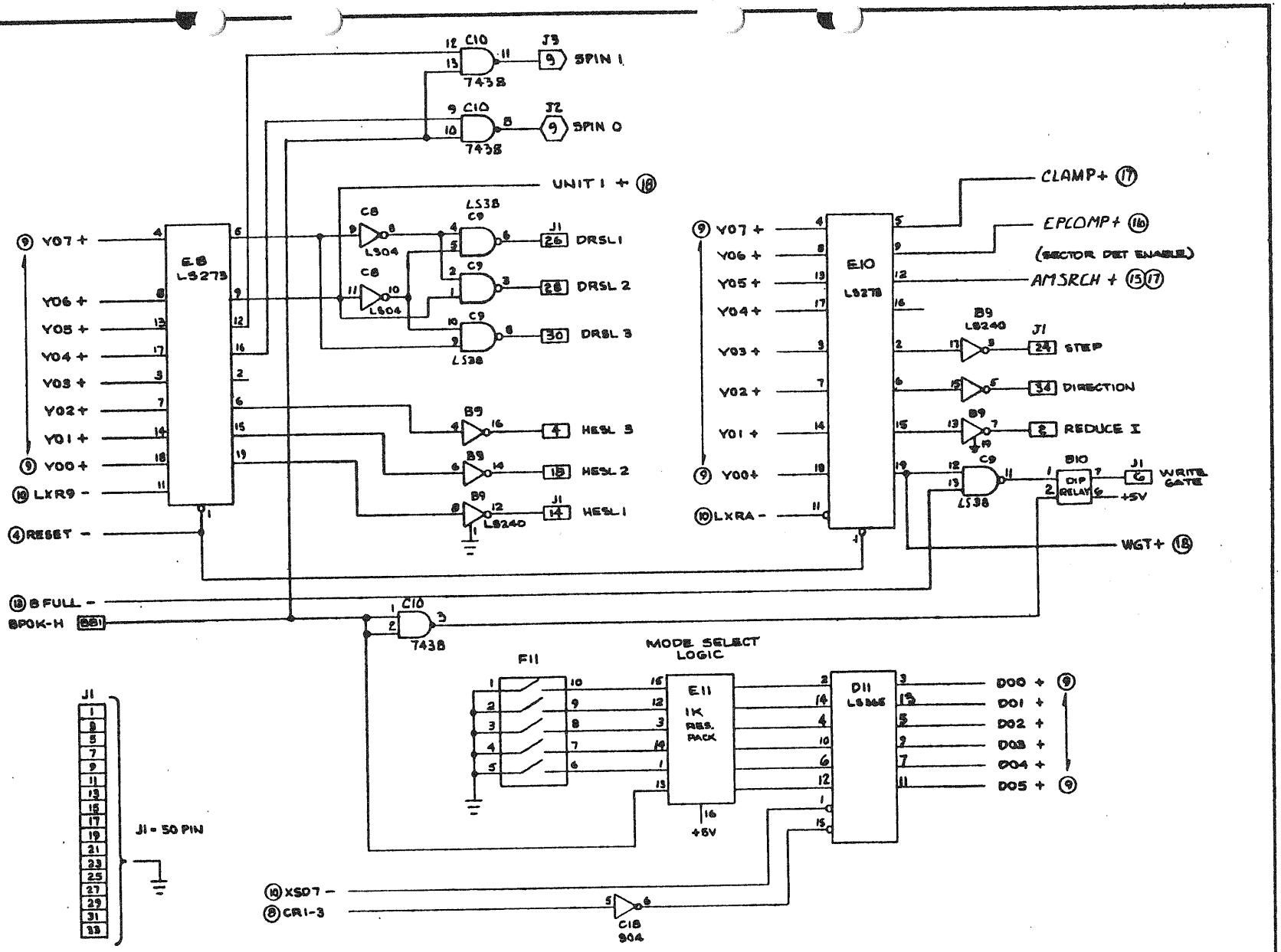


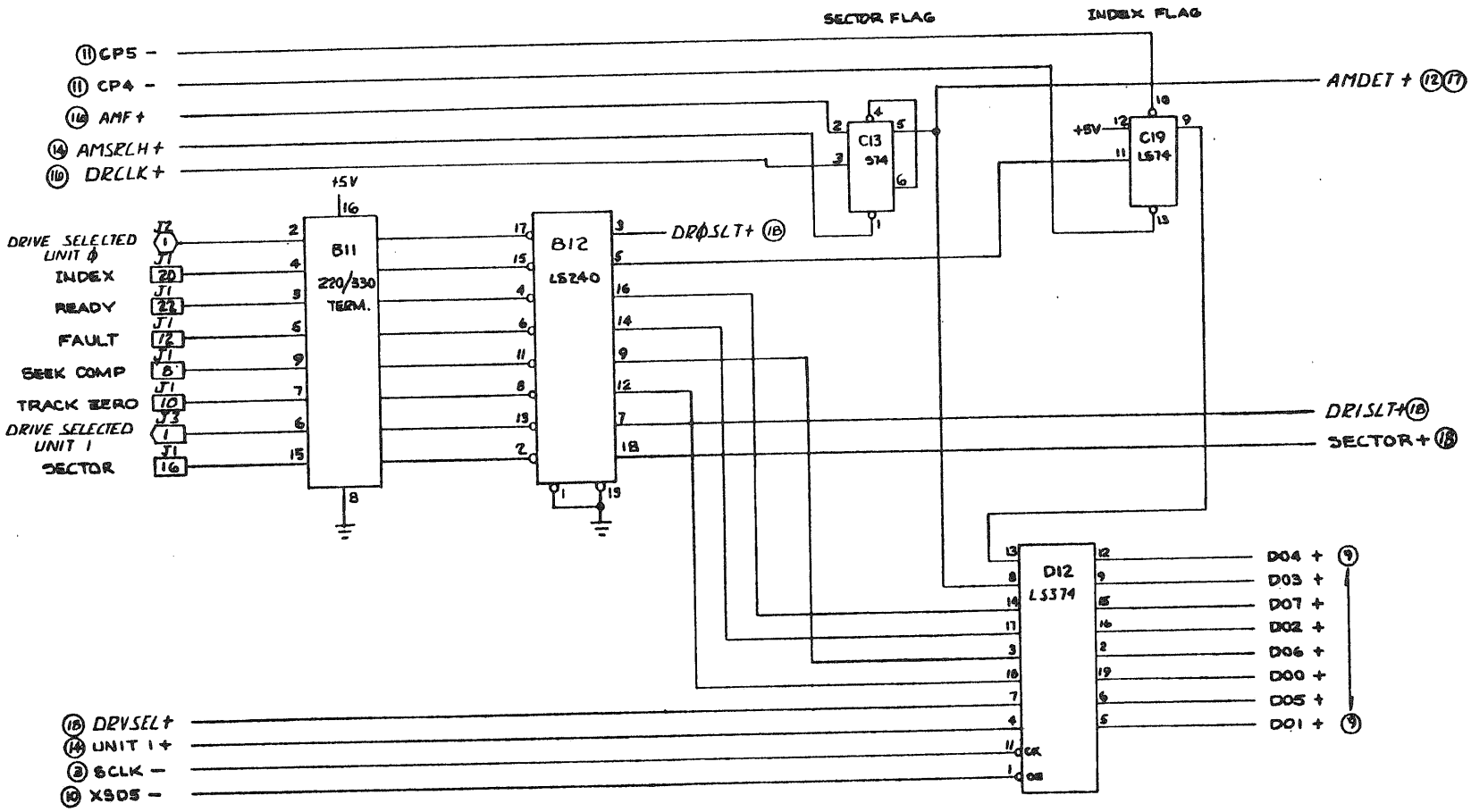
DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 12 OF 18
		DRAWING NUMBER 8830128 B



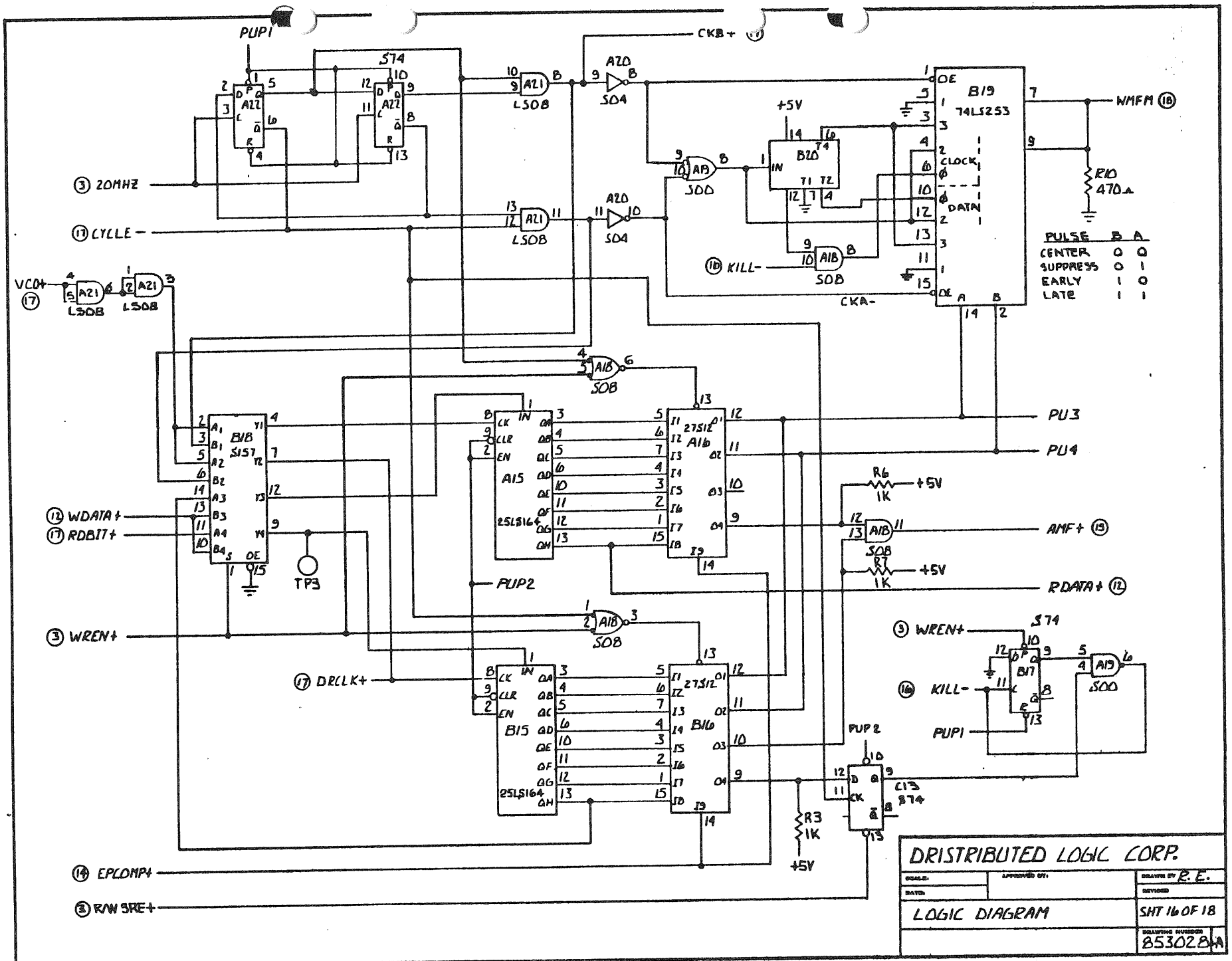
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY RL.
DATE:		DESIGNED
LOGIC DIAGRAM,		SHT 13 OF 18
		DRAWING NUMBER 853028 B

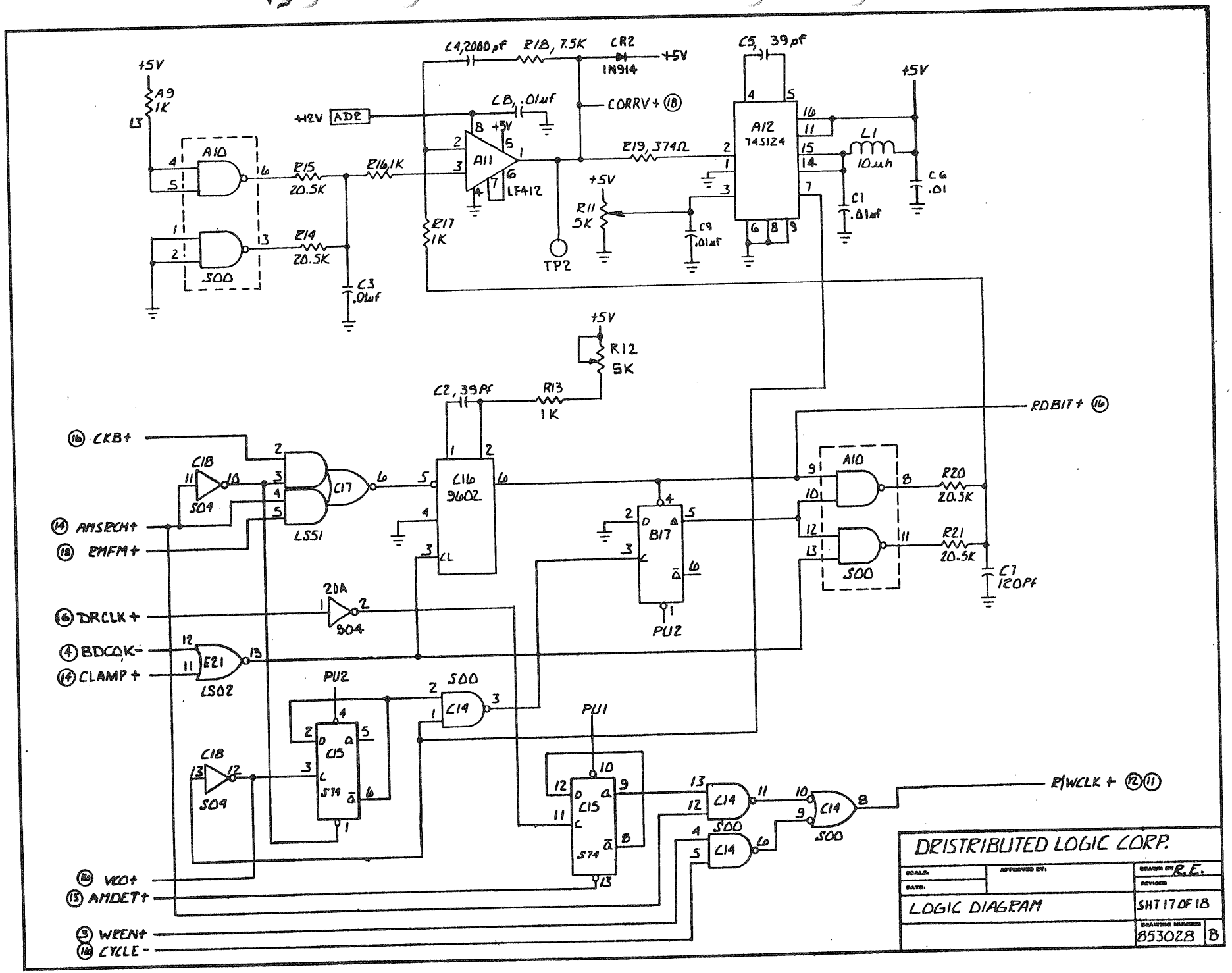

C10
7438
J3
SPIN 1
J2
SPIN 0
UNIT 1 + (18)
CLAMP+ (17)
EPCOMP+ (16)
(SECTOR DET ENABLE)
AMSRCH + (15)(17)
E8
LS273
E10
LS273
C8
LS04
LS38
C9
J1
26 DRSL1
28 DRSL 2
30 DRSL 3
B9
LS240
4 HESL 3
18 HESL 2
14 HESL 1
B9
LS240
J1
24 STEP
34 DIRECTION
8 REDUCE I
C9
LS38
B10
DIP RELAY
J1
6 WRITE GATE
+5V
WGT+ (18)
(9) Y07 +
Y06 +
Y05 +
Y04 +
Y03 +
Y02 +
Y01 +
(9) Y00 +
(10) LXR9 -
(4) RESET -
(10) LXRA -
(18) B FULL -
BPOK-H 881
C10
7438
MODE SELECT LOGIC
F11
E11
1K RES. PACK
+5V
D11
LS365
D00 + (9)
D01 +
D02 +
D03 +
D04 +
D05 + (9)
J1
J1 = 50 PIN
(10) XS07 -
(8) CR1-3
C18
904
DISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY D.L.
DATE:
REVISED
LOGIC DIAGRAM
SHT 14 OF 18
DRAWING NUMBER
853028 B

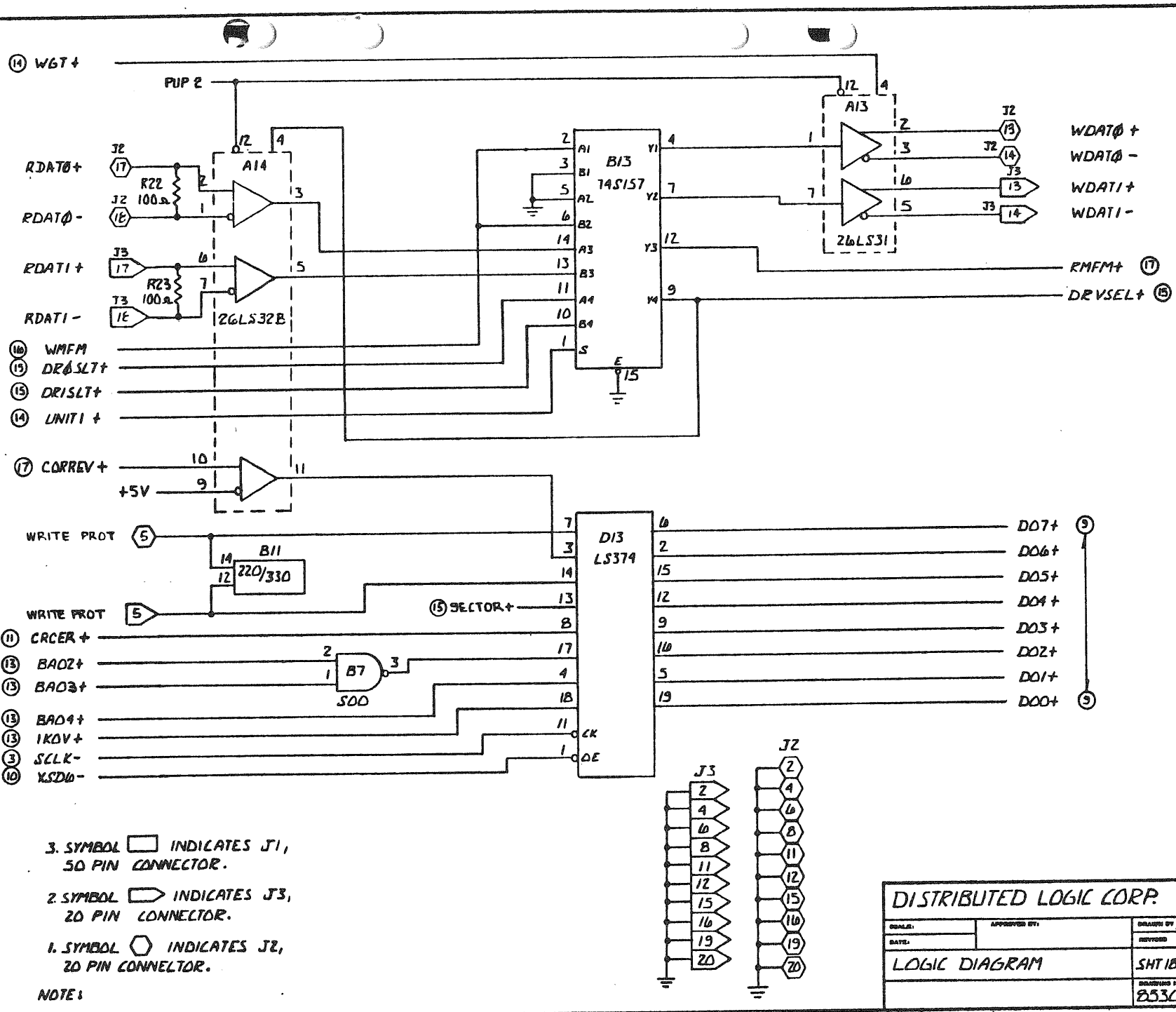


DISTRIBUTED LOGIC CORP.

SCALE:	APPROVED BY:	DRAWN BY D.L.
DATE:		REVISED
LOGIC DIAGRAM		SHT 15 OF 18
		DRAWING NUMBER 853028 B


PUP1
S74
A22
A21
LS08
A20
S04
CKB+
B19
74LS253
WMFM
R10
470Ω
CLOCK
DATA
+5V
B20
A19
S00
KILL-
A18
S08
CKA-
20MHZ
CYCLE-
VCO+
PULSE B A
CENTER 0 0
SUPPRESS 0 1
EARLY 1 0
LATE 1 1
B18
S157
A15
25LS164
27S12
A16
PU3
PU4
R6
1K
AMF+
R7
RDATA+
WDATA+
RDBIT+
TP3
PUP2
WREN+
DRCLK+
B15
B16
B17
C13
R3
EPCOMP+
RAW SRE+
DRISTRIBUTED LOGIC CORP.
LOGIC DIAGRAM
R. E.
SHT 16 OF 18
853028


+5V
A9 1K
L3
A10
S00
R15 20.5K
R16 1K
R14 20.5K
C3 .01uf
+12V ADR
C4, 2000 pF
R18, 7.5K
CR2 IN914
+5V
CORRV+ (18)
C8, .01uf
A11 LF412
R17 1K
TP2
R19, 374Ω
C5, 39 pF
A12 74S124
L1 10 μh
C6 .01
C1 .01uf
R11 5K
C9 .01uf
R12 5K
C2, 39 pF
R13 1K
RDBIT+ (16)
(16) CKB+
C18 S04
C17 LS51
C16 9602
B17
PU2
R20 20.5K
R21 20.5K
C7 120 pF
(14) AMSPCH+
(18) RMFM+
20A S04
(16) DRCLK+
(4) BDCOK-
(14) CLAMP+
E21 LS02
C15 S74
C19
PU1
C14 S00
R/WCLK+ (12)(11)
(20) VCO+
(15) AMDET+
(5) WPEN+
(14) CYCLE-
DRISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY R.E.
DATE:
REVISED
LOGIC DIAGRAM
SHT 17 OF 18
DRAWING NUMBER
853028 B



3. SYMBOL ▭ INDICATES J1, 50 PIN CONNECTOR.

2. SYMBOL ⬭ INDICATES J3, 20 PIN CONNECTOR.

1. SYMBOL ⬡ INDICATES J2, 20 PIN CONNELTOR.

NOTE:

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 18 OF 18
		DRAWING NUMBER 853028 B