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**TECHNICAL  
STATEMENT**

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TEXT LISTING

068-001069-01

PROGRAM

ARRAY PROCESSOR EXERCISER-E

TEXT TAPE

097-001069-01

ABSTRACT

THIS PROGRAM IS A FUNCTIONAL TEST FOR THE ARRAY PROCESSOR (AP).  
IT IS EXECUTED BY A CENTRAL PROCESSOR (OR IOP) CONTROLLING THE  
AP AND TESTS SPECIFIC AP INSTRUCTIONS.

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PROGRAM DESCRIPTION/THEORY OF OPERATION
7.0
7.1
INSTRUCTIONS TESTED:
LDR= LOAD A VECTOR TO RAM
STR= READ A VECTOR FROM AP RAM
IPC= REAL INNER PRODUCT
EPR= COMPLEX INNER PRODUCT
EPC= REAL POLYNOMIAL EVALUATION
CRE= COMPLEX POLYNOMIAL EVALUATION
MOD= CREATE A REAL VECTOR
MOD= MODIFY A REAL VECTOR

7.2
TEST DESCRIPTION
7.2.1
7.2.1
IPR = IPC
THE REAL VECTORS STORED AT BLOCKS "DIPRA"
AND "DIPRB" ARE LOADED INTO AP-RAM WITH AN
LDR INSTRUCTION. THE INNER (DOT) PRODUCT
OF THESE TWO VECTORS IS CALCULATED WITH
AN IPR INSTRUCTION AND THE RESULT LOCATED
TO CATCH. A COMPARISON ROUTINE THEN CHECKS
THE RESULT AGAINST THE KNOWN ANSWERS CHECKS
AT DIPRB. IN ANOTHER TEST RANDOM NUMBERS
ARE GENERATED WHEREBY AN IPR SIMULATOR
IS USED TO COMPARE RESULTS. THE IPC TEST
CHECKS THE INNER PRODUCT OF COMPLEX NUMBERS.

7.2.2
EPR = EPC
THE REAL VECTOR STORED AT DEPR IS LOADED
TO RAM. THESE ELEMENTS ARE THE COEFFICIENTS
FOR THE POLYNOMIAL IN ASCENDING ORDER FROM
W(0), W(1), ... W(N). THEY ARE MULTIPLIED
BY THE REAL SCALAR IN THE PARAMETER BLOCK
AND SUMMED. THE ANSWER IS COMPARED AGAINST
NUMBERS STORED AT DEPRR. A SIMULATOR IS
THEN USED TO VERIFY RANDOM NUMBERS. EPC DOES
THE SAME FOR COMPLEX COEFFICIENTS AND A
COMPLEX SCALAR.

7.2.3
CRE = MOD
TO TEST CRE, DATA IS LOADED TO RAM FROM
DEPR AND A SIMULATION IS PERFORMED
CREATING AN ARRAY OF ELEMENTS FROM DEPR
AS SPECIFIED BY INDICES STORED AT DCRMD.
THE RESULTS ARE STORED AT CATC2 AND THEN
COMPARED AGAINST THE RESULTS OF THE AP
INSTRUCTION, CRE.

TESTING MOD IS SIMILAR EXCEPT THAT THE
VECTOR STORED AT CATC2 IS MODIFIED BY
TAKING SEQUENTIAL ELEMENTS FROM IT AND
STORING THEM INTO POSITIONS OF CATC3
AS SPECIFIED BY ELEMENTS OF VECTOR DCRMD.

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S?WPD 8
?8.
SWITCH SETTINGS
LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS
(NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS,
THIS LOCATION WILL BE LOADED BY THE MONITOR.
HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS
LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED
BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED
OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC.
8.2

SWITCH OPTIONS
DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION
"SWREG" IS AS FOLLOWS:
BIT OCTAL BINARY INERPRETATION
VALUE VALUE
1 40000 1 LOOP ON ERROR
SKIP LOOPING ON ERROR
2 20000 1 PRINT TO CONSOLE
ABORT PRINT OUT TO CONSOLE
3 10000 1 DO NOT PRINT % FAILURE
PRINT % FAILURE
4 04000 1 ALLOW END OF PASS PRINT OUT
SUPPRESS END OF PASS PRINT OUT
5 02000 1 DO NOT PRINT ON THE LINE PRINTER
PRINT ON THE LINE PRINTER
6 01000 1 DO NOT HALT ON ERROR
HALT ON ERROR
7 0 0 DO NOT PRINT SUMMARY AND/OR
PASSING OF EACH SUBTEST
PRINT SUMMARY AND/OR
8 00400 1 PASSING OF EACH SUBTEST
PRINT ONLY THE FIRST ERROR
PRINT EVERY ERROR
00200 1

SWITCH COMMANDS
ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS.
EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
(DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0).
THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE
BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE
CHANGED BEFORE CONTROL IS ALLOWED TO RETURN TO THE
MAIN PROGRAM.

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; 8.2.1 OTHER COMMANDS  
"CR" A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM  
AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE  
"D THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG"  
TO DEFAULT MODE AND RESTART THE PROGRAM.  
"R THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE  
PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY  
HAD BEFORE THE COMMAND WAS ISSUED.  
"O THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE  
PROGRAM CONTROL TO GO TO ODT (NOTE: THIS IS AN  
OPTIONAL COMMAND AND IS AVAILRLE ONLY IF  
ODTPK IS PRESENT)  
M THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE  
CURRENT OPERATING MODES.

10006 .MAIN

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OPERATING PROCEDURE/OPERATOR INPUT  
1. LOAD THE PROGRAM IN THE HOST COMPUTER  
USING THE BINARY LOADER OR DTOS TAPE.  
2. SET SWITCHES EQUAL TO ONE OF THE FOLLOWING  
STARTING ADDRESSES:  
200.500 RUNALL TESTS  
501 IPR INSTRUCTION  
502 IPC INSTRUCTION  
503 EPR INSTRUCTION  
504 EPC INSTRUCTION  
505 CRE INSTRUCTION  
506 MOD INSTRUCTION  
507 ENTER MEMORY DUMP (SEE 7.0)  
3. PRESS START.  
4. THE PROGRAM PRINTS "PASS" FOLLOWING ALL  
SUCCESSFUL COMPLETION OF TESTS.  
ERRORS  
; 9.0  
; 10.0  
WHEN AN ERROR IS DETECTED A VALUE FOR AN  
ERROR PC WILL BE PRINTED ALONG WITH AC'S 0,1 AND 2  
OF THE HOST COMPUTER.  
THE PC VALUE PRINTED MAY POINT TO ONE OF THE  
FOLLOWING:  
1. A CALL TO EHALT  
2. A CALL TO THE ROUTINE WHICH DETECTED  
THE ERROR AND SUBSEQUENTLY EXITED  
TO EHALT SUCH AS THE VECTOR COMPARE  
ROUTINES TCOMP,CCOMP,RCOMP, AND RCCOMP.  
SUBROUTINES OF THIS TYPE HAVE SPECIAL ERROR PRINTOUTS  
CALLED IN THE ERROR ROUTINE. IN THE CASE OF THE REAL  
VECTOR COMPARE ROUTINES, TCOMP AND RCOMP, UP TO 3  
PAIRS OF GOOD/BAD DATA IS PRINTED INS 2-16. BIT HEX  
OR OCTAL FORMAT (SEE SW10), ALONG WITH THE HW ADDRESS  
OF THE DATA AND THE RELATIVE INDEX WITHIN THE VECTOR.  
A TOTAL ERROR COUNT IS PRINTED ALONG WITH  
THE VECTOR/VECTOR N,I,J,K DATA. IN THE CASE OF THE  
COMPLEX VECTOR COMPARE ROUTINES, CCOMP AND RCCOMP, THE  
GOOD/BAD DATA IS PRINTED IN 4-16. BIT HEX OR OCTAL  
FORMAT.  
THE SIGNIFICANCE OF ERROR PRINTOUTS IS EXPLAINED IN THE  
LISTING AT THE SOURCE OF THE ERROR. IN GENERAL  
AC0 CONTAINS THE CHECKWORD AND AC1 THE DATA IN  
QUESTION.  
AFTER PRINTING THE ABOVE THE PROGRAM HALTS ALLOWING  
THE OPERATOR TO SET THE SWITCHES. UPON PRESSING  
CONTINUE THE PROGRAM MAY EITHER GO ON TO THE NEXT  
TEST OR GO INTO A SCOPE LOOP BETWEEN THE APPROPRIATE  
CALLS TO .SETUP AND .LOOP (SEE 4.1 SWITCH SETTINGS)





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0012 .MAIN  
070TD 001551 MC 9/02  
S2WPD 001075 MC 4/02

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113. SPECIAL NOTES/SPECIAL FEATURES  
 13.1 FOR A COMPLETE TEST ALL PROGRAMS SHOULD BE EXECUTED WITH CAT/KITTEN.  
 13.2 A NOTE ABOUT AP ADDRESSING ADDRESSES IN THE AP CAN BE OF SEVERAL MODES:  
 1) ONE WORD MODE (IE) SAME AS STANDARD ADDRESSING  
 2) TWO WORD MODE (2WM) - EACH 32 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY REAL NUMBER ADDRESSING.  
 3) FOUR WORD MODE (4WM) - EACH 64 BITS IS NOW ONE ADDRESS SPACE. THIS IS USED IN THE AP TO SIMPLIFY COMPLEX NUMBER ADDRESSING.  
 THE AP ACCESSES AN ADDRESS RELATIVE TO THE START OF THE AP RAM. THUS AP RAM LOC 0 WOULD BE THE FIRST LOCATION THAT IS IN THE AP. HOWEVER, AS FAR AS THE ECLIPSE CPU IS CONCERNED, AP LOC 0 IS CONTAINED AT LOCATION LABEL "RAMPT". (IN PAGE ZERO. SO, IF RAMPT CONTAINS 64000+2000+2000=70000.  
 NOTE: "STOP ON STORE" OR "STOP ON ADDRESS" IN AP RAM SPACE WILL NOT WORK IF THE AP IS USING THE INTERNAL AP ADDRESS LINES TO ACCESS AP RAM.

14.0 RUN TIME  
 14.1 PASS 1 1 MIN  
 14.2 SUBSEQUENT PASSES 1 MIN 10 SEC

\*\*00000 TOTAL ERRORS, 00000 PASS 1 ERRORS