

TEXT LISTING

068-000539-01

PROGRAM

MICRO NOVA ANALOG TO DIGITAL
INTERFACE DIAGNOSTIC

TEXT TAPE

097-000539-01

ABSTRACT

THIS PROGRAM IS A LOGIC LEVEL TEST OF THE MODEL 4223 MICRO NOVA
ANALOG TO DIGITAL INTERFACE.


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18.1
OPERATING MODES/SWITCH COMMANDS:
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LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS
(NOT SYSTEM CONFIGURATION), WHILE RUNNING UNDER DTOS,
THIS LOCATION WILL BE LOADED BY THE MONITOR,
HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS
LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED
BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED
OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC.
6.2

SWITCH OPTIONS
DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION
"SWREG" IS AS FOLLOWS:

BIT      OCTAL  BINARY  INTERPRETATION
        VALUE  VALUE
1         00000  1       LOOP ON ERROR
2         00001  1       SKIP LOOPING ON ERROR
3         00002  1       PRINT TO CONSOLE
4         00004  1       ABORT PRINT OUT TO CONSOLE
5         00008  1       DO NOT PRINT % FAILURE
6         00016  1       PRINT % FAILURE
7         00032  1       ALLOW END OF PASS PRINT OUT
8         00064  1       SUPPRESS END OF PASS PRINT OUT
9         00128  1       DO NOT PRINT ON THE LINE PRINTER
10        00256  1       PRINT ON THE LINE PRINTER
11        00512  1       DO NOT HALT ON ERROR
12        01024  1       HALT ON ERROR
13        02048  1       DO NOT PRINT SUMMARY AND/OR
14        04096  1       PASSING OF EACH SUBTEST
15        08192  1       PRINT SUMMARY AND/OR
16        16384  1       PASSING OF EACH SUBTEST
17        32768  1       PRINT ONLY THE FIRST ERROR
18        65536  1       PRINT EVERY ERROR

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10008 .MAIN
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18.2
SWITCH COMMANDS
ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS.
EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
(DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0)
THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE
BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE
CHANGED BEFORE CONTROL IS ALLOWED TO RETURN TO THE
MAIN PROGRAM.

OTHER COMMANDS
"CR"      A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM
AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE
^D       THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG"
TO DEFAULT MODE AND RESTART THE PROGRAM.
^R       THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE
PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY
HAD BEFORE THE COMMAND WAS ISSUED.
^O       THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE
PROGRAM CONTROL TO GO TO ODT (NOTES THIS IS AN
ODTPK IS PRESENT)
M        THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE
CURRENT OPERATING MODES.

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18.3
SWITCH COMMANDS
ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS.
EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
(DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0)
THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE
BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE
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PROGRAM CONTROL TO GO TO ODT (NOTES THIS IS AN
ODTPK IS PRESENT)
M        THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE
CURRENT OPERATING MODES.

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NAME: MNADC.TX
PART NUMBER: 097-000539
DESCRIPTION: MICRO NOVA ANALOG TO DIGITAL INTERFACE DIAGNOSTIC
REVISION HISTORY:
REV.      DATE
00      11/16/77
01      06/10/78
*****
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10002 .MAIN
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PROGRAM NAME:
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MNADC = MICRO NOVA ANALOG TO DIGITAL INTERFACE
DIAGNOSTIC
REVISION HISTORY:
REV 00 = 11/16/77
REV 01 = 06/10/78
MACHINE REQUIREMENTS:
1. MICRO NOVA CENTRAL PROCESSOR WITH AT LEAST
4K READ/WRITE (RAW) MEMORY
2. MICRO NOVA ASYNCHRONOUS INTERFACE
3. TELETYPE OR CRT TERMINAL
4. PAPER TAPE READER AND/OR DISKETTE DRIVE
TEST REQUIREMENTS:
1. MICRO NOVA ANALOG TO DIGITAL INTERFACE MODEL 4023
2. MICRO NOVA ANALOG TO DIGITAL INTERFACE DIAGNOSTIC
" AB TAPE PART # 095 = 000539
LISTING PART # 096 = 000539
SUMMARY:
-----
THIS PROGRAM IS A LOGIC LEVEL TEST OF THE MODEL 4023
MICRO NOVA ANALOG TO DIGITAL INTERFACE.
RESTRICTIONS:
1. THIS DIAGNOSTIC CAN TEST ONE A/D INTERFACE
AT A TIME
2. THE FOLLOWING SIGNALS ARE NOT TESTED:
HANDSHAKING SIGNALS AND CONTROL FUNCTIONS:
ADC READY, SINCEND, DIFF, ADC CLOCK, ADC SERIAL
DATA, ADC CR PLY TEST, INTERNAL CLOCK (HANDSHAKING
SIGNAL ONLY).
ANALOG SIGNALS:
ANAS = ANAL7 (ANALOG MULTIPLEXOR INPUT LINES),
SAMPLE AND HOLD, ADMSB = ADDRESS (A/D DATA OUTPUT
LINES - NO ACTUAL DATA VALUES ARE EXPECTED OR
TESTED. HOWEVER, DURING DATA CHANNEL OPERATIONS,
A CHECK IS MADE TO THE INPUT DATA BLOCK TO
INSURE THAT SOMETHING HAS BEEN WRITTEN INTO IT).
THESE FUNCTIONS/SIGNALS ARE EXERCISED IS THE
"MICRO NOVA ANALOG TO DIGITAL EXERCISER",
" AB TAPE PART # 095 = 000037
LISTING PART # 096 = 000037
THIS INTERFACE CAN ALSO BE TESTED ON A SYSTEMS
LEVEL BY USING "MICRO NOVA ANALOG CONVERSION
SYSTEM EXERCISER",
" AB TAPE PART # 095 = 000109
LISTING PART # 096 = 000109

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10003 .MAIN

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PROGRAM DESCRIPTION/THEORY OF OPERATION:
NOTE: THE FOLLOWING CONVENTION IS USED IN THE
DESCRIPTION TO INDICATE LOW ACTIVE SIGNALS!

/SIGNALNAME/ = SIGNALNAME

17.1 ANALOG TO DIGITAL CONVERTER OPERATION:

THE A/D BOARD FOR THE MICRONOVA CONSISTS OF A TWO HYBRID
PACKAGE DATA ACQUISITION SYSTEM (DAS) ALONG WITH INTERFACE
AND LOGIC CIRCUITRY. AN ON-BOARD DC-DC CONVERTER
WILL PROVIDE +/- 15 VOLTS REQUIRED BY THE ANALOG CIRCUITRY.
THE HYBRID PACKAGE OF THE DAS CONSISTS OF TWO EIGHT-TWO-ONE
ANALOG MULTIPLEXERS, ANALOG SWITCH TO SELECT SINGLE ENDED
OR DIFFERENTIAL CHANNELS, INSTRUMENTATION AMPLIFIER, AND
SAMPLE AND HOLD. THE OTHER PACKAGE CONTAINS A 12-BIT A/D
CONVERTER WITH INTERNAL CLOCK. THE DAS CAN BE USED EITHER
WITH 16 SINGLE ENDED OR, FOR HIGHER COMMON-MODE REJECTION
RATIO, WITH 8 DIFFERENTIAL ANALOG INPUTS. THE SELECTION
OF SINGLE ENDED OR DIFFERENTIAL CHANNELS IS PROGRAM SELECT-
ABLE. VOLTAGE RANGES, WHICH ARE JUMPER SELECTABLE, ARE 0-5,
0-10, +/- 5, +/- 10 VOLTS. CONVERSION TIME IS 25 US MAXIMUM
WITH A THROUGHPUT RATE OF 30 KHZ LINEARITY AND DIFFERENTIAL
NONLINEARITY ERRORS ARE EACH TYPICALLY 1/2 LSB, CONVERSION
IS MONOTONIC, AND OVERALL RELATIVE ACCURACY AT 25 DEGREES C
IS 0.025% OF FULL SCALE READING.

THERE ARE SEVEN DIFFERENT CLOCK SOURCES FOR STARTING A/D
CONVERSIONS. FOR PROGRAMMED I/O THESE ARE /STRY/, NO
CLOCK SYNCHRONIZATION/ /STRY/, INTERNAL CLOCK SYNC/
/STRY/, EXTERNAL CLOCK SYNC, FOR DATA CHANNEL TRANSFERS
/THESE ARE: /IOPLS/ (ONE CONVERSION FOR EVERY /IOPLS/
COMMAND - THE TIME BETWEEN /IOPLS/ COMMANDS SHALL BE
GREATER THAN THE MAXIMUM DATA CHANNEL LATENCY OR 35 US,
WHICHEVER IS GREATER) /DCHY/, NO CLOCK SYNC (MAXIMUM
TRANSFER RATE) INTERNAL CLOCK SYNC/ EXTERNAL CLOCK SYNC.
THE EXTERNAL CLOCK SHOULD HAVE A PERIOD GREATER THAN
100 US. ALL DATA CHANNEL TRANSFER SEQUENCES BEGIN WITH
A /STRY/ COMMAND. THE CLOCK SOURCE IS SELECTED BY THREE
STATUS BITS IN A DOA INSTRUCTION. THIS INSTRUCTION MUST
ALSO CONTAIN AN INITIAL AND FINAL MULTIPLEXER ADDRESS.
A MUX CHANNEL COUNTER FIRST ADDRESSES THE INITIAL CHANNEL
AND IS INCREMENTED ONCE FOR EVERY CONVERSION. AFTER
THE VOLTAGE ON THE FINAL CHANNEL IS CONVERTED, THE
INITIAL CHANNEL IS AGAIN ADDRESSED. THIS SEQUENCE THEN
REPEATS ITSELF. HENCE, FOR CONVERSIONS ON ONLY ONE CHANNEL
THE FINAL AND INITIAL CHANNELS ARE SET EQUAL TO THE
DESIRED CHANNEL.

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CHANNEL NUMBERING IS AS FOLLOWS:

CHANNEL ADDRESS (OCTAL)	SINGLE-ENDED	CHANNEL SELECTED	DIFFERENTIAL
0	ANA0 (A49) HI	ANA0 (A49) LO	ANA0 (A49) HI
1	ANA0 SE RET (A47) LO	ANA0 (A49) LO	ANA0 (A49) HI
2	ANA1 (A45) HI	ANA1 (A45) HI	ANA1 (A45) HI
3	ANA1 SE RET (A43) LO	ANA1 (A45) LO	ANA1 (A45) HI
4	ANA2 (A41) HI	ANA2 (A41) HI	ANA2 (A41) HI
5	ANA2 SE RET (A39) LO	ANA2 (A41) LO	ANA2 (A41) HI
6	ANA3 (A37) HI	ANA3 (A37) HI	ANA3 (A37) HI
7	ANA3 SE SET (A35) LO	ANA3 (A37) LO	ANA3 (A37) HI
8	ANA4 (A33) HI	ANA4 (A33) HI	ANA4 (A33) HI
9	ANA4 SE RET (A31) LO	ANA4 (A33) LO	ANA4 (A33) HI
10	ANA5 (A29) HI	ANA5 (A29) HI	ANA5 (A29) HI
11	ANA5 SE RET (A27) LO	ANA5 (A29) LO	ANA5 (A29) HI
12	ANA6 (A25) HI	ANA6 (A25) HI	ANA6 (A25) HI
13	ANA6 SE RET (A23) LO	ANA6 (A25) LO	ANA6 (A25) HI
14	ANA7 (A21) HI	ANA7 (A21) HI	ANA7 (A21) HI
15	ANA7 SE RET (A19) LO	ANA7 (A21) LO	ANA7 (A21) HI
16	ANA8 (A17) HI	ANA8 (A17) HI	ANA8 (A17) HI
17	ANA8 SE RET (A15) LO	ANA8 (A17) LO	ANA8 (A17) HI
18	ANA9 (A13) HI	ANA9 (A13) HI	ANA9 (A13) HI
19	ANA9 SE RET (A11) LO	ANA9 (A13) LO	ANA9 (A13) HI
20	ANA10 (A9) HI	ANA10 (A9) HI	ANA10 (A9) HI
21	ANA10 SE RET (A7) LO	ANA10 (A9) LO	ANA10 (A9) HI
22	ANA11 (A5) HI	ANA11 (A5) HI	ANA11 (A5) HI
23	ANA11 SE RET (A3) LO	ANA11 (A5) LO	ANA11 (A5) HI
24	ANA12 (A1) HI	ANA12 (A1) HI	ANA12 (A1) HI
25	ANA12 SE RET (A0) LO	ANA12 (A1) LO	ANA12 (A1) HI
26	ANA13 (A130) HI	ANA13 (A130) HI	ANA13 (A130) HI
27	ANA13 SE RET (A128) LO	ANA13 (A130) LO	ANA13 (A130) HI
28	ANA14 (A26) HI	ANA14 (A26) HI	ANA14 (A26) HI
29	ANA14 SE RET (A24) LO	ANA14 (A26) LO	ANA14 (A26) HI
30	ANA15 (A22) HI	ANA15 (A22) HI	ANA15 (A22) HI
31	ANA15 SE RET (A20) LO	ANA15 (A22) LO	ANA15 (A22) HI

CODING JUMPERS:
DAS 0 LO = W7
DAS 0 HI = W6

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18999 .MAIN
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19. OPERATING PROCEDURE/OPERATOR INPUT
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NOTE: POWER SHOULD ALWAYS BE OFF DURING INSERTION
AND REMOVAL OF THE A/C INTERFACE (OR ANY BOARD)
INTO MICRO NOVA CHASSIS

TO RUN THIS DIAGNOSTIC:

1. INSERT A/D INTERFACE INTO AN I/O SLOT
WITH THE INTERRUPT PRIORITY (/INTP/) AND
DATA CHANNEL PRIORITY (/DCHP/) I/O LINES
PROPERLY JUMPED.
2. LOAD THE DIAGNOSTIC VIA PAPER TAPE OR
OOOS DISKETTE.
3. STARTING ADDRESS IS 800 (OR 500) OCTAL
AFTER THE PROGRAM HAS BEEN STARTED, THE
MEMORY WILL BE SIZED AND THE MESSAGE
"STOP OF MEMORY = XXXXX"
WILL BE PRINTED WHERE XXXXX IS THE
HIGHEST LOGICAL MEMORY ADDRESS IN
OCTAL.
5. ANSWER THE FOLLOWING QUESTIONS:

"DEVICE CODE = "

ENTER THE 6-BIT DEVICE CODE OF THE
DIA INTERFACE IN OCTAL.
(MUST BE < 77 OCTAL).

"DATA BIT 0 = (0 OR 1)"

THIS REFERS TO THE CODING TYPE OF THE A/D DATA.
(SEE SECTION 7.1)
USE BIT 0 = 0 FOR UNIPOLAR AND OFFSET BINARY BIPOLAR
USE BIT 0 = 1 FOR THEIR COMPLEMENT BINARY BIPOLAR

THE DIAGNOSTIC WILL THEN BEGIN OPERATION ACCORDING TO
THE MODES SELECTED BY "SMREG" (SEE SECTION 8). IF
IF AN INCORRECT RESPONSE IS MADE TO ANY QUESTION
IT WILL BE RE-TYPED.

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18.3 SELECTION OF SPECIAL TEST FUNCTIONS:
THE FOLLOWING "SMREG" SWITCHES CONTROL THE OPERATION
OF CERTAIN OPTIONAL TESTS, FOR ALL OF THE FOLLOWING:

SWITCH # 0 TEST IS SKIPPED
SWITCH # 1 TEST IS PERFORMED

SWITCH
C EXTERNAL CLOCK TEST
D EXTERNAL INTERRUPT TEST

NOTE THAT IF THESE FUNCTIONS DO NOT OPERATE BECAUSE
OF A HARDWARE ERROR, IT IS POSSIBLE FOR THE DIAGNOSTIC
TO REMAIN IN THE TEST LOOP. HOWEVER, FOR ANY OF THE
ABOVE TESTS SELECTED, THE PROGRAM WILL PRINT A MESSAGE
TO THE OPERATOR INDICATING WHICH TEST IS BEING
PERFORMED (AND INDICATING OPERATOR ACTION). IF THE
FUNCTION IS OPERATING PROPERLY, A "COMPLETED SUBTEST"
MESSAGE WILL BE PRINTED. THE ABSENCE OF THIS MESSAGE
AFTER THE OPERATOR HAS PERFORMED THE OPERATION
INDICATES A HARDWARE FAILURE. IN THIS CASE THE ERROR
CAN BE FOUND BY USING AN OSCILLOSCOPE FOR ERROR
TRACING, AS THE DIAGNOSTIC IS IN A SCOPE LOOP.

THE FOLLOWING OPERATOR ACTIONS ARE EXPECTED FOR
THE ABOVE TESTS (IF SELECTED):

TEST ACTION EXPECTED
EXT CLK PULSE THE EXTERNAL CLOCK LINE (AS)
AT LEAST (4) TIMES (A PULSE GENERATOR
CAN BE USED FOR THIS)
EXT INTERRUPT EXTERNAL CLOCK IS HIGH ACTIVE.
GROUND THE EXTERNAL INTERRUPT.
REQUEST LINE (AS) ONCE (LOW ACTIVE).

NOTE: EXTERNAL CLOCK CAN BE SELF-TESTED BY CONNECTING
THE INTERNAL CLOCK OUTPUT (AI) TO THE EXTERNAL CLOCK
INPUT (AS) AND SELECTING THE OPTIONAL EXTERNAL CLOCK
TEST (SEE ABOVE).

18.4 SETTING UP A SCOPE LOOP:

THIS DIAGNOSTIC CAN BE USED TO TRACE FAILURES ON
DETECTION OF AN ERROR. IF, AND WHEN AN ERROR IS
DETECTED DURING TESTING, A DIAGNOSTIC SCOPE LOOP CAN
BE FORMED BY DOING THE FOLLOWING:

1) "SMREG" SWITCH 1 MUST BE EQUAL 0 (LOOP ON ERROR).
2) NOTE THE PROGRAM COUNTER (PC) CONTENTS, THE SUB-
TEST #, THE ERROR # AND THE ACCUMULATOR CONTENTS.
3) SUPPRESS ALL TV/LPT OUTPUTS BY SETTING SWITCH 2 = 1
AND SWITCH 5 = 0.
4) GO TO THE FAILING ADDRESS ("PROGRAM COUNTER) IN THE
DIAGNOSTIC LISTING FOR THE INSTRUCTION SEQUENCE (AND
INFORMATION) THAT CAUSED OR DETECTED THE ERROR.
5) IF THE SCOPE LOOP FORMED WILL BE SLOW, IT CAN BE SPEEDED
UP BY FOLLOWING THE INSTRUCTIONS IN SECTION 11.7.
6) THE SCOPE LOOP SHOULD NOW BE READY TO USE. (HELPFUL
ITEMS ARE AN OSCILLOSCOPE, SCHEMATICS, PHYSICAL).

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PROGRAM OUTPUT/ERROR DESCRIPTION:
*****
ALL PROGRAM OUTPUTS, BOTH MESSAGES AND ERROR
REPORTS, ARE CONTROLLED BY THE VALUE OF "SMREG"
(SEE SECTION 8) SWITCHES 2 AND 3 AS FOLLOWS:

SWITCH 2 PRINTOUT TO
TY/CRY LPT
*****
0 0 YES
0 1 NO
1 0 YES
1 1 NO

IF AN ERROR IS ENCOUNTERED DURING DIAGNOSTIC
OPERATION, THE PROGRAM WILL PRINT OUT THE
FOLLOWING ERROR REPORT:

ERROR NUMBER # ENCOUNTERED SUBTEST #
CRY AC0 AC1 AC2 AC3 PC
X XXXXX XXXXX XXXXX XXXXX XXXXX

WHERE: CRY = CARRY COUNTER (FAILING ADDRESS)
AC0, AC1, AC2, AC3 = ACCUMULATOR CONTENTS
(CONTENTS DEPEND ON SPECIFIC TEST)

ALL NUMERIC VALUES ARE IN OCTAL. THE ACTION
TAKEN AFTER ERROR MESSAGE PRINTOUT DEPENDS ON
THE VALUE OF "SMREG" (SEE SECTION 8). IF SWITCH
6 = 1 THEN THE PROGRAM WILL HALT AFTER THE
MESSAGE "HALTED ON ERROR" IS PRINTED. IF SWITCH
1 = 0 THEN THE PROGRAM WILL LOOP ON THE ERROR
AFTER THE MESSAGE "LOOPING ON ERROR" IS PRINTED.
THIS FORMS A TEST SCOPE FOR FAILURE TRACING
WITH AN OSCILLOSCOPE. IF SWITCH 1 = 0 AND SWITCH 6 = 1
THE PROGRAM WILL FIRST HALT, THEN LOOP ON THE
ERROR. IF THE PROGRAM IS CONTINUED, IF SWITCH 6
= 1 THEN ONLY THE FIRST ERROR WILL BE REPORTED.
IF THE PROGRAM IS LOOPING ON AN ERROR AND "SMREG"
SWITCH 3 = 1, A SUBTEST FAILURE RATE IS REPORTED
AS "SUBTEST (#) FAILED (X) %", WHERE (#) IS THE
LOOP TEST NUMBER IN OCTAL AND (X) IS A DECIMAL %.
(NOTE: WHEN LOOPING ON A TEST THAT HAS MORE THAN
ONE ERROR BEING DETECTED, AND A % FAILURE RATE IS
BEING REPORTED, THE FAILURE RATE WILL APPEAR AS
X00% WHERE X IS THE # OF ERRORS OCCURRING. FOR
EXAMPLE, A SCOPE LOOP WITH 2 ERRORS WOULD REPORT
"SUBTEST (#) FAILED 200%").

AFTER ALL SUBTESTS HAVE BEEN PERFORMED (ONE PASS)
THE PROGRAM WILL REPORT "END OF PASS" (#). (#)
IS AN OCTAL VALUE.

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IF SWITCH 7 = 1, THE PROGRAM WILL INFORM THE
OPERATOR WHEN A SUBTEST HAS BEEN COMPLETED BY
PRINTING "COMPLETED SUBTEST (#)", WHERE (#) IS
THE SUBTEST NUMBER IN OCTAL. IN ADDITION, WHEN
SWITCH 7 GOES FROM 0 TO 1, AN ERROR SUMMARY WILL
BE PRINTED AS FOLLOWS:

ERROR SUMMARY REPORT FOLLOWS
ERROR NUMBER: (#1) (#2) ... (#N)
END OF SUMMARY

WHERE (#1) (#2) ... (#N) IS A LIST OF ALL ERROR
NUMBERS THAT HAVE BEEN DETECTED. IF NO
ERRORS HAVE OCCURRED THEN THE MESSAGE
"NO ERRORS ENCOUNTERED SINCE LAST SUMMARY"
WILL BE REPORTED INSTEAD.

OTHER ERRORS:

1. "FATAL SUBTEST SEQUENCE ERROR ENCOUNTERED"
IS REPORTED, FOLLOWED BY A HALT, IF ANY
TEST IS PERFORMED OUT OF SEQUENCE (I.E.
1, 2, 3, 5 INSTEAD OF 1, 2, 3, 4). NO.
SEQUENCE CHECK IS MADE FOR ANY SELECTED
OPTIONAL TESTS (SEE SECTION 8.3).

2. "FATAL STACK BOUNDARY VIOLATION. SP = (XXXXXX)"
IS REPORTED, FOLLOWED BY A HALT, IF A
STACK BOUNDARY IS CROSSED (256 WDS). XXXXXX
IS THE VALUE OF THE STACK POINTER (OCTAL).

3. "*** RTC FAILURE ***" IS REPORTED, FOLLOWED
BY A HALT IF THE REAL-TIME CLOCK FAILS TO
CAUSE INTERRUPTS DURING TIMER VALUE CALCULATIONS.

4. "UNIDENTIFIED INTERRUPT = (DVC)"
FOLLOWED BY AN ERROR PRINTOUT (SEE ABOVE) IS
REPORTED IF ANY DEVICE OTHER THAN THE A/D
INTERFACE REQUESTS AN INTERRUPT DURING DIAG-
NOSTIC OPERATION. DVC = THE OCTAL DEVICE CODE
OF THE DEVICE REQUESTING THE INTERRUPT. ALSO,
THE PROGRAM WILL ATTEMPT TO CLEAR THE INTERRUPT
BY ISSUING AN "INICC" INSTRUCTION TO THE DEVICE.

5. "EXTERNAL INTERRUPT = (DVC)"
FOLLOWED BY AN ERROR PRINTOUT (SEE ABOVE) IS
REPORTED IF AN UNEXPECTED A/D EXTERNAL INTERRUPT
(CAUSED BY GROUNDING THE /EXT INT REG/ LINE)
DURING DIAGNOSTIC OPERATION. THE INTERRUPT
IS NOT CLEARED BY THE INTERRUPT SERVICE ROUTINE.
HOWEVER, IF THE EXTERNAL INTERRUPT OCCURS
DURING THE EXTERNAL INTERRUPT TEST (SEE 8.3)
THE MESSAGE WILL BE PRINTED, INDICATING THAT
ONE WAS RECEIVED, BUT NO ERROR MESSAGE WILL
FOLLOW. DVC IS THE A/D DEVICE CODE (OCTAL).

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10013 .MAIN

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81 11.3.1 OPENING INTERNAL CELLS
82 ? THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF
83 ? THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN
84 ? 0 AND 7
85 ?
86 ? FOR ACCUMULATORS 0-3
87 ? FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN
88 ? THE EVENT OF A "P" COMMAND.
89 ? CPU AND TIO STATUS
90 ?
91 ? INTERPRETATION
92 ? 10 STATUS OF TIO DONE FLAG
93 ? 11 STATUS OF INTERRUPTS (ION FLAG)
94 ? 12 STATUS OF CARRY BIT
95 ? 13 ADDRESS OF LOCATION HAVING THE BREAK POINT (
96 ? ANY)
97 ? INSTRUCTION AT THE BREAK POINT LOCATION
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10014 .MAIN

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10015 .MAIN

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11.3.3 OTHER ODT COMMANDS

RUBOUT THIS KEY IS USED TO DELETE ERRONEOUSLY TYPED DIGITS. EACH TIME THE KEY IS PRESSED THE RIGHT M DIGIT IS DELETED AND ECHOED ON THE TERMINAL. IF THE RUBOUT KEY IS PRESSED RIGHT AFTER OPENING A CELL THEN IT DELETES THE RIGHT MOST DIGIT OF THE CONTENTS. THIS ALLOWS THE MODIFICATION OF THE CE AS IF ITS CONTENTS WERE TYPED IN JUST BEFORE THE KEY WAS PRESSED.

"ADR#B INSERT A BREAK POINT AT LOCATION "ADR#". ONLY ONE BREAK POINT CAN BE INSERTED AND ANY ENTRY TO ODT AFTER EXECUTING A BREAK POINT WILL CAUSE IT TO BE DELETED.

D DELETE THE BREAK POINT IF ANY.

P RESTART THE EXECUTION OF THE PROGRAM AT LOCATION POINTED BY 44.

"ADR#R START EXECUTING THE PROGRAM AT "ADR" AFTER AN ZO=RESET.

K KILL THE STRING TYPED SO FAR. THE ODT RESPONDS WITH A "B" AND THE OPEN CELL IS CLOSED WITHOUT MODIFICATION.

B PRINT THE OCTAL VALUE OF THE INPUT ONLY. THIS WILL CLOSE ANY OPEN CELLS WITHOUT MODIFICATION AND WILL NOT OPEN A CELL.

NOTE: IN PROGRAMS WHICH RELOCATE THEMSELVES THE USER SHOULD PLACE BREAK POINTS ONLY IN THE ORIGINAL PROGRAM AREA. IF A BREAK POINT IS PLACED OUTSIDE THIS AREA THE RESULTS WILL BE UNPREDICTABLE.

10016 .MAIN

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11.4 INSTRUCTION SET:

DOA1 OUTPUTS INITIAL DOA MUX CHANNEL, FINAL MUX CHANNEL, AND STATUS BITS TO THE INTERFACE.

D0, D1, D2 ARE THE CLOCK SOURCE SELECT BITS:

D0 D1 D2 CLOCK SOURCE TO START A/D CONVERSIONS

0 0 0 /STRY/, NO SYNC

PROGRAMMED 0 0 1 NO CONVERSIONS

I/O 0 1 0 /STRY/, INTERNAL CLOCK SYNC (FALLING EDGE)

0 1 1 /STRY/, EXTERNAL CLOCK SYNC (FALLING EDGE)

1 0 0 /IOPLS/, (1 DATA CHANNEL CONVERSION FOR EVERY /IOPLS/, NO SYNC

DATA 1 0 1 /DCHT/, NO SYNC (MAXIMUM TRANSFER RATE)

CHANNEL 1 1 0 INTERNAL CLOCK SYNC (FALLING EDGE)

1 1 1 EXTERNAL CLOCK SYNC (FALLING EDGE)

ALL DATA CHANNEL SEQUENCES BEGIN WITH THE NEXT CLOCK SOURCE SIGNAL AFTER STRY. SYNCHRONIZATION OCCURS ON THE FALLING EDGE OF THE INTERNAL OR EXTERNAL CLOCK.

D3 SINGLE-ENDED/DIFFERENTIAL CHANNEL SELECT

0 = DIFFERENTIAL

1 = SINGLE-ENDED

D4=D7 FINAL MUX CHANNEL, BIT 4 MSB

D12=D15 INITIAL MUX CHANNEL, BIT 12 MSB

TO READ DATA ON ONLY ONE CHANNEL, BOTH THE FINAL AND INITIAL CHANNELS SHOULD EQUAL THE DESIRED CHANNEL. /IORST/ CLEARS ALL STATUS BITS. THE DOA INSTRUCTION /S SHOULD NOT BE GIVEN IF BUSY IS SET.

10019 .MAIN

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111.5.2 TTY INPUT/OUTPUT INTERRUPT MASK OUT!
 THE CALL IS "NOTTY" AND WHEN PERFORMED, WILL MASK OUT
 ALL TTY (TY/TTO) INTERRUPTS. THE INTERRUPT MASK
 BITS FOR TY/TTO ARE BITS 14/15 RESPECTIVELY.

111.5.3 DCH STARTING ADDRESS/WORD COUNT GENERATOR!
 THE CALL IS "DSARC".

ON RETURN TO CALL + 1:
 AC0 = DCH RANDOM WORD COUNT (21'S COMPLEMENT)
 AC1 = DCH RANDOM STARTING ADDRESS
 AC2 = DCH FINAL ADDRESS (AFTER DCH CYCLE)

IF THE SUBTEST ERROR SWITCH IS SET, THEN THE LAST
 DCH WORD COUNT/STARTING ADDRESS/FINAL ADDRESS BEFORE
 THE ERROR OCCURRED WILL BE RETURNED IN AC'S 0, 1 & 2
 RESPECTIVELY.

THE RANDOM STARTING ADDRESSES/WORD COUNTS ARE
 DETERMINED SUCH THAT NO PROGRAM OR BINARY LOADER
 DESTRUCTION WILL OCCUR FOR PROPERLY FUNCTIONING
 DATA CHANNEL LOGIC, NOR WILL ANY MEMORY LOCATIONS
 RESERVED FOR THE CONSOLE DEBUG OPTION OR HAND
 HELD CONSOLE (077777=077377) BE ADDRESSED.

10020 .MAIN

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111.6 A/D CONVERTER SYSTEM MODEL 4223
 JUMPER CONFIGURATION INFORMATION:

JUMPER(S)

 W1
 IF INSERTED, A13 CONTAINS THE
 "Y" INFORMATION FOR ADC CROSS PLOT
 TEST. IT SHOULD NOT BE INSERTED
 NORMALLY.

W2, W3
 A/D CONVERTER RANGE/POLARITY SELECT
 AS FOLLOWS!

RANGE/POLARITY JUMPERS (INSERTED)

 +/- 10 VDC W3, W4
 +/- 5 VDC W2, W4
 0 = 5 VDC W2, W5
 0 = 10 VDC W2

W6, W7
 A/D CODING TYPE SELECT AS FOLLOWS!

W6 IN = TWO'S COMPLEMENT CODING
 W7 IN = OFFSET BINARY CODING
 (ONLY ONE MAY BE INSERTED).

W8 = W13
 A/D DEVICE CODE SELECT AS FOLLOWS!

***** DATA BIT *****
 10 11 12 13 14 15

 W10 W11 W12 W13 W14 W15
 DSB (MSB) DSB (LSB)

INSERT CORRESPONDING JUMPER FOR
 A "1" IN ANY OF ABOVE DEVICE CODE
 SELECT ("DS") BITS.

W14, W15
 "ADC READY" HANDSHAKING SIGNAL SELECT
 AS FOLLOWS!

W14 IN = TRUE LOW
 W15 IN = TRUE HIGH
 (ONLY ONE MAY BE INSERTED).

W16
 IF INSERTED, A "CLOCK OVERRUN" ERROR
 STATUS SIGNAL WILL SET DONE.

A/D CONVERTER POTENTIOMETER INFORMATION!

POTENTIOMETER

 FUNCTION *****
 R26
 INTERNAL CLOCK FREQUENCY
 (NOMINAL RANGE: 30 US = 500 US)
 R21
 A/D CONVERTER GAIN ADJUST
 R20
 A/D CONVERTER OFFSET ADJUST

18921 .MAIN

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111.7 SCOPE LOOP SPEED-UP INFORMATION:

? TESTS THAT HAVE AN I/O RESET IN THEM (MARST) USE
? "LTOPX" (JSR #ICV9C) AS THE SCOPE LOOP HANDLER ROUTINE.
? WHEN LOOPING ON AN ERROR, THIS ROUTINE ADDS A
? RATHER LARGE DELAY IN THE SCOPE LOOP IN ORDER TO ALLOW
? TTY INPUTS TO BE RECOGNIZED AND PROCESSED WITHOUT BEING
? CLEARED BY THE I/O RESET COMMAND IN THE LOOP. TO SHORTEN
? THE SCOPE TRACE TIME SIGNIFICANTLY WHEN LOOPING ON AN
? ERROR OCCURRING IN ONE OF THESE TYPE OF LOOPS, SIMPLY
? CHANGE THE "LTOPX" INSTRUCTION TO A "LLOOP" (JSR #ICV9E
? INSTRUCTION, THIS CAN BE DONE BY ENTERING THE OCTAL
? DEBUG TOOL (ODT). THE CONSTANTS "ICV9C" AND "ICV9E" ARE
? IN PAGE ZERO. REFER TO THESE LABELS IN THE LISTING TO
? OBTAIN THEIR RESPECTIVE ADDRESSES FOR THE COMMAND.

112. SPECIAL NOTES/SPECIAL FEATURES:

?
?
? SEE SECTION 6.3 FOR SPECIAL TEST INFORMATION.

113. RUN TIME:

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? THE FIRST TWO PASSES TAKE APPROXIMATELY 1 MINUTE.

18922 .MAIN

*-00000 TOTAL ERRORS, 00000 PASS 1 ERRORS