Technical Manual

NOVA 2

015-000026-01

DATA GENERAL TECHNICAL MANUAL

NOVA 2

Models

8331, 8332, 8333, 8334, 8335,
8336, 8337, 8338, 8339, 8340,
8351, 8352, 8353, 8354, 8355,
8356, 8357, 8358, 8359, 8360

Ordering No. 015-000026

Printed in the United States of America
Rev. 01, November 1974

Rev. 01

NOTICE

Data General Corporation (DGC) has prepared this manual for use by DGC personnel and customers as a guide to the proper installation, operation, and maintenance of DGC equipment and software. The drawings and specifications contained herein are the property of DGC and shall neither be reproduced in whole or in part without DGC prior written approval nor be implied to grant any license to make, use, or sell equipment manufactured in accordance herewith.

DGC reserves the right to make changes without notice in the specifications and materials contained herein and shall not be responsible for any damages (including consequential) caused by reliance on the materials presented, including but not limited to typographical or arithmetic errors, company policy and pricing information. The information contained herein on DGC software is summary in nature. More detailed information on DGC software is available in current released publications.

TABLE OF CONTENTS

SECTION O

INTRODUCTION

SECTION C

CENTRAL PROCESSOR

SECTION K

OPERATOR'S CONSOLE

TABLE OF CONTENTS (Continued)

SECTION P

POWER SUPPLY

SECTION M

MEMORY

SECTION I

NOVA 2 INSTALLATION

TABLE OF CONTENTS (Continued)

SECTION I (Continued)

SECTION N

MAINTAINING THE COMPUTER

SECTION T

REFERENCE TABLES

LIST OF ILLUSTRATIONS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

TABLE OF CONTENTS (Continued)

LIST OF TABLES (Continued)

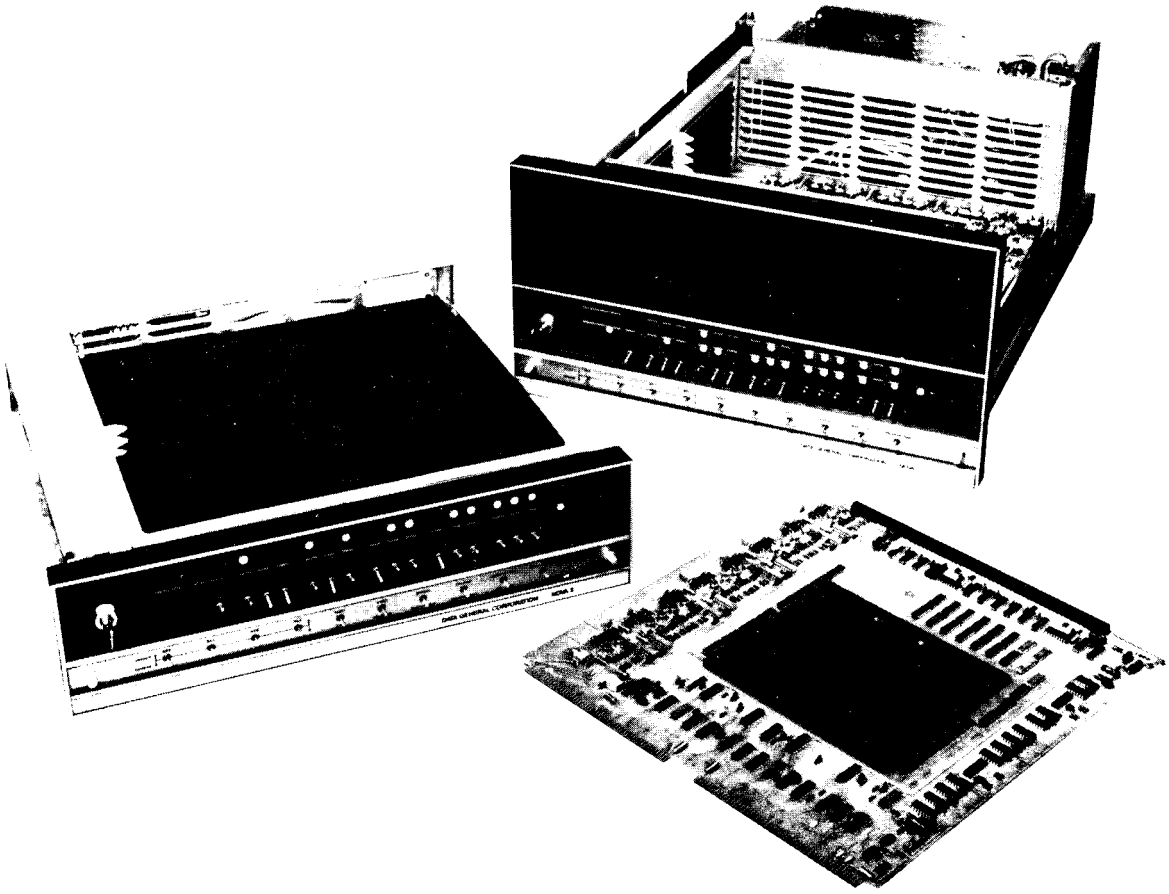


Figure O-1 Nova 2/4 and 2/10 With Memory Board

SECTION O

INTRODUCTION

THE NOVA 2 COMPUTER

The Data General Corporation Nova 2 minicomputer shown in Figure O-1 is a general purpose, four accumulator, stored-program computer employing a word length of sixteen bits. The Nova 2 is functionally compatible with other Nova machines, but uses new hardware and advanced computer technology to reduce size and cost and increase performance.

The basic computer as shown in Figure O-2 includes the chassis, back panel, power supply, console, central processor, and memory. Standard features include an I/O system with a sixteen bit word length, programmed data transfer, automatic interrupt source identification, sixty-four device addressing capability, sixteen level programmed priority interrupt, high speed direct memory access data channel with a maximum word transfer rate of 1.25MHz, and an external I/O bus connector. Options available are automatic program load, power monitor/auto restart, turnkey console, hardware multiply/divide, high speed floating point processor, real time clock, and 4K, 8K, or 16K memory modules.

The Nova 2 is available in two basic models, the 2/4 and the 2/10. The 2/4 has four slots and the 2/10 has ten slots available for subassembly circuit boards. The CPU, memory, high-speed I/O controllers, and other options are installed in these slots. Both models are available in either a rack-mounted configuration with slide mounts or in a table-top unit. It should be noted that the floating point processor is not available on the 2/4 because there are insufficient slots to accommodate it.

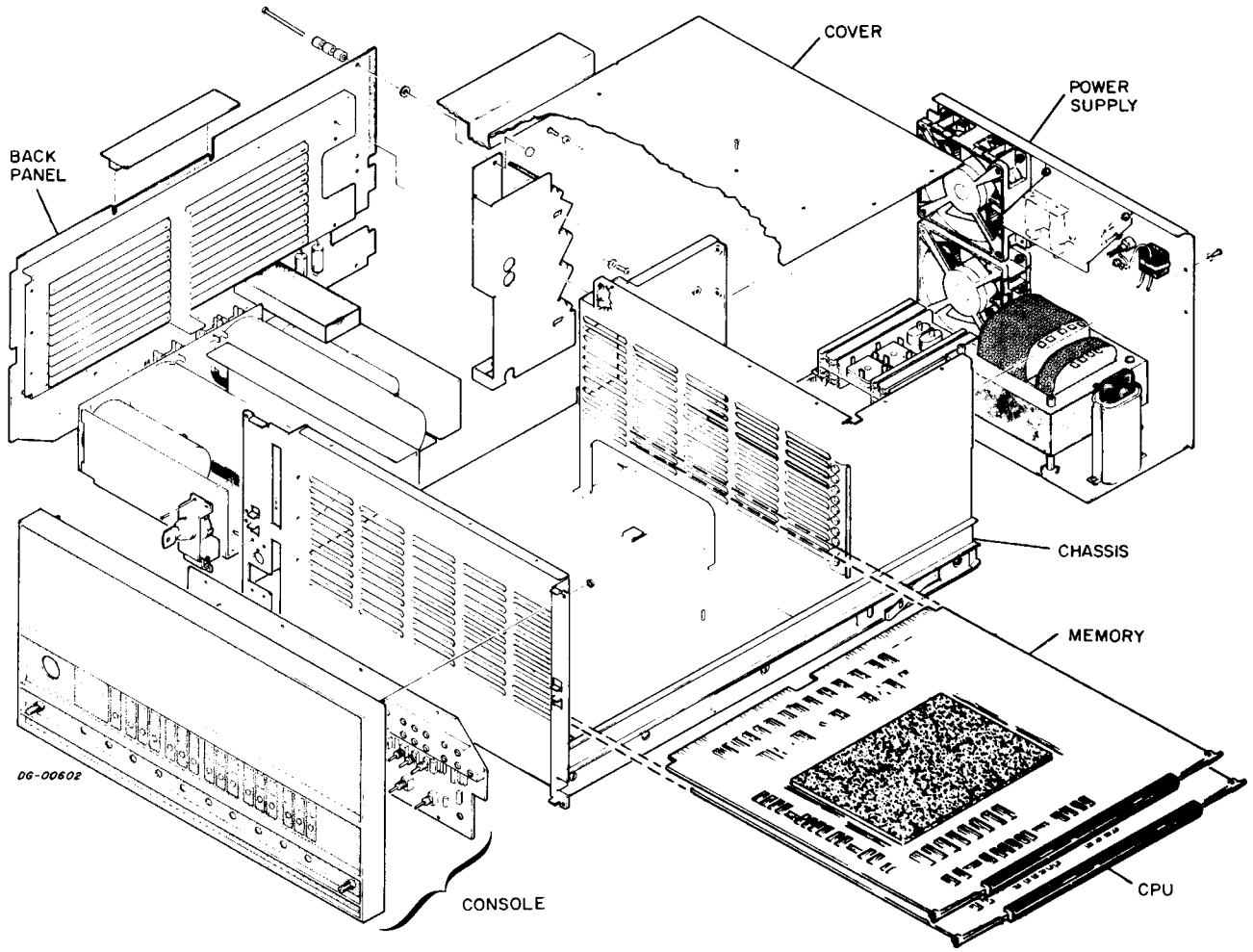


Figure O-2 Nova 2/10 Exploded View

THIS MANUAL

This Technical Manual explains how the NOVA 2 operates, how it is installed, and how it should be maintained. The manual is divided into eight sections:

Section O introduces the machine and this manual.

Section C explains the operation of the central processor.

Section K explains the operation of the console.

Section P explains the operation of the power supply.

Section M explains the operation of the memory.

Section I explains how to install the computer.

Section N includes maintenance information.

Section T has three reference tables--a signal list for the CPU, a signal list for the 4K and 8K memories, and a signal list for the 16K memory.

RELATED DOCUMENTS

Figure O-3 lists the manuals and engineering prints which relate to the NOVA 2. The Manual "How to Use the NOVA Computers" contains much valuable information on programming the machine and explains most of the basic information included in this manual. It is expected that the reader is familiar with the contents of this manual. The manual, the "Components Guide", gives logic diagrams and truth tables for the integrated circuits used in Data General machines.

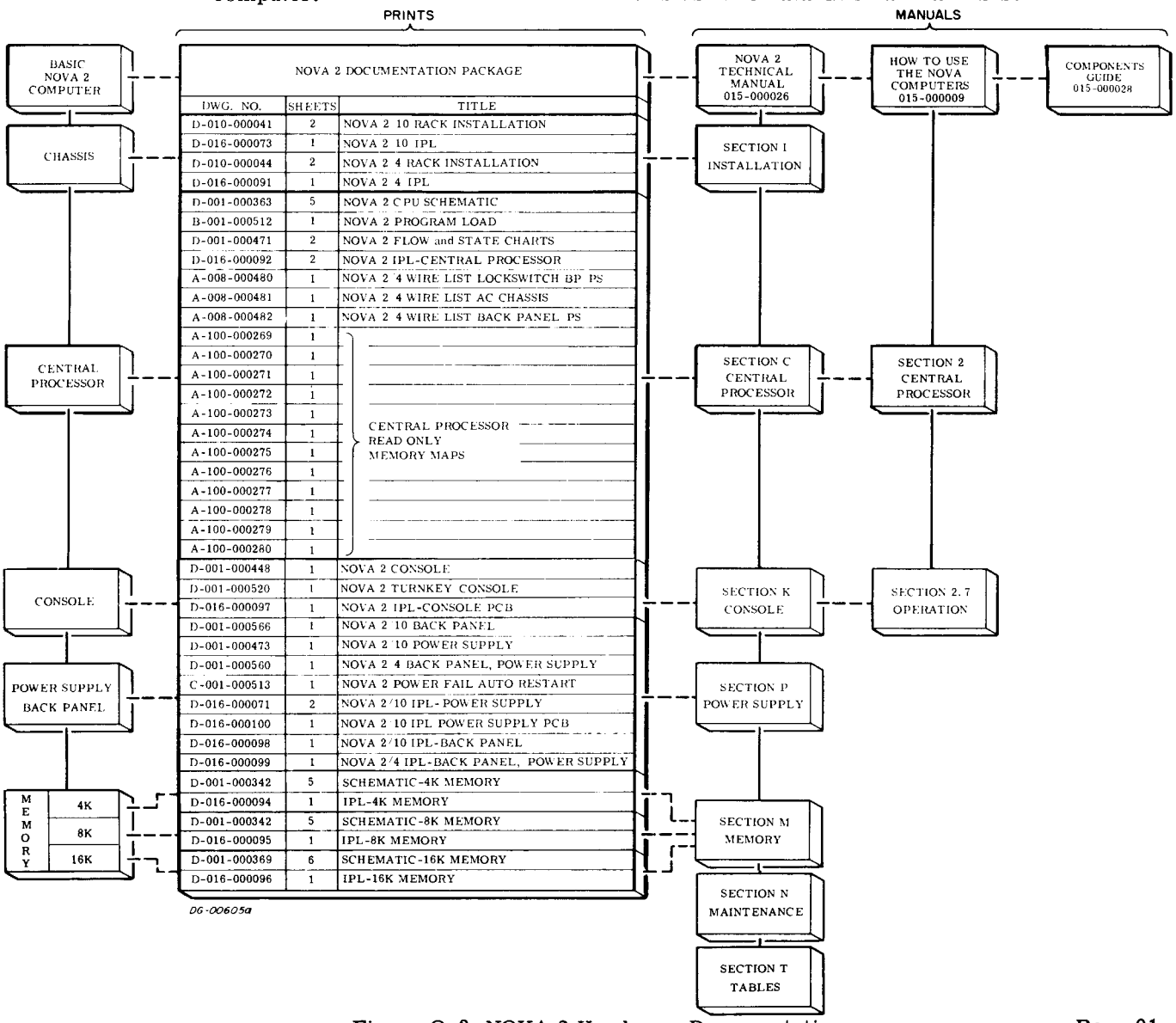


Figure O-3 NOVA 2 Hardware Documentation

Rev. 01

SIGNAL NAMES

In Data General equipment a signal can be asserted either when low or when high, depending on how it is defined. To distinguish between the two types of signals a naming convention has been adopted which defines the relationship between the logical and electrical levels of a signal. If the signal name includes a horizontal bar over the name, as "$\overline{\text{WRITE}}$", then that signal is asserted when it is at a low electrical level; conversely, a signal without the bar, "WRITE", is asserted when high. It should be apparent that two signals having the same name but differing by the bar must refer to the same logical function and thus must be true at the same time. That is, WRITE and $\overline{\text{WRITE}}$ will always be true at the same time, which is to say that $\overline{\text{WRITE}}$ is the electrical inverse of WRITE.

A bus is a collection of closely related signals which are individually identified by effectively subscripting the common label. For instance, 1WADR0, 1WADR1, and 1WADR2 are all part of a single bus. All or part of a bus is identified by placing brackets around the range of subscripts included, as 1WADR<0,2>. In this case, the suffix carries the information that there are three 1WADR lines under discussion, from 1WADR0 to 1WADR2, inclusive.

In an effort to minimize confusion, a distinction is made in this manual between electrical levels and logical levels or values. Electrical levels are always indicated by "H" or "L" and logical levels by "1" or "0". As an electrical level, an "H" indicates that the signal is high (greater than +2.4 volts) and an "L" indicates it is low (less than +0.8 volts). An asserted, or true, signal is indicated by a logical "1" and a false signal is described by a "0".

PRINT REFERENCES

Since this manual is primarily intended to assist the reader in understanding the NOVA 2, frequent reference must be made to the various engineering drawings associated with this machine. Where it is felt desirable to do so, a print reference is associated with each signal or functional block referred to, especially in the case of central processor signals. This print reference, which either points to the source of the signal or to the circuitry where the signal is being used, generally consists of two parts. The first, the print number, is the last three digits of the engineering drawing referred to, that is 001-000---. The second part contains two or three components, the sheet number, the vertical grid reference, and optionally, the horizontal grid reference.

SECTION C

CENTRAL PROCESSOR

INTRODUCTION

The central processor unit (CPU) used in the NOVA 2 is a binary, fixed word length, paralle, digital, programmable processor. The instruction set functions on a data path which includes four sixteen bit program accessible accumulators. The instructions, all a single word in length, can be divided into three classes: memory reference, input/output, and arithmetic/logical.

Using a fifteen bit memory address, the processor can address up to 32K words of memory. The eight bit displacement in a memory reference instruction may be used either as an absolute address or as a signed number for addressing relative to either the program counter or one of two accumulators. Both direct and indirect addressing is possible. Additionally there are sixteen memory locations which, when accessed by an indirect address, are automatically incremented or decremented before continuing the indirect address chain.

In addition to the standard I/O instructions, two facilities, program interrupt and direct memory access data channel, considerably improve input/output efficiency. The single-line interrupt facility allows input/output devices to interrupt normal processing and direct the software to its input/output processing routines. The two-speed direct memory access (DMA) data channel allows input/output devices to "steal" processor cycles with which to transfer data to and from memory. Use of this facility does not actually interrupt the program in progress, rather the program execution is simply suspended for the time that it takes to transfer each word.

The NOVA 2 processor consists of a collection of controlled data paths and the circuitry necessary to control these paths. The data paths are generally those blocks of circuitry which carry on sixteen bits of data at a time and include the buses, registers, arithmetic unit, etc. These data paths are controlled by two types of control signals, characterized as static levels or clock pulses. The levels, comprising the majority of the control signals, are determined by the various states of the machine, while the clock pulses keep all of the elements of the logic synchronized and time the transitions from one state to the next. To aid in clarifying the operation, the machine states are grouped by function into major states, during each of which the processor is in a specific operating "mode".

This section discusses the operation of the NOVA 2 processor in some detail. As the data paths are fundamental to the operation of the machine, they are discussed first. Where appropriate, the effect of control signals on the data paths is shown. The most important elements of the discussion of the control circuitry are the timing diagrams and processor flowcharts. The flowcharts, arranged by major states of the machine, serve to illustrate the relation between the control circuitry and data paths.

DATA PATHS

Organization

Figure C-1 shows the NOVA 2 data flow in block diagram form. As can be seen from this illustration, the central processor of the NOVA 2 is organized around a central processor bus ($\overline{CPB<0,15>}$), an eight word register file, and an arithmetic/logic unit. Other functional blocks consist of a shifter, carry logic, instruction register, input multiplexor, and device select, memory address, and output drivers. All data flow external to the central processor itself is on one bi-directional sixteen bit bus, $\overline{DATA<0,15>}$, which is common to the central processor, console, memories, and I/O controllers. All registers and major data paths are sixteen bits wide.

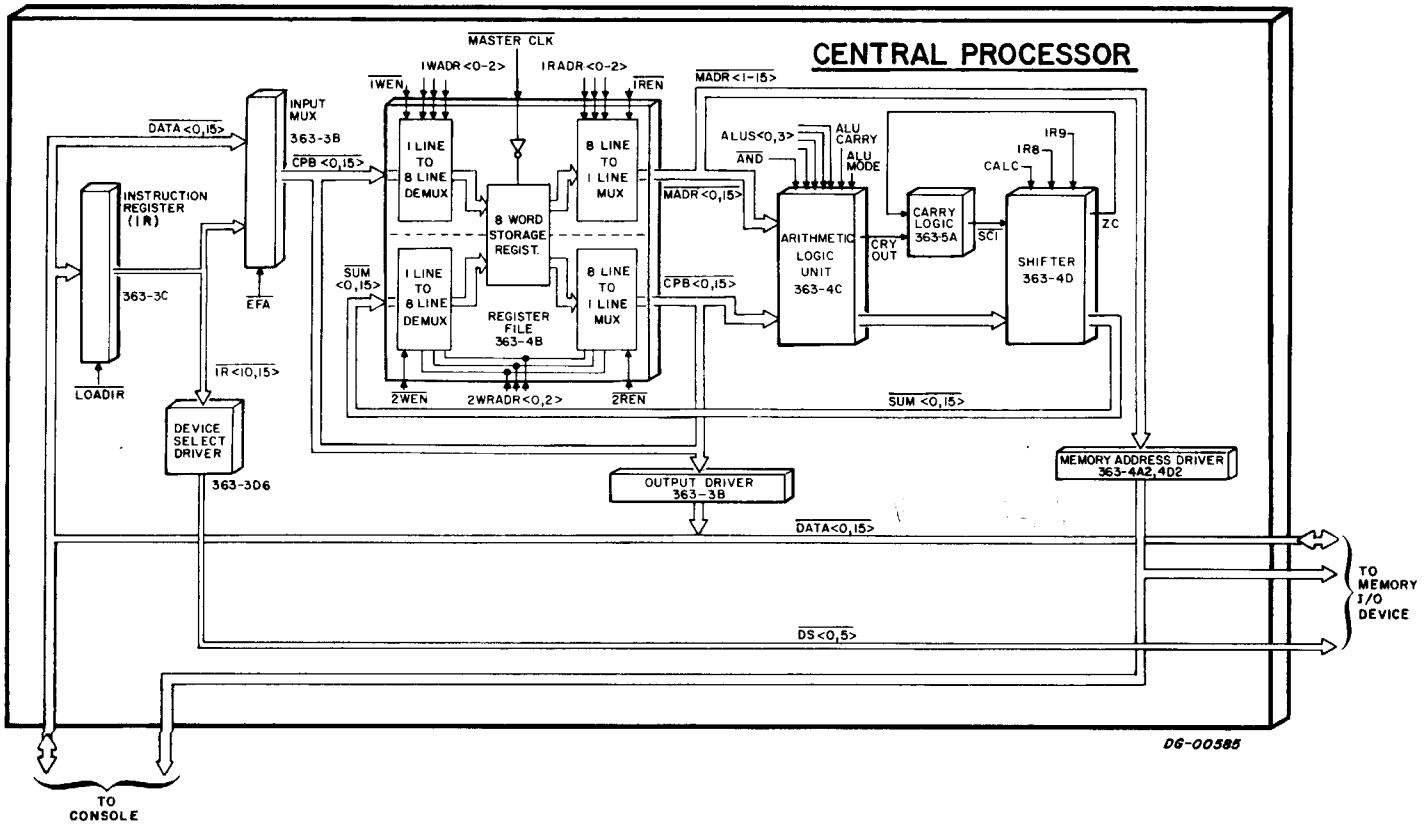


Figure C-1 NOVA 2 CPU Data Paths

Register File

The register file contains eight separate registers, as tabulated in Table C-1, including four accumulators, a program counter, memory address register, and two temporary registers, chiefly used for data channel transfers. The register file, shown in block form in Figure C-1, actually consists of eight integrated circuit chips; each chip contains eight words of two bits each. The register file has two input ports and two output ports; there are three independent address inputs.

Read Address One (1RADR<0,2>) determines which register's contents are to appear on $\overline{\text{MADR}}$<0,15>. Besides other functions, this address selects the source accumulator in an ALC instruction. The corresponding output is enabled by $\overline{\text{1REN}}$.

Write Address One (1WADR<0,2>) determines which register is to be written into from $\overline{\text{CPB}}$ <0,15>. The corresponding input is enabled by $\overline{\text{1WEN}}$, however, the data must be clocked into the register by the signal $\overline{\text{MASTER CLK}}$ going high.

Read-Write Address Two (2WRADR<0,2>) addresses the register whose contents are to appear on $\overline{\text{CPB}}$ <0,15>, and/or is to be written into from $\overline{\text{SUM}}$ <0,15>, the output of the shifter. This address selects the destination accumulator for an ALC instruction. The input and output for this address are enabled by $\overline{\text{2WEN}}$ and $\overline{\text{2REN}}$, respectively.

Table C-1

Register File Addressing

Address Lines			Register Selected	Function
0	1	2		
L	L	L	TEMP1	This register holds the input and output data during the data channel function.
L	L	H	Program Counter	The fifteen bit address of the next instruction to be fetched is held in the PC. During the fetch major state, the PC is incremented to point to the next sequential instruction. A JMP or JSR will replace the current contents of the PC with a new effective address, and a skip (See Fetch on flowcharts) will force an additional increment of the program counter.
L	H	L	TEMP2	This register holds the memory address to be accessed during the data channel function.
L	H	H	Memory Address	This register holds the fifteen bit address of the next memory location to be accessed whose contents are to be used as an operand by a memory reference instruction.
H	L	L	AC0	There are four sixteen bit accumulators which receive the results of processor functions and hold them available to be used for later operations, or to be stored in memory.
H	L	H	AC1	
H	H	L	AC2	
H	H	H	AC3	

Arithmetic/Logic Unit (ALU)

The arithmetic/logic unit consists of four arithmetic chips, as well as a look-ahead carry generator. The four chips are in parallel on the bus, with each processing four of the sixteen bits of the data word. Each arithmetic chip has two four-bit inputs, a four bit output, carry input and output information, and five function lines. The carry generator receives partial carry information from each of the four chips, and generates the resultant carry, CRY OUT. Table C-2 lists the control signals used to perform the various functions of the arithmetic/logic unit. "c(X)" indicates the logical contents of bus X.

Table C-2

ALU Control Signals

INSTRUCTION	IR5	IR6	IR7	ALUS 0	ALUS 1	ALUS 2	ALUS 3	AND	ALU CARRY	ALU MODE	ALU FUNCTION
Complement	L	L	L	L	H	H	L	L	L	L	c(CPB)* minus c(MADR) minus 1
Negate	L	L	H	L	H	H	L	L	H	L	c(CPB)* minus c(MADR)
Move	L	H	L	H	L	L	H	L	L	L	c(CPB)* plus c(MADR)
Increment	L	H	H	H	L	L	H	L	H	L	c(CPB)* plus c(MADR) plus 1
Add Complement	H	L	L	L	H	H	L	L	L	L	c(CPB) minus c(MADR) minus 1
Subtract	H	L	H	L	H	H	L	L	H	L	c(CPB) minus c(MADR)
Add	H	H	L	H	L	L	H	L	L	L	c(CPB) plus c(MADR)
And	H	H	H	H	L	L	H	H	H	L	c(CPB) AND c(MADR)
PROCESSOR FUNCTIONS											
Increment Register				H	H	H	H	L	H	L	c(CPB) plus 1
Page Zero EFA				H	H	H	H	L	L	L	c(CPB)
Decrement Register				L	L	L	L	L	L	L	c(CPB) minus 1
Pass MA				L	H	L	H	L	L	H	c(MADR)

*c(CPB) = 0, since 2REN = H

DG-00652

Carry Logic

In addition to the look-ahead carry generator, there is a block of logic which functions to set up the base value of the carry for an arithmetic operation, and to receive and store the carry results from that operation. The base value of the carry is set up without disturbing the previous carry, so that the previous carry value can be saved if an arithmetic instruction specifies "No Load". Table C-3 tabulates the functions of the carry logic.

Shifter

The shifter is made up of nine identical chips. Eight of these handle two bits of data apiece, resulting in one data word; the ninth outputs the new carry bit. The shifters are actually two-bit four-input multiplexors. Depending on the information present on the two control lines, one of the four inputs is selected and transferred to the output. The inputs to each bit position are connected to the outputs of the arithmetic/logic unit corresponding to the same bit position, the next right bit, the next left bit, and the equivalent bit from the other half of the word.

Instruction Register

The instruction register (IR) consists of four chips, each comprising a four bit latch. This register is loaded on the signal $\overline{\text{LOAD IR}}$, and outputs both the normal and inverted contents of the register. The output bits are connected to the control circuitry of the central processor, and the low-order eight bits also feed the input multiplexor for use in effective address calculations.

Input Multiplexor

This multiplexor usually connects the contents of the $\overline{\text{DATA}}$ bus to the central processor bus, $\overline{\text{CPB}}$. During the EFA (effective address calculation) major state, this multiplexor connects the low-order eight bits of the instruction register, along with a sign extension in the high-order eight bits, to the central processor bus.

Table C-3

Carry Chart For ALC Instructions

PRIOR TO INSTRUCTION	IR BITS 10	IR BITS 11	OVERFLOW OCCURRED?	CARRY AT COMPLETION
CARRY RESET	0	0	NO	RESET
CARRY RESET	0	0	YES	SET
CARRY SET	0	0	NO	SET
CARRY SET	0	0	YES	RESET
CARRY RESET	0	1	NO	RESET
CARRY RESET	0	1	YES	SET
CARRY SET	0	1	NO	RESET
CARRY SET	0	1	YES	SET
CARRY RESET	1	0	NO	SET
CARRY RESET	1	0	YES	RESET
CARRY SET	1	0	NO	SET
CARRY SET	1	0	YES	RESET
CARRY RESET	1	1	NO	SET
CARRY RESET	1	1	YES	RESET
CARRY SET	1	1	NO	RESET
CARRY SET	1	1	YES	SET

Drivers

The device select drivers always hold the contents of the low-order six bits of the instruction register on the device select ($\overline{DS<0,5>}$) lines of the I/O bus. The memory address driver similarly holds the contents of the $\overline{MADR}$ bus on the memory address bus (MAB) for communicating to the memories. The output driver, subject to various control signals, places the contents of the central processor bus on the $\overline{DATA}$ bus.

Data Buses

$\overline{DATA}$: All data transfers between the central processor and either memory or I/O devices take place on this bi-directional sixteen bit bus. Through the input multiplexor and output driver, the bus is tied to the principal central processor bus, $\overline{CPB}$.

$\overline{MADR}$: This sixteen bit bus carries the address for all memory accesses, and also serves to connect the source accumulators to the arithmetic unit. The fifteen bit memory address bus (MAB) is driven by the low order fifteen bits of $\overline{MADR}$.

$\overline{CPB}$: This is the primary bus in the central processor. Sixteen bits wide, it can be tied to $\overline{DATA}$ to receive or transfer data, and to either the input or output of any register.

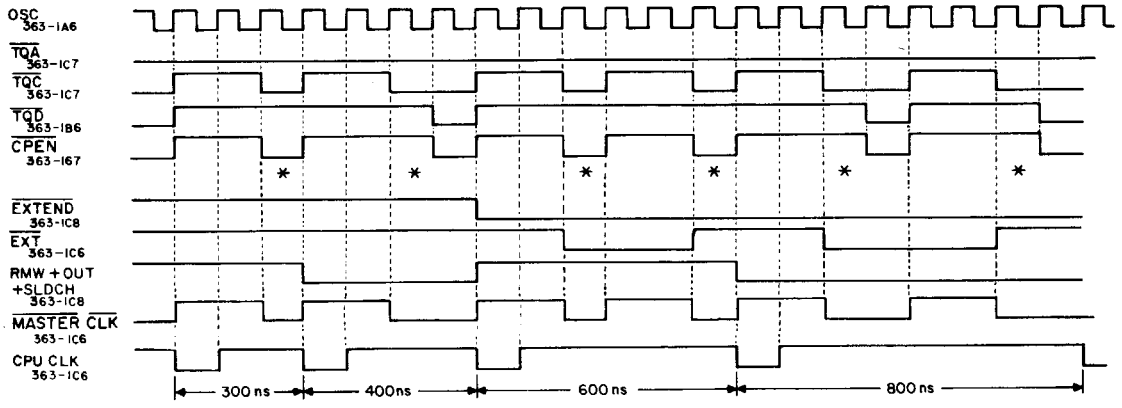
$\overline{SUM}$: This sixteen bit bus connects the output of the shifter (hence the entire arithmetic unit) to any accumulator or other register in the register file.

CONTROL

CPU Timing

The central processor of the NOVA 2 is a synchronous processor for which time is broken up by clock signals into discrete periods. All of the clocks are driven by a 20MHz crystal oscillator, the output of which is divided down to produce two complementary 10MHz or 100ns square waves, OSC and MEM CLK. MEM CLK is used chiefly to drive the memory logic. A four bit shift register which outputs $\overline{TQA}$, $\overline{TQC}$, and $\overline{TQD}$, serves as the center of the timing generator and is driven by OSC to produce CPU CLK, which is used to control most of the processor functions. CPU CLK is a 100ns pulse with a period of variable length, from 300ns, increasing by 100ns increments. As shown in Figure C-2, CPU CLK normally has four fixed periods 300ns, 400ns, 600ns and 800ns--depending on how EXTEND and either RMW, OUT, or SLDCH are asserted. Any or all of RMW, OUT, or SLDCH will increase the basic 300ns period to 400ns, while EXTEND will double the period, to either 600ns or 800ns.

While the processor of the NOVA 2 is inherently a synchronous machine, it is designed to run asynchronously with memory. This is possible by the use of the SYNC ENABLE signal, which normally floats high. When this signal is pulled low by a memory, as in Figure C-3 the timing generator is caused to freeze in the next $\overline{TQC}\cdot\overline{TQD}$ state and remain there until SYNC ENABLE is allowed to float high again, at which time the timing generator will continue its timing cycle. In this way, the processor is forced to wait until the lower speed memory has completed a read.



NORMAL PROCESSOR TIMING CYCLES

If $\overline{SYNC\ ENABLE}$ is held low, the processor timing halts in the $\overline{TQC}\cdot\overline{TQD}$ state, indicated by "*", and remains in that state until $\overline{SYNC\ ENABLE}$ returns high.

If processor operation is halted, $\overline{TQA}$, $\overline{TQC}$, and $\overline{TQD}$ remain high, and CPU CLK remains low. $\overline{TQA}$ is low whenever processor is running.

Figure C-2 Basic Central Processor Timing Generation

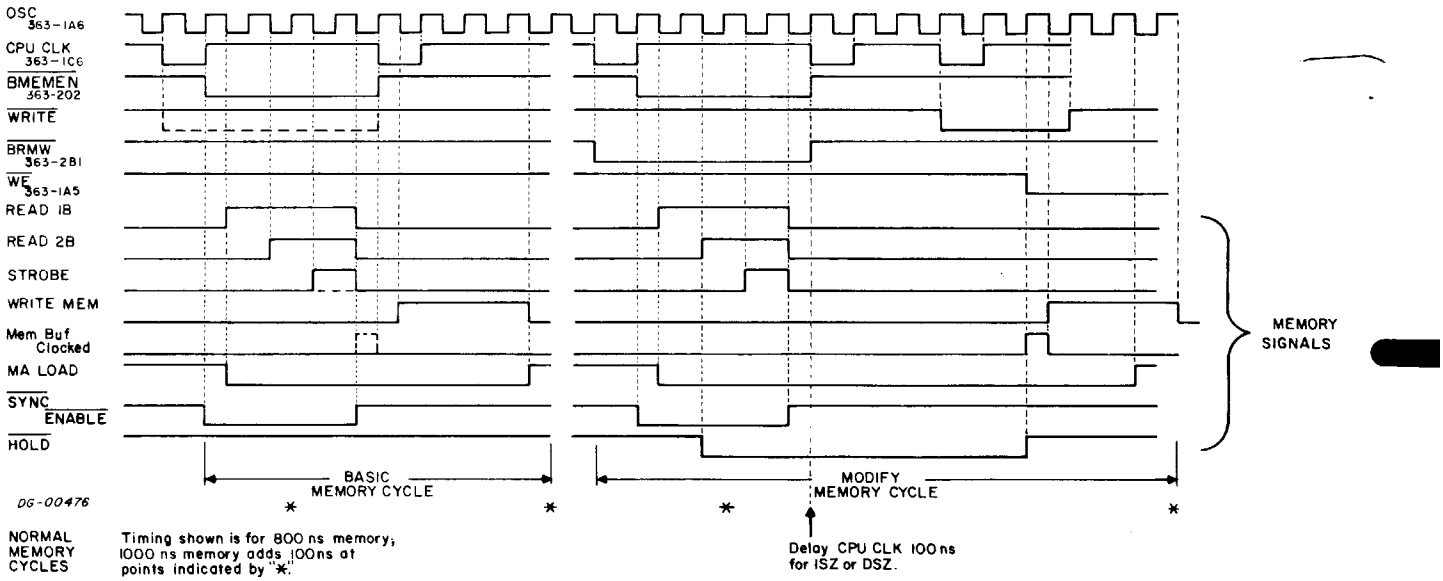


Figure C-3 NOVA 2 Central Processor/Memory Timing

ROM's and Wired-OR's

Two practices have substantially reduced the amount of logic hardware necessary in the NOVA 2 central processor. These are the use of read-only memories and so-called "wired-OR's". Both of these may be unfamiliar to the reader and it is felt worthwhile to discuss these at this point.

Ten read-only memories (ROM's) handle the major portion of the processor control functions. Each ROM has five address inputs, an enabling input, and eight output lines. The five input lines are decoded to produce thirty-two combinations of the eight output lines. The actual mapping of a ROM is described by the read-only memory map for that ROM (see Hardware Documentation, Figure O-3). These maps detail the relationship between the five input signals, numbered A0 thru A4, and the eight output signals, Y0 thru Y7 for each particular ROM. The maps are specified for positive logic signals, that is, a high electrical level is always indicated by a 1, and a low level by a 0. In general, not more than two ROMs are enabled at any one time. When a ROM is not enabled (pin 15=high), all of its outputs float at a high level.

Upon examination of the signal list or prints for the central processor, it will be noticed that a number of signals have more than one source. In actuality, this is merely an extension to the CPU itself of what has been common practice on the I/O bus for previous machines, where several sources must drive one line. Each gate driving the common signal is of the open collector type, and the line is normally held high by a pull-up resistor. Any such gate driving the signal can then pull it low independently of the action of the other gates. This is referred to as a "wired-OR" connection. Examples of this in the NOVA 2 CPU are the signals $\overline{2REN}$ and $\overline{2WRADR1}$.

Major States

As an aid to understanding the internal functions of the central processor, it is useful to segregate the various functions into generalized groups called "Major States". During each major state the processor is effectively dedicated to performing a specific internal function. In the NOVA 2 there are eight such major states each lasting from one to three CPU CLK periods. The major states are principally defined by the signals FETCH, MRI, KEY, DEFER, and DCH, and to a lesser extent by PTS0, or PTS1, PI, and AUTO. A brief summary of the action of each major state as well as the signals causing that state is given below; the flowcharts at the end of this section detail the actual internal functioning of the processor.

FETCH: (FETCH, PTS0) (Figure C-8).
If SKIP is set, the program counter is first incremented by one. The memory location defined by the program counter is read, and its contents are

considered an instruction and loaded into the instruction register. The program counter is then incremented by one.

EFA: (PTS1, MRI, DEFER) (Figure C-9).
The effective address of the operand for a memory reference instruction is determined.

DEFER: (PTS0, MRI, DEFER) (Figure C-10).
A memory location defined by the memory address register is read, and its contents are considered to be the address of an operand and loaded into the memory address register. If the memory location is to be auto-incremented or auto-decremented, the word is adjusted accordingly (PTS0, MRI, DEFER, AUTO) and written back into memory (PTS1, MRI, DEFER, AUTO).

EXECUTE·MRI: (PTS0, MRI) (Figures C-11, C-12).
A memory location is accessed and the word transferred to or from memory is the operand of a memory reference instruction. JMP or JSR do not cause a memory access, but otherwise execute in this state (a JMP direct is "executed" during the EFA state). An ISZ or DSZ instruction updates a memory location in an additional clock period (PTS1, MRI).

EXECUTE·$\overline{\text{MRI}}$: (PTS1) (Figure C-13).
A function is performed on operands existing in accumulators, without accessing memory. A programmed I/O instruction executes in this state with an additional clock period for an input or output transfer (PTS0).

PI: (PI, FETCH, PTS0; PI, FETCH, PTS1) (Figure C-14).
A program interrupt occurs prior to a FETCH state when there is an interrupt request. The processor stores the program counter in location 0, causes a JMP instruction (all zeroes) to be placed in the instruction register, sets 1 as the next effective address in the memory address register, and forces the next state to be DEFER.

DCH: (DCH) (Figures C-15, C-16).
A Data Channel transfer occurs as the result of a request from an I/O device for an automatic transfer of data to or from memory. The data channel state can in general be entered on any CPU CLK pulse. The exceptions are noted on the various flowcharts.

KEY: (KEY) (Figure C-17).
A key function occurs whenever a manual function is requested from the computer's console, except for STOP and RESET. The STOP function simply sets HLT PND, which halts the processor in the next FETCH major state, while the RESET function halts the processor immediately and forces it into the FETCH major state.

Power Monitor

In the event of a power failure it is important that the processor be halted before reliable power is lost. For this reason two signals from the power fail module in the power supply are monitored by the central processor. Additionally, if the power monitor and auto restart option is installed a third signal is monitored which gives an early warning of a power failure. These same signals cause a reset when power is returned and allow for an automatic restart of the processor.

The processor always monitors the MEM OK signal from the power fail module. Whenever MEM OK goes low the HLT PND and HRST signals are set. This action is equivalent to a console RESET function, including an IORST pulse to all devices. When power is returned, MEM OK remains low for a small time delay causing a reset function which sets the initial machine state. When MEM OK is asserted, the processor can be restarted.

If the Power Monitor and Auto Restart option is installed the $\overline{\text{PWR FAIL}}$ signal from the power fail module is also monitored. This signal will be the first to go low in the event of a power failure, approximately 1 to 2msec before MEM OK. When PWR FAIL is asserted the power monitor sets the PWR LOW flag which causes an interrupt request. When power is restored a 2msec delay is initiated after MEM OK and $\overline{\text{PWR FAIL}}$ have both gone high. If the console power switch is in the ON position, no further action is taken. However, if the switch is in the LOCK position, the RESTART function is performed at the end of the delay, causing a jump direct to location 0. The power fail and restart sequences are shown in Figure C-4.

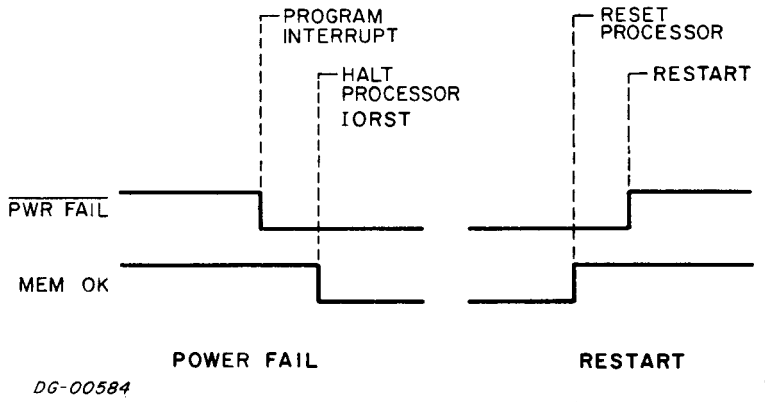


Figure C-4 Processor Response To Power Fail and Restart Signals

I/O Timing

Timing diagrams for the NOVA 2 programmed I/O and the standard and high speed data channels are shown in Figures C-5, C-6, and C-7. In addition to the various signals appearing on the I/O bus, the diagrams include some relevant signals which are internal to the processor, and do not appear on the I/O bus. OSC is the continuously running 100ns processor clock and is included in each figure primarily as a timing reference. Similarly, CPU CLK is included to show the relationship between the bus signals and internal processor functions. The I/O SKIP signal shown in Figure C-5, is issued internally by the processor instead of the data transfer signals, and gates in the state of the selected signal, SELD or SELB. The DCH signal shown in all of the data channel diagrams is set whenever the processor is in the data channel state. The CONMEM signal is shown set in those data channel states which retain data on the DATA bus.

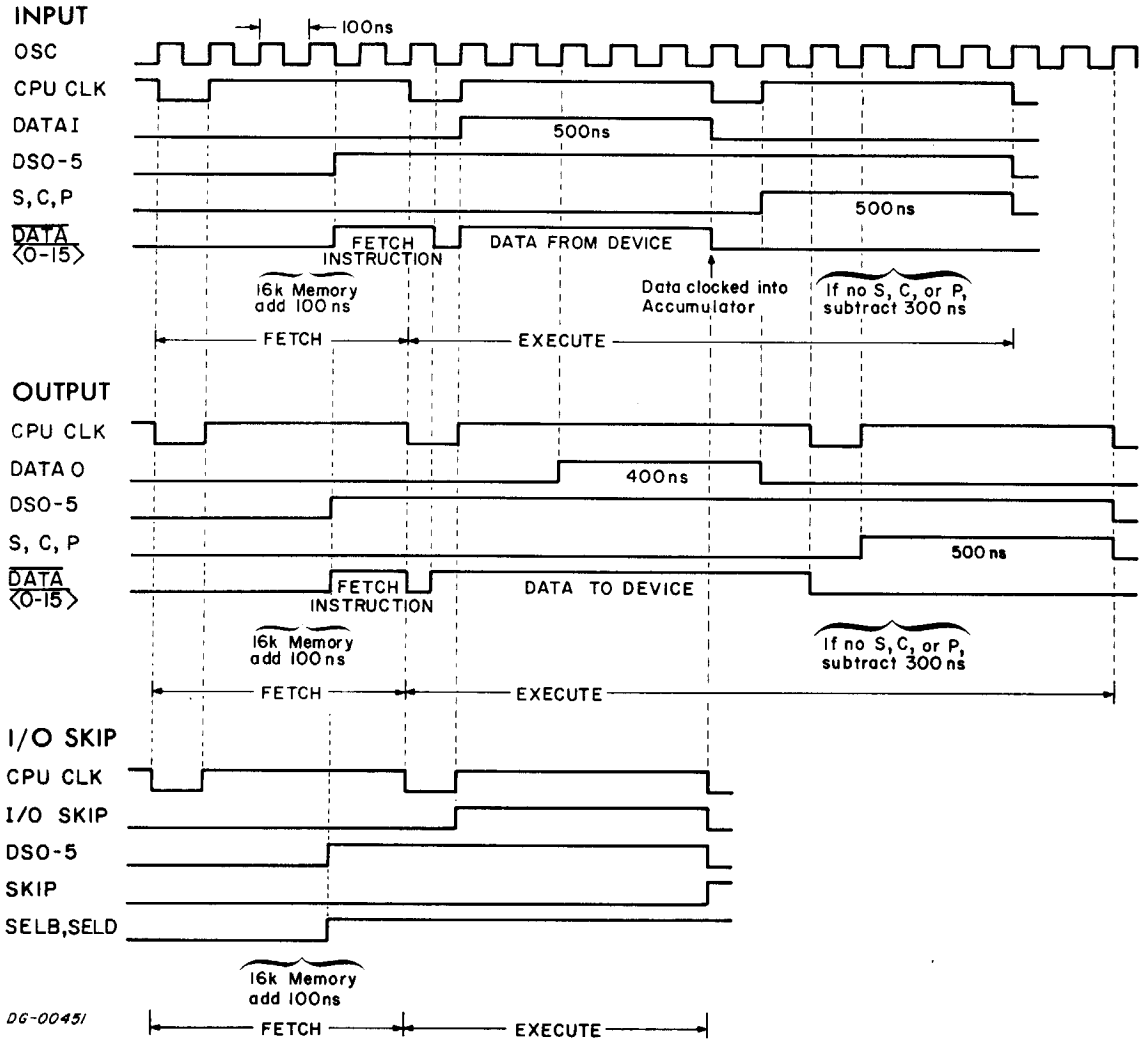


Figure C-5 Programmed I/O Timing

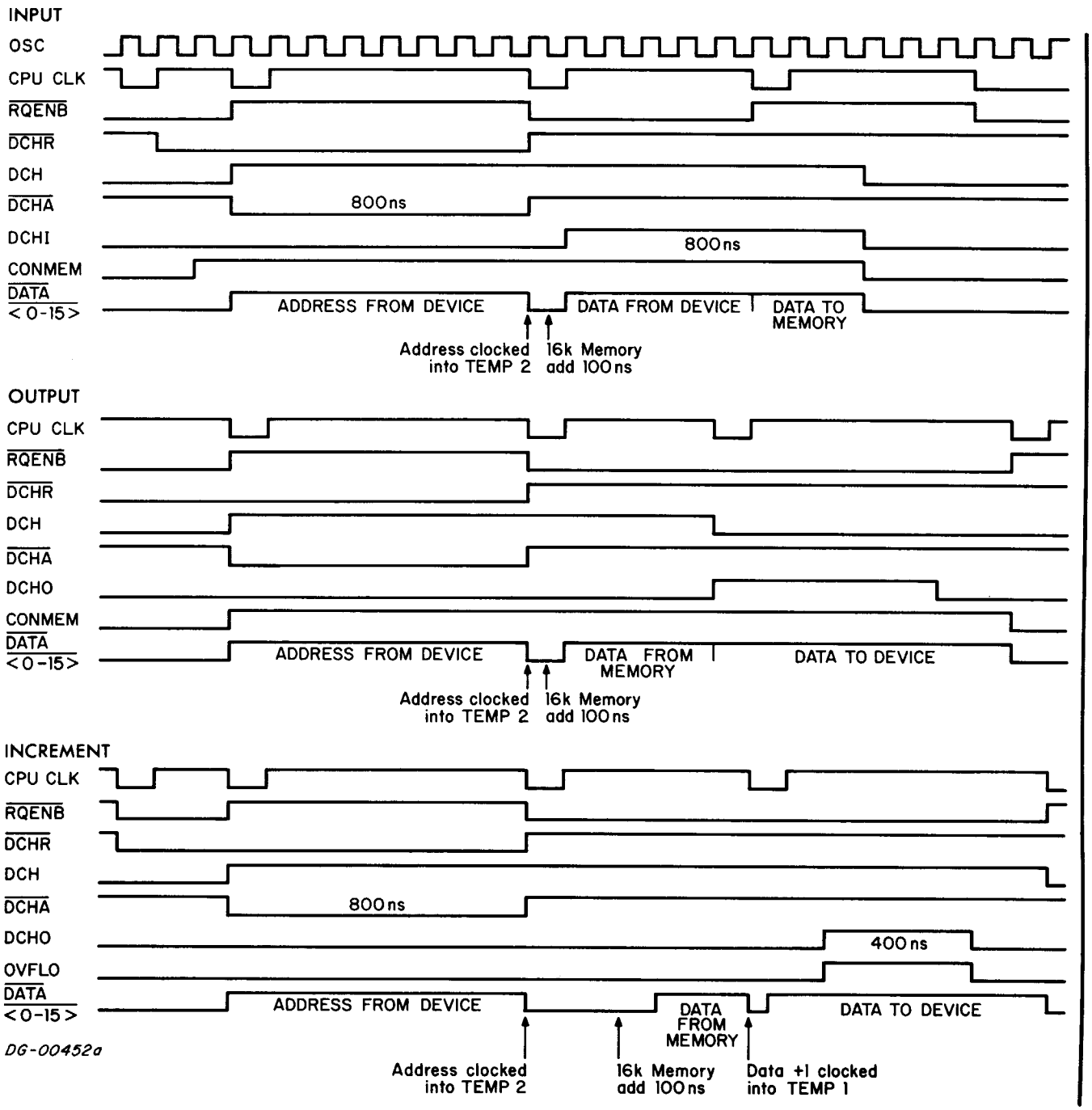


Figure C-6 Standard Data Channel Timing

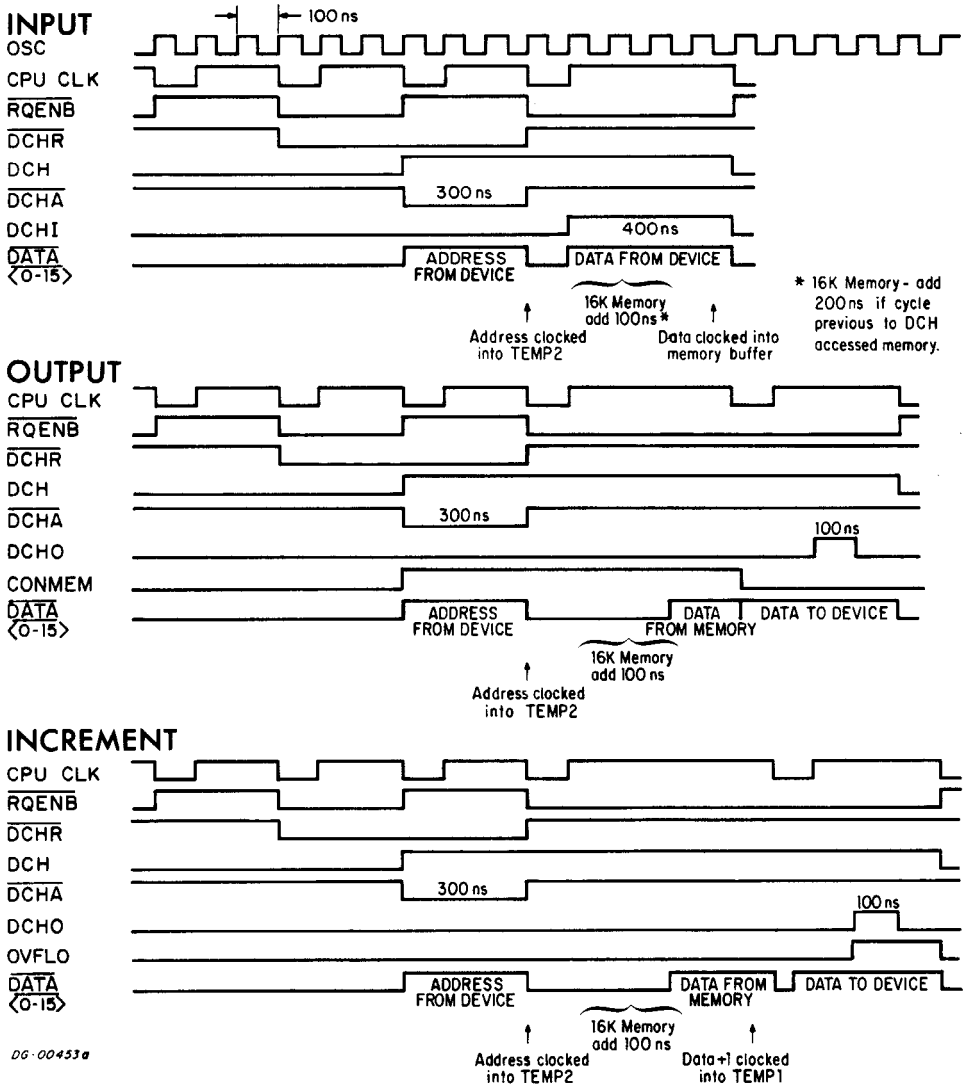


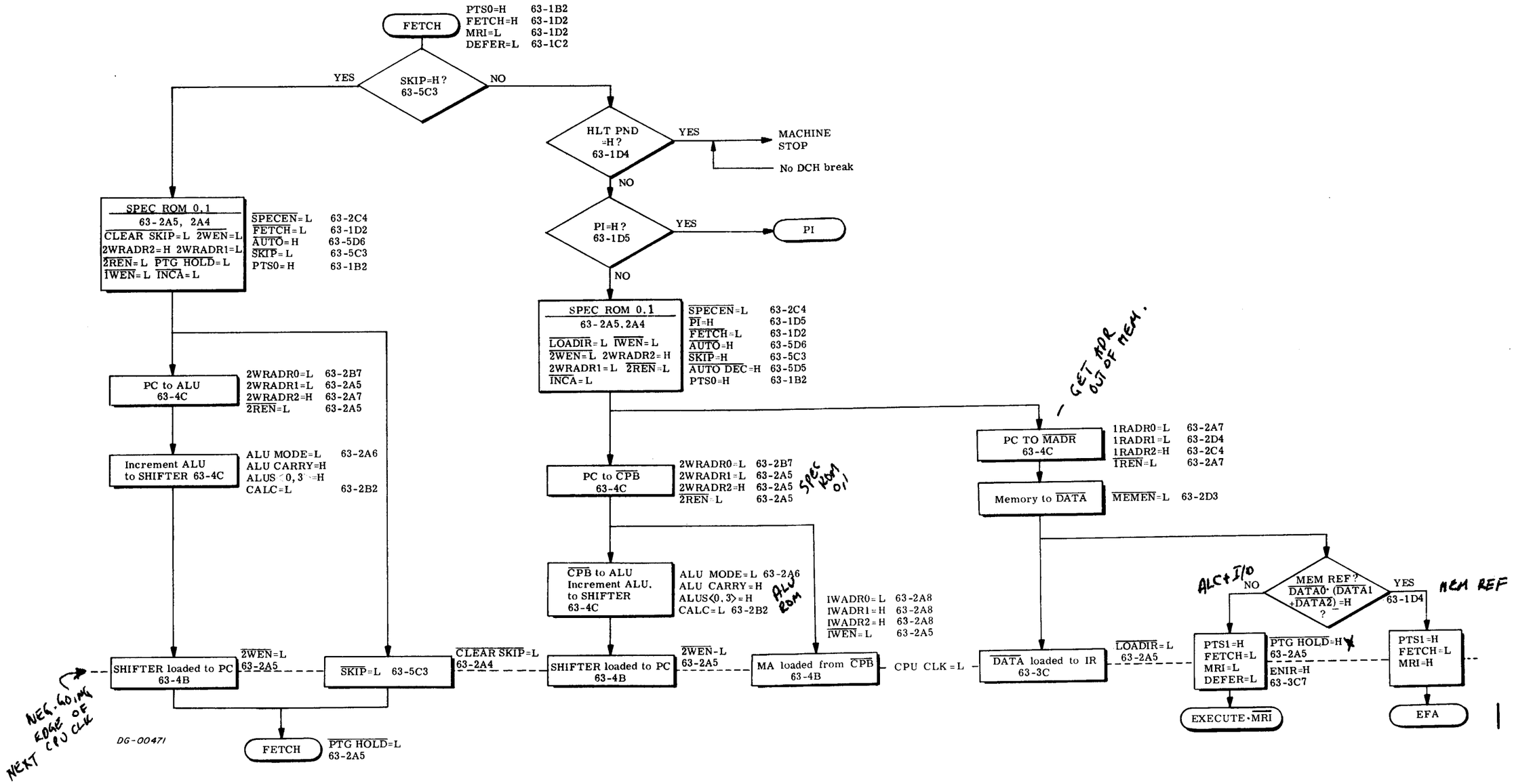
Figure C-7 High Speed Data Channel Timing

Central Processor Flowcharts:

Detailed flowcharts for the major states of the NOVA 2 processor follow. The diagrams are generally self-explanatory, once the conventions used have been realized. The outputs of the relevant read-only memories are listed at the beginning of each CPU CLK period. All data flows and control functions are indicated in the rectangular boxes. Alongside such functions are listed the conditions that cause that function and the location on the prints of the source of the signals involved. All signal coordinates refer to engineering drawing D-001-000363. The three components for each signal following the print number (i.e., 363-___) are sheet number, vertical coordinate, and (optionally) horizontal coordinate. Functions that are dependent on the CPU CLK (such as the setting of flip-flops) are shown intersecting a dotted line labeled CPU CLK = L. This indicates that such functions do not occur until the beginning of a CPU CLK pulse. The reader is also advised that processor state charts and simplified flowcharts can be found on engineering drawing D-001-000471, included in the documentation package.

REFERENCES

1. NOVA 2 CPU Schematic D-001-000363-08.
2. Console ROM0 Map A-100-000269-00.
3. Console ROM1 Map A-100-000270-00.
4. MRI ROM0 Map A-100-000271-00.
5. MRI ROM1 Map A-100-000272-00.
6. SPEC ROM0 Map A-100-000273-00.
7. SPEC ROM1 Map A-100-000274-00.
8. DCH ROM0 Map A-100-000277-00.
9. DCH ROM1 Map A-100-000278-00.
10. ALU ROM Map A-100-000279-00.
11. I/O ALC ROM Map A-100-000280-00.
12. Flow and State Charts D-001-000471-00.
13. Components Guide 015-000028-01
14. 8K Memory Schematic D-001-000342-01.
15. 16K Memory Schematic D-001-000369-02.



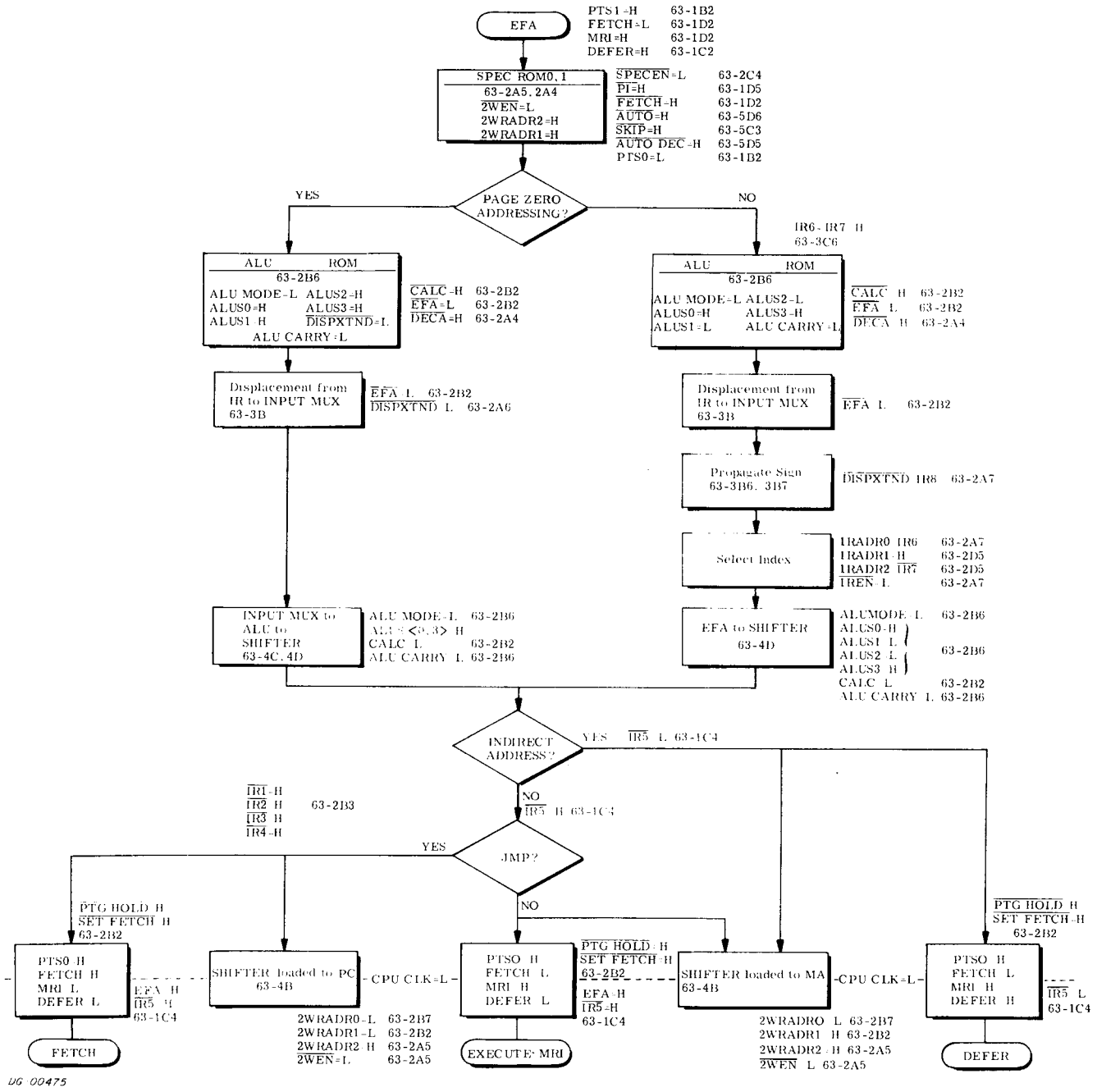


Figure C-9 EFA Major State

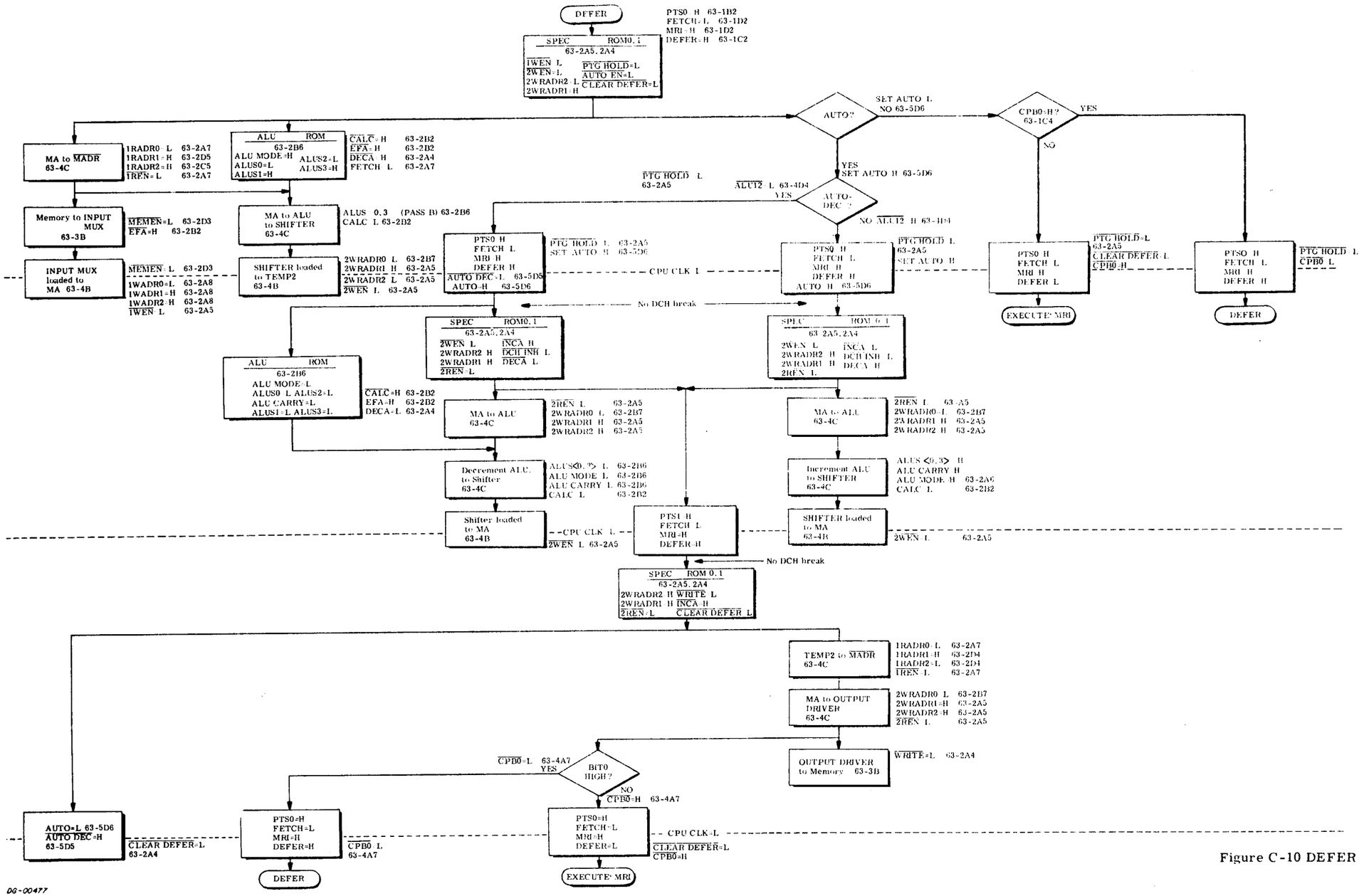


Figure C-10 DEFER Major State

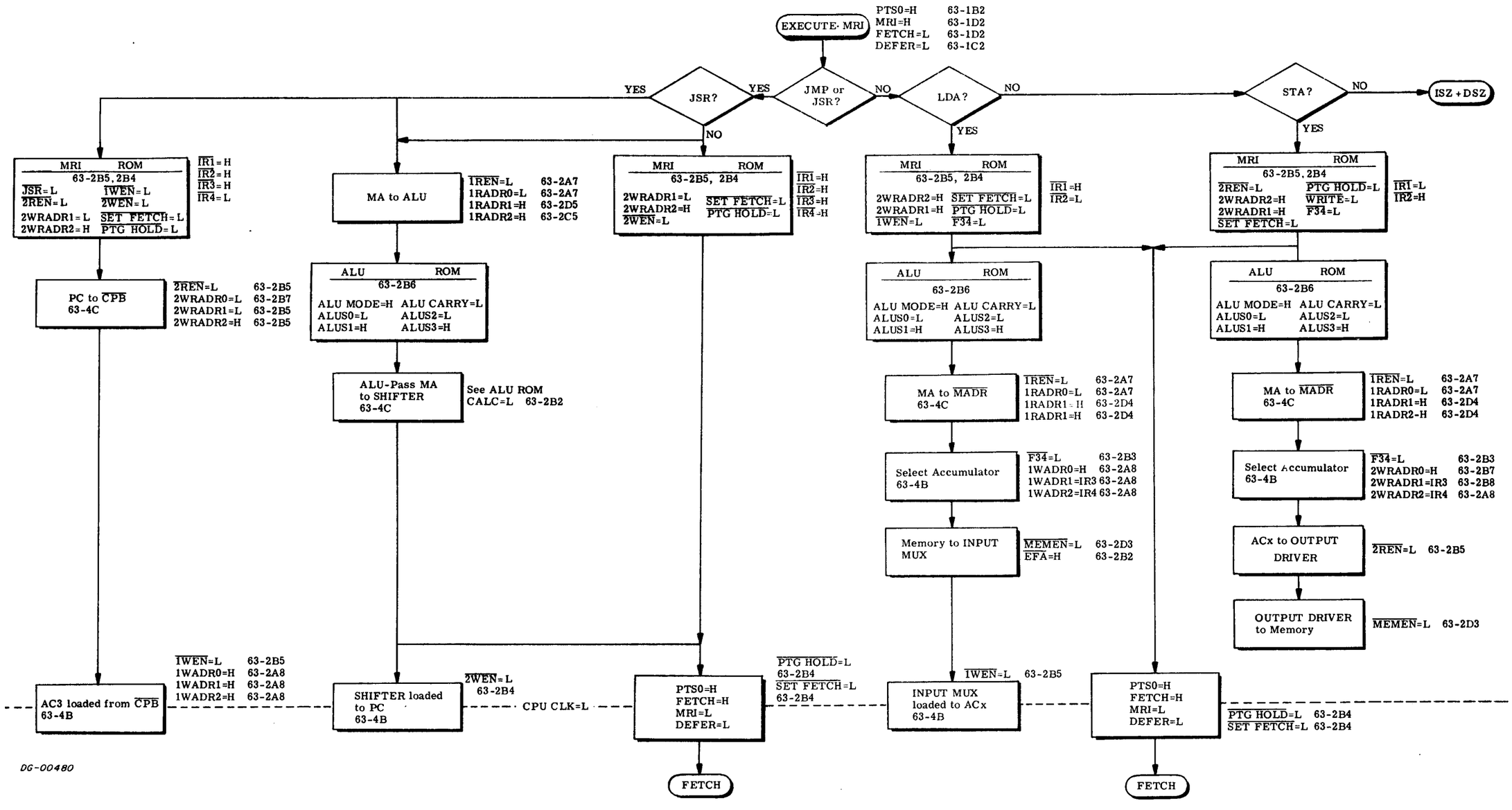


Figure C-11 EXECUTE·MRI Major State

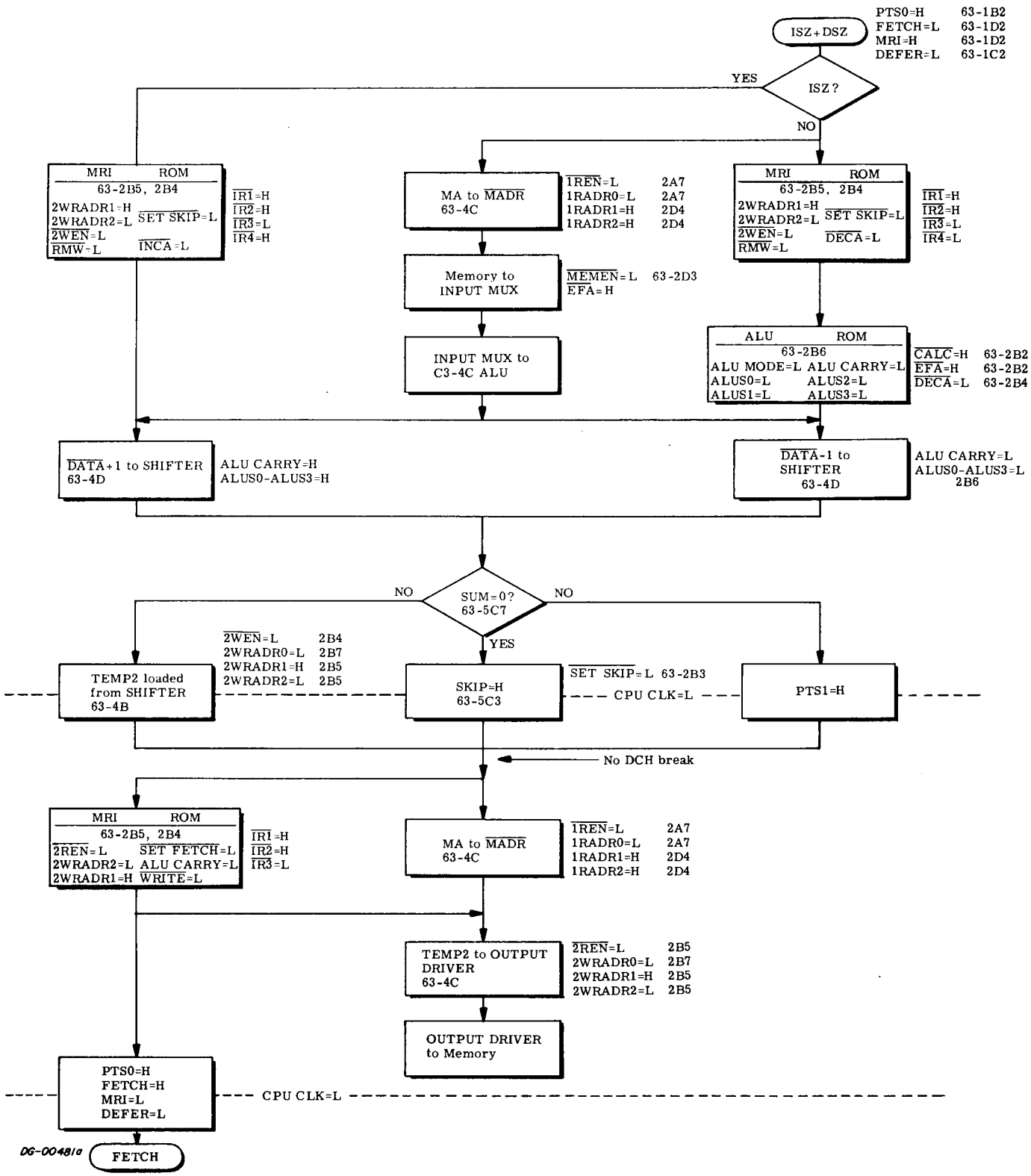


Figure C-12 EXECUTE·MRI Major State-ISZ+DSZ

C-25, C-26 missing

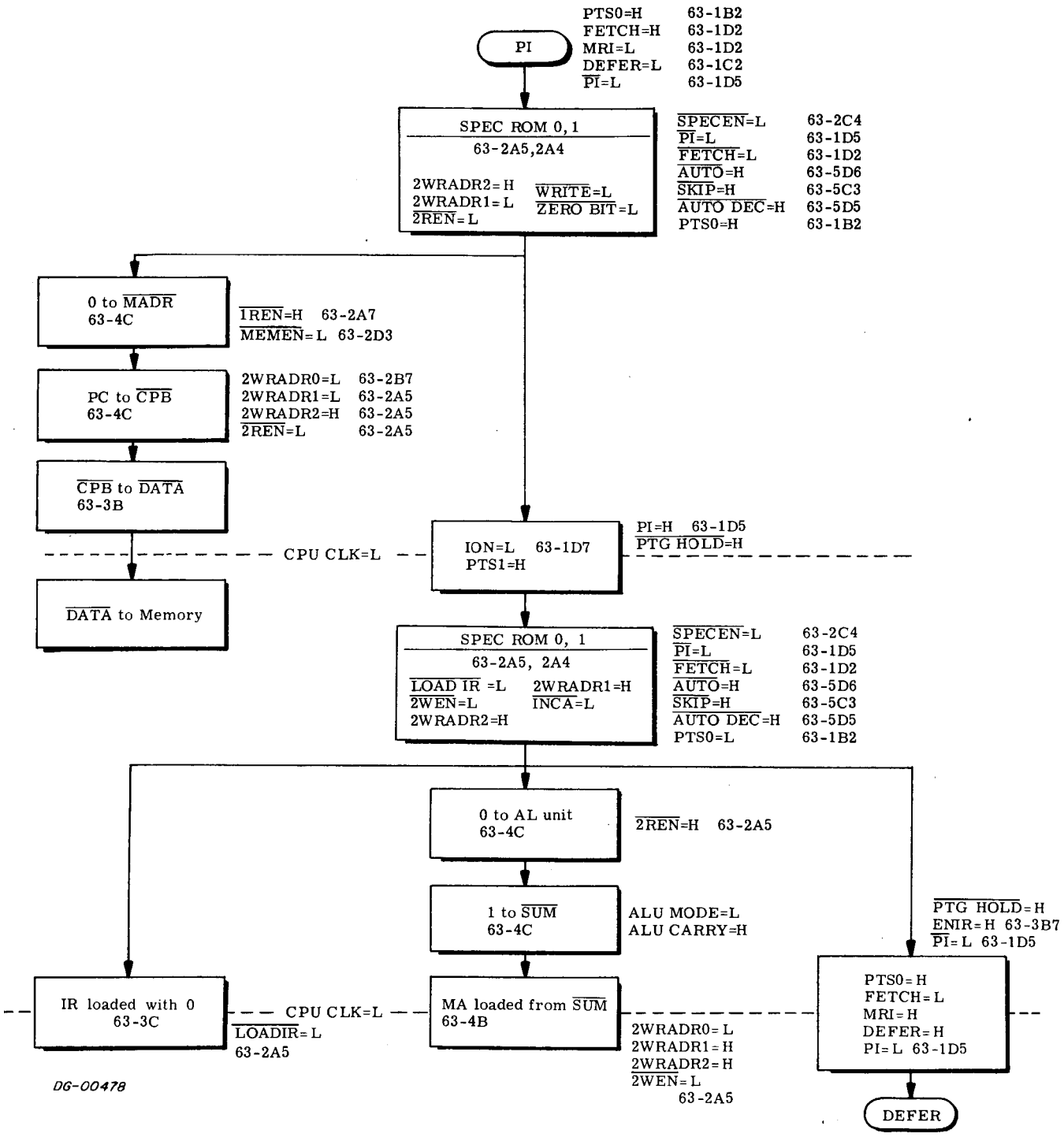


Figure C-14 PI Major State

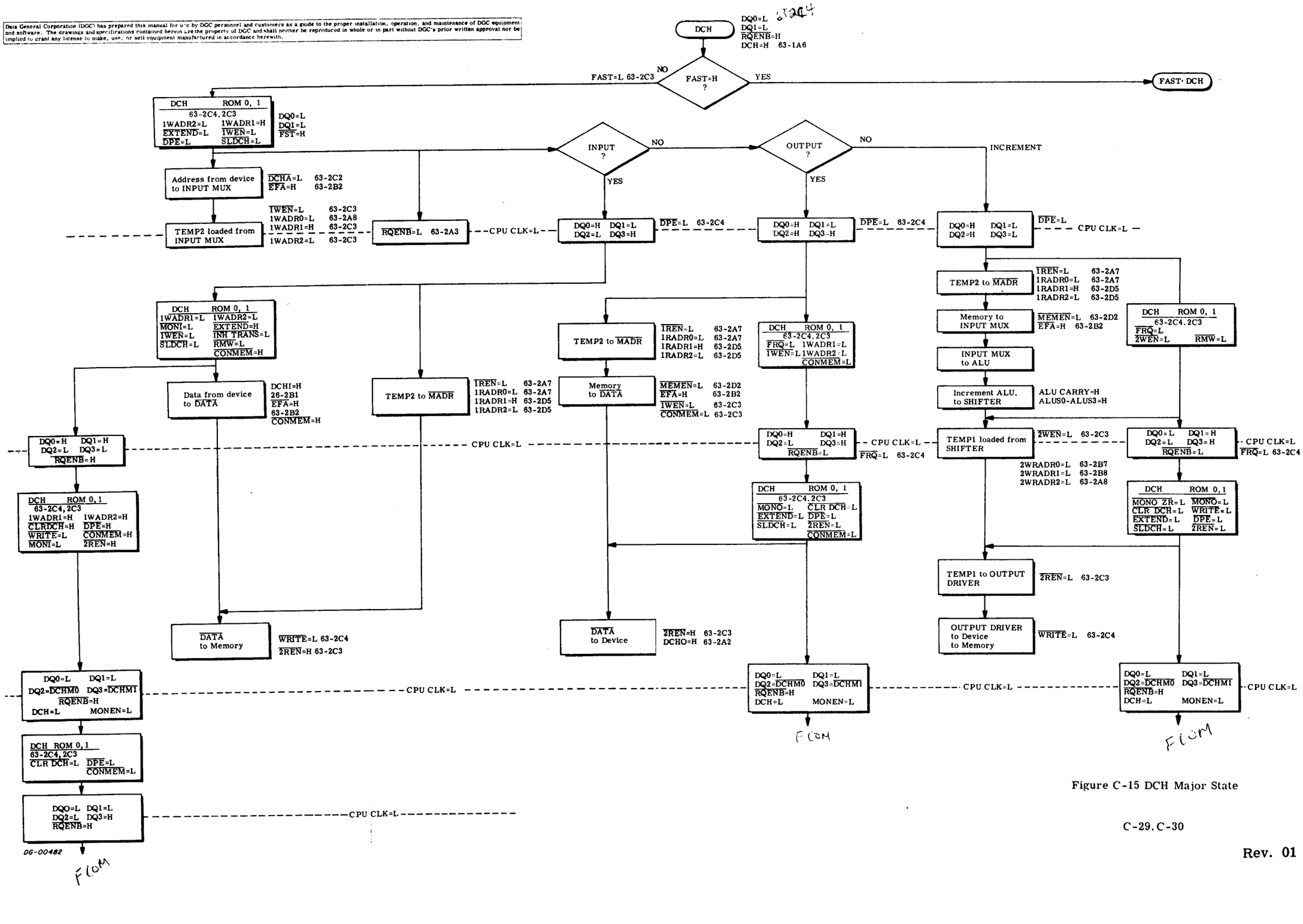


Figure C-15 DCH Major State

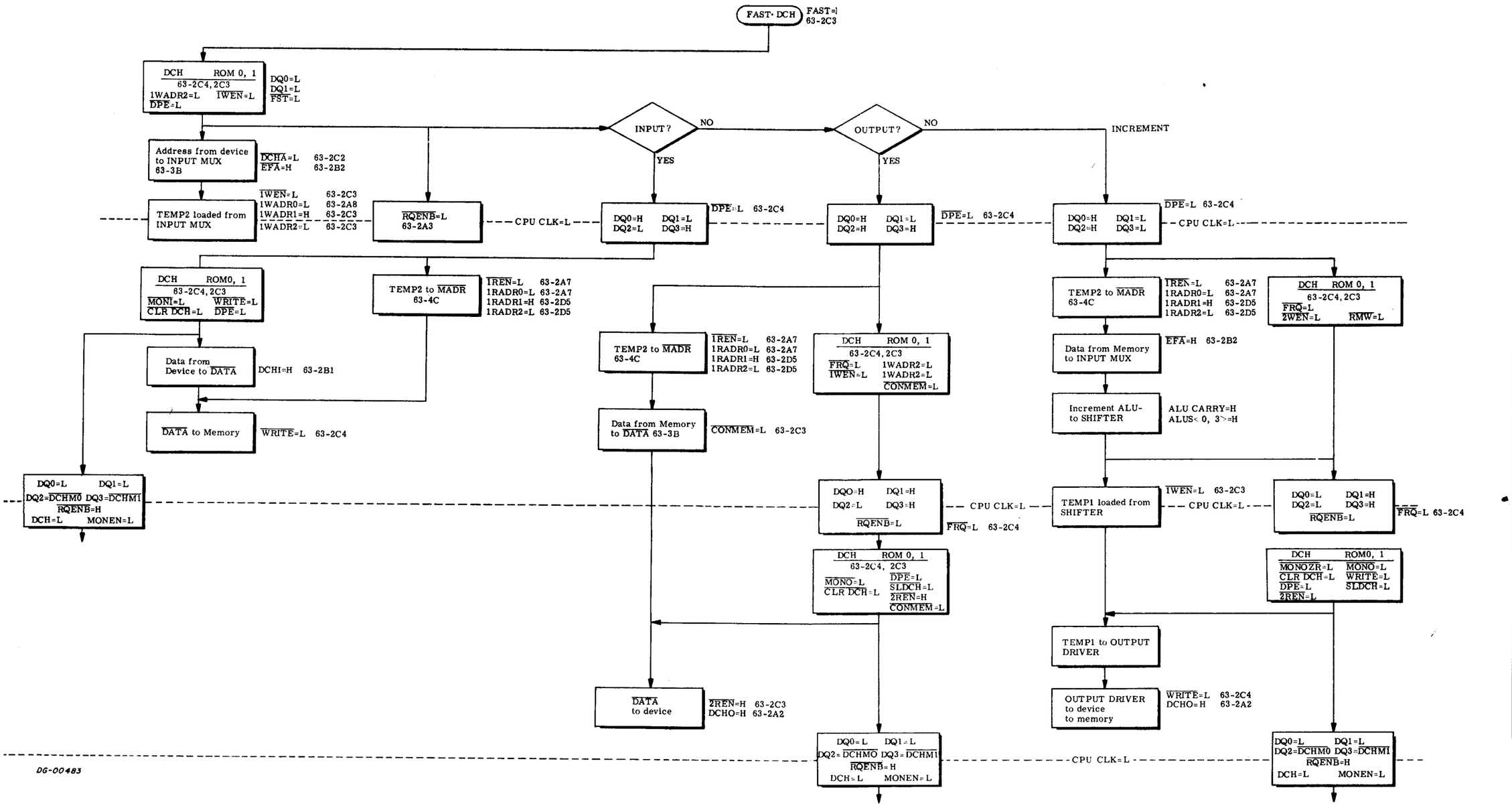


Figure C-16 DCH Major State - Fast Dch

SECTION K

CONSOLE

INTRODUCTION

The front panel of the console of the NOVA 2 displays useful information about the current state of the computer and includes the function switches necessary to operate the machine. A set of lights convey data concerning the internal operating state of the machine. A bank of fifteen address lights indicate the contents of the Memory Address Bus, and another bank of sixteen lights displays the current contents of the Data Bus.

The console, shown in Figure K-1, also includes a bank of sixteen data switches used to manually key in data or addresses to various registers. There are four accumulator switches used to examine or load accumulators. There are also switches to start and stop the machine and to alter or examine individual memory locations. All of the function switches, with the exception of the STOP/RESET switch, are locked out of operation when the machine is running, but the sixteen data switches are available to input data to the machine. A three position locking power switch allows the key to be removed, locking out all function switches while the machine is running.

A turnkey console is available as an option. This console, shown in Figure K-2, has only the locking key switch, RUN light, and PROGRAM LOAD, CONTINUE, START, and RESET switches.

CONSOLE LIGHTS AND SWITCHES

All of the lights in the console are continually drawing about 15ma each through series resistors, so their filaments are always hot (not glowing) and large surge currents are avoided when the filaments are driven on. The console block diagram, Figure K-3, shows the general relationship of the back panel buses and the console components.

Address Lights

These lights are always showing the logical state of the MADR bus, which is driven directly by the register file in the processor. When the machine is running, this output is continually changing, and as such is meaningless; after the machine is stopped, the contents of the PC register are output to the bus. After a memory step console function, the lights indicate the output of the 1REN port of the register file for the next processor CPU CLK period.

Data Lights

These lights always show the state of the DATA bus. When the machine is running, this bus carries data to and from the memory, processor, and I/O devices. When the machine is stopped, this bus contains the contents of the memory buffer of the last memory selected.

Console Operational Indicators

These lights are driven by gating the various signals that determine the major states of the processor. They function as follows:

RUN	is lit by the CPU signal RUN LIGHT whenever the processor is operating.
ION	is lit whenever processor interrupts are enabled.
FETCH	indicates that the processor is currently in the Fetch major state.
DEFER	is driven by the processor signal DLIGHT and indicates that the processor is currently in the Defer major state.
EXECUTE	indicates that the processor is currently in either the Execute·MRI or the Execute·$\overline{\text{MRI}}$ major state.

If neither FETCH, DEFER, nor EXECUTE is lit, the processor is currently in the EFA major state.

Data Switch Register

Each of these switches connects an open collector driver directly to a line of the $\overline{\text{DATA}}$ bus. The outputs of all drivers go low when the $\overline{\text{CON DATA}}$ level goes low; $\overline{\text{CON DATA}}$ is issued by the CPU during the READS instruction or during a console operation that requires input from these switches (such as EXAMINE).

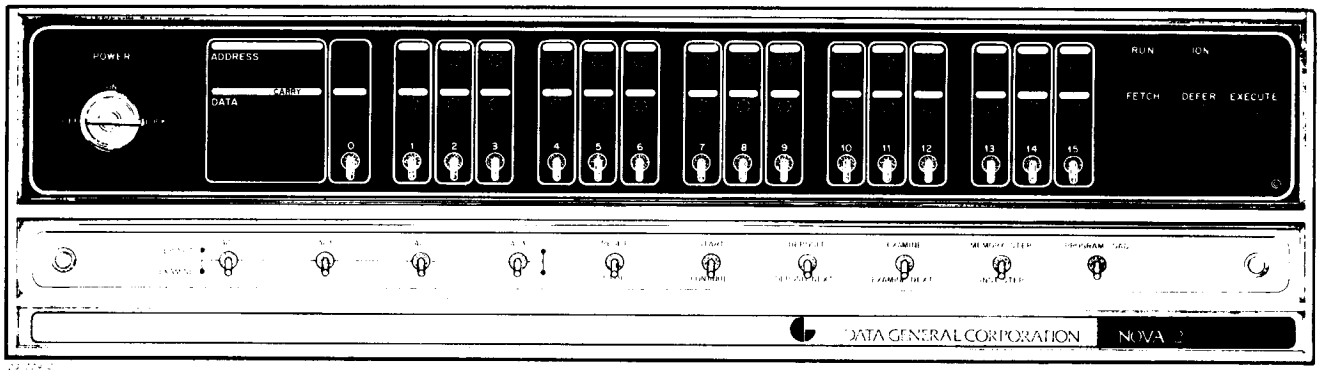


Figure K-1 NOVA 2 Console

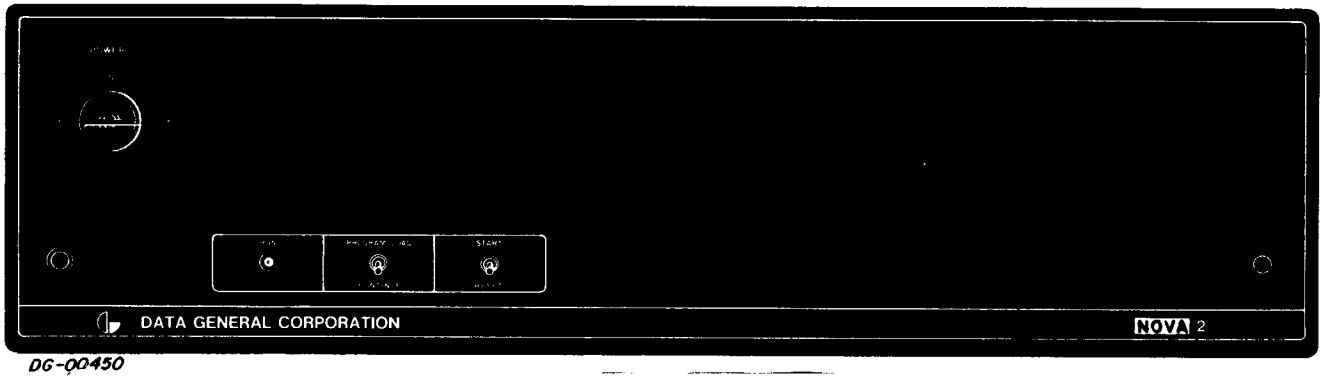


Figure K-2 NOVA 2 Turnkey Console

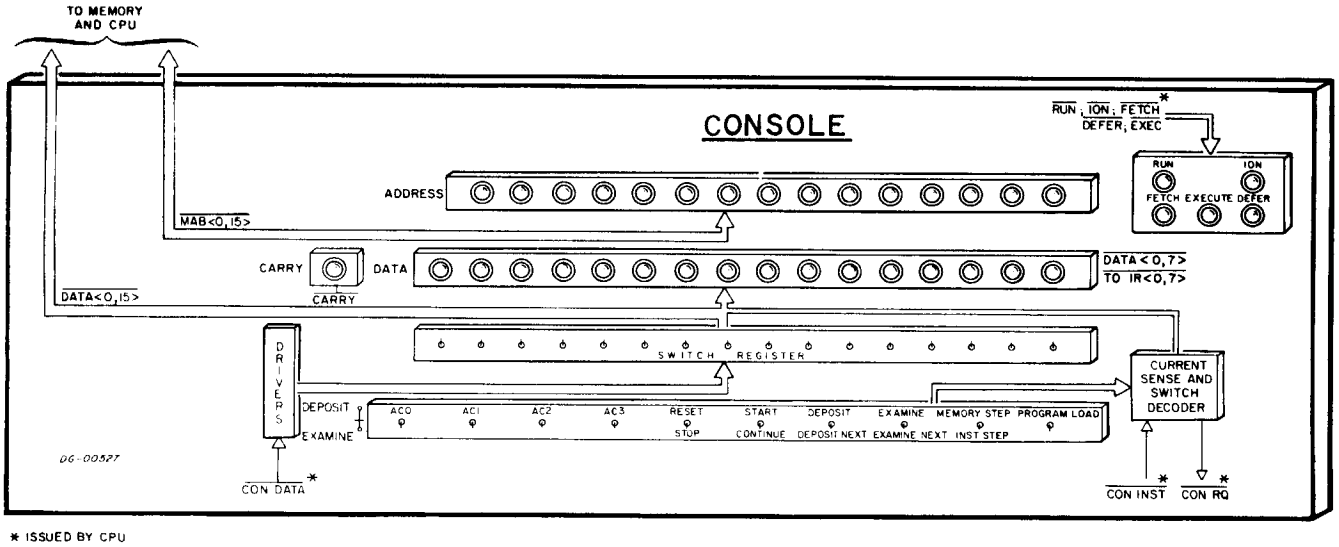


Figure K-3 Console Data Paths

Console Function Switches

All of the control switches except STOP and RESET are wired through pull-up resistors to a common circuit which detects current flowing through a switch, initiates a delay to suppress contact bounce, and issues the signal $\overline{\text{CONRQ}}$ to the central processor. This signal forces the processor (assuming that it was previously idle) into the KEY major state, and the processor follows the flow discussed in the processor section. At the console, the function switches are encoded through a diode matrix and the result is input to NAND gates which connect to $\overline{\text{DATA}}$ <0,7>. When $\overline{\text{CON INST}}$ is asserted by the processor, the NAND gates are enabled, and the function code, as shown in Table K-1, is asserted on $\overline{\text{DATA}}$ <0,7>. These lines are input to the instruction register and the processor completes the function. The RESET, STOP, MEMORY STEP, INSTRUCTION STEP, and PROGRAM LOAD switches are wired separately to the central processor.

The switch functions are as follows:

EXAMINE ACCUMULATOR — causes the contents of the selected accumulator to be loaded into the memory buffer of the last memory module accessed and displayed in the data lights.

DEPOSIT ACCUMULATOR — causes the contents of the switch register to be loaded into the selected accumulator and displayed in the data lights.

STOP — halts the processor at the end of the current instruction, and indicates the contents of the program counter in the data lights.

Table K-1

Console Function Switch Decoding

CONSOLE INSTRUCTION		IR0	IR1	IR2	IR3	IR4	IR5	IR6	IR7	IR8 TO 15
AC DEP.	AC0	0	0	1	0	0	0	1	1	0
	AC1	0	0	1	0	1	0	1	1	0
	AC2	0	0	1	1	0	0	1	1	0
	AC3	0	0	1	1	1	0	1	1	0
AC EXAM.	AC0	0	1	1	0	0	1	1	1	0
	AC1	0	1	1	0	1	1	1	1	0
	AC2	0	1	1	1	0	1	1	1	0
	AC3	0	1	1	1	1	1	1	1	0
DEPOSIT		1	1	0	1	1	1*	0	1	0
DEPOSIT NEXT		1	1	0	1	1	1*	0	0	0
EXAMINE		1	1	1	1	1	0	0	1	0
EXAMINE NEXT		1	1	1	1	1	1	0	0	0
MEMORY STEP		1	1	1	1	1	1	1	1	0
INSTRUCTION STEP		1	1	1	1	1	1	1	1	0
PROGRAM LOAD		1	1	1	1	1	1	0	1	0
START		1	1	1	1	1	0	1	1	0

WHEN BIT GOES FALSE

ACDP+ACEX

ACDP

DP.+DP. NEXT

AC SELECT ON ACDP+ACEX

DATA TAKEN FROM SWITCHES

MEMORY ACCESS

DEPOSIT NEXT + EXAMINE NEXT

ALWAYS FALSE ON KEY

DG-00036

*DATA ALSO TAKEN FROM SWITCHES

RESET	halts the processor at the next CPU CLK pulse and additionally initiates the machine state by setting or resetting the various flip-flops of the processor. The IORST pulse is also issued to all I/O devices, clearing their Busy, Done, and Interrupt Disable flags.
START	loads the contents of the data switches into the program counter and then begins normal processor operation with the instruction at that address.
CONTINUE	continues normal processor operation from the current machine state, regardless of the setting of the data switches.
DEPOSIT	deposits the contents of the data switches at the address specified by the current contents of the program counter. The address and data are displayed in the respective light banks.
DEPOSIT NEXT	increments the program counter and then stores the contents of the data switches at the new address indicated by the program counter. This address is displayed in the address lights, and the data is displayed in the data lights.
EXAMINE	loads the contents of the data switches into the program counter and then reads the contents of the address specified by the program counter, and displays the data in the data lights and the address in the address lights.
EXAMINE NEXT	increments the program counter, displays this new address in the address lights, reads the contents of that address, and displays the data in the data lights.
MEMORY STEP	takes the processor through one CPU CLK period. The processor always halts at the beginning of the next period, with CPU CLK low, so that the indicators on the console show conditions for the following period.
INSTRUCTION STEP	takes the processor through enough CPU CLK periods to complete execution of the current instruction. The processor is stopped at the beginning of the next FETCH major state.
PROGRAM LOAD	loads the bootstrap loader (if installed) into the first thirty-two locations in memory, and then begins normal execution starting at location 0.

Power Switch

The three position key-operated rotary switch controls power to the machine. In the OFF position, all power is removed from the power supply. The machine is powered up in the ON and LOCK positions. In the LOCK position, the STOP/RESET switch is disabled. In either the ON or the LOCK position, all of the other function switches are disabled during processor operation (i.e., when the RUN light is lit). The key may be removed from the switch when the switch is in the LOCK position. Note that the switch must be in the LOCK position in order for the auto-restart function of the power monitor to be functional.

REFERENCES

1. NOVA 2 Console Schematic
   D-001-000448-01.
2. NOVA 2 Turnkey Console Schematic
   D-001-000520-00.
3. How to Use the NOVA Computers
   015-000026.

This page left intentionally blank

SECTION P

POWER SUPPLY

INTRODUCTION

Function

The power supply converts the available ac primary power to the dc voltages required by the computer. The power supply also monitors these dc voltages and shuts down the computer when they fail.

Regulators

Two important design parameters for a computer power supply are the output voltage regulation and the current capacity. In order to provide a constant dc level, some form of magnetic or electronic regulation is usually necessary. In smaller power supplies, a linear series-pass transistor generally provides electronic regulation, but has poor efficiency. At the higher current levels associated with a computer, the losses may become excessive, and for this reason the switching regulator is often used, as in the NOVA 2/4. At still higher current levels, as in the NOVA 2/10, the constant voltage transformer offers an economical alternative to electronic regulation, although a series-pass regulator is used for the memory drive. The description of the power supplies of the NOVA 2/4 and 2/10 are preceded here by a study of the two regulators used and the constant voltage transformer.

Series-Pass Regulator

The series-pass regulator serves to control the output voltage of a power supply by controlling current flow. The output voltage is monitored and the current flow is adjusted to maintain the desired voltage.

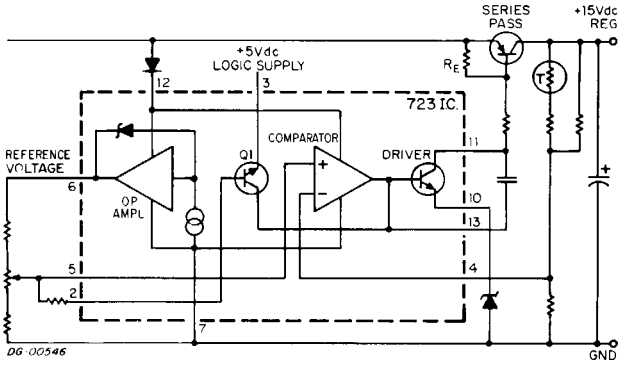


Figure P-1 Series-Pass (linear) Regulator

In operation, referring to Figure P-1, a 7.15 volt reference is developed by the operational amplifier and the zener diode. This reference voltage is divided and applied to the non-inverting (+) input of the comparator. The +15Vdc output voltage of the regulator is divided and applied to the inverting (-) input of the comparator. The output of the comparator, proportional to the difference between the divided reference voltage and the divided output voltage, causes a proportional current flow in the driver. This current causes a voltage drop across R_e, which determines the drive on the series pass transistor. To assure that the memories are shut down before the logic stops functioning in the event of a power failure, cut-off transistor, Q1, conducts and shuts off the driver whenever the +5Vdc logic supply falls appreciably below the divided reference voltage.

Series-Pass Switching Regulators

A series-pass switching regulator is essentially a multivibrator which sets when a low output voltage is detected and resets when a high output voltage is detected. When the regulator is set, current is gated from the 30V non-regulated supply into an LC circuit. When the regulator is reset, current flow is stopped and the load draws power from the LC circuit until the voltage drops to a level that sets the regulator again. The frequency at which the regulator toggles in this manner varies from 5 to 15kHz, depending on the load. Figures P-2 and P-3 show series-pass switching regulators for +5Vdc and +15Vdc in simplified form, including brief operation descriptions.

Constant Voltage Transformer

The operation of the constant voltage transformer (CVT) is based on the principle of the saturable reactor, with a magnetic shunt. What follows is a discussion of this operation. In the process of describing the constant voltage transformer, the operation of a conventional transformer will first be investigated.

In a conventional transformer (see Figure P-4) the sinusoidal primary voltage, V_p, causes a current flow, I_p, through the primary winding. This primary current is limited by the existence of a back emf, E_p, the reverse voltage induced on the primary winding by the varying magnetic flux, ϕ, within the core. The primary current is generally proportional to the difference between V_p and E_p. This same flux also induces a voltage on the secondary winding, E_s, which is related to E_p by the

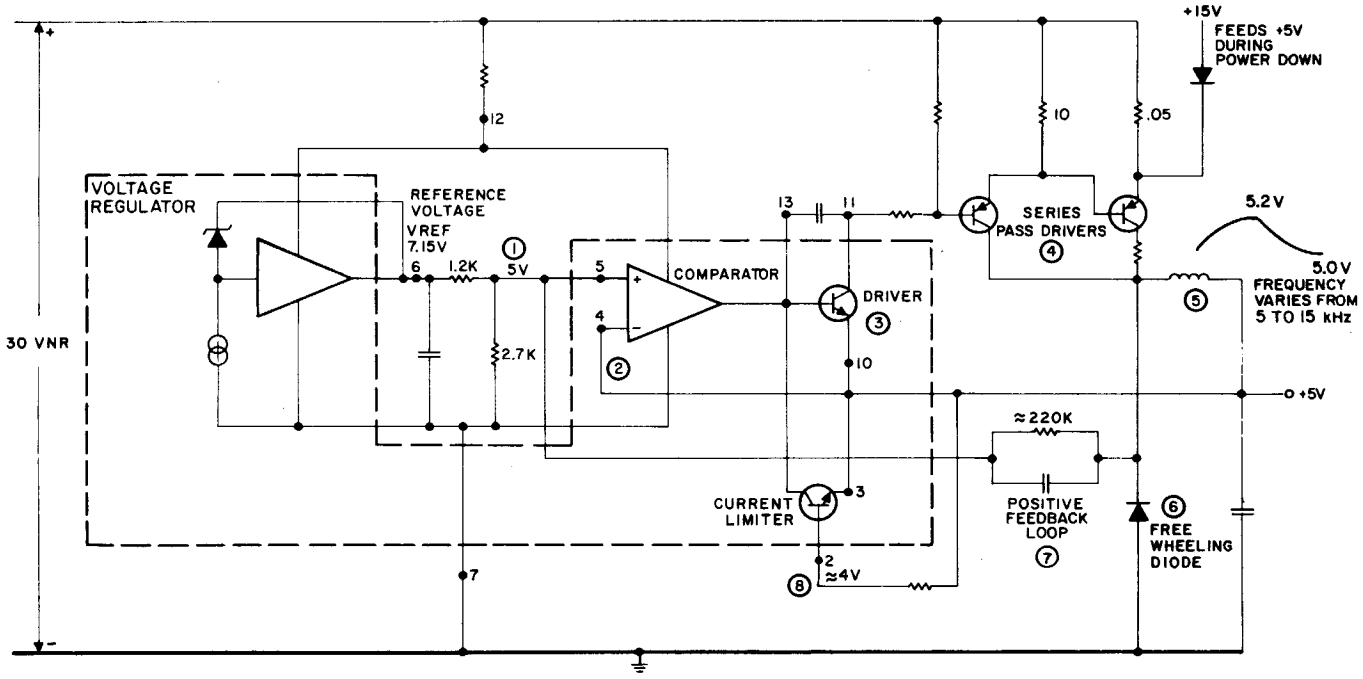


Figure P-2 Simplified Schematic of the +5Vdc Series Switching Regulator. When the comparator senses a difference between the (divided) reference voltage (1) and the output voltage (2) it switches, turning on the driver transistor (3) and consequently the serier pass transistors (4). Current is shunted through the series pass transistors to the coil, output capacitor and load (5). The output voltage rises, reducing the error voltage to the comparator, which resets, turning off the driver (3) and consequently the series pass transistors. Now the load is supplied from power stored in the LC circuit. The back emf developed across the coil as a result of this switching is dropped across the free wheeling diode (6). Note that each time the comparator is forced to switch it is driven into saturation by the positive feedback loop which includes the 220K resistors (7).

The current limiter (8) turns on if the output voltage drops below about 4V, turning the driver (3) and subsequently the series pass transistors (4) off. The supply is latched in this state until power is removed and then returned.

The diode at (9) feeds the 15V into the -5V supply during power down, forcing the 15V to drop faster but the +5V to the IC's to hold longer. The memory driver supply is switched at (9) of Figure P-3, when the 15V drops too low.

turns ratio, where N_p and N_s are the number of turns on the primary and secondary, respectively, and

$$E_s = \frac{N_s}{N_p} E_p$$

A current, I_s, which is proportional to the load will flow in the secondary. Both the primary current and the secondary current will cause magnetization forces, H_p and H_s, each proportional to the product of the current and the number of turns in that winding. The algebraic sum H_p-H_s, of these forces will always be positive, and it is this net magnetization force that causes the flux in the core. It is important to realize that for a given transformer and primary voltage, the net flux is a constant. Since the flux is proportional to the net magnetization force, it is apparent that this value must also be constant. Therefore, as the secondary current and thus the secondary magnetization force vary, the primary current and the primary magnetization force must vary by the same amount. In this way an increased load is reflected back to the primary.

If the primary voltage, V_p, changes, the net flux must make a similar adjustment, so that the induced voltage on the primary will be essentially equal to the applied voltage. Since the same flux

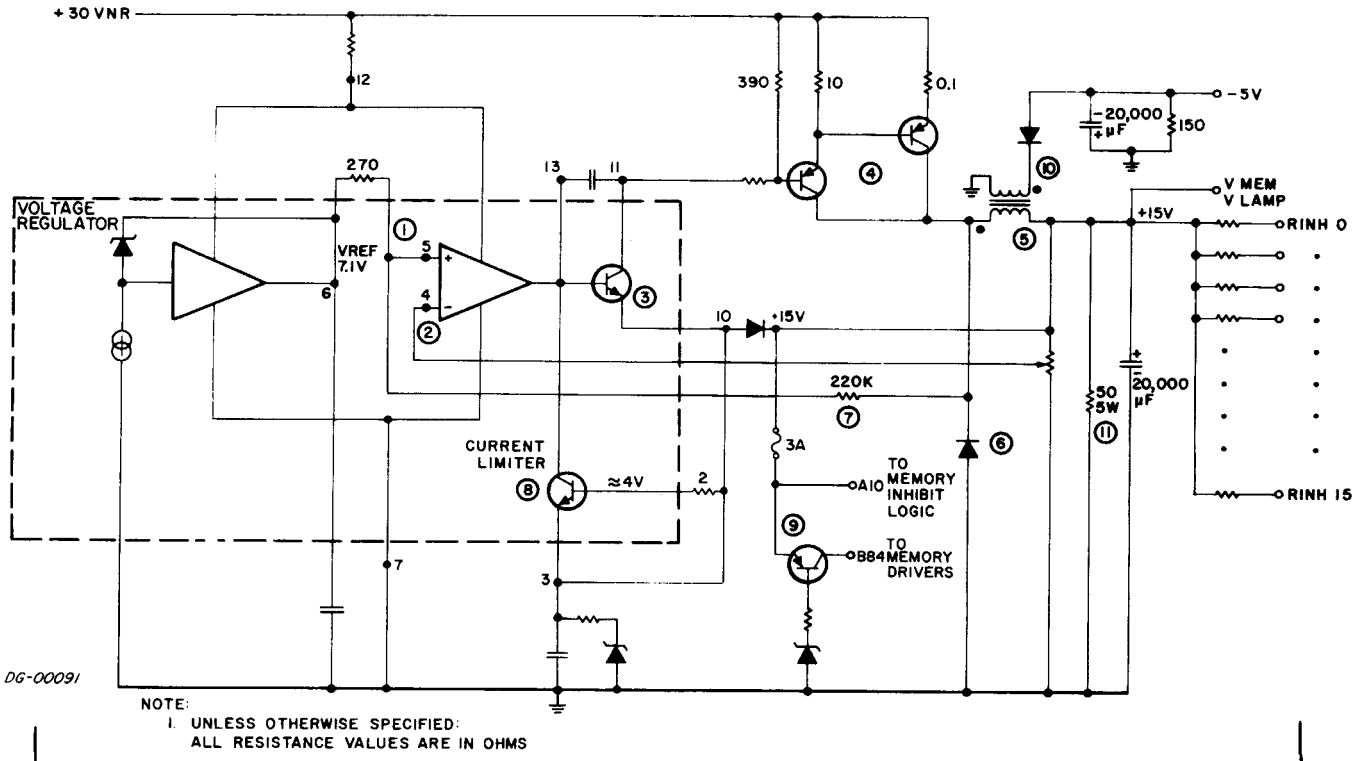


Figure P-3 Simplified Schematic of the -15Vdc Series Switching Regulator and the -5V Supply. When the comparator senses a difference between the reference voltage (1) and the divided output voltage (2), it switches, turning on the driver transistor (3) and consequently the series pass transistors (4). Current is shunted through the series pass transistors to the coil, output capacitor and load (5). The output voltage rises, reducing the error voltage to the comparator, which resets, turning off the driver (3) and consequently the series pass transistors. Now the load is supplied from power stored in the LC circuit. The back emf developed across the coil as a result of this switching is dropped across the free wheeling diode (6). Note that each time the comparator is forced to switch it is driven into saturation by the positive feedback loop which includes the 220K resistor (7).

The current limiter (8) turns on if the output voltage V MEM drops too low, or if the current at either terminal of (9) (memory inhibit and memory drive) is too high. When on, the current limiter turns off the driver and subsequently the series pass transistors, latching the supply into this mode until power is removed and then returned.

The transistor at (9) will switch off when the -15V drops too low for memory to function properly, thus removing power to the memory drivers.

The -5V is generated through the 3:1 transformer at (10). The 50Ω resistor at (11) guarantees -5V (i.e., voltage across the coil) during No Load.

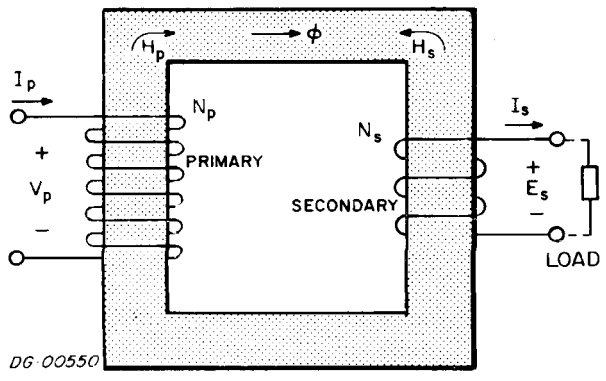


Figure P-4 Conventional Transformer Construction

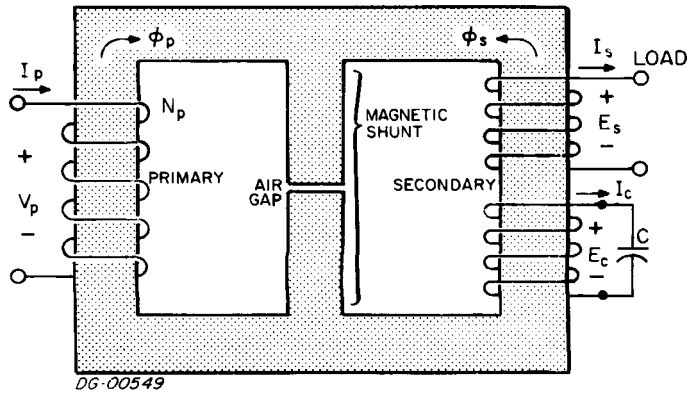


Figure P-5 Constant Voltage Transformer Construction

links both the primary and secondary windings, the induced voltage on the secondary will vary so that it is still defined by the turns ratio discussed earlier. Thus, any variations in the primary voltage will be evident in the secondary.

The constant voltage transformer incorporates two modifications to the conventional transformer (see Figure P-5). The first is a change in the core design to include a magnetic shunt between the primary and secondary windings. This shunt has a small air gap in its length, so that its magnetic reluctance (the magnetic equivalent of electrical resistance) is greater than that of the outer path through the core. Under ordinary circumstances, most of the flux would link both windings. Referring to the figure, this implies that $\phi_p = \phi_s$, similar to the situation of the conventional transformer. Until the second modification is made, the operation of both transformers would be essentially the same.

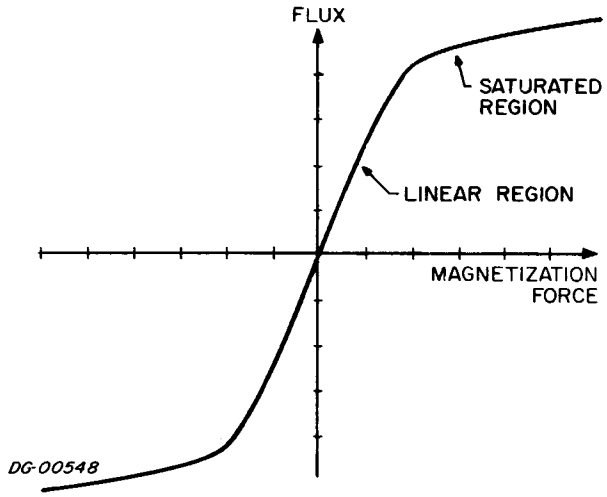


Figure P-6 Magnetic Flux as a Function of Magnetization Force

The second modification is to attach a capacitive load either to a separate secondary winding (as shown in the figure), or across a portion of the main secondary winding. As before, the flux linking the primary coil must be sufficient to induce a voltage approximately equal to the applied voltage. This is always a necessary condition. The capacitor on the secondary will cause a large reactive current to flow in the secondary, which will in turn cause a large magnetization force. This flux will link the primary winding, but will be in a direction to induce a voltage opposite to the applied voltage, causing an increased current flow. This current flow, in turn, will cause a larger flux to flow from the primary. This increased primary flux now tends to link only the primary coil, flowing through the shunt instead of linking the secondary. This is due to the fact that the secondary core has already been saturated by the high secondary current. It is now possible for a much greater flux to link the secondary windings than links the primary, so that the secondary voltage developed will be greater than would be indicated by the turns ratio between primary and secondary.

Since the secondary flux in this configuration is so great, the core is actually operating in the saturated portion of its ϕ-H curve (see Figure P-6). Therefore, a large change in in magnetization force produces only a small change in flux. If the primary voltage, V_p, were to vary, the current, I_p, would also vary and the primary flux would adjust as necessary to induce a voltage E_p approximately equal to V_p. However, since the secondary core is saturated, the increased magnetization force would cause only a small increase in secondary flux, and, thus, in secondary voltage. The constant voltage transformer requires a minimum load at all times. If the load is reduced below this minimum, the output voltage of the transformer will tend to rise. Figure P-7 shows a three transistor shunt which maintains a minimum load to prevent this.

In operation, the base of transistor Q1 is clamped by the zener diode at 5.1 volts. This transistor will be off until the voltage on the collector (output of voltage divider) rises to approximately 0.7 volt higher than this (5.8 volts). At this point, Q1 will conduct, raising the base voltage on Q2, and causing it to conduct. As the collector voltage of Q2 falls, the feedback loop, R_f, will tend to drive the base of Q1 lower, raising its base-emitter voltage, and causing it to saturate. At the same time the current flow through R_C will cause a voltage drop which raises the base-emitter voltage of Q3 sufficiently to cause that transistor to turn on and saturate. The current drawn by Q3 is essentially given by V_{CC} divided by R_L. This circuit will remain in this state until V_{CC} falls low enough that the base-emitter voltage of Q1 falls below 0.7 volt.

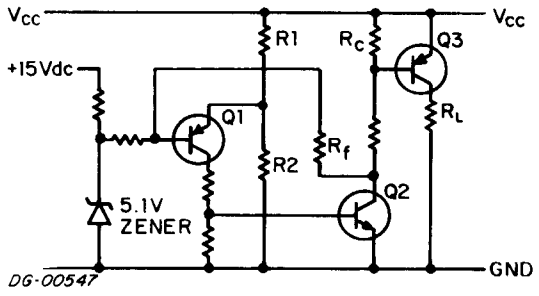


Figure P-7 Transistor Shunt for CVT

Power Supply Monitors

In the event of a power failure, it is essential that the hardware be shut down in an orderly manner. A unit called the power fail module performs the function of monitoring the various supply voltages and detecting a drop in any voltage level below the nominal range for that level. It halts the processor as the power available becomes marginal. Additionally, if the Power Monitor and Auto Restart is installed in the processor, the processor is interrupted just as the power begins to falter, but is sufficient time (on the order of 1 to 2 msec) to allow the software to prepare for a "soft" shut down before the power becomes marginal .

NOVA 2/4 POWER SUPPLY

The main functional component of the NOVA 2/4 power supply is the series-pass switching regulator. The supply furnishes sufficient power to drive four Data General circuit boards, that is, a central processor and three memories, controllers, or other assemblies.

Configuration

The transformer used in the NOVA 2/4 power supply has a split primary winding to allow operation from either a 115 volt source or a 230 volt source. The two windings are wired to the source in parallel for 115Vac operation, and in series for 230Vac operation. The cooling fan always operates from 115Vac so is wired across only one primary winding of the transformer.

A single 30 volt secondary winding drives a bridge rectifier which supplies unregulated 30Vdc. This 30 volt supply drives two series-pass switching regulators, described earlier, which produce +5Vdc, -5Vdc, and +15Vdc regulated outputs.

Distribution

All power is supplied to the various printed circuit boards via the back panel etch. The +5Vdc for the logic is supplied to the boards through back panel connections A3, A4, A97, A98, B3, B4, B97, and B98. The -5Vdc is supplied to all circuit boards except the central processor board through back panel pin A6. The teletype connector also is supplied -5Vdc. Console lamps and memory X, Y, and inhibit lines are all supplied with +15Vdc. The lamps are supplied by connector number 33 on the console connector. The X and Y drivers for the memory stacks are supplied through back panel pins B46 and B84. The inhibit drivers receive their power through back panel connectors A10 and A24.

Mounting

The NOVA 2/4 power supply, shown in Figure P-8, can be divided into two subassemblies. Mounted on the chassis itself are the transformer, bypass capacitors, and other major components. The dc filter capacitors, regulator coils, power fail module, and various small components are found as part of the back panel assembly, where the distribution etch is located.

Fuses

There are three fuses in the NOVA 2/4 power supply. The 5A (3A for 230Vac) line fuse, mounted on the rear chassis panel, protects the primary supply from faults occurring in the rectifier bridge, transformer, or primary wiring. The 10A secondary fuse, mounted on the inside of the back panel as shown in Figure P-8, protects the bridge assembly and transformer from faults occurring in the regulators. In the event of a fault on a circuit board, the respective regulator will detect the over-current condition (actually characterized by a low-voltage condition), remove the drive from the series-pass transistors and latch in this mode until power is removed from the supply. If the voltage on either the +5Vdc or the +15Vdc line should rise too high, the crowbar circuit shown in Figure P-9 will shut the supply down. This is accomplished by triggering the SCR, which effectively shorts the 30 volt output of the bridge rectifier to ground and blows the secondary fuse. A 3A fuse, also mounted on the inside of the back panel, protects the +15V memory lines.

Primary Requirements

The NOVA 2/4 should be powered from a source of 115Vac or 230Vac at a frequency of from 47 to 63Hz. The voltage tolerance is ±20%. The primary supply capacity should be greater than 10A for a 115 volt supply and greater than 5A for a 230 volt supply. It is imperative that the transformer be wired properly for the primary supply voltage. The computer is equipped with a standard 3-wire power cord, and it is essential that the third (green) wire be connected to a solid earth ground.

Specifications

The NOVA 2/4 power supply, under normal operating conditions, is capable of delivering 12A at 5Vdc, 0.8A at -5Vdc, and 6A at 15Vdc.

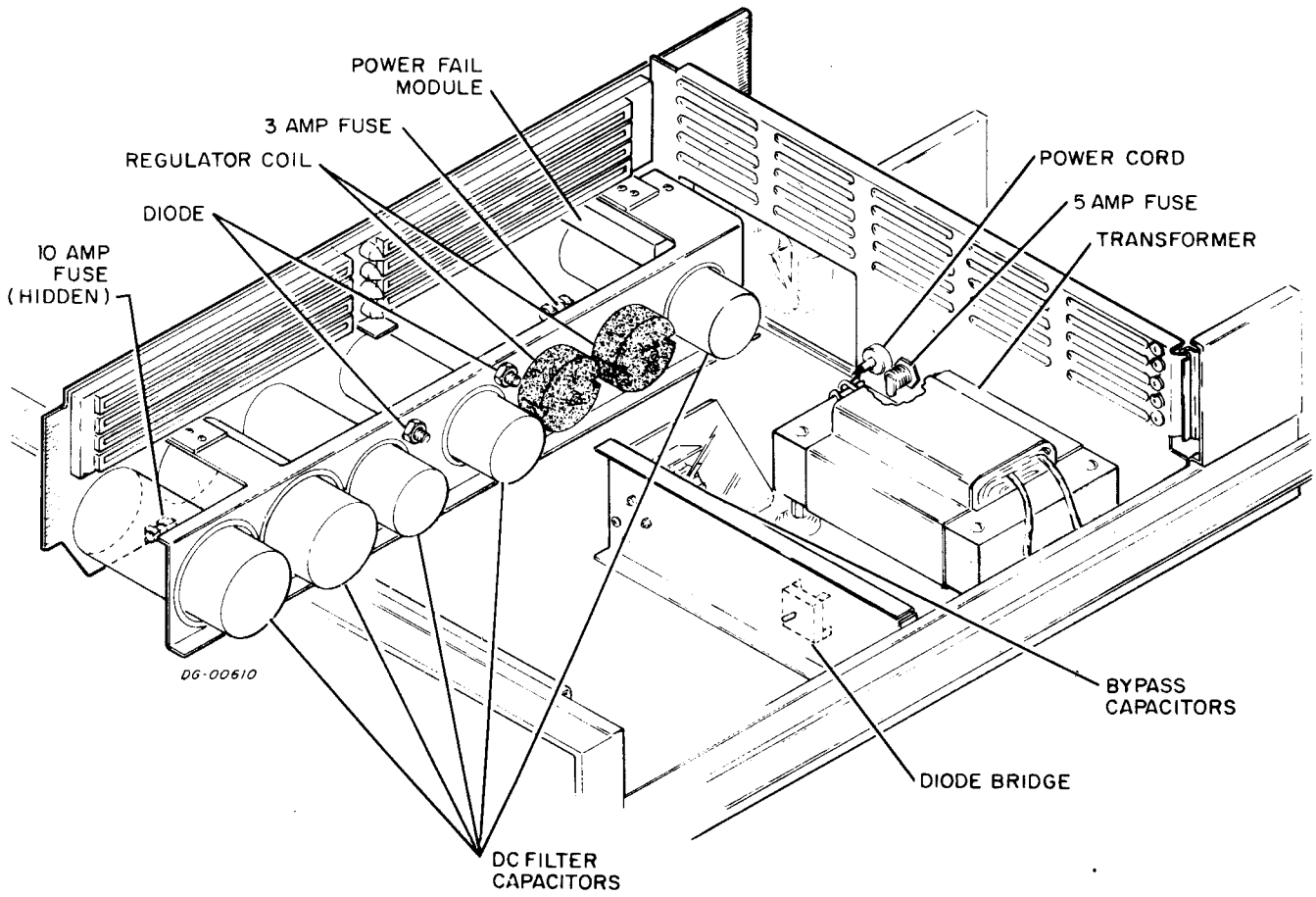


Figure P-8 NOVA 2/4 Power Supply Components

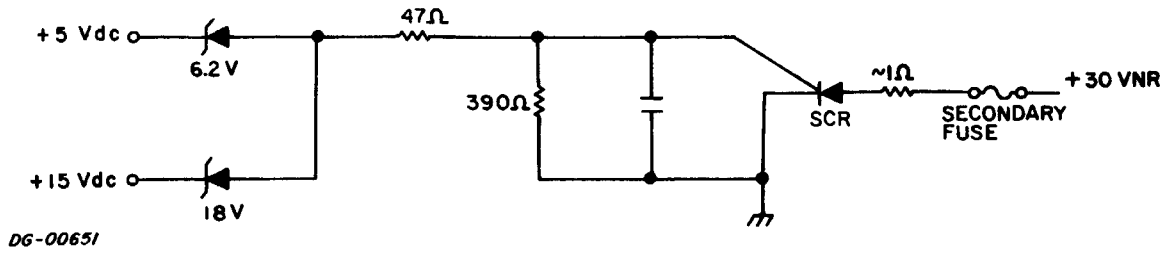


Figure P-9 "Crowbar" Circuit

Power Fail Module

The power fail module monitors the operation of the NOVA 2/4 power supply and furnishes status information to the processor. Both the +5Vdc output voltage and the +30Vdc non-regulated output of the bridge rectifier (+30VNR) are monitored. There are three status signals, $\overline{\text{PWR FAIL}}$, PWR OK, and +5V OK.

During a power failure, the $\overline{\text{PWR FAIL}}$ signal will be asserted as soon as the output of the bridge rectifier falls to +24volts. (See the processor section of this manual for a discussion of the actions taken by the processor in response to these various signals.) The PWR OK signal is cleared when the +5Vdc voltage falls below +4.7volts. The +5V OK signal is cleared as the last step of the power-down sequence, as the +5Vdc line continues to fall.

As the supply is powered back up, the +5V OK signal sets as the +5Vdc line approaches its normal range. When the +5Vdc line reaches +4.7volts, the PWR OK signal is asserted and the $\overline{\text{PWR FAIL}}$ signal is cleared.

NOVA 2/10 POWER SUPPLY

The NOVA 2/10 power supply is based on the constant voltage transformer. The regulation of this transformer is sufficient to make further regulation of the dc voltages unnecessary, with the exception of the supply for the memory X and Y drivers. The supply furnishes sufficient +5Vdc current to power a NOVA 2 central processor plus a full complement of Data General memories, controllers, and other boards.

Configuration

The constant voltage transformer used in the NOVA 2/10 supply has a split primary winding to allow operation from either a 115 volt source or a 230 volt source. The two windings are wired to the source in parallel for 115Vac operation, and in series for 230Vac operation. The two cooling fans always operate from 115Vac so are wired separately across the two primary windings. Two secondary windings, a 10-volt center-tapped and a 30-volt center-tapped, supply power, via the remaining power supply components, to the memory stacks and logic on the various circuit boards.

The 10 volt winding drives dual full-wave rectifiers which supply +5Vdc and -5Vdc. The -5Vdc is filtered and made available on the back panel. The unfiltered +5Vdc is monitored by the power fail module. This same winding also drives another full-wave rectifier to produce +5Vdc for the logic supply. Because of the self-regulation of the constant voltage transformer, no electronic regulation is necessary for this supply. As described earlier there are two three-transistor shunts across the rectified outputs to maintain a minimum load to the transformer.

The 30 volt winding drives dual full-wave rectifiers supplying +15Vdc and -15Vdc. The -15Vdc is supplied filtered to a back panel pin. The +15Vdc is filtered to power the memory inhibit lines and console lamps. A series-pass regulator provides +15Vdc to drive the memory X and Y lines. As with the +5Vdc supply, there is a three-transistor shunt across the +15Vdc supply to maintain a minimum load on this winding of the transformer.

Distribution

All power is supplied to the various printed circuit boards via the back panel etch. The +5Vdc for the logic is first passed through four fuses protecting sets of printed circuit boards. The power is supplied to the boards through back panel connections A3, A4, A97, A98, B3, B4, B97, and B98. The -5Vdc is supplied to all circuit boards except the central processor board through back panel pin A6.

The Teletype® connector also is supplied -5Vdc. Console lamps and memory X, Y, and inhibit lines all are supplied with +15Vdc. The lamps are supplied by connector number 33 on the console connector. The X and Y drivers for the memory stacks are supplied through back panel pins B46 and B84. The inhibit drivers receive their power through back panel connectors A10 and A24.

Mounting

As seen in Figure P-10, the NOVA 2/10 power supply can be divided into three subassemblies. At the rear of the chassis is found the power transformer and other major components. The dc filter capacitors are mounted to the power supply printed circuit board, where the majority of the smaller components are found. This printed circuit board, the power fail module, +5Vdc fuses, and various other small components are found on the back panel, where the distribution etch is located. In order to provide a modular construction, these major divisions, as well as the major components at the rear of the chassis, are interconnected with male/female connectors.

Teletype® is a registered trademark of Teletype Corporation, Skokie, Illinois. All references to teletypes in this manual shall apply to this mark.

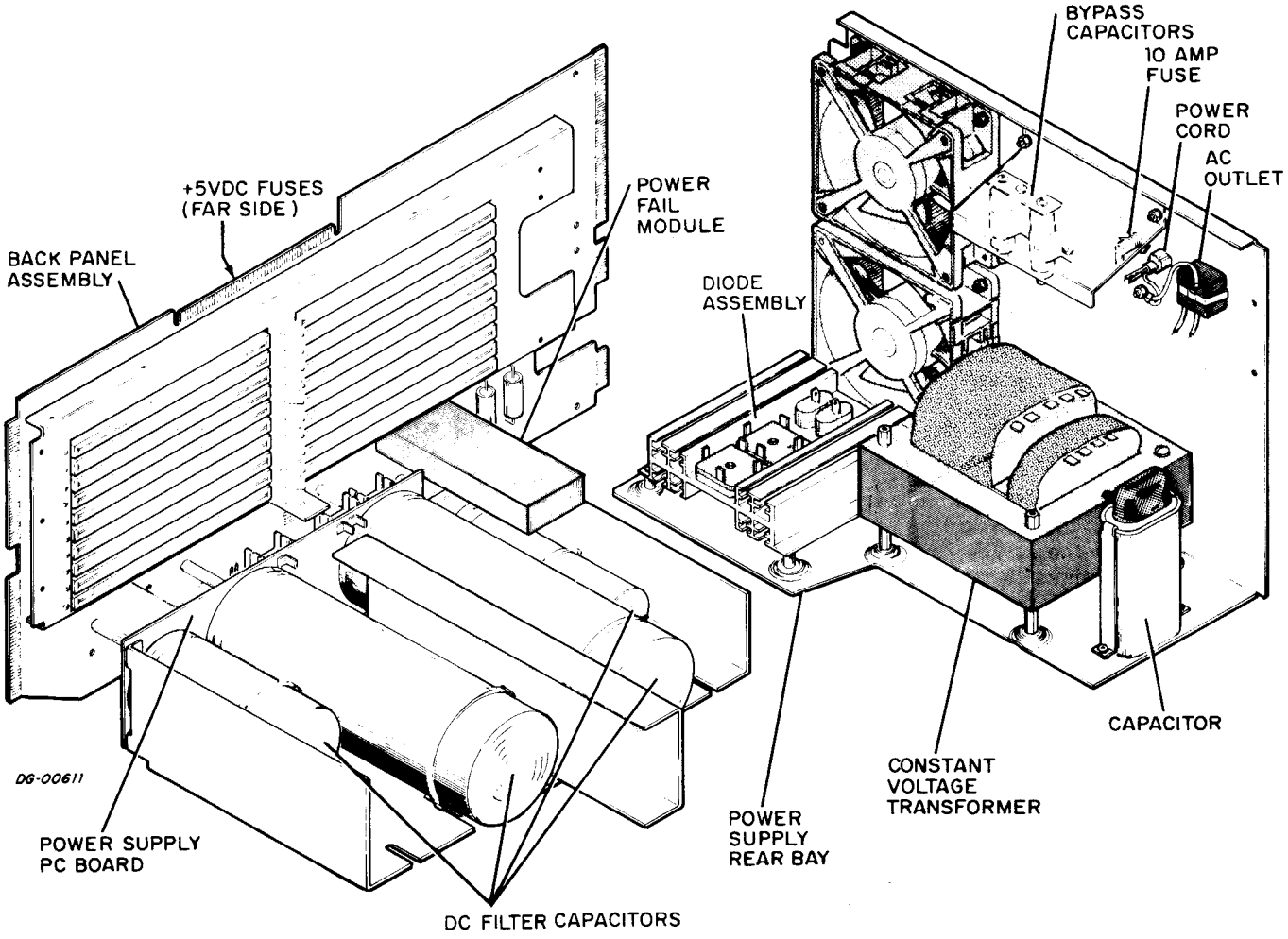


Figure P-10 NOVA 2/10 Power Supply Components

Fuses

The constant voltage transformer in the NOVA 2/10 is inherently current limiting, and so lessens the need for current protection for the power supply. The primary consideration is to protect the printed circuit boards against high currents or voltages which could potentially burn the etch or damage the integrated circuit chips. Fusing in the 2/10 exists at two levels. The first is the 10A line fuse, which is mounted on the rear chassis panel. This fuse protects the primary power source from faults in the primary circuit of the power supply. The remainder of the fusing is found on the outside of the back panel. These are the 10A and 15A fuses in the +5Vdc lines to protect the logic boards.

Primary Power Requirements

The NOVA 2/10 should be powered from a source of 115Vac or 230Vac at either 50Hz or 60Hz. Tolerances are ±1Hz for the frequency and ±20% for the voltage. The primary supply capacity should be greater than 10 amperes for a 115 volt supply, and greater than 5 amperes for a 230 volt supply. Because the constant voltage transformer is frequency sensitive, the frequency should not deviate beyond this tolerance. A particular power supply configuration is intended to be operated from a single voltage/frequency combination; physical changes to the supply are necessary if either the voltage or the frequency of the primary line are to be changed. A new transformer, as noted on engineering drawing

D-001-000473, must be installed if the frequency is to be changed. A voltage change can be accommodated by making the wiring change noted on this drawing. The computer is equipped with a standard 3-wire power cord, and it is essential that the third (green) wire be connected to a solid earth ground.

Specifications

The NOVA 2/10 power supply, under normal operating conditions, is capable of delivering 28A at 5Vdc, 2A at -5Vdc, 10A at 15Vdc, and 3A at -15Vdc. Ripple is less than 0.5 volt on any dc voltage.

Power Fail Module

The power fail module monitors the operation of the NOVA 2/10 power supply and furnishes status information to the processor. Both the dc output voltages of the supply and the output of the transformer are monitored. There are three status signals, $\overline{\text{PWR FAIL}}$, PWR OK, and +5V OK.

During a power failure, the $\overline{\text{PWR FAIL}}$ signal will be asserted as soon as the ac supply falters. (See the processor section of this manual for a discussion of the actions taken by the processor in response to these various signals.) The PWR OK signal is cleared when any of the four output voltages fall below the thresholds listed in Table P-1. The +5V OK signal is cleared as the last step of the power-down sequence, as the +5Vdc line continues to fall.

As the supply is powered back up, the $\overline{\text{PWR FAIL}}$ signal clears and the +5V OK signal sets as the +5V dc line approaches its normal range. When the four dc voltages have reached the thresholds listed, the PWR OK signal is asserted.

Table P-1 Power Fail Threshold, NOVA 2/10

Voltage	Threshold
+ 5Vdc	+ 4.5Vdc
- 5Vdc	- 4.5Vdc
+15Vdc	+13.8Vdc
-15Vdc	-13.7Vdc

REFERENCES

1. NOVA 2/4 Power Supply D-001-000560-00.
2. NOVA 2/10 Power Supply D-001-000473-03.

This page left intentionally blank

SECTION M

MEMORY

CORE MEMORIES

Core memory is made up of many thousands of tiny ferrite rings, called cores. As shown in Figure M-1, such a core can be magnetized in either the clockwise or counterclockwise direction. A binary digit can be stored in a core based on the direction of magnetization. Because of an effect known as hysteresis a core will retain its magnetization indefinitely; hence core memory is non-volatile. It is possible to electrically detect magnetization changes in a core and thereby read the contents of the core.

A core can be magnetized by causing a sufficient current, I_m, to flow through its center. If the current flows as shown in Figure M-1, the core will be magnetized in the direction shown. If however, the current were to flow in the opposite direction, the magnetization of the core would change direction.

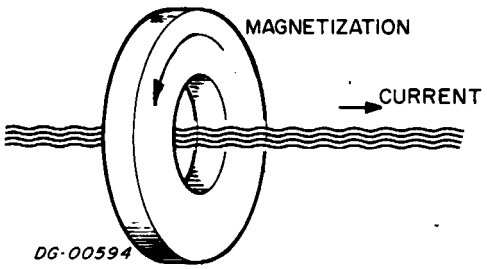


Figure M-1 Current Flow and Magnetization of a Core

Like all magnetic materials, the ferrite cores display a phenomenon known as hysteresis. This phenomenon, shown in Figure M-2, causes the magnetization direction to lag behind the current and to display what may be referred to as thresholds. The direction and intensity of the magnetization always follows the curve in a counterclockwise direction, as shown by the arrows. To illustrate, suppose that the magnetization is presently at point A, that is, a value of +3 (units are unimportant to this discussion). Now, if a current of -1 were sent through the core, the magnetization would move to point B, still +2.5. If the current were doubled, that is to -2, the magnetization would now move to point C, -3. It can also be seen that if the current is removed, the core will retain its previous state (point D). Thus a core memory will retain its contents even after power is removed.

This hysteresis effect provides both the means to store information in a core and a means to address a particular core. The cores are usually laid out by threading them on a wire matrix so that each core has a unique pair of X and Y wires passing through it. To set a specific core, partial select currents of $I_m/2$ each are sent down the particular X and Y wires. Only at the point where the two wires cross will there be sufficient current flow to

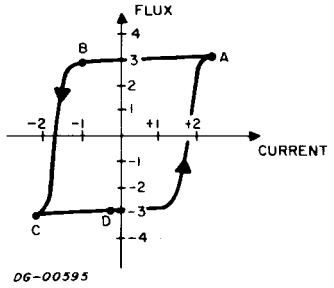


Figure M-2 Hysteresis Curve (typical) of a Ferrite Core

cause a core to change its magnetic state. As shown by the hysteresis curve, cores on only the X or Y lines will not see sufficient current flowing through them to change state.

If a wire is held in a varying magnetic field, a voltage will be induced on the wire proportional to the rate of change of the magnetic field. A third wire, the "sense wire," threaded through all of the cores, allows us to use this induced voltage to read the state of a core. To read a selected core, the X and Y lines corresponding to the core location are both driven with $I_m/2$ to set the core to the "0" state. If the core was already in this state there is no further effect. However, if the core was in the "1" state, the sudden flux reversal causes a voltage pulse on the sense wire which can be detected by a differential amplifier. Thus if a pulse occurs, the core was in the "1" state. After reading, the core is always left in the "0" state; this is known as "destructive read-out" and it is then necessary to rewrite the contents of that core.

A core is written into by sending currents down the X and Y lines that would normally set the proper core to the "1" state (i. e., $-I_m/2$). If a 0 is to be written, a current of $I_m/2$ sent down an inhibit wire, which is threaded through all of the cores, cancels the effect of one of the X or Y currents, thus leaving the core in the "0" state.

It should be apparent that the "0" and "1" states are symmetrical. Thus the memory could similarly be operated by first driving all cores to the "1" state, and then inhibiting those cores that should be set to "1".

NOVA 2 CORE MEMORY

NOVA 2 core memory, shown in Figure M-3 is arranged in words of sixteen bits apiece, each selected by a unique pair of X and Y coordinates. In addition to the X and Y drive lines there are sixteen sense/inhibit lines, each one threaded through all of the cores corresponding to the particular bit position in a word. Although controlled by the processor, the NOVA 2 memory operates asynchronously with the processor, developing its own control signals based on timing signals received from the processor. Each memory array is mounted on a daughter board with the diode addressing matrices. This board is mounted on the 15-inch square printed circuit board containing the remaining memory data paths, shown in Figure M-4, and control circuitry.

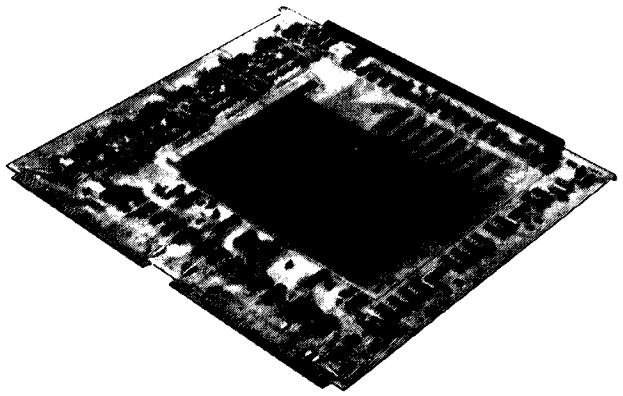


Figure M-3 NOVA 2 Memory Board

Address Selection

Every location within a memory array is selected by decoding bits of the memory address register and driving the proper pair of X and Y lines for that address. The drivers have the capability of driving the lines in either direction, so that the cores can be set to one for a read and to zero for a write (neglecting inhibit currents).

Figure M-5 shows a simplified circuit illustrating how one of a pair of drive lines is selected. This could be considered the X drive of a sixty-four word memory. The eight X lines are selected by three bits of the address, labeled MA13, MA14, and MA15. The Y lines would be selected by other bits.

The driver chips, of which three are shown, have three sets of inputs and two pair of output terminals. Each pair of output terminals consists of a electronic source switch and a return switch, labeled S and R respectively. The arrows show the direction of current flow. The seven address inputs, labeled A thru G, are divided into three groups. Inputs E, F, and G are AND'ed together to enable the chip. Inputs A and D determine which pair of outputs is enabled, and inputs B and C select either the source switch or the return switch of that pair.

In this example, chip U1 is always enabled. MA15 selects either the upper pair or the lower pair of outputs. Similarly, the two lower chips are controlled by bits MA13 and MA14. The READ and WRITE signals control the source/return functions. The accompanying table shows the switches enabled by different bit combinations. A similar procedure would be used to select the Y drive.

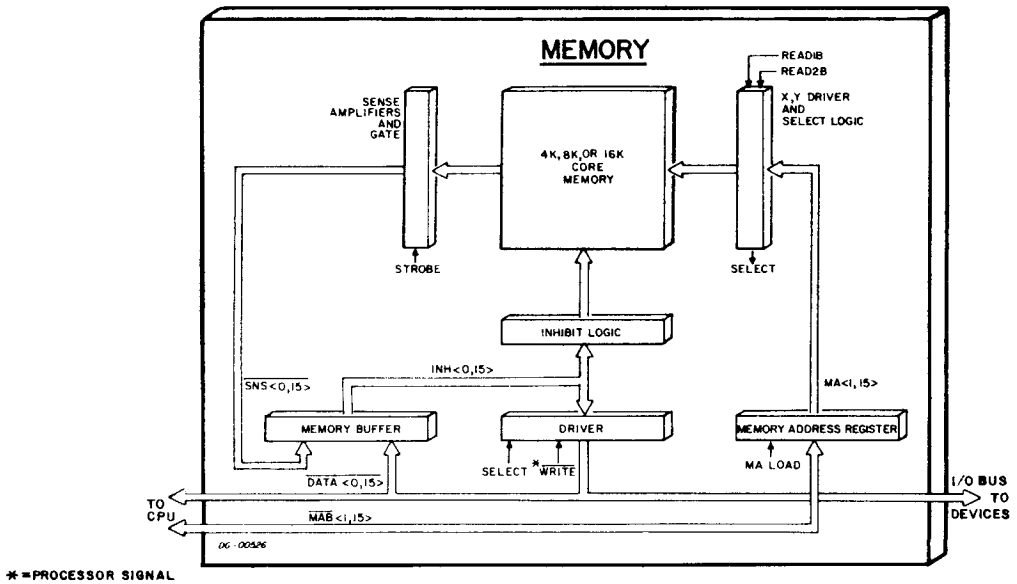
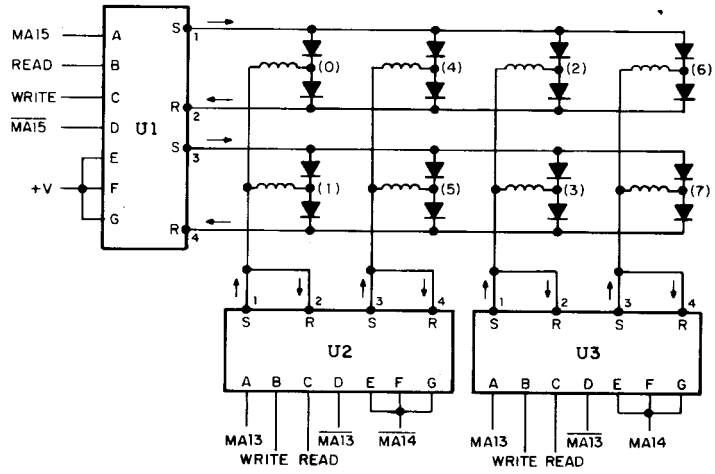


Figure M-4 NOVA 2 Memory Data Paths



LINES		0	1	2	3	4	5	6	7
ADDRESS BITS		000	001	010	011	100	101	110	111
OUTPUTS	READ	U1-1, U2-2	U1-3, U2-2	U1-1, U3-2	U1-3, U3-2	U1-1, U2-4	U1-3, U2-4	U1-1, U3-4	U1-3, U3-4
	WRITE	U1-2, U2-1	U1-4, U2-1	U1-2, U3-1	U1-4, U3-1	U1-2, U2-3	U1-4, U2-3	U1-2, U3-3	U1-4, U3-3

DG-00627

Figure M-5 Core Memory Address Selection

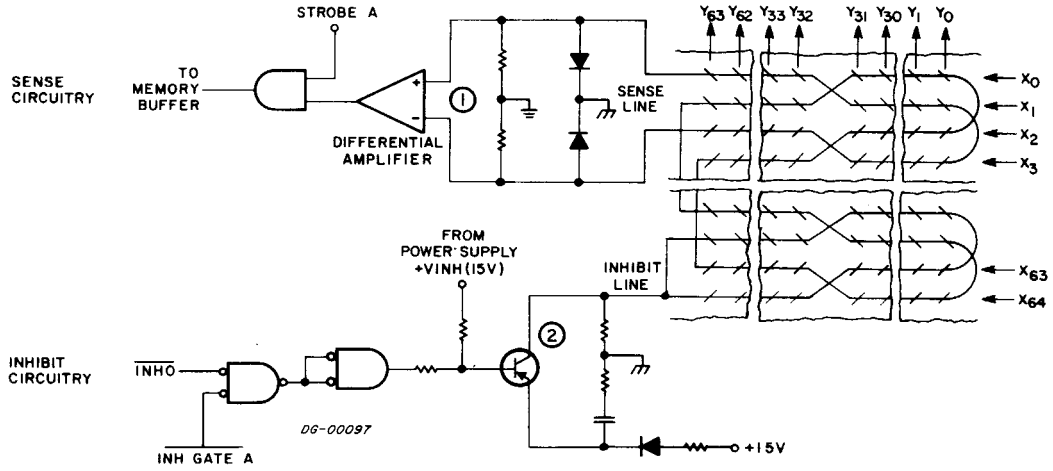


Figure M-6 Simplified Sense/Inhibit Circuitry

Sense/Inhibit Lines

The sense/inhibit wire is used both to sense a change of flux in a core and to inhibit setting a core to one. The sense differential amplifiers connect to the ends of each of these sixteen lines, while the inhibit currents are driven from the center of the line. Figure M-6 illustrates how this line is threaded through the cores and connected to the relevant circuitry.

In the NOVA 2 memory, the cores are driven to the "1" state to read them. Thus a pulse on the sense line indicates that the core was previously in the "0" state. To write information into a core, it is driven towards the "0" state by the X and Y drive. Inhibit currents cause the core to be left in the "1" state.

Whenever a memory is read, partial select currents are driven down a pair of X and Y lines, as explained previously. As predicted, the core at the intersection of these two lines causes a pulse on the sense line if it changes state. A significant problem, however, is the fact that the cores which see only the X or Y current will also change their magnetization slightly, (i. e., from point A to point B in Figure M-2). While this is not a change of state, the slight flux change will introduce a small pulse on the sense wire. Considering that each sense line intersects at least 4096 such cores in the Nova 2, these small pulses could sum to become a substantial noise problem. To help reduce this noise, the sense line is threaded in the zig-zag or checkerboard pattern seen in Figure M-6. Now the sense line threads half of the cores in each row and column in opposite directions, with the result that a

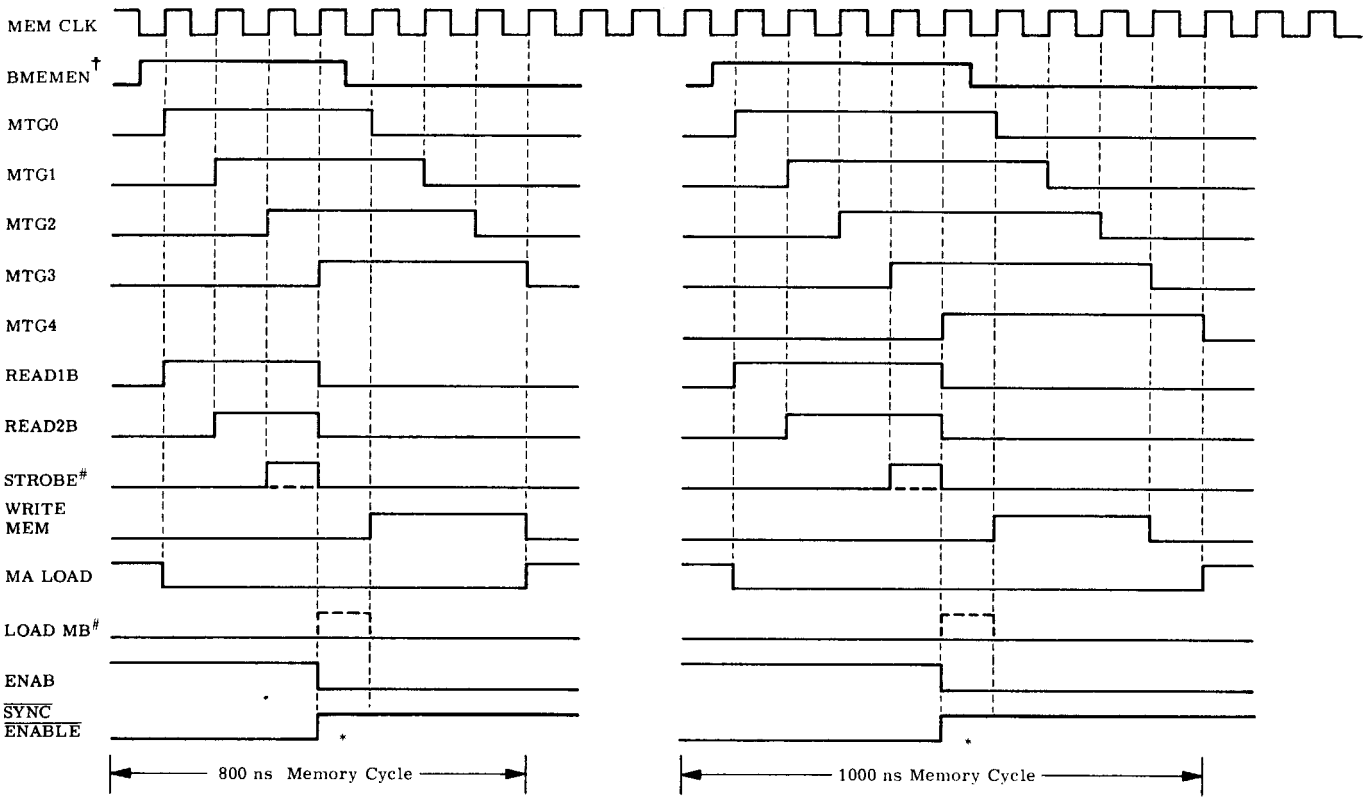
large portion of this additive noise cancels out. Threading the sense line this way also reduces noise caused by coupling between the X or Y lines and the sense line.

Processor/Memory Control

Data is transferred between memory and the central processor on one sixteen bit bidirectional bus called $\overline{\text{DATA}}$. Additionally, there is a fifteen bit bus, $\overline{\text{MAB}}$, which communicates the memory location to be accessed to the memory.

To start the selected memory in operation, the CPU issues $\overline{\text{BMEMEN}}$, which starts the memory cycle timing generator. The processor can halt the memory cycle before the write half, by issuing $\overline{\text{BRMW}}$, which sets HOLD. The processor must issue $\overline{\text{WE}}$ in order to finish the cycle, and $\overline{\text{WRITE}}$ if data is to be received off the DATA bus and written into memory. The memory in turn communicates with the processor by issuing SYNC ENABLE at the beginning of the memory cycle, and releasing it when its data is ready for the processor. The $\overline{\text{WAIT}}$ signal is issued by an active memory module to prevent any other memories from operating until that board has finished its cycle. The memories used in the NOVA 2 are asynchronous; that is, they develop their own timing signals from rudimentary signals received from the central processor. Basic timing information is contained in MEM CLK, a 10MHz square wave. The basic memory cycle consists of a fetch followed by a write. Figure M-7 shows the important internal signals of the complete memory cycle for the 800ns and 1000ns memories.

To fetch data from a memory location, the address in the memory address register is decoded to drive on READ1B and READ2B, respectively, the appropriate pair of X and Y lines. The sense circuitry detects pulses with a differential amplifier connected to both ends of the sense/inhibit wire. The output of this amplifier is examined at STROBE time and loaded into the memory buffer register. For writing into memory, the middle of the sense/inhibit wire is driven with +15Vdc by the inhibit logic at INHIBIT time. This current is divided and passes through all cores to ground through the diodes at either end.



* = Memory Remains in this state if stopped by $\overline{\text{BRMW}}$.

† = Signal Issued by Central Processor.

\# = If memory access is a write, STROBE is not pulsed, and Memory Buffer is clocked.

Figure M-7 NOVA 2 Memory Timing Cycles

Memory Board Selection

The Data General NOVA 2 computer can address any one of 32K memory locations (words). Memory boards, however, are available covering 4K, 8K, or 16K segments. In order to configure a number of boards to cover a larger segment of memory, without overlapping, it is necessary to be able to assign each board to a unique segment of memory. This is accomplished through the memory select logic on each board. Every memory address consists of fifteen bits. The high-order bits are used to select a particular memory board (i. e., a segment of memory), while the remaining lower order bits select an address within that segment, or on that board. A 16K board uses the highest order bit for board selection; an 8K uses the two highest and a 4K the three highest order bits for board selection. (Note that the highest order bit of a memory address is equivalent to bit 1 of a word in storage). In order to assign a board to a particular segment of memory, the memory select logic must be wired so that the board responds only to addresses within the assigned memory segment; that is, only to addresses which have the proper highest order bits set. The memory select logic accomplishes this by ANDing the proper high-order bits in either their normal state (as sent by the processor) or after inverting them. A board is assigned to a particular segment of memory by wiring it so that the proper bits are inverted. The output from the AND gate then, will be true only for an address that has the proper high-order bits set.

Jumpers are used to connect either the normal or the inverted side of the proper high-order bits of the memory address bus to the "and" gate. The jumpers are forced into points on the board located on the logic side of the board along the contact edge.

Each such selection must be unique to a particular memory board. If there is a mixture of boards of different capacities (i. e., 4K, 8K, 16K) it is best to assign the largest boards to lowest core, and use smaller boards for higher memory segments. In this way, there will not be any gaps in the system's core map. Figures M-8, M-9, and M-10, show how the memory segment is selected on the various boards.

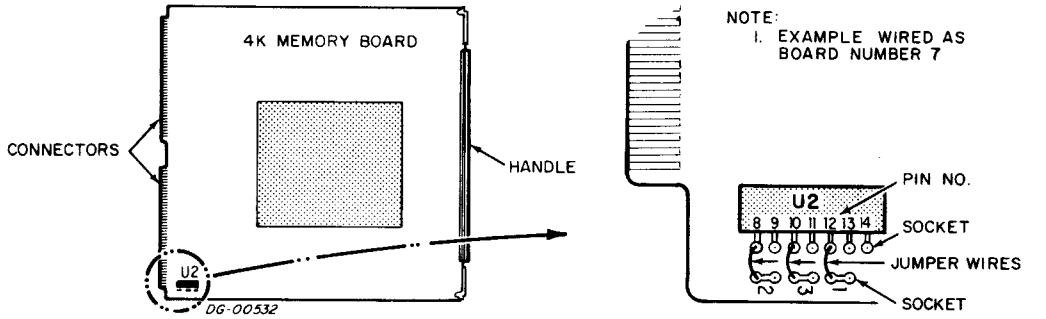
Table M-1

NOVA 2 External Memory Signals

$\overline{\text{MAB 1-15}}$	Memory Address bus--communicates from the CPU to the memory the address of the next word to be referenced.
$\overline{\text{DATA 0,15}}$	Bidirectional bus which transfers data between the CPU and the memory.
$\overline{\text{INH SELECT}}$	Inhibits selection of the memory module.
$\overline{\text{B MEMEN}}$	Issued by the CPU to start a memory cycle.
$\overline{\text{WRITE}}$	Causes the memory to write data into core.
$\overline{\text{BRMW}}$	Issued by the CPU--causes the memory to pause between the read and write halves of its cycle.
$\overline{\text{WE}}$	Issued by the CPU--allows a memory to complete its cycle after a read-modify-write (BRMW).
$\overline{\text{SYNC ENABLE}}$	When low, allows the memory to halt the processor until the read cycle is complete.
$\overline{\text{RELOAD DISABLE}}$	Inhibits loading of the memory buffer.
$\overline{\text{WAIT}}$	Issued by a memory to prevent operation of any other memory boards until it has completed its write cycle.
MEM CLK	Basic timing information supplied to the memories by the CPU.
$\overline{\text{EXTERNAL SELECT}}$	Allows a particular board to be selected regardless of what high-order bits are set in the memory address.
EXT MBLD	Allows data to be stored in the memory buffer without actually causing a memory cycle.

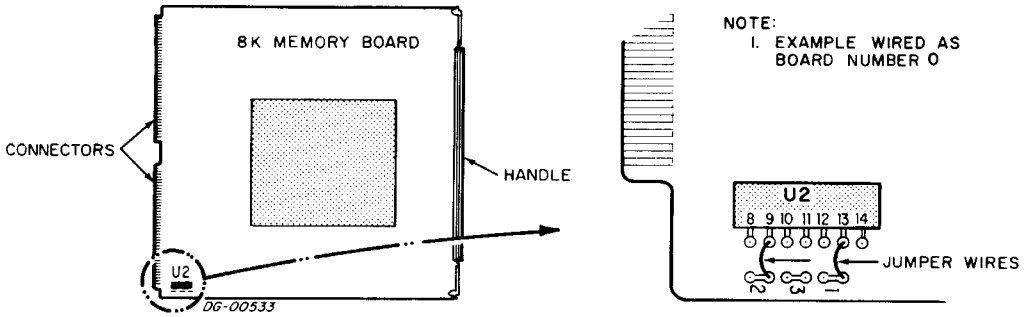
REFERENCES

1. NOVA 2 4K and 8K Memory Schematic D-001-000342-01.
2. NOVA 2 16K Memory Schematic D-001-000369-02.



MA BITS JUMPERED 1	2	3	BOARD NUMBER	ADDRESSES ENABLED (OCTAL)	JUMPER WIRE PLACEMENT (3 WIRES) CONNECT SOCKET OF U2 TO SOCKET DIRECTLY OPPOSITE		
0	0	0	0	00000-07777	13-1,	9-2,	11-3
0	0	1	1	10000-17777	13-1,	9-2,	10-3
0	1	0	2	20000-27777	13-1,	8-2,	11-3
0	1	1	3	30000-37777	13-1,	8-2,	10-3
1	0	0	4	40000-47777	12-1,	9-2,	11-3
1	0	1	5	50000-57777	12-1,	9-2,	10-3
1	1	0	6	60000-67777	12-1,	8-2,	11-3
1	1	1	7	70000-77777	12-1,	8-2,	10-3

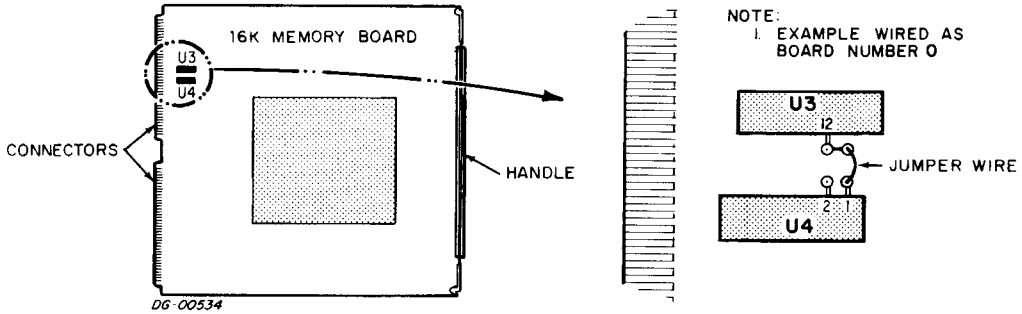
Figure M-8 Wiring the Select Logic of NOVA 2 4K Memory Boards



MA BITS JUMPERED 1	2	BOARD NUMBER	ADDRESSES ENABLED (OCTAL)	JUMPER WIRE PLACEMENT (2 WIRES) CONNECT JUMPER FROM SOCKET OF U2 TO SOCKET DIRECTLY OPPOSITE	
0	0	0	00000-17777	13-1,	9-2
0	1	1	20000-37777	13-1,	8-2
1	0	2	40000-57777	12-1,	9-2
1	1	3	60000-77777	12-1,	8-2

(NOTE: Position 3, i.e., U2 pins 10 and 11, should not be jumpered).

Figure M-9 Wiring the Select Logic of NOVA 2 8K Memory Boards



MA BITS JUMPERED 1	BOARD NUMBER	ADDRESSES ENABLED (OCTAL)	JUMPER WIRE PLACEMENT (1 WIRE)
0	0	00000-37777	12-1
1	1	40000-77777	12-2

Figure M-10 Wiring the Select Logic of NOVA 2 16K Memory Boards

SECTION 1

NOVA 2 INSTALLATION

INTRODUCTION

The NOVA 2 computer is either mounted on slides in a standard 19-inch rack, or installed in a table top cabinet. Power is supplied to the computer through a standard 6-foot 3-wire cord.

Installing the computer normally involves placing it, unpacking it, assembling it, and cabling the assemblies together.

PLACING THE COMPUTER

Care should be used in selecting a location for the computer. The primary power supply should be reliable and of adequate capacity. The temperature and humidity of the operating environment must fall within acceptable tolerances of the most sensitive peripheral. The electrical and environmental specifications of the NOVA 2 are shown in Table I-1.

Overhead sprinklers should be "dry pipe" systems that remove primary power from the room and turn on a battery operated light source before opening the master valve. If power connections are made under the floor, use waterproof receptacles and connections. Any carpeting should be of the type that minimizes static electricity, and metal flooring must be well insulated from ground. It is important that an earth ground for the computer be supplied through the 3-wire power cord.

Table I-1

NOVA 2 Electrical, Mechanical and Environmental Specifications

		NOVA	
		2 4	2 10
Power Supply		115V (±20%) @ 10 Amps 230V (±20%) @ 5 Amps	115V (±20%) @ 10 Amps 230V (±20%) @ 5 Amps
Frequency		47-63Hz	50 or 60Hz, (±1Hz)
Power Dissipation (max)		300 Watts	725 Watts
Heat Dissipation (max)		1050 BTU hr	2500 BTU hr
Operating Temperature		32° to 130°F	32° to 130°F
Storage Temperature		-30 to +150°F	-30 to +150°F
Relative Humidity		20% to 90%	20% to 90%
Maximum Length of In Out Bus Cable		50 Feet	50 Feet
Dimensions (inches)	Height	5-1 4	10-1 2
	Width	19	19
	Depth	19	24
Service Clearance (inches)	Back	3	3
	Front	36	36
	Right Side When Extended	24	24
Weight Unpacked (pounds)		50	115

UNPACKING THE COMPUTER

The computer is shipped in the kit shown in Figures I-1 and I-2.

1. Open the top of the shipping carton, remove all cables, manuals, packing filler, etc.
2. Remove the styrofoam container and place it on a flat surface right side up.
3. Unstrap the container and remove the cover and expansion rings.
4. Remove the computer, placing your hands under the chassis front and back.
5. Remove the (phillips head) shipping screw located on the bottom of the computer, 2/3 of the distance back from the console. (NOVA 2/10 computers only.)
6. The computer is shipped with 1/2" foam layers between the boards. This foam must be removed before using the computer, otherwise damage from excessive heat may result.

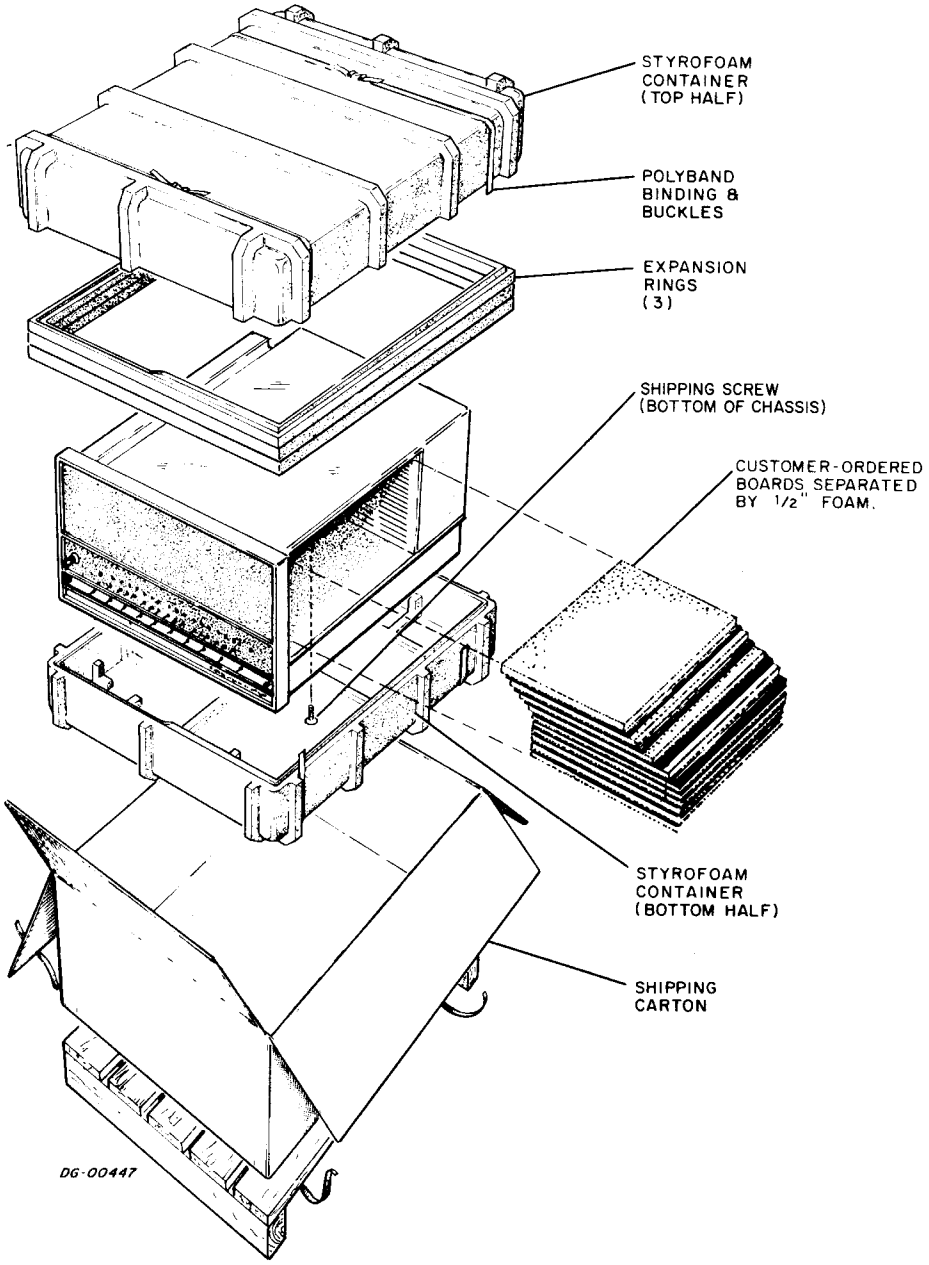


Figure I-1 NOVA 2/10 Shipping Kit

PACKING THE COMPUTER

1. Locate the original shipping container and packing material. If it is not available, order a shipping kit from Data General Corporation. DO NOT SHIP THE COMPUTER IN ANY OTHER CONTAINER.
2. Install the (phillips head) shipping screw into its location on the bottom of the computer, 2/3 of the distance back from the console. (NOVA 2/10 computers only.)
3. Fill the spaces between the boards with layers of 1/2" foam. Note that the 8K and 16K memory boards should be shipped separately. For packing procedures for individual boards, see the section "Unpacking and Packing Boards".
4. Place the computer in the bottom half of the styrofoam container, "front justified" with the back end on top of the extra rib. Pack the power cord into the hollow area at the back.
5. Add the expansion rings as needed.
6. Put on the cover of the styrofoam container and strap the pieces together.
7. Put the styrofoam container into the shipping carton. Place any odds and ends on top of the container, and fill in any empty spaces with cardboard or pieces of styrofoam.
8. Close and seal the cardboard box.
9. Call your local Field Service Representative for the correct address if the equipment is to be shipped to Data General Corporation.

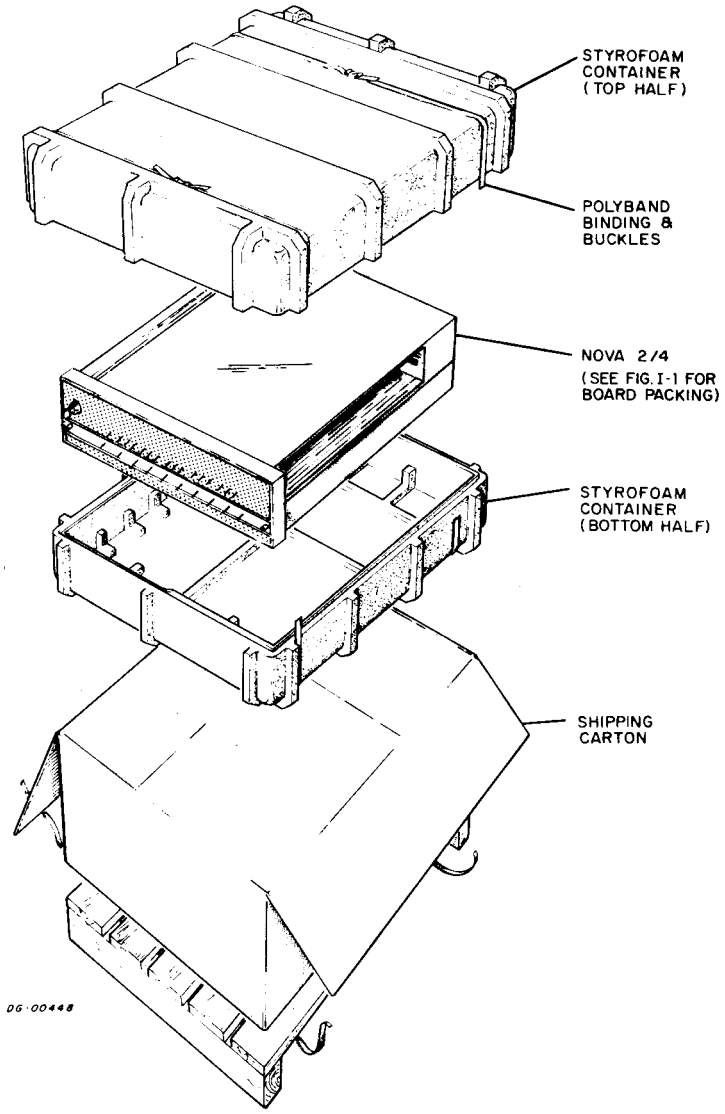


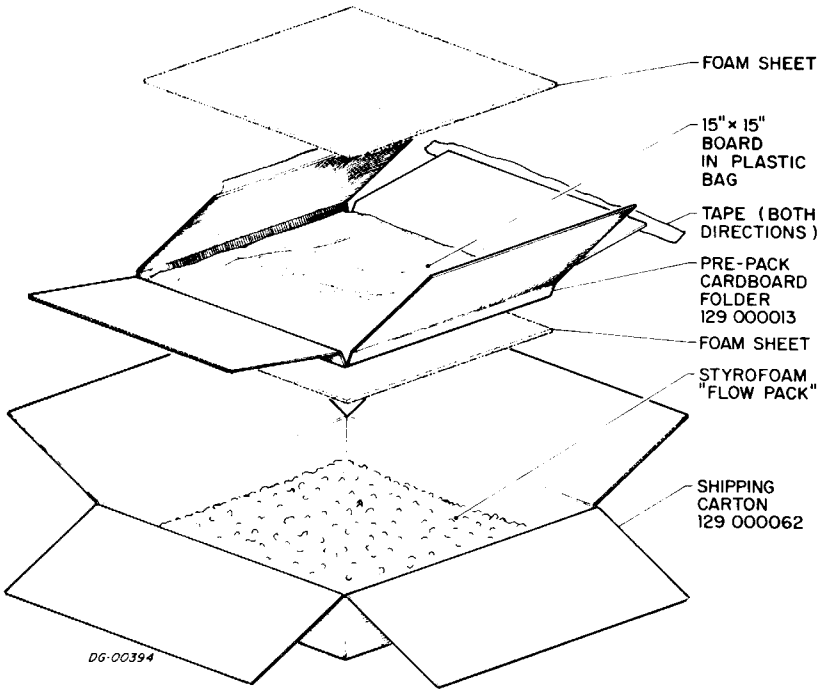
Figure I-2 NOVA 2/4 Shipping Kit

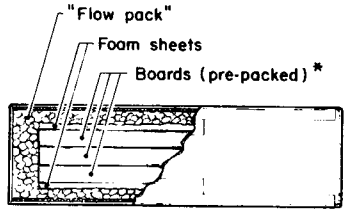
UNPACKING AND PACKING BOARDS

Memories and other circuit boards are shipped in the kit shown in Figure I-3. Unpack this kit carefully and save it in case the boards have to be shipped again. NEVER SHIP THE BOARDS IN ANY OTHER TYPE OF CONTAINER.

To pack the boards, proceed as follows:

1. Locate the shipping kit or order another from Data General Corporation.
2. Place each board into the plastic bag supplied with the kit.
3. Place each bagged board on its pre-pack cardboard folder. Tape each folder closed.
4. Partially fill the outside shipping carton with loose styrofoam "flow pack." Place one sheet of foam on top of the "flow pack."
5. Place one of the pre-pack folders containing a board on top of the foam sheet.
6. If a second board is being packed, place its pre-pack folder containing the board on top of the first folder.
7. Place a second sheet of foam on top of the second pre-pack folder, or on top of the first if only one board is shipped.
8. Fill in any empty space in the shipping container with "flow pack."
9. Close and seal the outside shipping container.





MULTIPLE PACKING

* Up to three (3) 15"x 15" boards, enclosed in plastic bags and sealed in pre-pack folders as shown, can be put in shipping carton No. 129 000062. For four (4) to seven (7) boards, use shipping carton No. 129 000012.

Figure I-3 Shipping Kit for Individual Circuit Boards

INSTALLING OR REMOVING BOARDS

The Nova 2 computer has slots for either four or ten fifteen by fifteen inch circuit boards which plug into sets of 100 pin connectors on the printed circuit back panel. The slots are numbered from the bottom up and assigned as shown in Table I-2. It should be noted that the multiply/divide option must be installed in slot 2, and the TTY, PTP, or PTR interfaces in slot 3. Note that the Data General convention is to install memory boards from the lower numbered slots up, and I/O controllers from the highest slots down.

If boards are removed or installed in the computer chassis, it is important that the integrity of the program interrupt and data channel priority systems is preserved. The program interrupt and data channel priority systems each use a scheme in which a signal is passed through each controller in turn, to the end of the chain. This signal is used by the controllers in such a way that only when the signal to the controller is enabled (low), can that controller request interrupt or data channel service. Any controller that successfully requests such service removes the enabling level to all controllers further along that particular chain. Memories and other boards that do not use either signal pass it across their slot directly, with no interference. It is important to note that an unused slot or a user manufactured board that does not properly pass this signal will prevent any controllers further along the chain from requesting service. The $\overline{\text{INTP}}$ $\overline{\text{OUT}}$ and/or $\overline{\text{DCHP}}$ $\overline{\text{OUT}}$ (back panel pins A95 and A93, respectively, in slots 3 to 10) signals must be jumpered across the back panel slots of such boards that do not effectively pass them, and any unused slots, if there are controllers further along the chain. It is important that the following restrictions are observed when installing or removing boards:

1. All interfaces that use the interrupt system must be included in the interrupt chain; all interfaces that use the data channel must be included in the data channel chain.

2. The data channel and program interrupt chains are completely independent and must remain separate. All controller boards must be wired in series, relative to either chain, never in parallel.

3. The appropriate priority signal must be jumpered across the slot of any board that does not utilize either the program interrupt priority system or the data channel priority system. The Data General practice is to jumper this signal in the etched wiring of the board itself, and it is recommended that user manufactured boards do the same. Back panel jumpering will be required across unused slots and in cases where an unused priority signal is not jumpered on the board.

Interfaces that use the data channel are designed to use either the standard or the high speed data channel. High speed interfaces must be installed in the computer chassis, and must occupy lower slot positions than devices using the standard data channel. In order to define the mode of the data channel devices, the $\overline{\text{DCHP}}$ $\overline{\text{OUT}}$ (pin A93) signal of the last high speed device (highest slot) is returned to back panel pin A95 of slot 1, to control the processor's data channel logic.

This signal is returned from pin A93 of the highest slot in the chassis in the NOVA 2 to the processor via back panel etch. In this way, any controllers installed in the chassis that use the data channel will operate on the high speed data channel, while controllers mounted outside the chassis will use the standard data channel. If for some reason, it is necessary for a device mounted within the chassis to use the standard rather than the high speed data channel, the back panel must be modified as shown in Figure I-4. Note that all of the controllers installed above this low speed device will use the standard data channel.

Table I-2

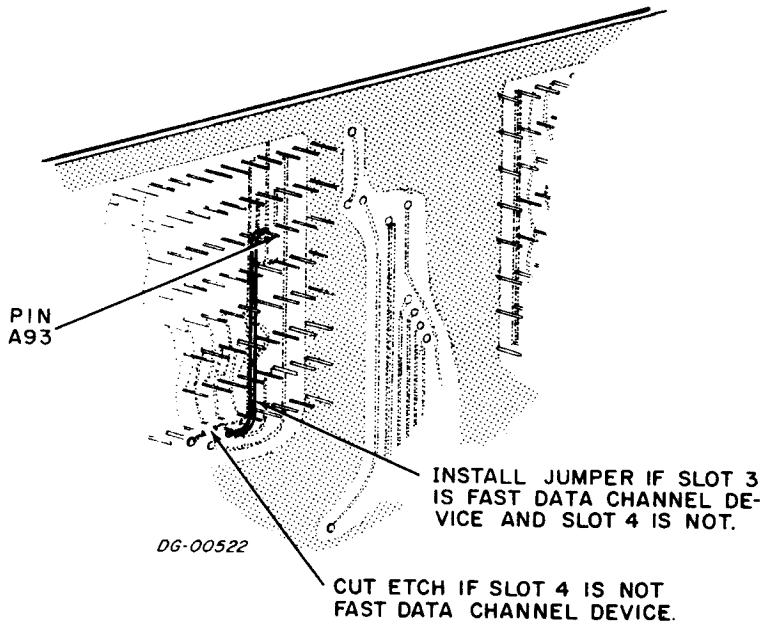
Slot Assignments for the NOVA 2

Slot	Assignment
1	Central Processor Unit
2	Memory or Multiply Divide
3	Memory or I O Interface*
4	Memory or I O Interface
5-6 (2 10)	Memory or I O Interface
7-10 (2 10)	I O Interface **

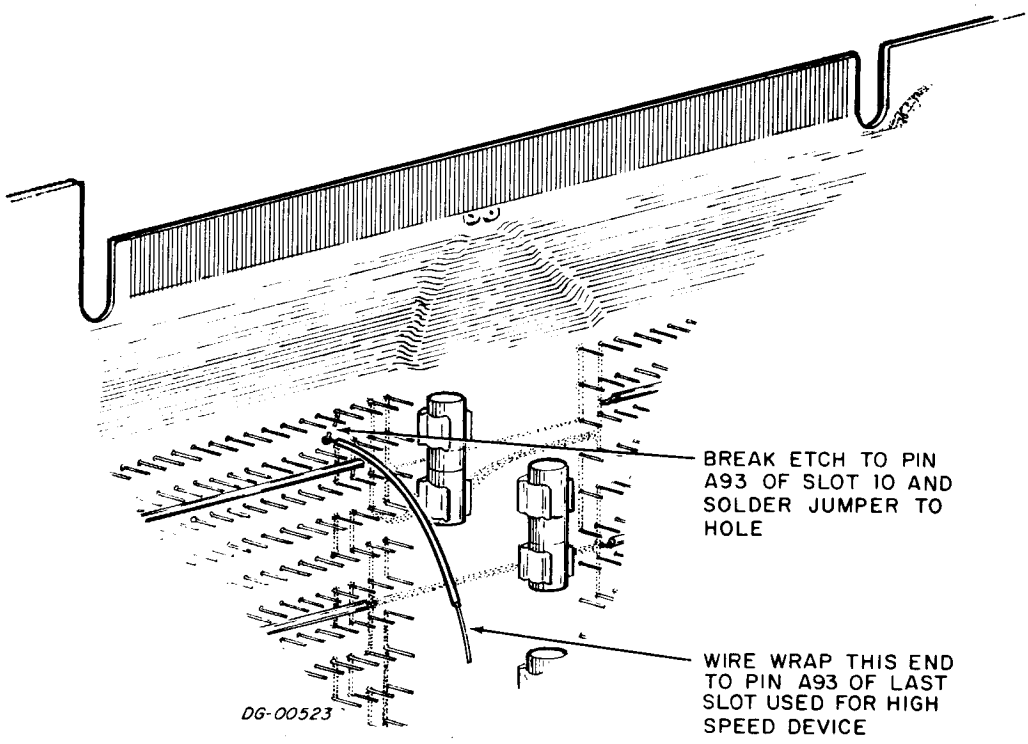
* If TTY, PTP, or PTR options are ordered, they must be installed in Slot 3.

** Slots 9 and 10 are configured to allow the customer use of a larger number of I/O pins (74 pins per slot extra).

Note: Slots are numbered starting from the bottom of the chassis.



NOVA 2/4



NOVA 2/10

Figure I-4 Modifying Fast Data Channel Designation

MOUNTING THE COMPUTER

Unless table-top mounting is specified, the NOVA 2 is shipped with rack slides attached and all of the necessary hardware included for mounting in a 19-inch rack. The outer portion of the right hand slide is assembled to the rack as shown in Figure I-5, the left side is similar. The chassis itself is mounted on the inner rails, which are in turn mounted to the outer slides as shown in the figure. At least two inches should be left open at the back for cables, and about thirty-six inches should be available at the front for servicing. The console normally protrudes 1 3/4 inches out of the front of the rack. It should be remembered that 24 inches will be required on the right side of the computer, when it is extended from the rack, to facilitate the installation or removal of boards. The completed rack installation is shown in Figure I-6.

If the table-top configuration is ordered, the computer will be supplied with a metal wrap-around cabinet. This should be installed after any back panel wiring is completed, and secured.

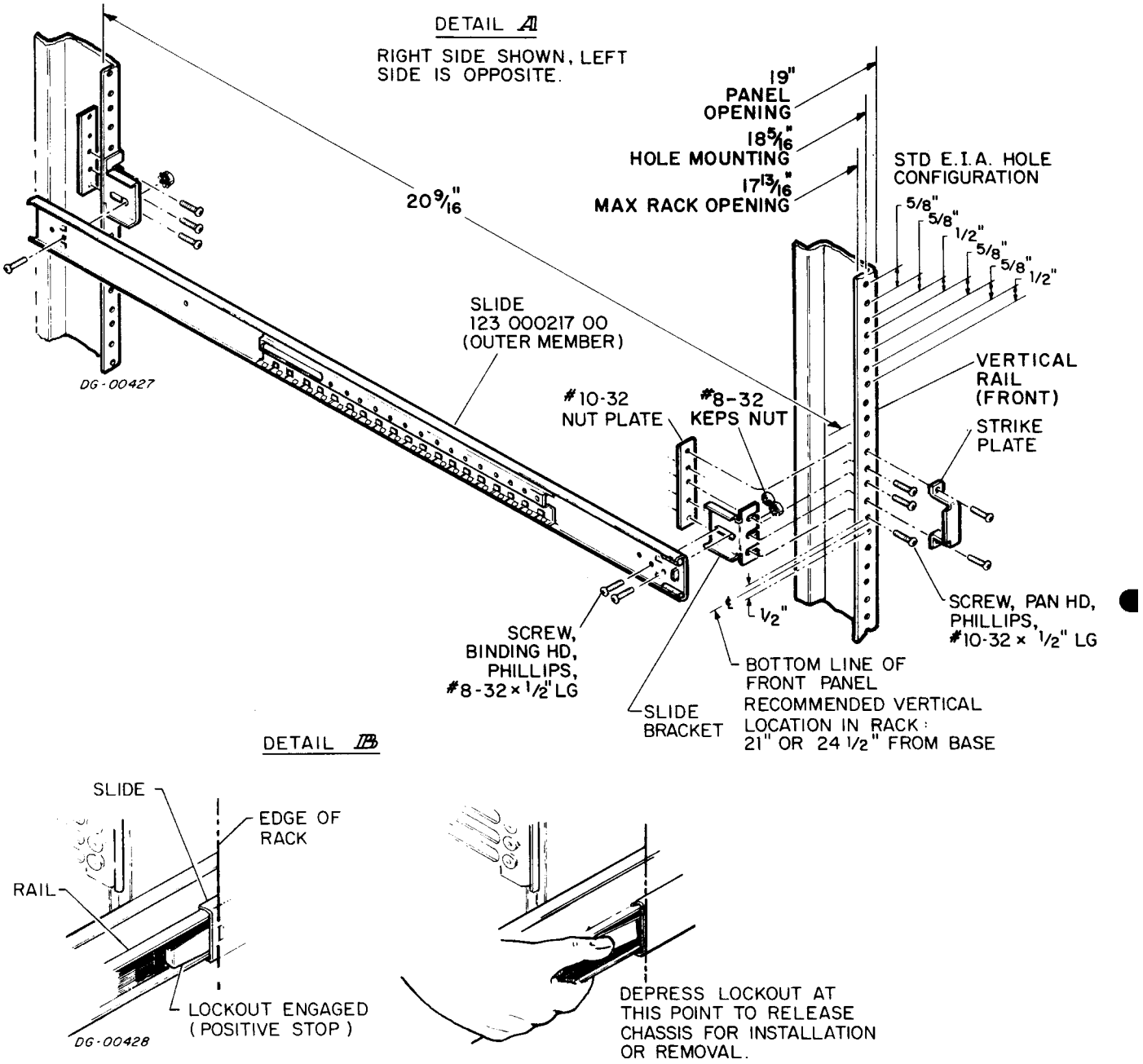
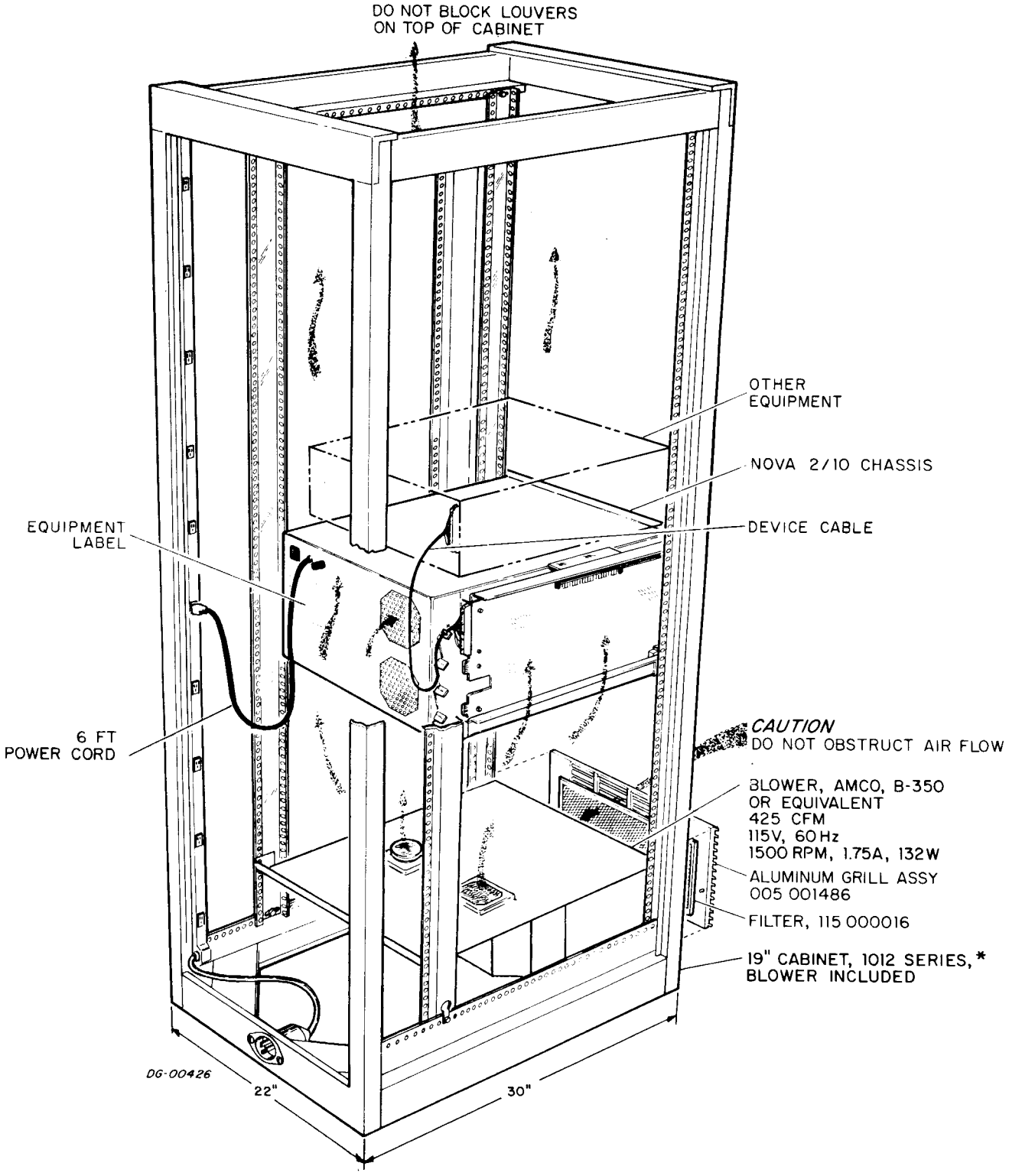
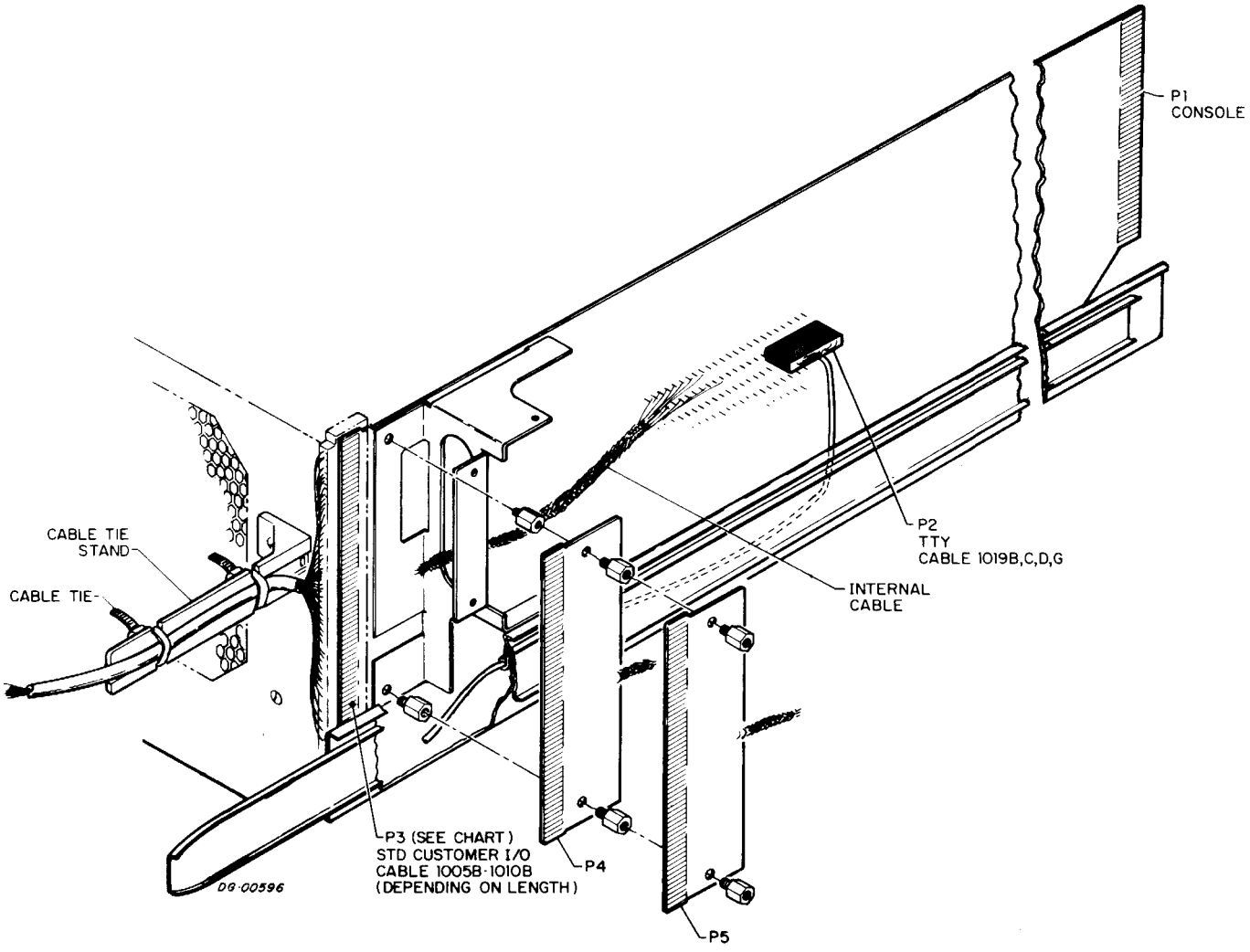


Figure I-5 Installing NOVA 2 in 19-Inch Rack

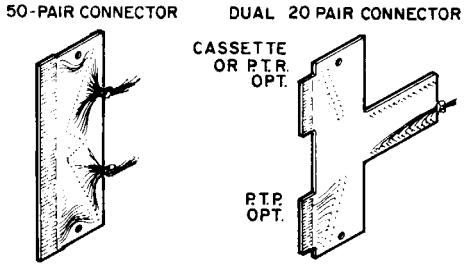


* FOR STABILITY, CABINETS 1012D (74" HT) AND 1012E (41" HT) ARE MOUNTED ON BASE, 112-000038; CABINETS 1012F (SINGLE BAY), 1012G (DOUBLE BAY) AND 1012H (TRIPLE BAY) ARE EQUIPPED WITH ANTI-TIP LEGS, 112-000045, AND LEVELOR LEGS, 123-000138.

Figure I-6 NOVA 2 Installed in Rack



PADDLE BOARD P4 AND P5 MAY
BE EITHER CONNECTOR SHOWN BELOW



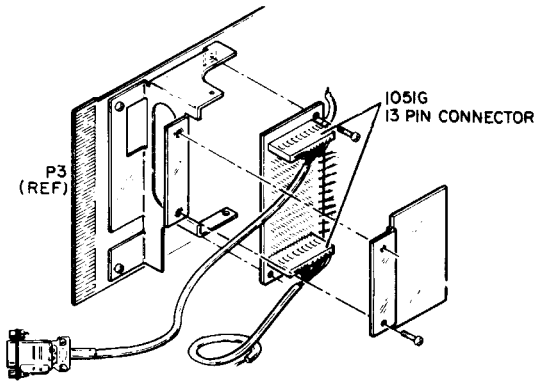
4192/NOVA 2—
BOARD WITH
INTERNAL
CABLE

10468/NOVA 2—
BOARD ALONE

005-1788
REFER TO 010-000020
FOR CONFIGURATIONS

005—001788 REFERS
TO BOARD ALONE

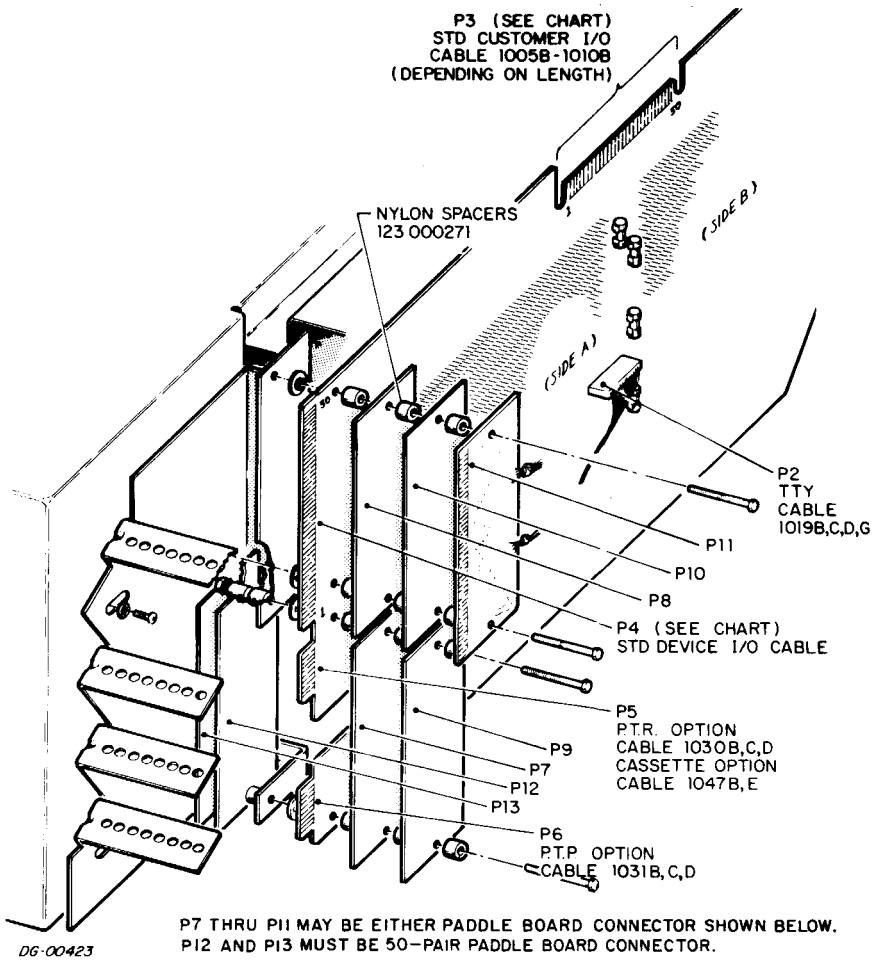
DG-00597

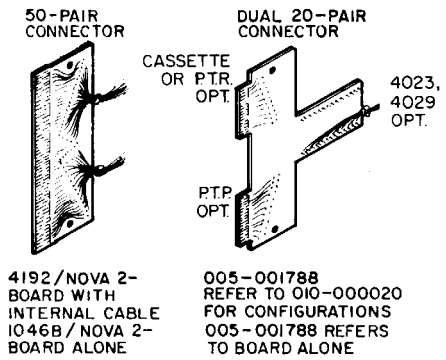


4083 OPTION BRACKET (002-000785)
MOUNTING CONFIGURATION WITH EIA
16-PIN JUNCTION PANEL

DG-00600

Figure I-7 Back Panel Connections for NOVA 2/4





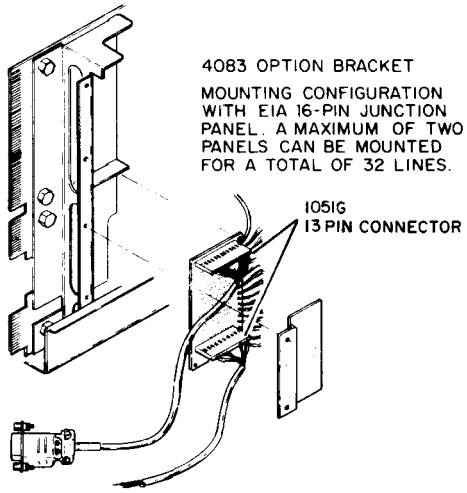


Figure I-8 Back Panel Connections for NOVA 2/10

CABLING ASSEMBLIES TOGETHER

Types of Cables

There are five types of cables used on a typical installation; internal cables, device cables, interdevice cables; I/O cables, and adapter cables. The correct cables are supplied with the equipment unless otherwise specified in the price list.

Internal Cables are run from the back panel pins to paddleboards mounted on standoffs on the chassis. They are added when the controller is added, and each shipment includes a wire list for the internal cable, and the internal cable itself.

Device Cables connect each peripheral controller to the device it is controlling. When such a controller is inserted into the NOVA 2 chassis, an internal cable is run from the appropriate back panel pins to a male connector such as P4 of Figure I-8. The device cable must then run between the male paddleboard on the computer chassis and the device.

Interdevice Cables interconnect peripheral devices. Some controllers will drive more than one device of the same kind, such as industry compatible tape controllers. In this case, the device cables are daisy chained from device to device in the same way that the I/O cables are chained between controllers. The cables which interconnect the devices are not always the same as the device cable that runs from the controllers to the first device, however, so these cables are called "interdevice cables".

I/O Cables connect peripheral controllers mounted outside the computer chassis to the computer In/Out bus. The cables form a daisy chain, from controller to controller and finally to the computer chassis, where the first cable must terminate in a female connector compatible with the 100-finger male connector called P3 shown in Figures I-7 and I-8. All I/O bus signals must be carried over twisted pair lines, with all of the returns properly grounded. Controllers mounted inside the chassis are connected to the In/Out bus through back panel etching, and therefore do not need an I/O cable.

Note that it is necessary that the lines of the external I/O bus cable be properly terminated at the far end of the bus for the system to operate properly. Figure I-9 shows the recommended termination for the I/O cables supplied by Data General. As can be seen, a somewhat different termination is used for bidirectional signals and signals issued by the devices to the central processor than is used for signals issued by the processor to devices. The power (+5Vdc) for the terminations must be supplied at the far end of the bus; it must not be taken from the PWR ON pin on the external I/O bus connector, which is to be used only to control power turn-on for a remote chassis. The Data General terminator, type 1013A, provides the proper termination for all I/O bus signals. This terminator is equipped with an I/O cable plug for plugging into the last device on the bus in place of another I/O bus cable.

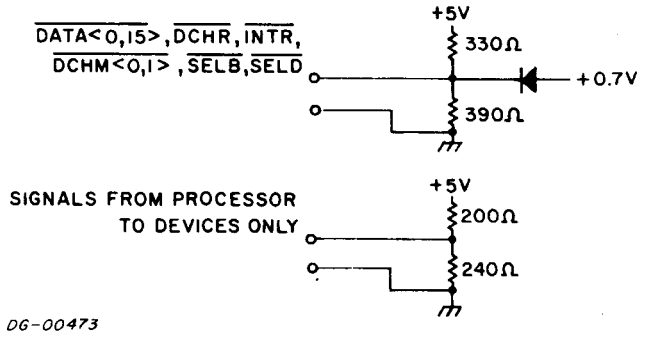


Figure I-9 External I/O Bus Termination

Adapter Cables reconcile different cabling schemes. The NOVA and SUPERNOVA computers, NOVA 1200, and NOVA 800 series computers use Cannon connectors instead of paddleboards for their device and I/O cables, and Data General supplies adapters so that peripherals used on these machines can also be used on the new models, or the other way around.

Back Panel Cabling Scheme

NOVA 2/4

Figure I-7 is a sketch of the back panel of the NOVA 2/4, showing the usual cabling scheme. Signals from the back panel pins are connected to edge connectors called P3-P5, which are mounted parallel to the back panel. The fingers of P3 are permanently connected to the In/Out bus signals according to Table I-3 via etched tracks on the back panel circuit board. P4 and P5 are additional paddleboards which are mounted and wire-wrapped to back panel pins as needed. If the paper tape punch or reader option is installed in slot 3, one of the connectors will be the dual forty-pin connector shown in the figure. The Teletype cable is run from its back panel pins (marked TTY) of slot 3, through a

cable clamp to the Teletype. All external cables should be protected from excessive strain; Figure I-10 illustrates a suggested procedure for attaining this strain relief.

NOVA 2/10

Figure I-8 is a sketch of the back panel of the NOVA 2/10, showing the usual cabling scheme. Signals from the back panel pins are connected to edge connectors called P3-P12, which are mounted parallel to the back panel. The fingers of P3 are permanently connected to the In/Out bus signals according to Table I-3 via etched tracks on the back panel printed circuit board. The fingers of P4 are permanently connected to pins of slot 9 according to Table I-4. P5 and P6 are all part of a two plug, forty finger paddlboard which is permanently connected, but used only when the paper tape punch options are installed in slot 3. P7-P12, 100 finger paddleboards which accept 48 signal wires and two ground wires, can be mounted on standoffs next to P4 or P5-P6 and wire wrapped to back panel pins as they are needed. The Teletype cable is run from its back panel pins (marked TTY) of slot 3, through a cable clamp to the Teletype. All external cables should be protected from excessive strain; Figure I-10 illustrates a suggested procedure for attaining this strain relief.

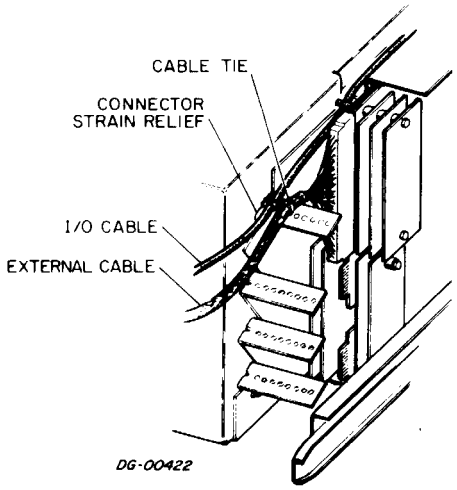


Figure I-10 Suggested Strain Relief of External Cable

Cabling the System

Turn all systems off and unplug all power cords; then:

1. Install all internal cables not factory installed following the appropriate wire list.
2. Install all device cables remembering not to exceed the maximum length in each case. Be careful to protect each cable from wear and tear.
3. Install the Teletype cable as shown in Figure I-7 or I-8.
4. Measure the line voltage of each service outlet, and check that it is correct for the computer. The power outlet must be of the three wire type with the third wire grounded.
5. Measure the voltage between the ac return line and the frame ground at each outlet. This must be ZERO. The NOVA 2 should be operated from a power source whose neutral (white wire) is at or near ground potential. This is in addition to the non-current carrying chassis ground (green wire). Do not attempt to power this computer from the outer legs of a three-wire system.
6. Plug the power cord of each device into its service outlet.

REFERENCES

1. NOVA 2/4 Rack Installation D-010-000044-00.
2. NOVA 2/10 Rack Installation D-010-000041-02.

Table I-3
P3 Connections for the NOVA 2

P3 PIN CONNECTOR	BACK PANEL PIN	SIGNAL NAME
1 THRU 50		GND
A		GND
B	A3	PWR ON (+5V)
C	A38	$\overline{\text{MSKO}}$
D	A40	INTA
E	A42	DATIB
F	A44	DATIA
H	A46	$\overline{\text{DS3}}$
J	A48	DATOC
K	A50	CLR
L	A52	STRT
M	A54	DATIC
N	A56	DATOB
P	A58	DATOA
R	A60	$\overline{\text{DCHA}}$
S	A62	$\overline{\text{DS4}}$
T	A64	$\overline{\text{DS5}}$
U	A66	$\overline{\text{DS2}}$
V	A68	$\overline{\text{DS1}}$
W	A70	IORST
X	A72	$\overline{\text{DS0}}$
Y	A74	IO PLS
Z	A80	$\overline{\text{SELD}}$
a	A82	$\overline{\text{SELB}}$
b	3-10 A93	$\overline{\text{DCHP OUT}}$
c	3-10 A95	$\overline{\text{INTP OUT}}$
d	B17	$\overline{\text{DCHM0}}$
e	B21	$\overline{\text{DCHM1}}$
f	B29	$\overline{\text{INTR}}$
h	B33	DCHO
j	B35	$\overline{\text{DCHR}}$
k	B37	DCHI
l	B39	OVFLO
m	B41	$\overline{\text{RQENB}}$
n	B55	$\overline{\text{DATA7}}$
p	B56	$\overline{\text{DATA14}}$
r	B57	$\overline{\text{DATA5}}$
s	B58	$\overline{\text{DATA11}}$
t	B59	$\overline{\text{DATA12}}$
u	B60	$\overline{\text{DATA8}}$
v	B61	$\overline{\text{DATA4}}$
w	B62	$\overline{\text{DATA0}}$
x	B63	$\overline{\text{DATA9}}$
y	B64	$\overline{\text{DATA13}}$
z	B65	$\overline{\text{DATA1}}$
AA	B66	$\overline{\text{DATA15}}$
AB	B73	$\overline{\text{DATA3}}$
AC	B75	$\overline{\text{DATA10}}$
AD	B82	$\overline{\text{DATA2}}$
AE	B95	$\overline{\text{DATA6}}$
AF		GND

Table I-4

P4 Connections for the NOVA 2/10

P4		BACK PANEL SLOT-SIDE-PIN No.
NUMBER SIDE	LETTER SIDE A THRU AF GND	
1		GND
2		9 A 92
3		9 A 91
4		9 A 78
5		9 A 77
6		9 A 76
7		9 A 75
8		9 A 73
9		9 A 71
10		9 A 69
11		9 A 67
12		9 A 65
13		9 A 63
14		9 A 61
15		9 A 59
16		9 A 57
17		9 A 47
18		9 A 49
19		9 A 79
20		9 A 81
21		9 A 84
22		9 A 83
23		9 A 86
24		9 A 85
25		9 A 88
26		9 A 87
27		9 A 89
28		9 A 90
29		9 B 6
30		9 B 11
31		9 B 13
32		9 B 15
33		9 B 19
34		9 B 23
35		9 B 25
36		9 B 27
37		9 B 31
38		9 B 34
39		9 B 36
40		9 B 38
41		9 B 40
42		9 B 48
43		9 B 49
44		9 B 51
45		9 B 52
46		9 B 53
47		9 B 54
48		9 B 67
49		9 B 69
50		RESERVED

SECTION N

MAINTENANCE

INTRODUCTION

Data General Corporation supports its equipment with a large field service organization, customer training programs and technical documentation. This section summarizes these services and includes tips on preventive maintenance, recommended tools and trouble-shooting.

FIELD SERVICE ORGANIZATION

Field Service Programs

Data General's field service organization currently offers its users a choice of three maintenance services. These services are subject to change without notice.

1. On Call Service Contract under which DGC will repair equipment at the installation when DGC is notified of a problem by the user. DGC also provides preventive maintenance on a regular schedule under this contract. Parts, labor and travel are included in the monthly payment schedule, which is determined by the type and amount of equipment to be serviced and the distance between the installation and the nearest DGC service center.

2. Factory Service Contract under which DGC will:
   a. Repair equipment when it is returned to the DGC factory in Southboro, Mass. The user assumes full responsibility for freight and insurance charges to and from the plant. Parts and labor are included in the monthly payment schedule.
   b. Repair equipment at the installation when notified of a problem by the user. Parts are included in the monthly maintenance schedule, labor is charged at reduced rates and travel is charged at the prevailing standard rates.

3. Hourly Service under which parts, labor and travel are charged as needed at prevailing rates. No contract is signed for this service.

The field service organization will also generate on request a complete spare parts list for any installation, and rent or sell replacement and loaner boards.

General Terms and Conditions (subject to change without notice):

1. Equipment which is not under a DGC service contract or normal warranty is subject to an inspection by DGC Field Service before it is eligible for a service contract. All costs for this inspection are borne by the user.

2. The user must bear all maintenance costs incurred as a result of unauthorized changes to DGC equipment. These costs will be charged as Hourly Service, regardless of the type of service contract existing between DGC and the user.

3. No additional service charge will be added for new (add-on) equipment until the warranty period of that equipment has expired.

4. All services are offered between 9 a. m. and 5 p. m. Monday through Friday, excluding DGC holidays.

5. The minimum contract period is 6 months.

6. Field Service price schedules are available on request from:

   Data General Corporation
   Field Service Department
   Southboro, MA. 01772

   Telephone 617-485-9100

TRAINING ORGANIZATION

Data General's Training organization currently offers its users four training courses related to the NOVA 2. These courses are subject to change without notice; consult the Data General Price List for latest information.

Fundamentals of Programming

This course reviews basic programming concepts, number systems, machine architecture, and the Nova instruction set.

Assembly Language Programming

Covers NOVA computer assembly language common to all NOVA line computers, and use of utility software such as Assembler, Text Editor, Bootstrap and Binary Loaders, and debuggers.

Real-Time Disc Operating System (RDOS)

This course is designed for the experienced NOVA computer programmer. It introduces RDOS and covers principles of operation, command capabilities, and use of the RDOS system.

Hardware, NOVA 2 Series

This course covers memory and CPU architecture, logic and flow analysis, instruction repertoire, basic I/O programming concepts, and operating procedures of the NOVA 2.

Courses are scheduled regularly in the training department at Southboro, Mass., and occasionally in field offices. Special courses can be arranged.

For more information call or write:

Registrar
Training Department
Data General Corporation
Southboro, MA. 01772
Telephone 617-485-9100

PREVENTIVE MAINTENANCE

Periodically carry out the checks listed in Table N-1, and remember the following points:

1. It is very poor practice to use the equipment as a counter top, particularly for liquids like coffee or soft drinks.
2. Always check the line voltage before plugging an expensive piece of equipment into an unknown socket, as explained in Section I.
3. Be careful not to get metal filings into the equipment; for example never let the equipment room be cleaned with steel wool.
4. Never clean the equipment with a vacuum cleaner that has a metal (conducting) nozzle.
5. Always be aware that too much heat, moisture or contaminants can do much to harm the equipment (see Section I).
6. Be very careful when routing cables; they should never be strained, cramped or crushed underfoot.

Table N-1

Preventive Maintenance Check List

Item	Check
Mechanical Connections	1. that all screws are tight and that all mechanical assemblies are secure. 2. that all crimped lugs are secure and properly inserted onto their mating connectors.
Wiring and Cables	1. all wiring and cables for breaks, cuts, frayed leads, or missing lugs. 2. wire wraps for broken or missing pins. 3. that no wires or cables are strained or cramped. 4. that cables do not interfere with doors, and that they do not chafe when doors are opened and closed.
Air Filters	all air filters for cleanliness and for normal air movement through cabinets.
Modules and Components	1. that all modules are properly seated. Look for areas of discoloration and all exposed surfaces. 2. all exposed capacitors for signs of discoloration, leakage, or corrosion. 3. power supply capacitors for bulges.
Indicators and Switches	all indicators and switches for tightness; check for cracks, discoloration, or other visual defects.
Fans	for broken fan blades.
Diagnostics	that all diagnostics are run periodically.

Table N-2

Recommended Maintenance Tool Kit

ITEM	QTY	DESCRIPTION	MFG. & PART No.
1	1	6" combination slip joint pliers	Utica # 5-6
2	2	5 1/2" needle nose pliers	Utica # 654-5 1/2
3	1	4" needle nose pliers	Utica # 23-4
4	1	5" diagonal wire cutters	Utica # 44-5
5	1	4" diagonal wire cutters	Utica # 347-4 CFJS
6	1	5" ignition pliers	Utica # 517-5
7	1	Screwdriver kit, including handle, 3/16", 1/4", 5/16" slotted #1, #2 phillips blades, each 4" long	Xcelite # 99 PV-6
8	1	3/32 slotted screwdriver with 2" blade	Xcelite # R3322
9	1	1/8" #0 phillips screwdriver	Xcelite # P12S
10	1	Magnetic pick up tool	Bonney # K26
11	1	3/32 through 3/8, 10 pc nut driver set	Xcelite # PS120
12	1	Xacto knife	
13	1	6" adjustable wrench	Utica # 91-6
14	1	Ignition wrench	Bonney # N24R
15	1	Set of 25 feeler gauges with 3" blades	Bonney # K53
16	1	Set of 15 hex keys	Bonney # N6R
17	1	Slotter 5" screw starter	Bonney # 5527
18	1	Phillips 6 1/4" screw starter	Bonney # 556
19	1	5" adjustable wire strippers	Utica # 110-5
20	1	Set of 4 cut needle files	Hunter # F228A
21	1	4 1/2" electrical tweezers	Hunter # B3M3
22	1	Flashlight	
23	1	Can Quick Freez (circuit cooler)	

Table N-2 (Continued)

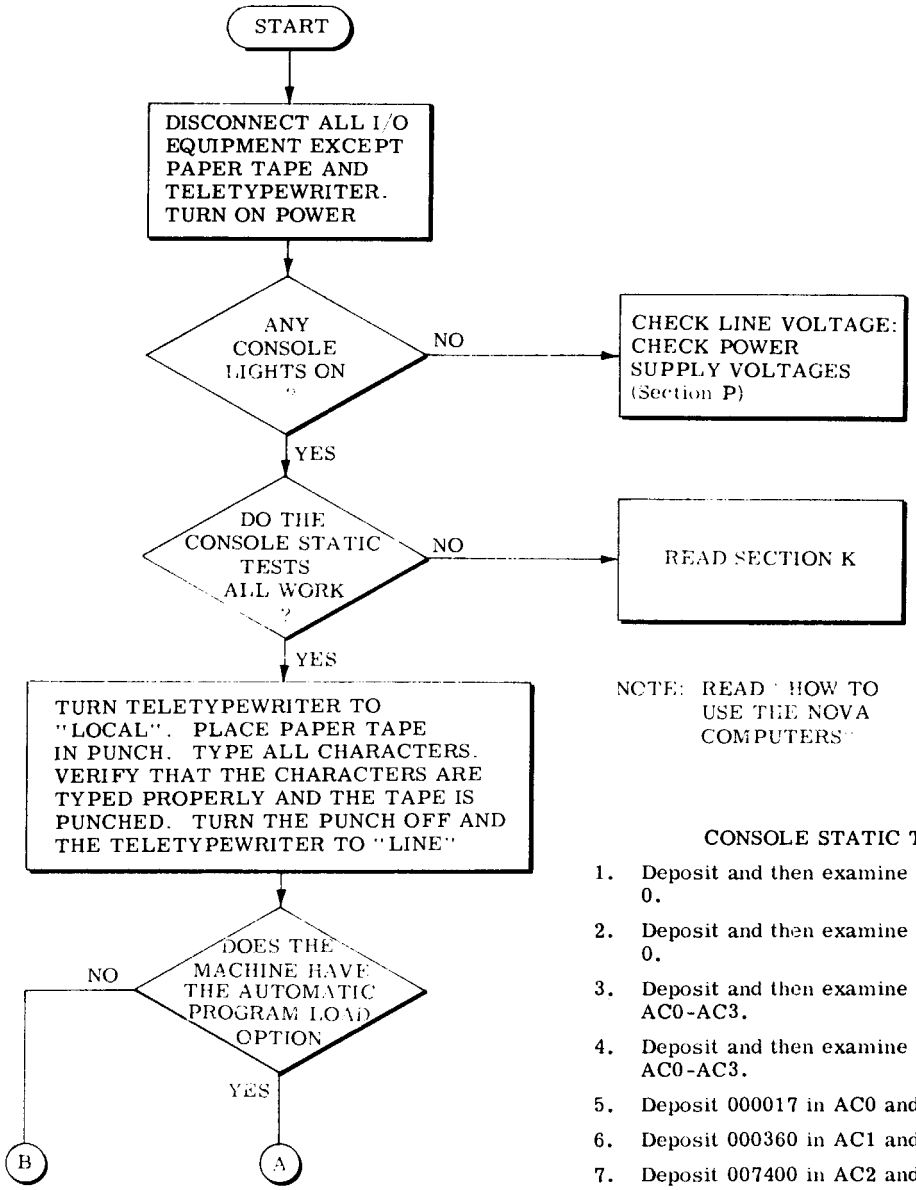
Recommended Maintenance Tool Kit

ITEM	QTY	DESCRIPTION	MFG. & PART No.
24	1	Can degreaser (flux remover)	
25	2	16P I/C test clip	
26	1	23 1/2 watt soldering iron with iron plated chisel tip	Ungar
27	1	47 1/2 watt soldering iron element	
28	1	1lb, 60/40 resin core solder	Kester
29	3	Spools of solder wick	
30	2	Acid brushes	
31	1	Vacuum solder removal tool	
32	1	Multimeter	Simpson # 260
33	1	Tool carrying case	
34	1	Oscilloscope	Tektronix # 453
35	1	Current probes	Tektronix # P60-22

Table N-3

Nova 2 Diagnostics

Diagnostic	Part No.	Binary Tape No.	Description
Address Test	096-000145	095-000002	Checks memory address selection logic
Exerciser	096-000144	095-000012	Tests CPU logic, Teletype, reader, punch, and real-time clock
Checkerboard III	097-000014	095-000031	Tests memory sense amplifiers and inhibit logic
Arithmetic Test	096-000146	095-000037	Exercises arithmetic and logic instructions in central processor
NOVA 1200 TTY Test	096-000152	095-000041	Tests Teletype logic, interrupt system, and I/O bus system
Checkerboard IV	096-000101	095-000132	Tests memory sense amplifiers and inhibit logic
NOVA 2 Logic Test	096-000110	095-000141	Tests CPU logic other than I/O
Checkerboard V	096-000137	095-000168	Tests memory sense amplifiers and inhibit logic



DG-00102

NOTE: READ "HOW TO USE THE NOVA COMPUTERS"

CONSOLE STATIC TESTS

1. Deposit and then examine 000000 in location 0.
2. Deposit and then examine 111111 in location 0.
3. Deposit and then examine 000000 in AC0-AC3.
4. Deposit and then examine 111111 in AC0-AC3.
5. Deposit 000017 in AC0 and verify.
6. Deposit 000360 in AC1 and verify.
7. Deposit 007400 in AC2 and verify.
8. Deposit 170000 in AC3 and verify.
9. Deposit 000000 in location 000000.
10. Raise START/CONTINUE switch to START. RUN indicator should be lit.
11. Lock the computer and try pushing the RESET/STOP switch. Computer should keep running.
12. Unlock the computer and hit STOP.
13. Depress DEPOSIT NEXT several times and check that the PC increments.
14. Depress EXAMINE NEXT several times and check that the PC increments.

Figure N-1 NOVA 2 Diagnostic Procedure

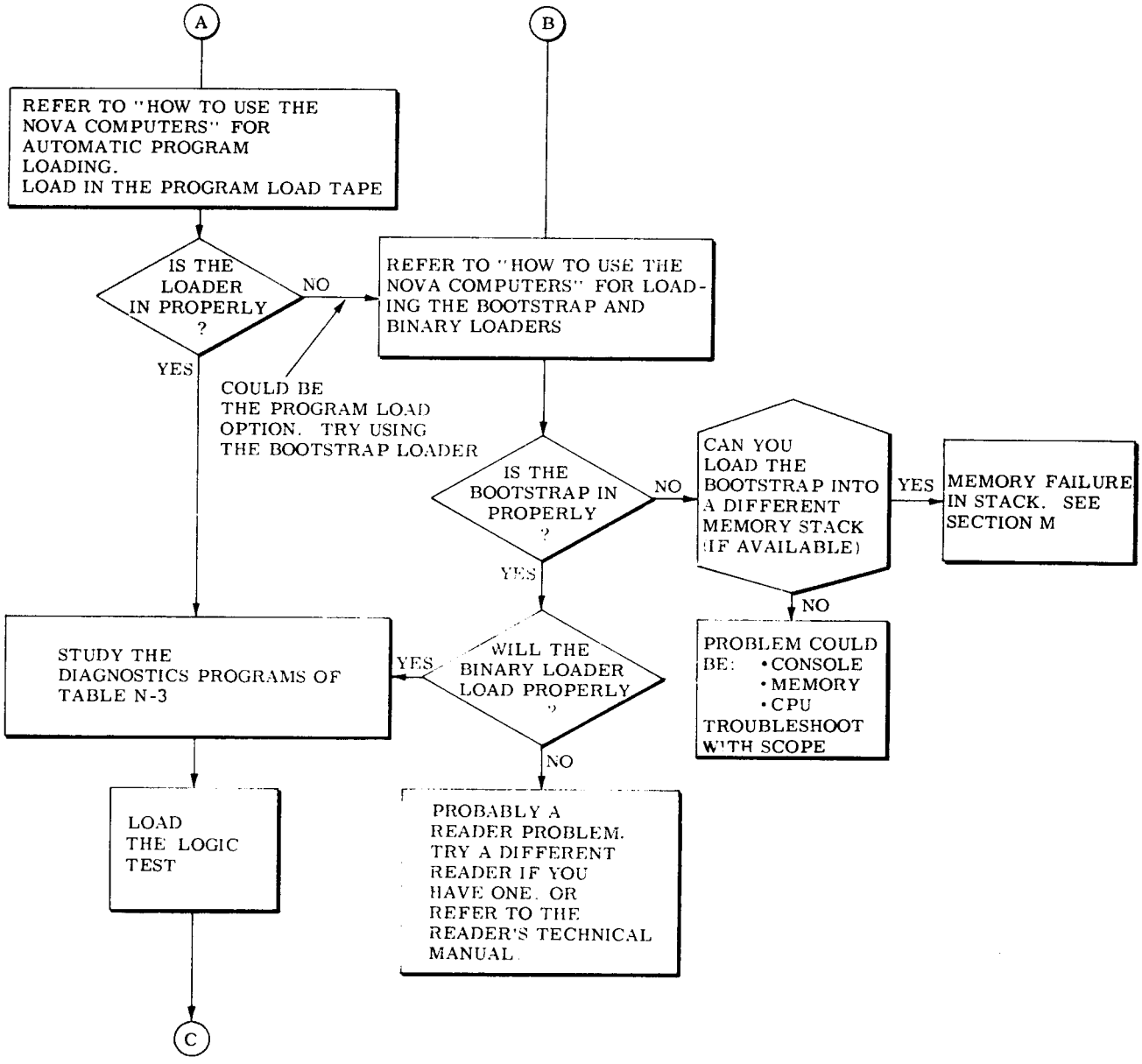


Figure N-1 NOVA 2 Diagnostic Procedure (Continued)

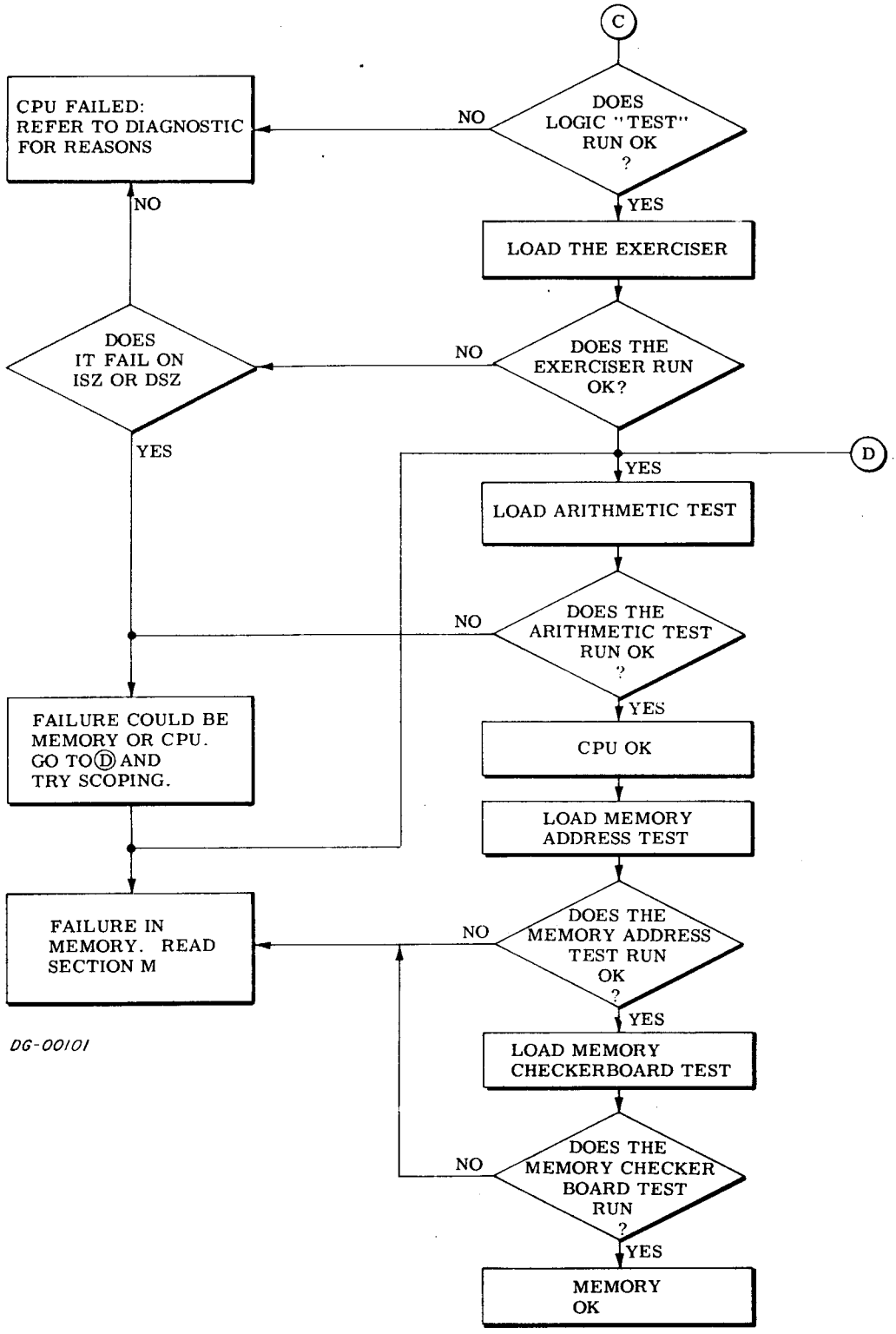


Figure N-1 NOVA 2 Diagnostic Procedure (Continued)

SECTION T

REFERENCE TABLES

INTRODUCTION

This section consists of three reference tables:

1. A signal list for the NOVA 2 central processor, page T-2.
2. A signal list for the NOVA 2 4K and 8K memories, page T-17.
3. A signal list for the NOVA 2 16K memory, page T-23.

Each signal list is an alphanumeric compilation of all signals found on each board, showing their sources and destinations. The source or destination location for a signal consists of two components. The first is the last three digits of the engineering drawing number and the page of that drawing. The second component is the grid reference on that sheet of the drawing.

The prime (') indicates that the signal name appears on the drawing as a barred signal; that is $\overline{\text{WRITE}}$ on the drawing is listed here as WRITE'.

The following engineering drawings, including revision numbers, are referenced by these signal lists:

1. Central Processor 001-000063-08
2. 4K and 8K Memory 001-000342-02
3. 16K Memory 001-000369-02

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
(C+I+M)'	363-2	D8	363-2	C7, D3
(CONT+MSTP+ISTP)'			363-2	D8
(TQC · (TQD'))'	363-1	C5	363-1	B7
1RADR0	363-2	A7	363-4	B4, B5, B6, B7, C4, C6, C7, C8
1RADR1	363-2	D5	363-4	B4, B5, B6, B7, C4, C6, C7, C8
1RADR2	363-2	D5	363-4	B4, B5, B6, B7, B8, C4, C7
.				
1REN'	363-2	A7	363-4	B3, B4, B6, B7, C4, C5, C6, C7
1WADR0	363-2	A8	363-4	B4, B5, B6, B7, B8
1WADR1	363-2	A8, C3, C6	363-4	B4, B5, B6, B7, B8
1WADR2	363-2	A8, C3	363-4	B4, B5, B6, B7, B8
1WEN'	363-2	A5, A6, B5, B6, C3, C6	363-4	B3, B4, B6, B7, C4, C5, C6, C7
2REN'	363-2	A5, A6, B5, B6, B7, C3	363-3	B8
			363-4	B3, B4, B6, B7, C4, C5, C6, C7
	363-3	B2		
2WEN'	363-2	A5, B4, B6, B7, B8, C3	363-4	B3, B4, B5, B6, B7
2WRADR0	363-2	B7	363-4	B3, B4, B5, B6, B7
2WRADR1	363-2	A5, B2, B5, B8, C8	363-4	B3, B4, B5, B6, B7
2WRADR2	363-2	A5,A8, B5	363-4	B3, B4, B5, B6, B7
A11	363-2	B1		
A12	363-2	B1		
A13	363-1	D2		
A14	363-1	C5		
A16	363-1	D6		
A17			363-2	D8
A19			363-2	C8
A20			363-2	D8
A22	363-2	C8		
A24	363-3	B2		
A25			363-2	D8
A27			363-2	D8
A28	363-2	B6		

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
A30			363-2	B8
A31			363-1	D8
A35	363-3	B4	363-3	B4
A36	363-3	B4	363-3	B4
A37	363-4	B2		
A38	363-3	B2		
A39	363-4	B2		
A40	363-3	C2		
A41	363-4	A2		
A42	363-3	D2		
A43	363-4	B2		
A44	363-3	D2		
A45	363-3	B5	363-3	B5
A46	363-3	D6		
A47	363-1	B5		
A48	363-3	D2		
A50	363-3	C2		
A51	363-3	B5	363-3	B5
A52	363-3	C2		
A53	363-3	B5	363-3	B5
A54	363-3	D2		
A55	363-3	B5	363-3	B5
A56	363-3	D2		
A57	363-1	C6		
A58	363-3	D2		
A60	363-2	C2		
A61			363-2	C7
A62	363-3	C6		
A64	363-3	C6		
A65			363-3	B8
A66	363-3	D6		
A68	363-3	D6		
A69	363-1	C5		
A70	363-3	B2		
A71			363-1	D8
A72	363-3	D6		
A74	363-3	C2		
A75	363-1	C2		
A79	363-1	C2		
A80			363-5	C7
A82			363-5	C7
A83			363-5	B6
A86	363-1	B2		
A9			363-1	B4, D8
			363-2	B8
A92	363-1	D5		
AEQB	363-4	C6	363-5	C8

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
ALU CARRY	363-2	B2, B3, B6, C8	363-4	C4, D2
ALU MODE	363-2	A6, B6	363-4	C4, C5, C7, C8
ALU0'	363-4	D7	363-4	D3, D5
ALU1'	363-4	D7	363-4	D5
			363-5	C8
ALU10'	363-4	D5	363-4	D7
			363-5	C3
ALU11'	363-4	D5	363-4	D7
			363-5	B8, D8
ALU12'	363-4	D4	363-4	D6,
			363-5	B8, D6
ALU13'	363-4	D4	363-4	D6
			363-5	B8
ALU14'	363-4	D3	363-4	D6
			363-5	C8
ALU15'	363-4	D3	363-4	D6
ALU2'	363-4	D7	363-4	D5
			363-5	C8
ALU3'	363-4	D7	363-4	D4
			363-5	C8
ALU4'	363-4	D6	363-4	D4
ALU5'	363-4	D6	363-4	D4
ALU6'	363-4	D6	363-4	D3
ALU7'	363-4	D6	363-4	D3
ALU8'	363-4	D5	363-4	D8
			363-5	C8
ALU9'	363-4	D5	363-4	D7
			363-5	C8
ALUS0	363-2	B6	363-4	D8
ALUS1	363-2	B6	363-4	C8
ALUS2	363-2	B6, C8	363-4	C8
ALUS3	363-2	B6, C8	363-4	C8
AND'	363-2	A6	363-4	C8
			363-5	A5
AUTO	363-5	D6	363-2	D5

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
AUTO DEC'	363-5	D5	363-2	A6
AUTO EN'	363-2	A4	363-5	D8
AUTO'	363-5	D6	363-2	A5, B3, D4
B MEMEN'	363-2	C2		
B WRITE	363-1	B5		
B11	363-3	C5		
B12	363-4	B2		
B13	363-3	C5		
B14	363-4	C2		
B15	363-2	B7		
B16	363-4	C2		
B17			363-2	B4
B18	363-3	B4	363-3	B4
B19	363-2	B7		
B21			363-2	B4
B22	363-3	B6	363-3	B6
B24	363-3	B6	363-3	B6
B26	363-3	B6	363-3	B6
B27	363-2	D6		
B28	363-3	B6	363-3	B6
B29			363-1	D6
B30	363-2	B1		
B32	363-4	C2		
B33	363-2	A2		
B35			363-1	A8
B37	363-2	B1		
B38			363-2	B8
B39	363-2	B1		
B41	363-2	A3		
B42	363-4	C2		
B43	363-4	C2		
B44	363-4	C2		
B45	363-2	C2		
B46			363-5	A6
B47	363-3	B7	363-3	B7
B48			363-5	A6
B49	363-1	A6		
B5	363-4	B2		
B51	363-2	D5		
B52	363-2	A8		
B53			363-2	D7
B54	363-2	A7		
B55	363-3	B6	363-3	B6

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
B56	363-3	B4	363-3	B4
B57	363-3	B6	363-3	B6
B58	363-3	B5	363-3	B5
B59	363-3	B4	363-3	B4
B60	363-3	B5	363-3	B5
B61	363-3	B6	363-3	B6
B62	363-3	B7	363-3	B7
B63	363-3	B5	363-3	B5
B64	363-3	B4	363-3	B4
B65	363-3	B7	363-3	B7
B66	363-3	B4	363-3	B4
B67	363-2	B8		
B68	363-3	B7	363-3	B7
B69	363-2	A2		
B7			363-1	B8
B70	363-3	B7	363-3	B7
B71	363-3	B7	363-3	B7
B73	363-3	B7	363-3	B7
B74	363-2	B5		
B75	363-3	B5	363-3	B5
B76	363-3	B4	363-3	B4
B77	363-4	D2		
B8	363-4	B2		
B82	363-3	B7	363-3	B7
B83	363-2	D7		
B87	363-1	A6		
B88	363-2	D7		
B9	363-4	B2		
B90	363-1	A5		
B95	363-3	B6	363-3	B6
BRMW'	363-2	B1		
C CLEAR'			363-5	A6
C SET'			363-5	B6
CALC	363-2	B2	363-2	B7
			363-4	D8,
			363-5	B8, C5
CALC'	363-2	B2	363-2	A7, B7
CLEAR DCH'			363-1	A7
CLEAR DEFER'	363-2	A4	363-1	C4
			363-5	D8
CLEAR SKIP	363-2	A5	363-5	C4
CLR	363-3	C2		
CLR DCH	363-1	A7	363-2	D7
CLR DCH'	363-2	C4		
CLR ION	363-3	C2	363-1	D7

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
CN+X	363-4	D2	363-4	C5
CN+Y	363-4	D2	363-4	C7
CN+Z	363-4	D2	363-4	D8
CONDATA'	363-2	B5, B6		
	363-3	C2	363-3	B8
CONINST'	363-2	C8		
CONMEN'	363-2	D6		
CONRQ'			363-2	D8
CPBQ'			363-2	D8
CPB0'	363-3	A7, B7,	363-1	C4
	363-4	A7, C8	363-3	A7
			363-4	A7, C8
CPB1'	363-3	A7, B7,	363-3	A7
	363-4	C8	363-4	B8, C8
CPB10'	363-3	A5, B5,	363-3	A5
	363-4	C4	363-4	B5, C4
CPB11'	363-3	A5, B5,	363-3	A5
	363-4	C4	363-4	B5, C4
CPB12'	363-3	A4, B4,	363-3	A4
	363-4	C4	363-4	B4, C4
CPB13'	363-3	A4, B4,	363-3	A4
	363-4	C4	363-4	B4, C4
CPB14'	363-3	A4, B4,	363-3	A4, B4
	363-4	C3	363-4	C3
CPB15'	363-3	A4, B4,	363-3	A4
	363-4	C3	363-4	B3, C3
CPB2'	363-3	A7, B7,	363-3	A7
	363-4	C7	363-4	B7, C7
CPB3'	363-3	A7, B7,	363-3	A7
	363-4	C7	363-4	B7, C7
CPB4'	363-3	A6, B6,	363-3	A6
	363-4	C7	363-4	B6, C7
CPB5'	363-3	A6, B6,	363-3	A6
	363-4	C7	363-4	B6, C7
CPB6'	363-3	A6, B6,	363-3	A6
	363-4	C6	363-4	B6, C6
CPB7'	363-3	A5, B6,	363-3	A5
	363-4	C6	363-4	B6, C6

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
CPB8'	363-3	A5, B5	363-3	A5
	363-4	C6	363-4	B5, C6
CPB9'	363-3	A5	363-3	A5
	363-4	B5, C6	363-4	B5, C6
CPU CLK	363-1	C6	363-1	A7, D3, D6, D7
			363-2	A4, B1, C2, C5, D6
			363-3	C8, D4
			363-5	A6, C4, D6, D7
CPU CLK2	363-1	B5	363-2	A3
CPU CLK'	363-2	B5	363-1	B6
			363-2	C7
			363-5	A6
CPU INST			363-3	C3
			363-5	C7
CRY OUT	363-4	C7	363-5	A5
CST1	363-2	D8		
CST2	363-2	C7		
CST3	363-2	C6	363-2	D3
CST3'	363-2	C5	363-2	D7
CST4	363-2	D7		
CST4'	363-2	C7		
D CPU CLK	363-1	C6		
DATA0'	363-3	B7	363-1	D4
			363-3	B7, C7
DATA1'	363-3	B7	363-1	D4
			363-3	B7, C7
DATA10'	363-3	B5	363-3	B5, C5
DATA11'	363-3	B5	363-3	B5, C5
DATA12'	363-3	B4	363-3	B4, C4
DATA13'	363-3	B4	363-3	B4, C4
DATA14'	363-3	B4	363-3	B4, C4
DATA15'	363-3	B4	363-3	B4, C4
DATA2'	363-3	B7	363-1	D4
			363-3	B7, C7
DATA3'	363-3	B7	363-3	B7, C7
DATA4'	363-3	B6	363-3	B6, C6
DATA5'	363-3	B6	363-3	B6, C6
DATA6'	363-3	B6	363-3	B6, C6

'Indicates "NOT"

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
DATA7'	363-3	B6	363-3	B6, C6
DATA8'	363-3	B5	363-3	B5, C5
DATA9'	363-3	B5	363-3	B5, C5
DATAIA	363-3	D2	363-3	C3
DATAIB	363-3	D2	363-3	C3
DATAIC	363-3	D2	363-3	B3
DATAOA	363-3	D2		
DATAOB	363-3	D2	363-3	B3
DATAOC	363-3	D2	363-3	B3
DCH	363-1	A6	363-2	A8, B8
DCH'	363-1	A6	363-2	C4, C5
DCH INH'	363-2	A4	363-1	A8
DCHA'	363-2	C2	363-2	B3, B8
DCHI	363-2	B1		
DCHM0'			363-2	B4
DCHM1'			363-2	B4
DCHO	363-2	A2		
DCHR'			363-1	A8
DECA'	363-2	A4, B4	363-2	A7
DEFER	363-1	C2	363-2	B1, B3, C5, D4, D5
DEFER'	363-1	C2	363-2	B5, D4
DISPXTND'	363-2	A6, A7	363-3	B7
DLIGHT'	363-2	B1		
DPE'	363-2	C4	363-2	C5
DQ0	363-2	C4	363-2	D3
DQ1	363-2	C4	363-2	C5
DQ1'	363-2	C5	363-2	D3
DRIVE'	363-3	A4		

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
DS0'	363-3	D6		
DS1'	363-3	D6		
DS2'	363-3	D6		
DS3'	363-3	D6		
DS4	363-3	C6		
DS5'	363-3	C6		
EFA	363-2	B2	363-1	C4
			363-2	B3
EFA'	363-2	B2	363-2	A7, B1, B7
			363-3	B7, B8
ENIR	363-3	C7	363-1	D3, D6
EXECUTE'	363-2	B1		
EXT	363-1	C7	363-1	D4
EXT'	363-1	C6	363-1	B7
			363-2	A3
EXTEND'	363-2	A6, C4	363-1	C8
F34'	363-2	B3, B5, B6	363-2	A8, B8
FAST			363-2	C3
FETCH	363-1	D2	363-1	B7
			363-2	A7, C5, D4, D5
FETCH'	363-1	D2	363-2	A5, A7, B3
FRQ'	363-2	C4	363-2	A4
G0'	363-4	C3	363-4	D2
G1'	363-4	C4	363-4	D2
G2'	363-4	C6	363-4	D2
HALT'	363-1	D8	363-1	D8
	363-2	C6		
	363-3	B2		
HLT PND	363-1	D7	363-1	B7
			363-2	C7
HLT PND'	363-1	D7	363-1	A8
HRST	363-2	D7		
HRST'	363-2	B7	363-1	A6, B3, B5, B7, C3, C7, D3, D5, D8
			363-2	C4, C6, D8
			363-3	C2
			363-5	C4, D5

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
IN'	363-2	A6	363-2 363-3	A1 B8, D4
INCA'	363-2	A4, B4	363-2	A7
INHTRNS'	363-2	C3	363-1	B6
INIT			363-1	D8
INIT'	363-2	B5		
INTA	363-3	C2		
INTR'			363-1	D6
IOALCEN'	363-2	A6	363-2 363-3	B1, B8 C4
ION	363-1	D7	363-5	C7
IOPLS	363-3	C2		
IORST	363-3	B2		
IOSKIP	363-3	D2	363-5	C5
IR0	363-3	C7	363-2	B3, B7, D5
IR0'	363-3	C7	363-2	A7
IR1	363-3	C7	363-2	B7
IR1'	363-3	C7	363-2	B3, B5, D5
IR10	363-3	C5	363-3	D5, D7
IR10'	363-3	C5	363-3 363-5	B5 B5
IR11	363-3	C5	363-3 363-5	C5, D7 B5
IR11'	363-3	C5	363-3	B5
IR12	363-3	C4	363-3	C5, D7
IR12'	363-3	C4	363-2 363-3 363-5	B7 B4 B8
IR13	363-3	C4	363-3 363-5	C5, D7 C6
IR13'	363-3	C4	363-3	B4
IR14	363-3	C4	363-3 363-5	C5, C7 C6
IR14'	363-3	C4	363-3	B4

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
IR15	363-3	C4	363-3	C5, C7
			363-5	C6
IR15'	363-3	C4	363-3	B4
IR2	363-3	C7		
IR2'	363-3	C7	363-2	B3, B5, D5
IR3	363-3	C7		
IR3'	363-3	C7	363-2	A8, B3, B5, B8
IR4	363-3	C6		
IR4'	363-3	C6	363-2	A8, B3, B5
IR5	363-3	C6	363-2	A7, B7
			363-3	D3
IR5'	363-3	C6	363-1	C4
			363-2	B3
IR6	363-3	C6	363-2	A7, B6
			363-3	D3
IR6'	363-3	C6	363-2	A7, B7, D3
IR7	363-3	C6	363-2	B7
			363-3	D3
IR7'	363-3	C6	363-2	A7, B7, D5
IR8	363-3	C5	363-3	C3
			363-4	D8
			363-5	C6
IR8'	363-3	C5	363-2	A7, A8
			363-3	B5
			363-5	C6
IR9	363-3	C5	363-3	C3
			363-4	D8
			363-5	C5
IR9'	363-3	C5	363-2	A7
			363-3	B5
			363-5	C5
ISTP'	363-2	D8	363-2	C6, C7, D8
J'	363-2	B3	363-2	D4
JSR'	363-2	B5	363-2	A8
			363-4	A8
KEY	363-2	D7	363-1	B8
			363-2	C7
KEY'	363-2	D7	363-2	D6

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
LOAD IR'	363-2	A5, C8	363-1	D5
			363-3	B8, C8
LSTC	363-2	C7	363-1	B7
M/D RET'			363-3	B8
MADR0'	363-4	C8	363-4	C8
MADR1'	363-4	C8	363-4	C8, D3
MADR10'	363-4	C4	363-2	C7
			363-4	B3, C4
MADR11'	363-4	C4	363-4	B3, C4
MADR12'	363-4	C4	363-4	B3, C4
MADR13'	363-4	C4	363-4	B3, C4
MADR14'	363-4	C3	363-4	B3, C3
MADR15'	363-4	C3	363-4	A3, C3
MADR2'	363-4	C7	363-4	C3, C7
MADR3'	363-4	C7	363-4	C3, C7
MADR4'	363-4	C7	363-4	C3, C7
MADR5'	363-4	C7	363-4	C3, C7
MADR6'	363-4	C6	363-4	C3, C6
MADR7'	363-4	C6	363-4	C3, C6
MADR8'	363-4	C6	363-4	C3, C6
MADR9'	363-4	C6	363-4	B3, C6
MASTER CLK'	363-1	C6	363-2	B2
			363-4	A8
MB LOAD'	363-2	C5		
MD0'			363-2	A8, B8
MD1'	363-2	B8		
MD2'	363-2	A8		
MDB'	363-2	A7		
MDBC'	363-2	A2		
MDR'	363-2	B7		
MDW'	363-2	A7		
MEM CLK	363-1	A6		
MEM OK			363-1	D8
			363-2	B8
MEM0'	363-3	B7	363-3	B7
MEM1'	363-3	B7	363-3	B7
MEM10'	363-3	B5	363-3	B5
MEM11'	363-3	B5	363-3	B5
MEM12'	363-3	B4	363-3	B4
MEM13'	363-3	B4	363-3	B4
MEM14'	363-3	B4	363-3	B4
MEM15'	363-3	B4	363-3	B4
MEM2'	363-3	B7	363-3	B7
MEM3'	363-3	B7	363-3	B7
MEM4'	363-3	B6	363-3	B6

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
MEM5'	363-3	B6	363-3	B6
MEM6'	363-3	B6	363-3	B6
MEM7'	363-3	B6	363-3	B6
MEM8'	363-3	B5	363-3	B5
MEM9'	363-3	B5	363-3	B5
MEMEN	363-2	D2	363-1	B3
			363-2	D7
MEMEN'	363-2	D3	363-3	B8
MONA	363-2	C3	363-2	B5
MONEN	363-2	D5	363-1	B3, C4
			363-2	A7, D5
			363-3	B8
MONEN'	363-2	D5	363-2	A7, B3, B5, D3
MONI'	363-2	C4	363-2	B2
			363-3	B8
MONO'	363-2	C4	363-2	A3
MONOZR'	363-2	C4	363-2	B2
MRI	363-1	D2	363-2	B5, D4
MRI'	363-1	C2	363-2	A7
MRIEN'	363-2	B5	363-2	B1
MSKO'	363-3	B2		
MSTP'	363-2	D8	363-2	C6, D7, D8
MUL DIV'			363-2	D7
OSC	363-1	A6	363-1	A4
			363-2	A3
OUT TIME'	363-1	B5	363-3	D4
OUT'	363-2	A6	363-1	A8, B6, C8
			363-2	A1
OVFLO	363-2	B1		
P0'	363-4	C3	363-4	D2
P1'	363-4	C4	363-4	D2
P2'	363-4	C6	363-4	D2
PI	363-1	D5	363-1	D7
PI'	363-1	D5	363-1	D4
			363-2	A5, A7
PL	363-2	C8		
PL ROMEN'	363-2	B5		
PL'			363-2	C6, C8
PTG HOLD'	363-2	A5, A6, B4	363-1	C3
PTS0	363-1	B2	363-2	A5,A7,B5,D3,D6
PTS1	363-1	B2, C2	363-2	B3
			363-3	C4

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
RESTART			363-2	B6
RESTART'			363-2	C6, D8
RMW'	363-2	B4, C3	363-1	A8, C8
			363-2	B1
RQ0'	363-2	A1	363-2	A3
RQENB	363-2	A3	363-1	A8
RQENB'	363-2	A3		
RST'			363-2	B8
RUN LIGHT	363-1	C5		
SCI'	363-5	B3	363-4	D3, D8
SELB'			363-5	C7
SELD'			363-5	C7
SET AUTO	363-5	D6	363-1	C4
SET AUTO'	363-5	D6	363-1	A8
			363-2	B1
SET FETCH	363-1	D3	363-1	B7
SET FETCH'	363-2	A6, B2, B4, B5	363-1	D4, D6
SET ION	363-3	C2	363-1	D7
SET SKIP	363-2	B3	363-5	C5
SKIP	363-5	C3	363-1	B7
SKIP'	363-5	C3	363-1	B7
			363-2	A6, D4
SLDCH'	363-2	C3	363-1	C8
SPECEN'	363-2	C4	363-2	A5
SPFIN CLR'	363-2	D6		
STDCH'	363-1	A7	363-2	D7
STOP'			363-1	D8
STRT	363-3	C2		
SUM0'	363-4	D8	363-4	B8
			363-5	B8
SUM1'	363-4	D7	363-4	B8
			363-5	B8
SUM10'	363-4	D5	363-4	B5
SUM11'	363-4	D4	363-4	B5
SUM12'	363-4	D4	363-4	B4
SUM13'	363-4	D4	363-4	B4
SUM14'	363-4	D3	363-4	B3
			363-5	B8
SUM15'	363-4	D3	363-4	B3
			363-5	B8

'Indicates "NOT"

NOVA 2 CENTRAL PROCESSOR

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
SUM2'	363-4	D7	363-4	B7
SUM3'	363-4	D7	363-4	B7
SUM4'	363-4	D6	363-4	B6
SUM5'	363-4	D6	363-4	B6
SUM6'	363-4	D6	363-4	B6
SUM7'	363-4	D6	363-4	B6
			363-5	C8
SUM8'	363-4	D5	363-4	B5
			363-5	C8
SUM9'	363-4	D5	363-4	B5
SYNC ENABLE			363-1	B8
SYNC ENABLE'	363-1	B3		
TQA	363-1	C5	363-1	B8
TQA'	363-1	C8	363-2	D7
TQC	363-1	C5	363-1	C6, C7
			363-2	A3
TQC'	363-1	C8	363-1	B4
			363-2	C5
TQD	363-1	C6	363-1	B6
WE'	363-1	A5		
WRITE'	363-2	A4, B4, B5, C4	363-1	B6
			363-3	B8
ZC	363-4	D3	363-5	B7, C6
ZERO BIT'	363-2	A4	363-4	A8
ZR	363-5	C6	363-2	B1

'Indicates "NOT"

8K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
+SL1			342-2	D7
+SL10			342-2	D4
+SL11			342-2	C4
+SL12			342-2	C4
+SL13			342-2	C4
+SL14			342-2	B4
+SL15			342-2	B4
+SL2			342-2	C7
+SL3			342-2	C7
+SL4			342-2	C7
+SL5			342-2	B7
+SL6			342-2	B7
+SL7			342-2	A7
+SL8			342-2	D4
+SL9			342-2	D4
+SL0			342-2	D7
-SL1			342-2	C7
-SL10			342-2	C4
-SL11			342-2	C4
-SL12			342-2	C4
-SL13			342-2	B4
-SL14			342-2	B4
-SL15			342-2	A4
-SL2			342-2	C7
-SL3			342-2	C7
-SL4			342-2	B7
-SL5			342-2	B7
-SL6			342-2	B7
-SL7			342-2	A7
-SL8			342-2	D4
-SL9			342-2	D4
-SL0			342-2	D7
A11			342-2	C7
A13			342-2	C7
A15			342-2	B7
A17			342-2	A7
A18			342-2	B7
A19			342-2	D4
A21			342-2	C4
A23			342-2	D4
A24			342-2	D4
A25			342-2	C4
A27			342-2	B4
A28			342-2	C4
A29			342-2	B4
A37			342-1	C3
A39			342-1	C3

8K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
A41			342-1	C3
A43			342-1	C3
A5			342-2	D7
A7			342-2	D7
A9			342-2	C7
B MEMEN	342-1	D6	342-1	A8
B MEMEN'			342-1	D7
B SELECT	342-1	C8		
B12			342-1	C5
B14			342-1	C5
B16			342-1	C6
B20			342-1	B8
B30			342-1	A6
B32			342-1	C6
B42			342-1	C6
B43			342-1	C6, D8
B44			342-1	D8
B45			342-1	D7
B5			342-1	C4
B55	342-1	B5	342-1	B5
B56	342-1	B3	342-1	B3
B57	342-1	B6	342-1	B6
B58	342-1	B4	342-1	B4
B59	342-1	B4	342-1	B4
B60	342-1	B5	342-1	B5
B61	342-1	B6	342-1	B6
B62	342-1	B7	342-1	B7
B63	342-1	B5	342-1	B4
B64	342-1	B3	342-1	B3
B65	342-1	B7	342-1	B7
B66	342-1	B3	342-1	B3
B7	342-1	A7		
B72			342-1	B8
B73			342-1	B6, B7
B74			342-1	B8
B75	342-1	B4	342-1	B4
B77			342-1	D8
B8			342-1	C4
B80			342-1	D7
B82	342-1	B7	342-1	B7
B83	342-1	C8		
B85	342-1	D8		
B86	342-1	A4	342-1	C8

' Indicates "NOT"

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
B87			342-1	D6
B88			342-1	D7
B9			342-1	C4
B90			342-1	A5
B95	342-1	B5	342-1	B5
BRMW'			342-1	A6
CONMEM	342-1	C8	342-1	C8
CONMEM'			342-1	C8
DATA0'	342-1	B7	342-1	B7
DATA1'	342-1	B7	342-1	B7
DATA10'	342-1	B4	342-1	B4
DATA11'	342-1	B4	342-1	B4
DATA12'	342-1	B4	342-1	B4
DATA13'	342-1	B3	342-1	B3
DATA14'	342-1	B3	342-1	B3
DATA15'	342-1	B3	342-1	B3
DATA2'	342-1	B7	342-1	B7
DATA3'	342-1	B6	342-1	B6
DATA4'	342-1	B6	342-1	B6
DATA5'	342-1	B6	342-1	B6
DATA6'	342-1	B5	342-1	B6
DATA7'	342-1	B5	342-1	B5
DATA8'	342-1	B5	342-1	B5
DATA9'	342-1	B5	342-1	B5
ENAB'	342-1	D5	342-1	B8
EXT MBLD'			342-1	B8
EXTERNAL SELECT'			342-1	D7
HOLD'	342-1	A6	342-1	D6
HRST			342-1	D7
INH SELECT'			342-1	D8
INH'	342-1	D3	342-2	A5, A8
INH0	342-1	B7	342-2	D8
INH1	342-1	B7	342-2	D8
INH10	342-1	B4	342-2	C5
INH11	342-1	B4	342-2	C5
INH12	342-1	B4	342-2	C5
INH13	342-1	B3	342-2	B5
INH14	342-1	B3	342-2	B5
INH15	342-1	B3	342-2	B5
INH2	342-1	B7	342-2	C8
INH3	342-1	B7	342-2	C8
INH4	342-1	B6	342-2	B8
INH5	342-1	B6	342-2	B8
INH6	342-1	B6	342-2	B8
INH7	342-1	B5	342-2	A8

'Indicates "NOT"

8K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
INH8	342-1	B5	342-2	D5
INH9	342-1	B5	342-2	D5
INHB0	342-2	D7		
INHB1	342-2	C7		
INHB11	342-2	C4		
INHB12	342-2	C4		
INHB13	342-2	B4		
INHB14	342-2	B4		
INHB15	342-2	A4		
INHB10	342-2	C4		
INHB2	342-2	C7		
INHB3	342-2	C7		
INHB4	342-2	B7		
INHB5	342-2	B7		
INHB6	342-2	B7		
INHB7	342-2	A7		
INHB8	342-2	D4		
INHB9	342-2	D4		
MA10	342-1	C4		
MA10'	342-1	C4	342-3	C8
MA10B	342-3	C8	342-3	B7, C7, D7
MA10B'	342-3	C7	342-3	B7, C7, D7
MA11	342-1	C4	342-3	D8
MA11B	342-3	D7	342-3	C7, D7
MA11B'	342-3	D8	342-3	B7, C7
MA12	342-1	C4	342-3	B8
MA12B	342-3	B8	342-3	C7, D7
MA12B'	342-3	B8	342-3	B7, C7
MA13	342-1	C3	342-3	A8
MA13B	342-3	A8	342-3	A3, A4, A5, A6
MA13B'	342-3	A7	342-3	A8
MA14	342-1	C3	342-3	A3, A6, A8
MA14B	342-3	A8	342-3	A4, A5,
MA14B'	342-3	A7, A8	342-3	A4
MA15	342-1	C3	342-3	A8
MA15B	342-3	A7	342-3	A3, A5
MA15B'	342-3	A8	342-3	A4, A6
MA3	342-1	C6	342-4	A7
MA3B	342-4	A6	342-5	A4, A5, A6
MA3B'	342-4	A7	342-4	A4, A5, A6
MA4	342-1	C6	342-4	A8
MA4B	342-4	A8	342-4 342-5	A4, A5, A3, A4
MA4B'	342-4	A8	342-4 342-5	A5, A6, A5, A6

'Indicates "NOT"

8K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
MA5	342-1	C6	342-4	A8
MA5B	342-4	A8	342-4	A4, A5, A6
			342-5	A4, A5, A6
MA5B'	342-4	A8	342-4	A4, A5, A6
			342-5	A3, A4, A5, A6
MA6	342-1	C5	342-4	A8
MA6B	342-4	A8	342-4	A4, A5
			342-5	A3, A5
MA6B'	342-4	A8	342-4	A5, A6
			342-5	A4, A6
MA7	342-1	C5	342-4	D8
MA7B	342-4	D7	342-4	C7, D7
MA7B'	342-4	D8	342-4	B7, C7
MA8	342-1	C5		
MA8'			342-4	C8
MA8B	342-4	C8	342-4	B7, C7, D7
MA8B'	342-4	C8	342-4	B7, C7, D7
MA9	342-1	C5	342-4	B8
MA9B	342-4	B8	342-4	C7, D7
MA9B'	342-4	B8	342-4	B7, C7
MAB1'			342-1	D8
MAB10'			342-1	C4
MAB11'			342-1	C4
MAB12'			342-1	C3
MAB13'			342-1	C3
MAB14'			342-1	C3
MAB15'			342-1	C3
MAB2'			342-1	D8
MAB3'			342-1	C6, D8
MAB4'			342-1	C6
MAB5'			342-1	C6
MAB6'			342-1	C5
MAB7'			342-1	C5
MAB8'			342-1	C5
MAB9'			342-1	C4
MALOAD	342-1	C7		
MEM CLK			342-1	C8, D6
MTG0	342-1	D6	342-1	A8, B8, C5, D5
MTG0'	342-1	C5	342-1	C6, C8, D3, D6
MTG1	342-1	D5	342-1	B8, D4
MTG1'	342-1	B8		
MTG2	342-1	D5	342-1	A4, A6, A8, D5
MTG3	342-1	D5	342-1	C3, D3, D6
MTG3'	342-1	D5	342-1	C8, D4

'Indicates "NOT"

8K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
READ 1B	342-1	D4	342-3 342-4	A7, B7
READ 2B	342-1	D4	342-4 342-5	A7, B7, A7
RELOAD DISABLE			342-1	B8
RINH0			342-2	D7
RINH1			342-2	D7
RINH10			342-2	D4
RINH11			342-2	C4
RINH12			342-2	C4
RINH13			342-2	C4
RINH14			342-2	B4
RINH15			342-2	B4
RINH2			342-2	C7
RINH3			342-2	C7
RINH4			342-2	C7
RINH5			342-2	B7
RINH6			342-2	B7
RINH7			342-2	A7
RINH8			342-2	D4
RINH9			342-2	D4
SELECT	342-1	D6	342-1	A8
SNS0'	342-2	D6	342-1	B7
SNS1'	342-2	D6	342-1	B7
SNS10'	342-2	D3	342-1	B4
SNS11'	342-2	C3	342-1	B4
SNS12'	342-2	C3	342-1	B4
SNS13'	342-2	B3	342-1	B3
SNS14'	342-2	B3	342-1	B3
SNS15'	342-2	B3	342-1	B3
SNS2'	342-2	C6	342-1	B7
SNS3'	342-2	C6	342-1	B7
SNS4'	342-2	C6	342-1	B6
SNS5'	342-2	B6	342-1	B6
SNS6'	342-2	B6	342-1	B6
SNS7'	342-2	A6	342-1	B5
SNS8'	342-2	D3	342-1	B5
SNS9'	342-2	D3	342-1	B4
STROBE	342-1	D4	342-2	A3, A6, C3, C6
SYNC ENABLE	342-1	A6		
WAIT'	342-1	A4	342-1	C8
WE'	342-1	B5		
WRITE	342-1	B8	342-1	B8
WRITE'			342-1	D5
WRITE MEM	342-1	D2	342-3	A7
			342-4	A7, B7
			342-5	A7

'Indicates "NOT"

16K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
+SL1			369-2	D7
+SL10			369-2	C4
+SL11			369-2	C4
+SL12			369-2	C4
+SL13			369-2	B4
+SL14			369-2	B4
+SL15			369-2	B4
+SL2			369-2	C7
+SL3			369-2	C7
+SL4			369-2	C7
+SL5			369-2	B7
+SL6			369-2	B7
+SL7			369-2	A7
+SL8			369-2	D4
+SL9			369-2	D4
+SL0			369-2	D7
-SL1			369-2	C7
-SL10			369-2	C4
-SL11			369-2	C4
-SL12			369-2	B4
-SL13			369-2	B4
-SL14			369-2	B4
-SL15			369-2	A4
-SL2			369-2	C7
-SL3			369-2	C7
-SL4			369-2	B7
-SL5			369-2	B7
-SL6			369-2	B7
-SL7			369-2	A7
-SL8			369-2	D4
-SL9			369-2	D4
-SL0			369-2	D7
A11			369-2	C7
A13			369-2	C7
A15			369-2	B7
A17			369-2	A7
A18			369-2	B7
A19			369-2	D4
A21			369-2	C4
A23			369-2	D4
A24			369-2	D4
A25			369-2	B4
A27			369-2	B4
A28			369-2	B4, C4
A37			369-1	B4
A39			369-1	B3
A41			369-1	B4

16K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
A43			369-1	B4
A5			369-2	D7
A7			369-2	D7
A9			369-2	C7
A93	369-1	C8		
A94			369-1	C8
A95	369-1	C8		
A96			369-1	C8
B MEMEN	369-1	D7	369-1	D3
B MEMEN'			369-1	D8
B SELECT	369-1	B7	369-1	B8
B12			369-1	B6
B14			369-1	B7
B16			369-1	B7
B20			369-1	B8
B30			369-1	C6
B32			369-1	B5
B42			369-1	B5
B43			369-1	B5
B44			369-1	B6
B45			369-1	D8
B5			369-1	B3
B55	369-1	B5		
B56	369-1	B3		
B57	369-1	B6		
B58	369-1	B4		
B59	369-1	B4		
B60	369-1	B5		
B61	369-1	B6		
B62	369-1	B7		
B63	369-1	B4		
B64	369-1	B3		
B65	369-1	B7		
B66	369-1	B3		
B7	369-1	D2		
B72			369-1	A8
B73	369-1	B6		
B74			369-1	A8
B75	369-1	B4		
B77			369-1	D8
B8			369-1	B3
B80			369-1	D8
B82	369-1	B7		
B83			369-1	D8
B85			369-1	D8
B86	369-1	D2		

'Indicates "NOT"

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
B87			369-1	D6
B88			369-1	D6
B9			369-1	B4
B90			369-1	C6
B95	369-1	B5		
BRMW'			369-1	C6
CONMEM	369-1	D7	369-1	B8
CONMEM'			369-1	D8
DATA0'	369-1	B7	369-1	A7
DATA1'	369-1	B7	369-1	A7
DATA10'	369-1	B4	369-1	A4
DATA11'	369-1	B4	369-1	A4
DATA12'	369-1	B4	369-1	A3
DATA13'	369-1	B3	369-1	A3
DATA14'	369-1	B3	369-1	A3
DATA15'	369-1	B3	369-1	A3
DATA2'	369-1	B7	369-1	A7
DATA3'	369-1	B6	369-1	A6
DATA4'	369-1	B6	369-1	A6
DATA5'	369-1	B6	369-1	A5
DATA6'	369-1	B5	369-1	A5
DATA7'	369-1	B5	369-1	A5
DATA8'	369-1	B5	369-1	A5
DATA9'	369-1	B4	369-1	A4
ENAB	369-1	D6		
ENAB'	369-1	D5	369-1	A8
ENDC	369-1	D2	369-1	B8, D6
EXT MBLD'			369-1	B8
EXT SELECT'			369-1	D8
HOLD'	369-1	C5	369-1	D6
HRST			369-1	D6
INH SEL'			369-1	D8
INH'	369-1	C3	369-2	A5, A8
INH0	369-1	B7	369-2	D8
INH1	369-1	B7	369-2	D8
INH10	369-1	B4	369-2	D5
INH11	369-1	B4	369-2	C5
INH12	369-1	B3	369-2	C5
INH13	369-1	B3	369-2	B5
INH14	369-1	B2	369-2	B5
INH15	369-1	B3	369-2	B5
INH2	369-1	B7	369-2	C8
INH3	369-1	B6	369-2	C8

'Indicates "NOT"

16K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
INH4	369-1	B6	369-2	B8
INH5	369-1	B6	369-2	B8
INH6	369-1	B5	369-2	B8
INH7	369-1	B5	369-2	A8
INH8	369-1	B5	369-2	D5
INH9	369-1	B4	369-2	D5
INHB0	369-2	D7		
INHB1	369-2	C7		
INHB10	369-2	C4		
INHB11	369-2	C4		
INHB12	369-2	B4		
INHB13	369-2	B4		
INHB14	369-2	B4		
INHB15	369-2	A4		
INHB2	369-2	C7		
INHB3	369-2	C7		
INHB4	369-2	B7		
INHB5	369-2	B7		
INHB6	369-2	B7		
INHB7	369-2	A7		
INHB8	369-2	D4		
INHB9	369-2	D4		
MA10	369-1	C3	369-3 369-4	A3, A4, A3, A4
MA10'	369-1	C3	369-3 369-4	A5, A6, A5, A6
MA11	369-1	C3	369-3 369-4	A3, A5, A3, A5
MA11'	369-1	C3	369-3 369-4	A4, A6, A4, A6
MA12	369-1	C3	369-3 369-4	A4, A5, A6, A4, A5, A6
MA12'	369-1	C3	369-3 369-4	A4, A5, A6 A4, A5, A6
MA13	369-1	C4	369-3	C8, D8
MA13'	369-1	C5	369-3	B8, C8
MA14	369-1	C4	369-3	B8, C8, D8
MA14'	369-1	C4	369-3	B8, C8, D8
MA15	369-1	C4	369-3	C8, D8
MA15'	369-1	C4	369-3	B8, C8
MA2	369-1	C6	369-6	A4, A5, A6,
MA2'	369-1	C6	369-5	A4, A5, A6
MA3	369-1	C6	369-5 369-6	A3, A4, A3, A4
MA3'	369-1	C6	369-5 369-6	A5, A6, A5, A6

'Indicates "NOT"

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
MA4	369-1	C6	369-5	A4, A5,
			369-6	A4, A5, A6
MA4'	369-1	C6	369-5	A4, A5, A6,
			369-6	A3, A4, A5, A6
MA5	369-1	C5	369-5	A5,
			369-6	A3, A5
MA5'	369-1	C5	369-5	A3, A4, A6,
			369-6	A4, A6
MA6	369-1	C7	369-5	B8, C8, D8
MA6'	369-1	C7	369-5	B8, C8, D8
MA7	369-1	C7	369-5	C8, D8
MA7'	369-1	C7	369-5	B8, C8
MA8	369-1	C7	369-5	C8, D8
MA8'	369-1	C7	369-5	B8, C8
MA9	369-1	C4	369-4	A4, A5, A6
MA9'	369-1	C4	369-3	A4, A5, A6
MAB1'			369-1	D8
MAB10'			369-1	B3
MAB11'			369-1	B3
MAB12'			369-1	B3
MAB13'			369-1	B4
MAB14'			369-1	B4
MAB15'			369-1	B4
MAB2			369-1	B6
MAB3'			369-1	B5
MAB4'			369-1	B5
MAB5'			369-1	B5
MAB6'			369-1	B7
MAB7'			369-1	B7
MAB8'			369-1	B6
MAB9'			369-1	B3
MEM CLOCK			369-1	B8, D6
MTG0	369-1	D4	369-1	A8, D3
MTG0'	369-1	D4	369-1	B8, C3, D6
MTG1	369-1	D4	369-1	D3
MTG1'	369-1	D4	369-1	A8
MTG2	369-1	D4	369-1	D2, D4
MTG3	369-1	D4	369-1	C6, D3
MTG3'	369-1	D4		
MTG4	369-1	D4	369-1	D2, D4, D6
MTG5	369-1	D4		
READ1B	369-1	D3	369-4	A2
			369-5	B8
READ2B	369-1	D3	369-6	A7
RELOAD DISABLE'			369-1	A8

'Indicates "NOT"

16K MEMORY

SIGNAL LIST

	SOURCE		DESTINATION	
	PAGE	GRID	PAGE	GRID
RINH0			369-2	D7
RINH1			369-2	D7
RINH10			369-2	D4
RINH11			369-2	C4
RINH12			369-2	C4
RINH13			369-2	B4
RINH14			369-2	B4
RINH15			369-2	B4
RINH2			369-2	C7
RINH3			369-2	C7
RINH4			369-2	C7
RINH5			369-2	B7
RINH6			369-2	B7
RINH7			369-2	A7
RINH8			369-2	D4
RINH9			369-2	D4
SELECT	369-1	D7	369-1	B8, D3
SNS0'	369-2	D6	369-1	A7
SNS1'	369-2	D6	369-1	A7
SNS10'	369-2	C3	369-1	A4
SNS11'	369-2	C3	369-1	A4
SNS12'	369-2	C3	369-1	A3
SNS13'	369-2	B3	369-1	A3
SNS14'	369-2	B3	369-1	A3
SNS15'	369-2	A3	369-1	A3
SNS2'	369-2	C6	369-1	A7
SNS3'	369-2	C6	369-1	A7
SNS4'	369-2	C6	369-1	A6
SNS5'	369-2	B6	369-1	A6
SNS6'	369-2	B6	369-1	A5
SNS7'	369-2	A6	369-1	A5
SNS8'	369-2	D3	369-1	A5
SNS9'	369-2	D3	369-1	A4
STRB	369-1	D3	369-2	A3, A6
SYNC ENABLE'	369-1	D2		
WAIT'	369-1	D2	369-1	C8
WE'			369-1	C6
WRITE	369-1	B7	369-1	A8, C4
WRITE MEM	369-1	C3	369-4	B2,
			369-5	A7
			369-6	A7
WRITE MEM YA			369-5	B7
WRITE'			369-1	B8

'Indicates "NOT"

READERS COMMENT FORM

DOCUMENT TITLE: .....

Your comments, accompanied by answers to the following questions, help us improve the quality and usefulness of our publications. If your answer to a question is "no" or requires qualification, please explain.

How did you use this publication?

( ) As an introduction to the subject.
( ) As an aid for advanced knowledge.
( ) For information about operating procedures.
( ) To instruct in a class.
( ) As a student in a class.
( ) As a reference manual.
( ) Other.....

Did you find the material:

- Useful.....YES ( ) NO ( )
- Complete.....YES ( ) NO ( )
- Accurate.....YES ( ) NO ( )
- Well organized.....YES ( ) NO ( )
- Well written.....YES ( ) NO ( )
- Well illustrated.....YES ( ) NO ( )
- Well indexed.....YES ( ) NO ( )
- Easy to read.....YES ( ) NO ( )
- Easy to understand.....YES ( ) NO ( )

We would appreciate any other comments; please label each comment as an addition, deletion, change, or error and reference page numbers where applicable.

COMMENTS

PAGE	COL	PARA	LINE	FROM	TO

From:

NAME..... TITLE.....
FIRM..... DIV. .....
ADDRESS.....
CITY..... STATE..... ZIP.....
TELEPHONE..... DATE.....

Data General Corporation
ENGINEERING PUBLICATIONS
COMMENT FORM
DG-00935

CUT ALONG DOTTED LINE

FOLD DOWN FIRST FOLD DOWN

FIRST CLASS
PERMIT NO. 26
SOUTHBORO
MASS. 01772

NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES

BUSINESS REPLY MAIL

Postage will be paid by:

DataGeneral
Southboro, Massachusetts 01772

ATTENTION: Engineering Publications

FOLD UP SECOND FOLD UP

STAPLE