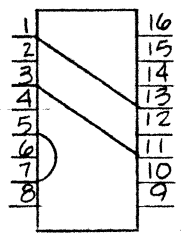
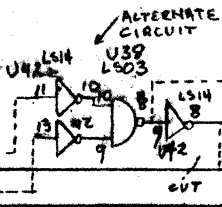


FOR U-BUS REMOVE U37 AND JUMPER LOCATION AS SHOWN BELOW.



NOTE FOR U46, U47 DMB136 CUT TRACES & INSTALL ALTERNATE CIRCUIT



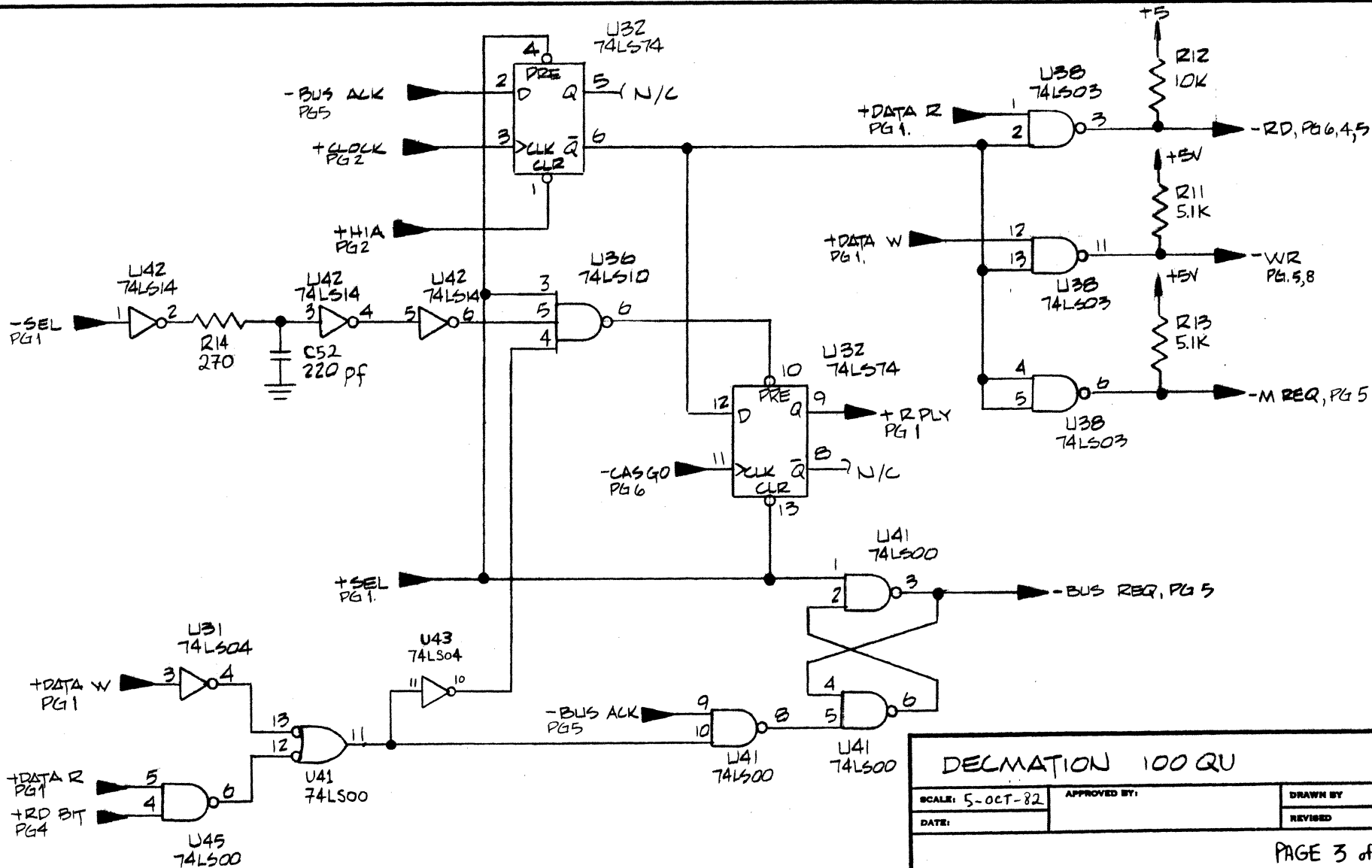
J12 - ADDRESS SELECTION JUMERS

BIT	Q-BUS	U-BUS
3	14	2
14	6	3
15	4	6
16	3	7
7	7	14
8	5	5
19	13	4
10	11	13
11	15	12
12	12	11
13	-	10
14	-	15

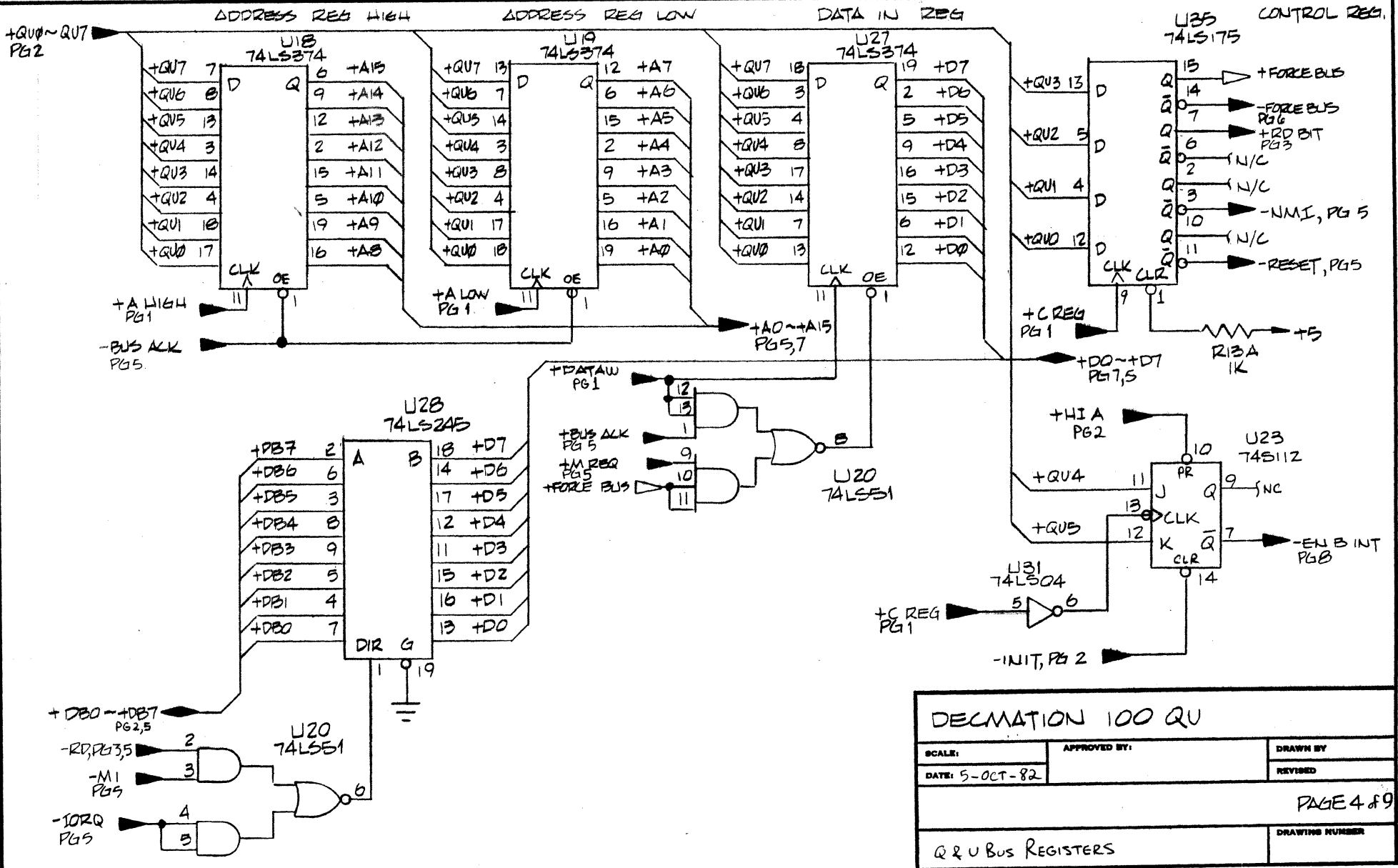
J12 pins 2 & 10 must be low for Q-Bus
 1 = set to low at factory (logic high); gives address 7FF16x

DECLAMATION 100QU REV B

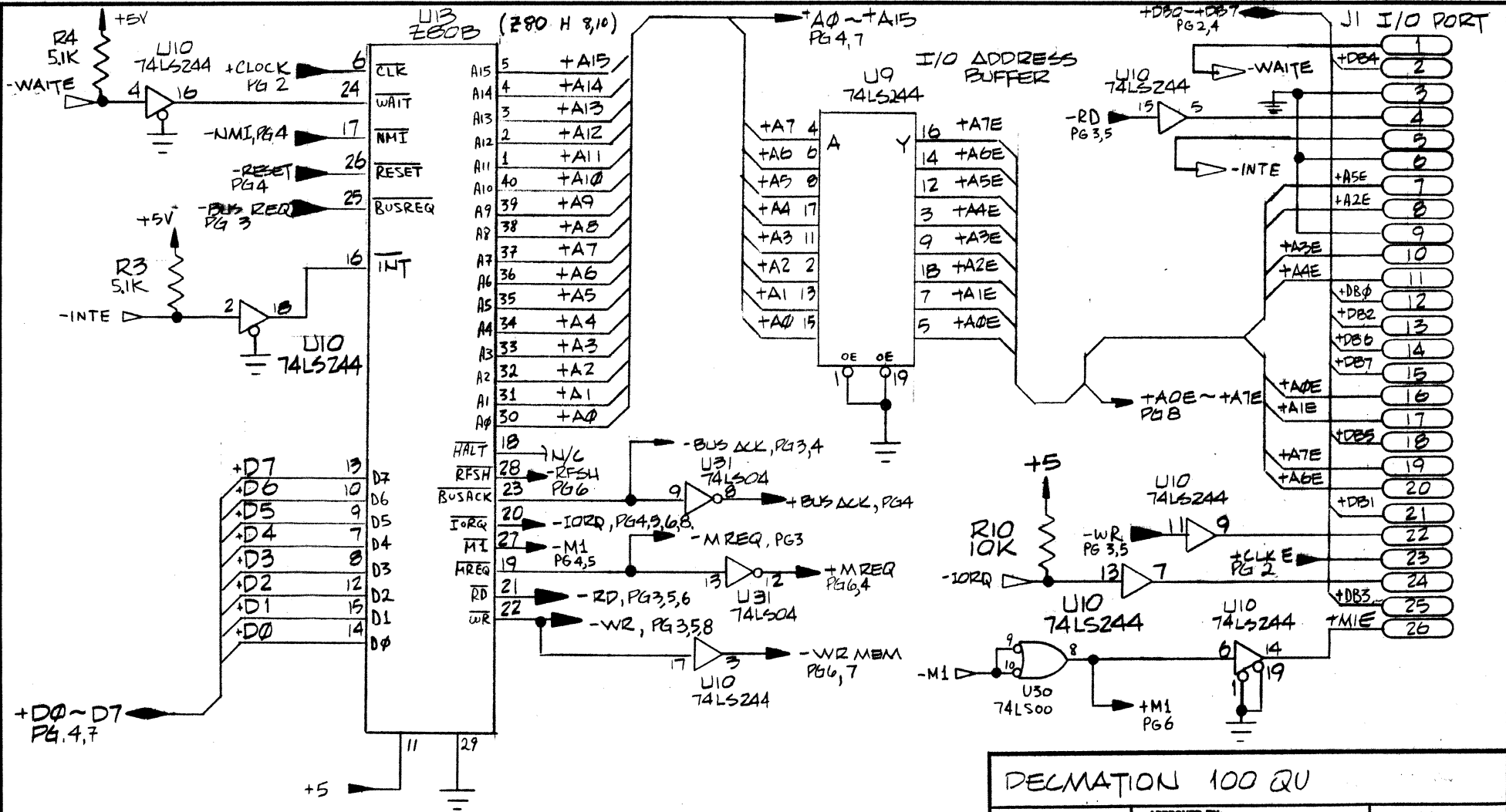
SCALE:	APPROVED BY:	DRAWN BY:
DATE: 16-MAY-83		REVISED:
PAGE 1 of 9		
Q&U Bus Address Decoding		DRAWING NUMBER:



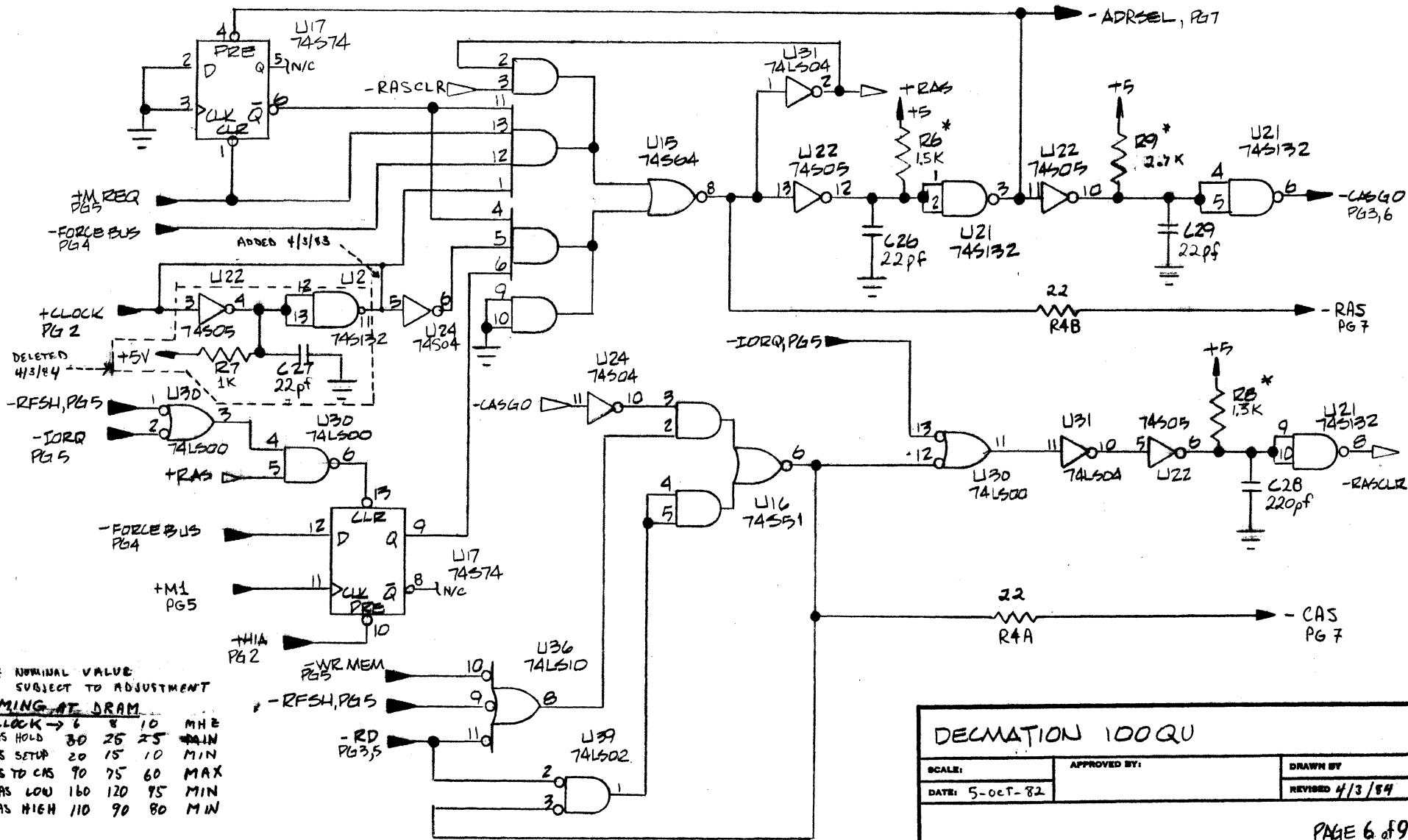
DECMA100 QU		
SCALE: 5-OCT-82	APPROVED BY:	DRAWN BY
DATE:		REVISED
PAGE 3 of 9		
DMA CONTROL LOGIC		DRAWING NUMBER



DECLARATION 100 QU		
SCALE:	APPROVED BY:	DRAWN BY:
DATE: 5-OCT-82		REVISED:
		PAGE 4 of 9
Q & U Bus Registers		DRAWING NUMBER:



DECLARATION 100 QU		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 5-OCT-82		REVISED 4/13/84
PAGE 5 of 9		
Z80 & I/O PORT		DRAWING NUMBER



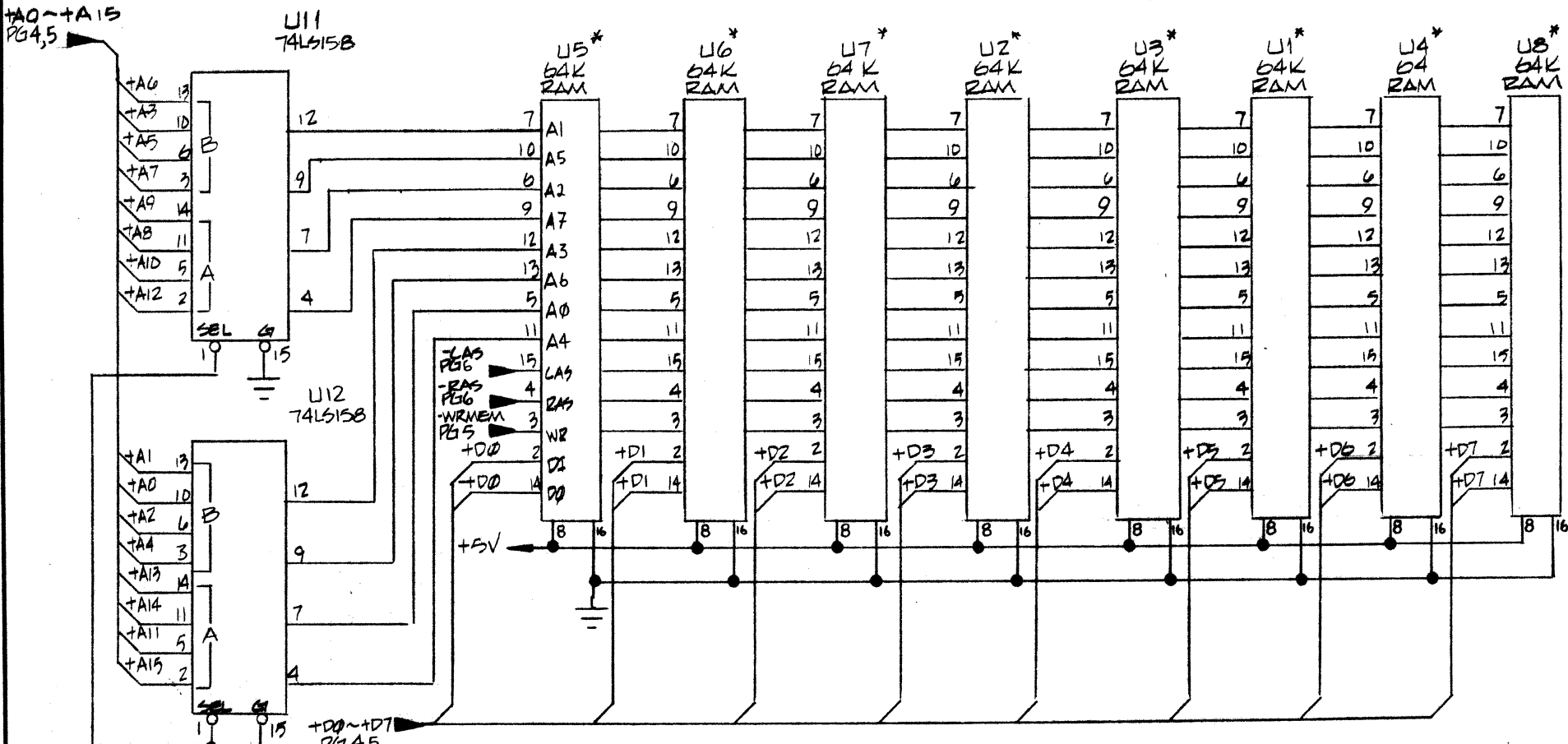
* NOMINAL VALUE SUBJECT TO ADJUSTMENT

TIMING AT DRAM

CLOCK →	6	8	10	MHZ
RAS HOLD	30	25	25	MIN
CAS SETUP	20	15	10	MIN
RAS TO CAS	90	75	60	MAX
RAS LOW	160	120	95	MIN
RAS HIGH	110	90	80	MIN

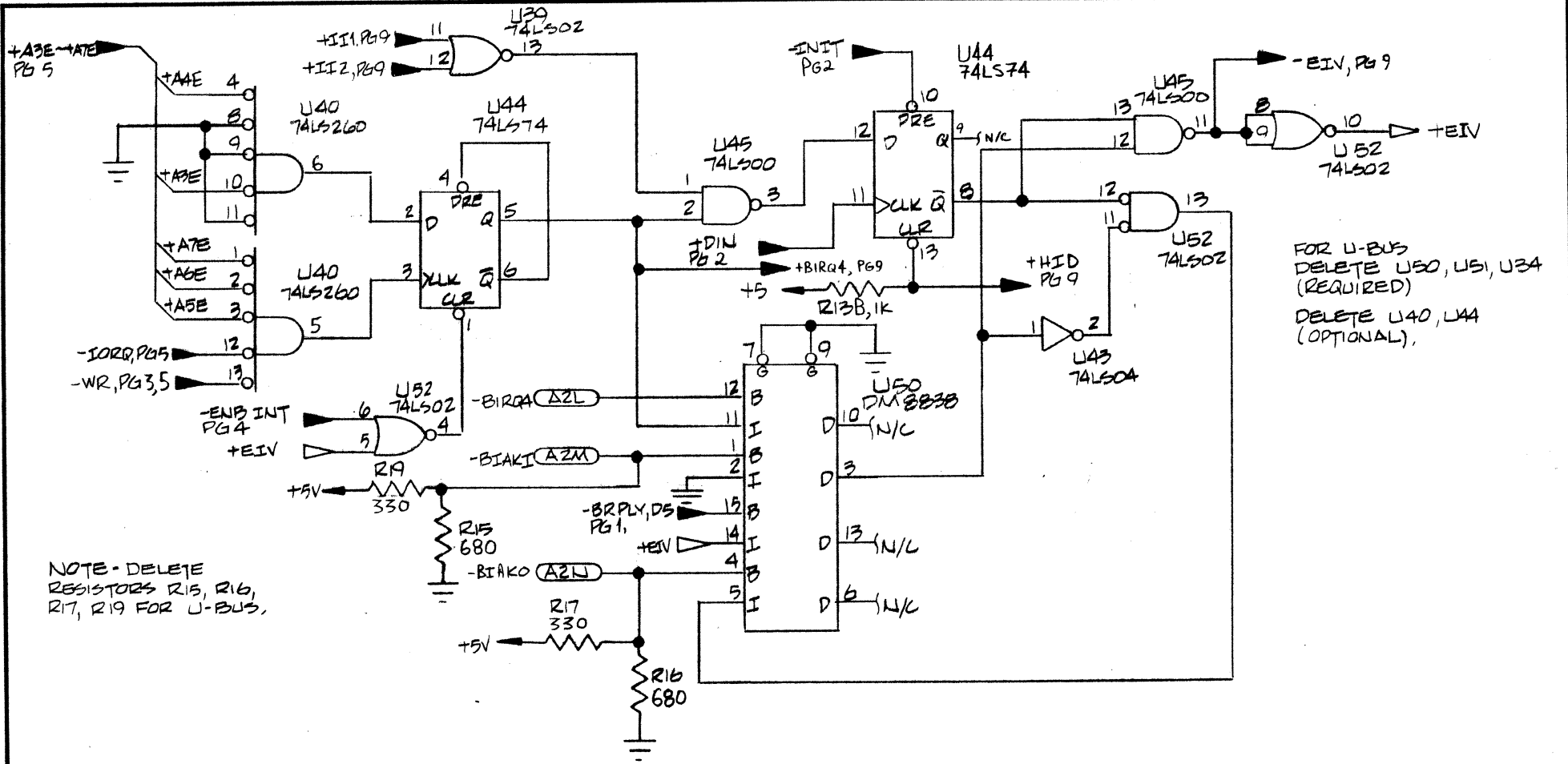
DECLARATION 100QU

SCALE:	APPROVED BY:	DRAWN BY
DATE: 5-oct-82		REVISED 4/3/84
PAGE 6 of 9		DRAWING NUMBER
DYNAMIC RAM TIMING GENERATION		



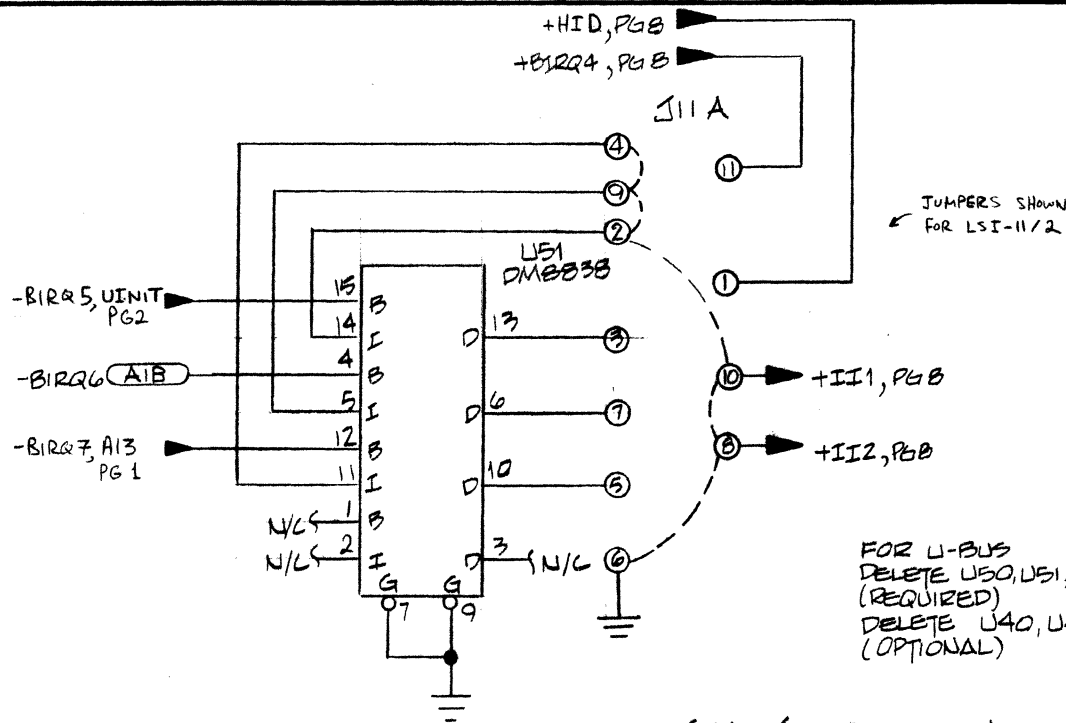
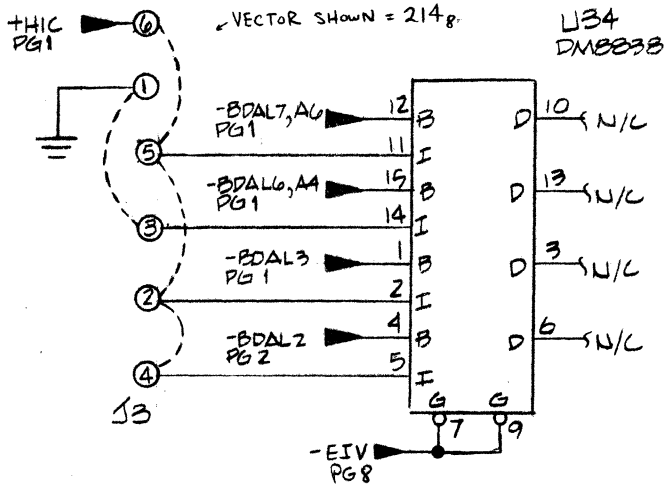
* 150 NS 6-MHZ CLOCK
 120 NS 8-MHZ CLOCK
 100 NS 10-MHZ CLOCK

DECIMATION 100 QU		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 5-OCT-82		REVISED 4/1/84
PAGE 7 of 9		
DYNAMIC RAMS		DRAWING NUMBER



NOTE - DELETE
RESISTORS R15, R16,
R17, R19 FOR U-BUS.

DECLAMATION 100 QU		
SCALE:	APPROVED BY:	DRAWN BY
DATE: 5-oct-82		REVISED
		PAGE 8 of 9
Q-BUS INTERRUPT LOGIC		DRAWING NUMBER



FOR U-BUS
DELETE U50, U51, U34
(REQUIRED)
DELETE U40, U44
(OPTIONAL)

INTERRUPT VECTOR (OCTAL)	INTERRUPT VECTOR SELECTION
	J3 JUMPER CHAIN
100	6-3/1-2-4-5
104	6-3-4/1-2-5
110	6-3-2/1-4-5
114	6-3-2-4/1-5
200	6-5/1-2-3-4
204	6-5-4/1-2-3
210	6-5-2/1-3-4
214	6-5-4-2/1-3
300	6-3-5/1-2-4
304	6-3-5-4/1-2
310	6-3-5-2/1-4
314	6-2-3-4-5/1-N/C

J11A JUMPER CHAIN

LSI-11/2	6-2-9-4-10-8 / N.C. 5,7,3,11,1
LSI-11/23 P4	6-2-9-4/3-10/7-8 / N.C. 5,1,11
INTERRUPT PRIORITY SELECTION.	P5 6-4-9-10/11-2/7-8 / N.C. 3,5,1
	P6 6-2-4-10/11-9/5-8 / N.C. 3,7,1
	P7 6-2-8-10/11-4-9 / N.C.

DECLARATION 100QU

SCALE:	APPROVED BY:	DRAWN BY:
DATE: 5-OCT-82		REVISED:
		pg 9 of 9
INTERRUPT VECTOR & PRIORITY SELECT		DRAWING NUMBER