

# **VAXBI MAINTENANCE GUIDE**

**(Preliminary)**

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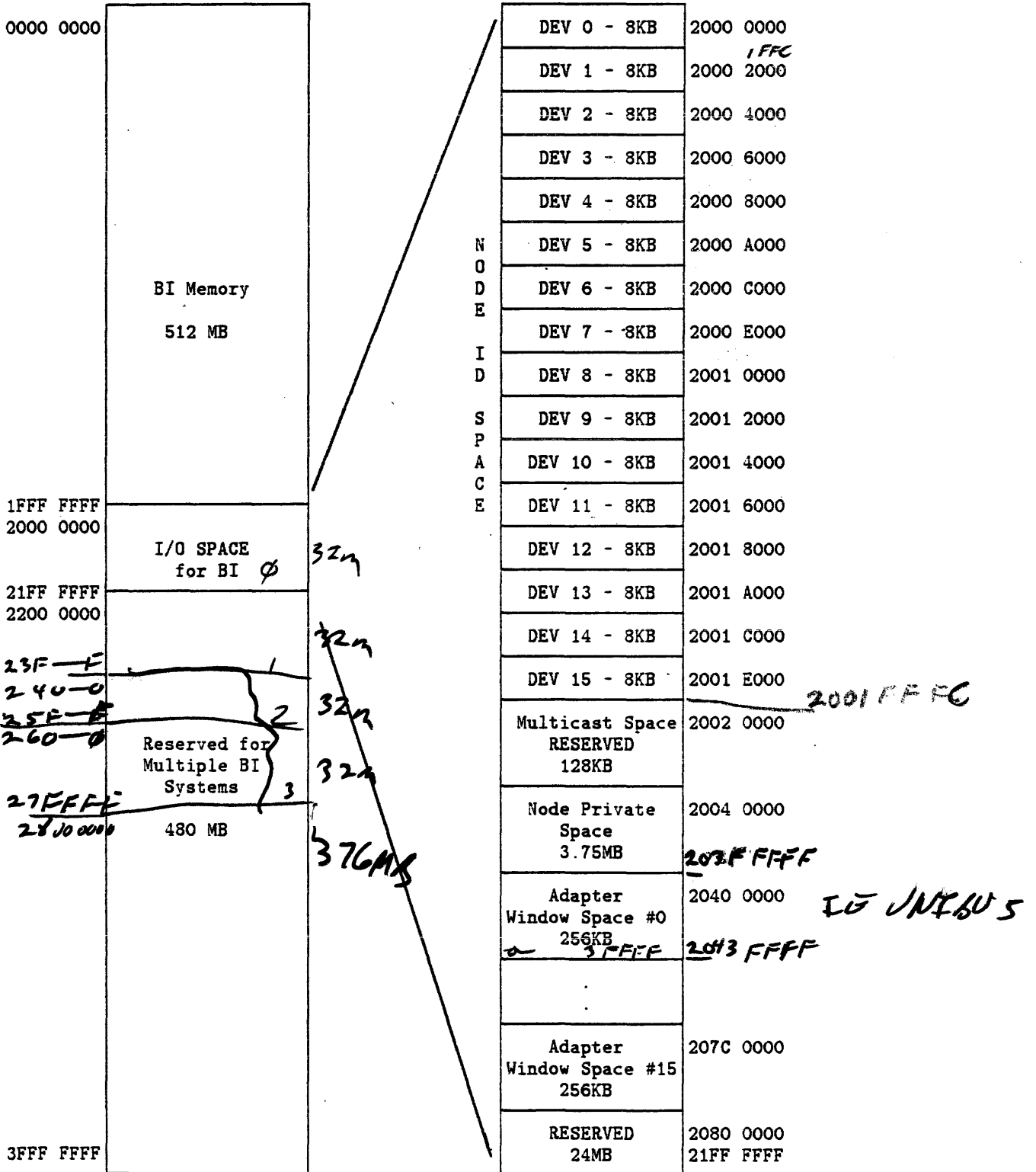
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8 TRANSACTION DESCRIPTIONS

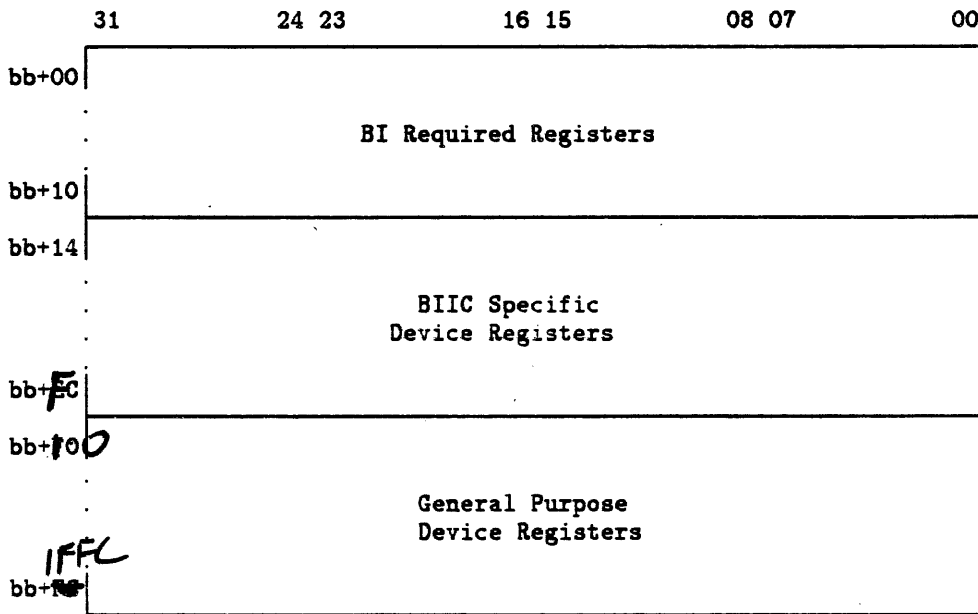
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9 TROUBLESHOOTING FLOWCHART ..... 33



bb = base address of node ID space  
(2000 0000 + 2000(H)\*NODE ID)

BIIC Register Map



*NODE 5*

$$2000\ 0000 + 2000 * 5 = 2000\ A000$$

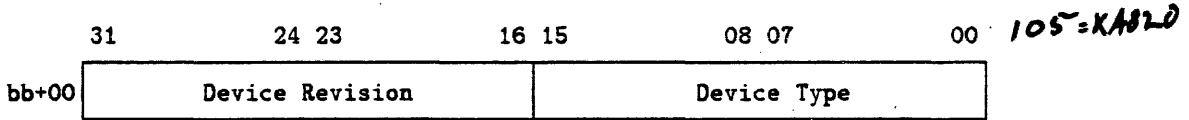
BI REQUIRED REGISTERS

	31	24 23	16 15	08 07	00
bb+00	Device Register				
bb+04	BI Control / Status Register				
bb+08	Bus Error Register				
bb+0C	Error Interrupt Control Register				
bb+10	Interrupt Destination Register				

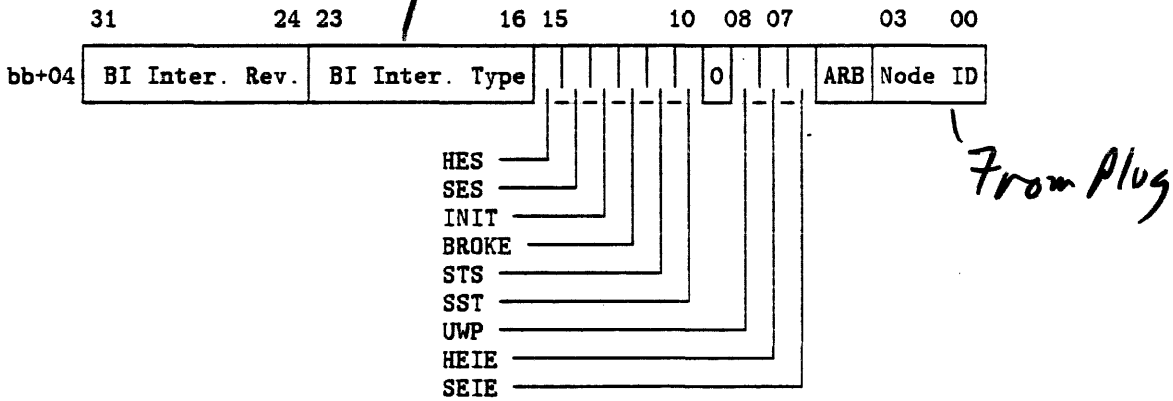
BIIC Specific Device Registers

	31	24 23	16 15	08 07	00
bb+14	IP Interrupt Mask Register				
bb+18	IP Interrupt Destination Register				
bb+1C	IP Interrupt Source Register				
bb+20	Starting Address Register				
bb+24	Ending Address Register				
bb+28	BCI Control Register				
bb+2C	Write Status Register				
bb+30	Unused				
bb+34	Unused				
bb+38	Unused				
bb+3C	Unused				
bb+40	User Interface Interrupt Control Register				
bb+44	Unused				
bb+EC	Unused				
bb+F0	General Purpose Register 0				
bb+F4	General Purpose Register 1				
bb+F8	General Purpose Register 2				
bb+FC	General Purpose Register 3				

Device Register:  
 (normal R/W, Diagnostic Mode Writable, loaded @DCLO deassertion)

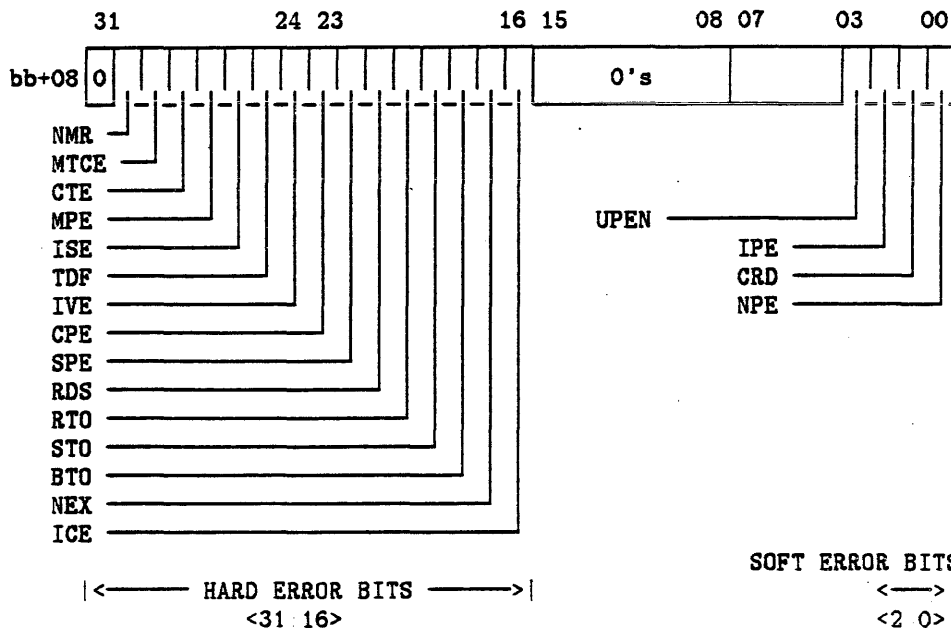


BI Control And Status Register:



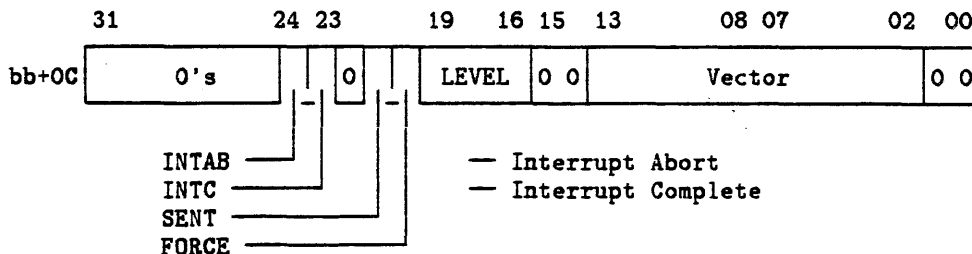
- HES (RO) — Hard Error Summary
- SES (RO) — Soft Error Summary
- INIT (Write-1-to-Clear, set @DCLO deassertion & by STOP command)
- BROKE (Write-1-to-Clear, set @DCLO deassertion)
- STS (R/W, Cleared @DCLO deassertion) — Self Test Status
- SST (Special Case) — Start Self Test
- UWP (Write-1-to-Clear, Cleared @DCLO deassertion & by STOP command) — Unlock Write Pending
- HEIE (R/W, Cleared @DCLO deassertion & by STOP command) — Hard Error Interrupt Enable
- SEIE (R/W, Cleared @DCLO deassertion & by STOP command) — Soft Error Interrupt Enable

Bus Error Register:  
(Write-1-to-Clear, Cleared @DCLO deassertion)

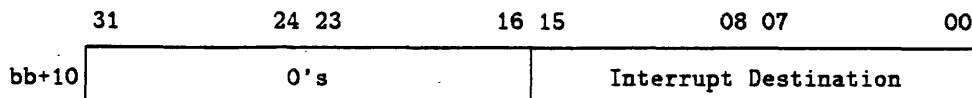


- |   |                                  |
|---|----------------------------------|
| NMR — NO ACK to Multi-Responder Command | RTO — Retry Time Out             |
| MTCE — Master Transmit Check Error      | STO — Stall Time Out             |
| CTE — Control Transmit Error            | BTO — Bus Time Out               |
| MPE — Master Parity Error               | NEX — Non-Existent Address       |
| ISE — Interlock Sequence Error          | ICE — Illegal Confirmation Error |
| TDF — Transmitter During Fault          | UPEN — User Parity Enable        |
| IVE — IDENT Vector Error                | IPE — Id Parity Err              |
| CPE — Command Parity Error              | CRD — Corrected Read Data        |
| SPE — Slave Parity Error                | NPE — Null bus Parity Error      |
| RDS — Read Data Substitute              |                                  |

Error Interrupt Control Register:

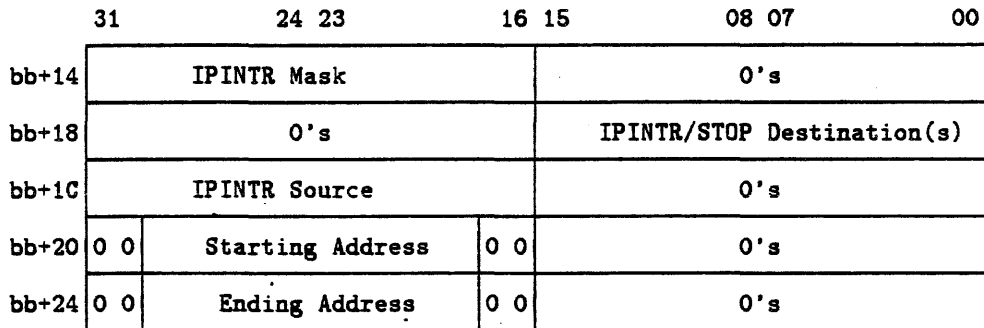


Interrupt Destination Register:  
(R/W, DCLOC)

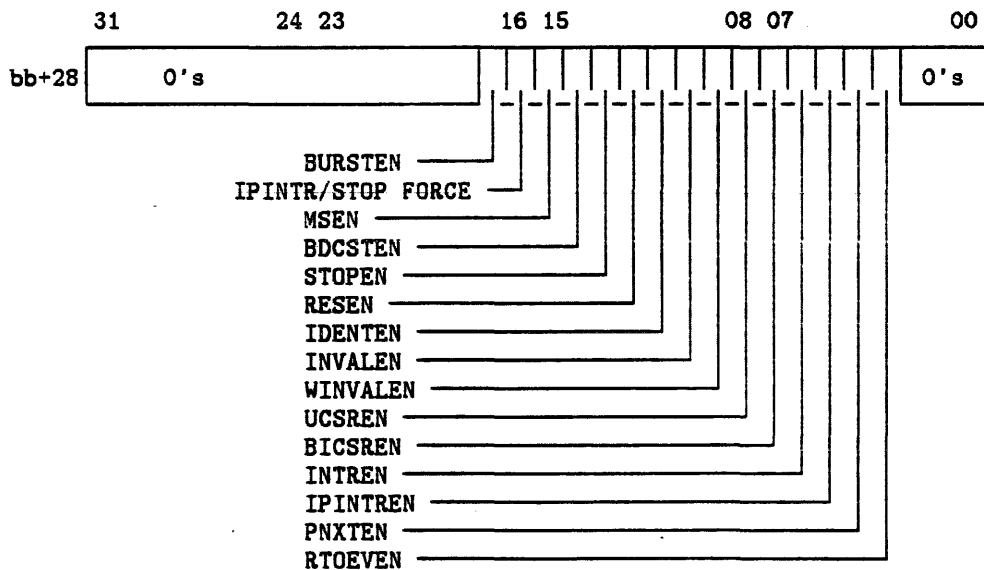




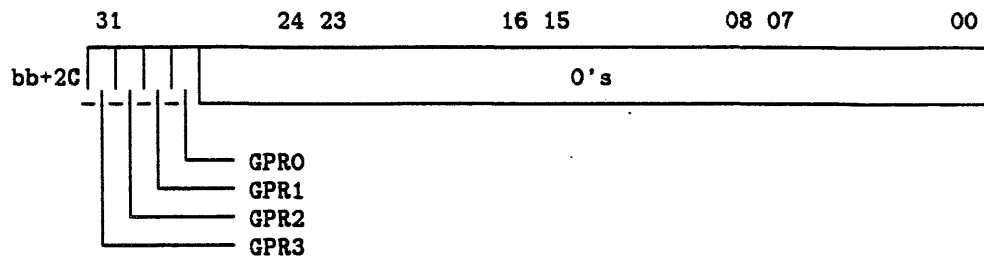
BIIC SPECIFIC REGISTERS



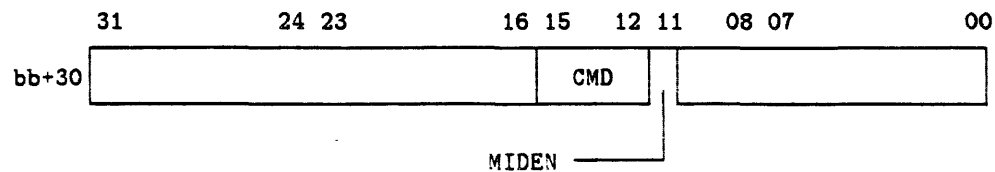
BCI Control Register: (R/W, cleared @DCLO deassertion)



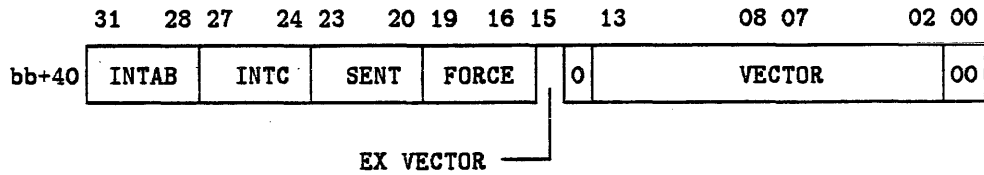
Write Status Register: (Write-1-to-Clear, cleared @DCLO deassertion)



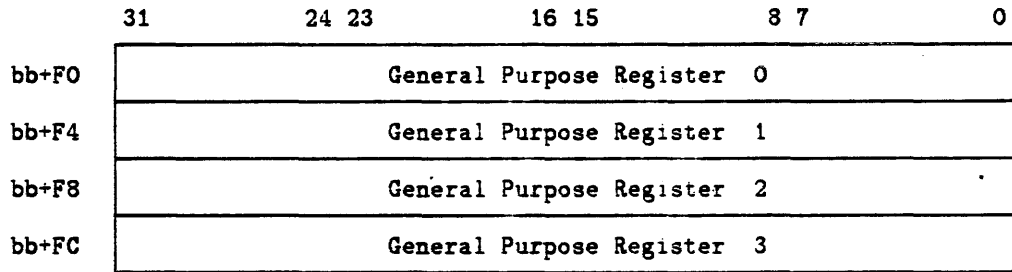
Force IPINTR/STOP Command Register:



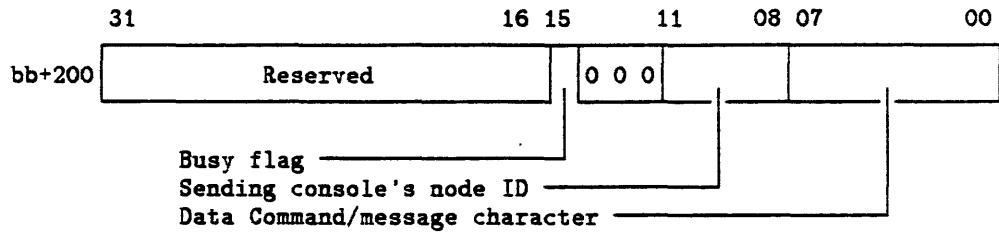
User Interface Interrupt Control Register:



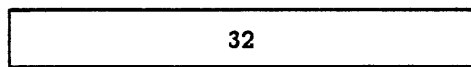
General Purpose Registers: (R/W, DCLOC)



The Receive Console Data Register (RXCD):



DATAPATH SIGNALS (37 Total)



BI D<31:00> L



BI I<3:0>



BI PO L

SYNCHRONOUS CONTROL SIGNALS (5 Total)



BI NO ARB L



BI BSY L



BI CNF<2:0>L

CLOCK SIGNALS (4 Total)



BI TIME +/-



BI PHASE +/-

ASYNCHRONOUS CONTROL SIGNALS (6 Total)



BI AC LO L



BI DC LO L



BI RESET L



BI STF L



BI BAD L



SPARE

Abbreviations used: OD - Open Drain  
 OC - Open Collector  
 DECL - Differential ECL

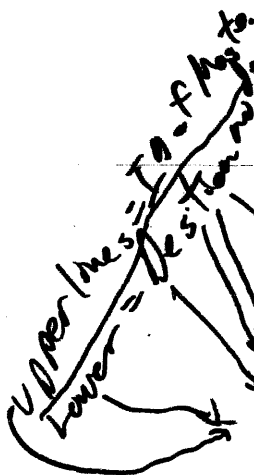
Signal Name	Number/Type	Description
<b>DATAPATH SIGNALS</b>		
BI D<31:00> L	32/OD	Bidirectional lines used for arbitration sequences and all address and data transfers
BI I<3:0> L	4/OD	Multipurpose bidirectional lines used to carry the Command, Identity of current BI Master, and the Byte Mask.
BI PO L	1/OD	Bidirectional line used to generate odd parity for the I lines during ARB and for the D and I lines during data cycles.
<b>SYNCHRONOUS CONTROL SIGNALS</b>		
BI NO ARB L	1/OD	Bidirectional line used to inhibit the use of the BI D lines for arbitration. This signal is also asserted during BIIC self test to prevent other nodes from starting transactions until all nodes are ready.
BI BSY L	1/OD	Bidirectional line indicating a transaction is in progress
BI CNF<2:0> L	3/OD	Bidirectional lines used for the response to command and data cycles.
<b>CLOCK SIGNALS</b>		
BI TIME +/-	2/DECL	20 MHz square wave used together with BI PHASE to provide timing for all nodes.
BI PHASE +/-	2/DECL	5 MHz square wave used together with BI TIME to provide timing for all nodes.
<b>ASYNCHRONOUS CONTROL SIGNALS</b>		
BI AC LO L	1/OD	Input only. Indicates that the AC line voltage has dropped below a safe limit.
BI DC LO L	1/OD	Input only. Indicates that the DC voltages are not within tolerance.
BI RESET L	1/OC	Wire-or'd signal, not connected to BIIC. Provides a system wide mechanism for initiating a BI power-up sequence.
BI STF L	1/OC	Self Test Fast - not connected to BIIC. Enables a faster system self-test.
BI BAD L	1/OC	Wire-or'd signal, not connected to BIIC. Provides system-wide mechanism for reporting BI Node self test failure.

CONFIRMATION LINES

BI CNF<2:0> L	Description
H H H	NO ACK (No Acknowledgement)
H H L	Illegal
H L H	Illegal
H L L	ACK
L H H	Illegal
L H L	STALL
L L H	RETRY
L L L	Illegal

COMMAND CODE TABLE

BI I<3:0> L	Description	Mnemonic	Single or Multiple
H H H H	(reserved)	—	—
H H H L	READ	READ	Single
H H L H	INTLK READ (CACHE INTENT)	IRCI	Single
H H L L	READ WITH CACHE INTENT	RCI	Single
H L H H	WRITE	WRITE	Single
H L H L	WRITE WITH CACHE INTENT	WCI	Single
H L L H	UNLOCK WRITE MASK (CACHE INTENT)	UWMC	Single
H L L L	WRITE MASK (CACHE INTENT)	WMCI	Single
L H H H	INTERRUPT	INTR	Multiple
L H H L	IDENTIFY - NOACK = service not needed	IDENT	Single
L H L H	(reserved)	—	—
L H L L	(reserved)	—	—
L L H H	STOP	STOP	Multiple - CPU's only
L L H L	INVALIDATE - cache locations	INVAL	Multiple
L L L H	BROADCAST	BDCST	*NOT USED*
L L L L	INTERPROCESSOR INTERRUPT - CPU or Fatell adapter	IPINTR	Multiple



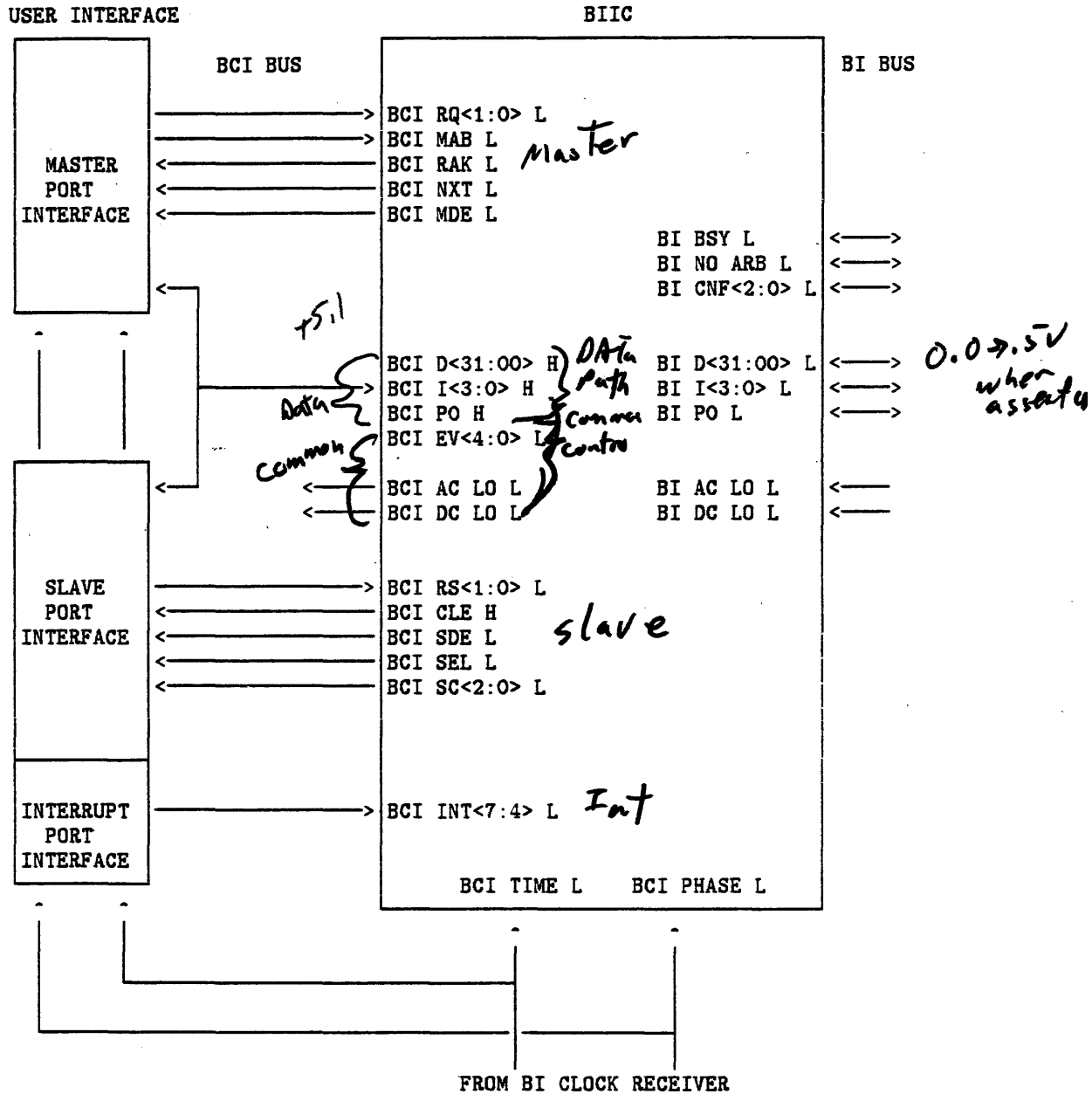
DATA LENGTH CODES

BI D<31:30> L	DATA LENGTH	MNEMONIC
H H	RESERVED CODE	-
H L	4 byte (long)	LW
L H	8 byte (quad)	QW
L L	16 byte (octa)	OW

DATA STATUS

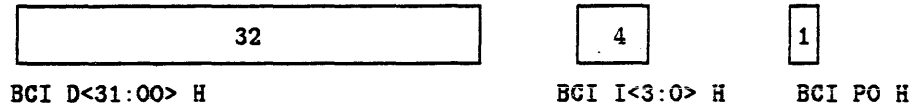
BI I<3:0> L	Description	Mnemonic
H X H H	— RESERVED CODE —	-
H X H L	READ DATA	RD
H X L H	CORRECTED READ DATA	CRD
H X L L	READ DATA SUBSTITUTE	RDS - uncorrectable
L X H H	— RESERVED CODE —	-
L X H L	READ DATA/DON'T CACHE	RDDC
L X L H	CORRECTED READ DATA/DON'T CACHE	CRDDC
L X L L	READ DATA SUBSTITUTE/DON'T CACHE	RDSDC

*starts command at master*

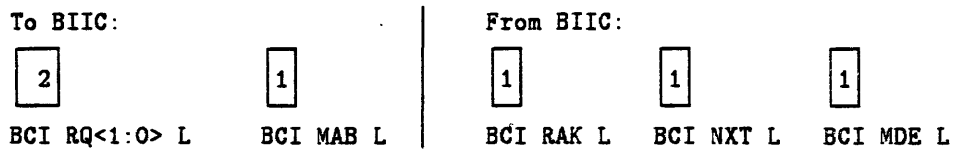


	14	13	12	11	10	09	08	07	06	05	04	03	02	01									
P	ACLO	i02	d00	d02	d03	d06	d07	d10	d11	d14	d16	d19	d20	VBB	P								
N	p0	aclo	i01	i03	d01	d05	d08	d09	d12	d15	d18	d22	N/C	d25	N								
M	nxt	cle	i00	+5V	GND	d04	GND	GND	d13	d17	d21	d23	d24	d26	M								
L	ev01	rak	GND	<p>TOP VIEW OF BIIC PACKAGE</p> <p>lower case — BCI signals upper case — BI, power, ground, special signals</p>								+5V	d27	d29	L								
K	ev03	ev00	GND									GND	d28	d31	K								
J	dclo	ev04	ev02									GND	d30	sc00	J								
H	sde	DCLO	GND									sel	sc01	sc02	H								
G	mde	int7	int6									GND	D29	D31	G								
F	int5	mab	rq0									GND	D28	D30	F								
E	int4	rs01	GND									D24	D26	D27	E								
D	rq01	phase	+5V									KEY PIN		D19	D22	D25	D						
C	rs00	NOARB	VBB									CNFO	GND	I03	GND	GND	D09	D16	GND	GREF	D20	D23	C
B	time	N/C	CNF1									I00	I02	D01	D04	D05	D08	D11	D13	D15	D18	D21	B
A	BSY	CNF2	I01	PO	D00	D02	D03	D06	D07	D10	D12	D14	D17	VREF	A								

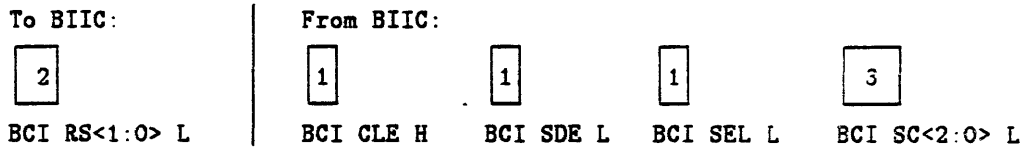
DATAPATH CLASS (37 Total)



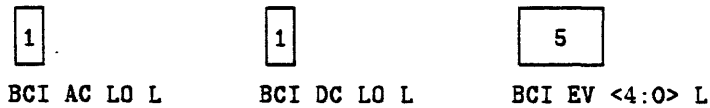
MASTER CLASS (6 Total)



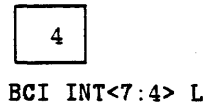
SLAVE CLASS (8 Total)



COMMON CONTROL CLASS (7 Total)



INTERRUPT CLASS (4 Total)





Signal Name	Description
<b>DATAPATH CLASS</b>	
BCI D<31:00> H	Bi-directional tri-state lines used for all address and data transfers.
BCI I<3:0> H	Bi-directional tri-state lines used to transfer the Command, Read Status and Write Mask.
BCI PO H	Bidirectional line used to generate odd parity for the BCI D<31:00> and BCI I<3:0> lines.
<b>MASTER CLASS</b>	
BCI RQ<1:0> L	REQUEST lines driven by the master port interface to cause the BIIC to perform a BI transaction, a loopback transaction or enter diagnostic mode.
BCI MAB L	MASTER ABORT line driven by the master port interface to abort the current master port transaction.
BCI RAK L	REQUEST ACKNOWLEDGE line driven by the BIIC to inform the master port that a transaction requested by the master port has been initiated.
BCI NXT L	NEXT line, driven by the BIIC to request the next data word from the master on write transactions and to indicate that the current data on BCI D<31:00> H is valid
BCI MDE L	MASTER DATA ENABLE line, driven by the BIIC to gate command/address information from the master port.
<b>SLAVE CLASS</b>	
BCI RS<1:0> L	RESPONSE lines driven by the slave port to indicate what confirmation code to send out on the BI in response to command and data cycles involving this slave port.
BCI CLE H	COMMAND LATCH ENABLE line driven by the BIIC to indicate the presence of a Command/address cycle.
BCI SDE L	SLAVE DATA ENABLE line driven by the BIIC to indicate that data to transmitted on the BI should be driven on BCI D<31:00> H, BCI I<3:0> H, and BCI PO H lines.
BCI SEL L	SELECT line driven by the BIIC to inform the slave that it has been selected by a BI transaction.
BCI SC<2:0> L	SELECT CODE lines driven by the BIIC to give detailed selection information. A select code always accompanies an assertion of BCI SEL L and vice-versa.

Signal Name	Description
<b>COMMON CONTROL CLASS</b>	
BCI AC LO L	Buffered and synchronized version of BI AC LO L.
BCI DC LO L	Buffered and synchronized version of BI DC LO L.
BCI EV <4:0> L	EVENT CODE lines used to indicate significant events in the BIIC or on the BI. There are three classes of event codes: Summary codes, used to indicate the result of a transaction involving this node, Status codes used to provide status during a transaction, and Special codes used to provide information not related to a particular transaction.
<b>INTERRUPT CLASS</b>	
BCI INT<7:4> L	INTERRUPT REQUEST lines used to cause the BIIC to generate a BI Interrupt transaction.

## SIGNAL ENCODING

## Event Code Table

BCI EV<4:0> L							
4	3	2	1	0	Mnemonic	Class	Type
H	H	H	H	H	NO EVENT	-	-
H	H	H	H	L	MCP	SUM	M:INFO
H	H	H	L	H	AKRSD	SUM	S:INFO
H	H	H	L	L	BTO	SPC	M:ERROR
H	H	L	H	H	STP	SPC	INFO
H	H	L	H	L	RCR	SUM	M:INFO
H	H	L	L	H	IRW	SUM	S:INFO
H	H	L	L	L	ARCR	STA	M:INFO
H	L	H	H	H	NICI	SUM	I:ERR/INFO
H	L	H	H	L	NICIP	SUM	I:ERR/INFO
H	L	H	L	H	AKRE	SUM	I:INFO
H	L	H	L	L	IAL	STA	I:INFO
H	L	L	H	H	EVS4	STA	I:INFO
H	L	L	H	L	EVS5	STA	I:INFO
H	L	L	L	H	EVS6	STA	I:INFO
H	L	L	L	L	EVS7	STA	I:INFO
L	H	H	H	H	STO	SUM	S:ERROR
L	H	H	H	L	BPS	SUM	S:ERROR
L	H	H	L	H	ICRSD	SUM	S:ERROR
L	H	H	L	L	BBE	SUM	S:ERROR
L	H	L	H	H	AKRNE4	SUM	I:INFO
L	H	L	H	L	AKRNE5	SUM	I:INFO
L	H	L	L	H	AKRNE6	SUM	I:INFO
L	H	L	L	L	AKRNE7	SUM	I:INFO
L	L	H	H	H	RDSR	SUM	M:ERROR
L	L	H	H	L	ICRMC	SUM	M:ERROR
L	L	H	L	H	NCRMC	SUM	M:ERR/INFO
L	L	H	L	L	BPR	STA	M/S:ERROR
L	L	L	H	H	ICRMD	SUM	M:ERROR
L	L	L	H	L	RTO	SUM	M:ERROR
L	L	L	L	H	BPM	SUM	M:ERROR
L	L	L	L	L	MTCE	SUM	M:ERROR

## Response Lines BCI - (RS&lt;1:0&gt; L)

BCI RS<1:0> L		RESPONSE CODE	RESULTING
1	0	DESCRIPTION	CNF CODE
H	H	NO ACK	NO ACK
H	L	ACK	ACK, NO ACK
L	H	STALL	STALL, ACK or NO ACK
L	L	RETRY	RETRY, NO ACK

FOR INTERNAL USE ONLY

## REQUEST LINES

<u>BCI RQ&lt;1:0&gt; L</u>	<u>Description</u>
H H	No Request
H L	BI Transaction Request
L H	Loopback Request
L L	Diagnostic Mode

## BCI COMMAND CODE TABLE

<u>BCI I&lt;3:0&gt; H</u>	<u>Description</u>	<u>Mnemonic</u>
L L L L	(reserved)	—
L L L H	READ	READ
L L H L	INTLK READ (CACHE INTENT)	IRCI
L L H H	READ WITH CACHE INTENT	RCI
L H L L	WRITE	WRITE
L H L H	WRITE WITH CACHE INTENT	WCI
L H H L	UNLOCK WRITE MASK (CACHE INTENT)	UWMC
L H H H	WRITE MASK (CACHE INTENT)	WMCI
H L L L	INTERRUPT	INTR
H L L H	IDENTIFY	IDENT
H L H L	(reserved)	—
H L H H	(reserved)	—
H H L L	STOP	STOP
H H L H	INVALIDATE	INVAL
H H H L	BROADCAST	BDCST
H H H H	INTERPROCESSOR INTERRUPT	IPINTR

## Data Length Codes

<u>BCI D&lt;31:30&gt; H</u>	<u>DATA LENGTH</u>	<u>MNEMONIC</u>
L L	RESERVED CODE	-
L H	4 byte (long)	LW
H L	8 byte (quad)	QW
H H	16 byte (octa)	OW

ARB FIELD - bits <5:4> of the BI Control and Status Register

<u>ARB</u>	<u>Meaning</u>
<5:4>	
0 0	Dual round robin arbitration
0 1	Fixed high priority
1 0	Fixed low priority
1 1	Disable arbitration

## Select Codes

BCI SC&lt;2:0&gt; L

2 1 0

Description

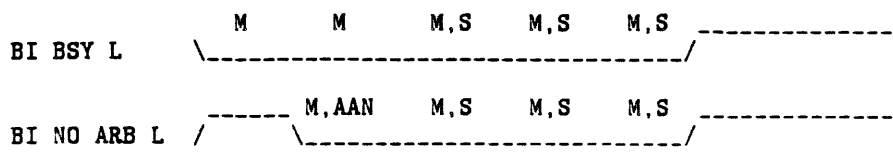
2	1	0	Description
H	H	H	No command received or not for this node
H	H	L	A read- or write-type command to the User CSR Space is received, and the UCSREN bit in the BCI Control Register is set, or a read- or write-type command to the BIIC CSR Space for this Node is received and the BICSREN bit in the BCI Control Register is set.
H	L	H	A read- or write-type command to the range of addresses defined by Starting Address Register and Ending Address Register is received.
H	L	L	A read- or write-type command to the range of addresses defined as "Multicast Space" in the BI Spec is received, and the MSEN bit in the BCI Control Register is set.
L	H	H	An IDENT transaction is received and the IDENTEN bit in the BCI Control Register is set
L	H	L	An INTR transaction whose destination matches this node is received and the INTREN bit in the BCI Control Register is set, or an IP INTR transaction whose destination matches this node and whose source matches the IP Interrupt Mask Register is received and the IPINTREN bit in the BCI Control Register is set.
L	L	H	An INVALID command, or a write-type command not directed to the range of addresses defined by the Starting and Ending Address registers and not having D<29> asserted (i.e. not I/O space), is received, and the INVALEN bit, or the WINVALEN bit, respectively, is set in the BCI Control Register.
L	L	L	A BROADCAST command, or a STOP command, or a RESERVED command is received, with a destination matching this node (except for RESERVED commands) and the BDCSTEN, STOPEN, or RSVDEN bit, respectively, is set in the BCI Control Register.

AAN	All Arbitrating Nodes
ADDR	Address
AN	All Nodes
APS	All Pending Slaves
C/A	Command/Address
CHK	Checked
CMD	Command
CNF	Confermation Lines
DEC'd	Decoded
DEST	Destination
GEN	Generated
IA	Imbedded Arbitration
INTR	Interrupt
M	Master
M,S	both Master and Slave
RES'd	Reserved
S	Slave
Ss	Slave or Slaves
STAT	Status Code
UNDEF	Undefined

> Indicates the CNF which occurred for this diagram, the rest of the CNF codes shown are valid for this cycle, but if they occurred, the rest of the diagram would be different

BI CYCLE	C/A	IA	D1	D2	D3	D4	
31	LENGTH						
30	<1:0>						
29							
28							
27							
26							
25		DEC'd					
24		ID					
23		LOW					
22		PRIOR					
21							
20							
19							
18							
17							
BI	30 BIT						
D<31:00> L	ADDR		DATA1	DATA2	DATA3	DATA4	
16							
15							
14							
13							
12							
11							
10							
9		DEC'd					
8		ID					
7		HIGH					
6		PRIOR					
5							
4							
3							
2							
1							
0							
Source	M	AAN	S	S	S	S	
BI	READ	MASTER	READ	READ	READ	READ	
I<3:0> L	CMD	ID	STAT	STAT	STAT	STAT	
Source	M	M	S	S	S	S	
BI PO L	M	M	S	S	S	S	
GEN	AN	AN	M	M	M	M	
CHK							
BI			>ACK	>ACK	>ACK	>ACK	>ACK
CNF<2:0> L			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
			STALL	STALL	STALL	STALL	
			RETRY				
Source			S	S	S	S	M
							M

*after last Data  
cycle 2 Ack  
is required →  
Master  
From  
Slave*



READ-type TRANSACTION FORMAT (Octaword length shown)

FOR INTERNAL USE ONLY

BI COMMAND DESCRIPTIONS

BI CYCLE	C/A	IA	D1	D2	D3	D4		
31	LENGTH							
30	<1:0>							
29								
28								
27								
26								
25		DEC'd						
24		ID						
23		LOW						
22		PRIOR						
21								
20								
19								
18								
17								
BI	30 BIT							
D<31:0> L	ADDR		DATA1	DATA2	DATA3	DATA4		
16								
15								
14								
13								
12								
11								
10								
9		DEC'd						
8		ID						
7		HIGH						
6		PRIOR						
5								
4								
3								
2								
1								
0								
Source	M	AAN	M	M	M	M		
BI	WRITE	MASTER	UNDEF	UNDEF	UNDEF	UNDEF		
I<3:0> L	CMD	ID	FIELD	FIELD	FIELD	FIELD		
Source	M	M	M	M	M	M		
BI PO L	GEN	M	M	M	M	M		
CHK	AN	AN	S	S	S	S		
BI			>ACK	>ACK	>ACK	>ACK	>ACK	>ACK
CNF<2:0> L			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
			STALL	STALL	STALL	STALL		
Source			S	S	S	S	S	S
			RETRY					
			S					
BI BSY L	M	M	M,S	M,S	M,S			
BI NO ARB L		M,AAN	M,S	M,S	M,S			

WRITE and WCI TRANSACTION FORMAT (Octaword Length Shown)

FOR INTERNAL USE ONLY

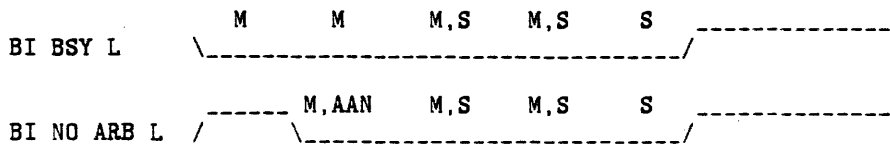


BI CYCLE	C/A	IA	D1	D2	D3	D4		
31	LENGTH							
30	<1:0>							
29								
28								
27								
26								
25		DEC'd						
24		ID						
23		LOW						
22		PRIOR						
21								
20								
19								
18								
17								
BI								
D<31:00> L	30 BIT							
16	ADDR		DATA1	DATA2	DATA3	DATA4		
15								
14								
13								
12								
11								
10								
9		DEC'd						
8		ID						
7		HIGH						
6		PRIOR						
5								
4								
3								
2								
1								
0								
Source	M	AAN	M	M	M	M		
BI								
I<3:0> L	WRITE	MASTER	WRITE	WRITE	WRITE	WRITE		
Source	CMD	ID	MASK	MASK	MASK	MASK		
	M	M	M	M	M	M		
BI PO L								
GEN	M	M	M	M	M	M		
CHK	AN	AN	S	S	S	S		
BI								
CNF<2:0> L			>ACK	>ACK	>ACK	>ACK	>ACK	>ACK
Source			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
			STALL	STALL	STALL	STALL		
			RETRY					
			S	S	S	S	S	S
BI BSY L	M	M	M,S	M,S	M,S	-----		
BI NO ARB L	M,AAN		M,S	M,S	M,S	-----		

WMCI and UWMCI TRANSACTION FORMAT (Octaword)

FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	DMID	INTR ARB	VECTOR	VECTOR	
31							
30							
29							
28							
27							
26	RESV'd						
25	FIELD	DEC'd	DEC'd	DEC'd	UNDEF	0's	
24		ID	MASTER	ID	FIELD		
23		LOW	ID	ARBing			
22		PRIOR		SLAVES			
21							
20							
19							
18	IDENT						
17	LEVEL						
16	BI						
15	D<31:00> L						
14							
13							
12							
11							
10							
9		DEC'd					
8	RESV'd	ID	RESV'd	RESV'd	UNDEF	VECTOR	
7	FIELD	HIGH	FIELD	FIELD	FIELD		
6		PRIOR					
5							
4							
3							
2							
1						0's	
0							
Source	M	AAN	M	APS	S	S	
BI	IDENT	MASTER	RESV'd	RESV'd	UNDEF	VECTOR	
I<3:0> L	CMD	ID	FIELD	FIELD	FIELD	STATUS	
Source	M	M	M	M	S	S	
BI PO L	M	M	M	RESV'd	S	S	
GEN	AN	AN	APS	FIELD	M	M	
CHK							
BI					ACK	>ACK	>ACK
CNF<2:0> L					NO ACK	NO ACK	NO ACK
					>STALL	STALL	
					RETRY	RETRY	
Source					S	S	M
							M



IDENT TRANSACTION FORMAT  
FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	
31			
30			
29			
28			
27			
26	RESV'd		
25	FIELD	DEC'd	
24		ID	
23		LOW	
22		PRIOR	
21			
20			
19			
18	INTR		
17	LEVEL		
16			RESV'd
BI D<31:00> L			FIELD
15			
14			
13			
12			
11			
10			
9	INTR	DEC'd	
8	DEST	ID	
7	MASK	HIGH	
6		PRIOR	
5			
4			
3			
2			
1			
0			
Source	M	AAN	
BI I<3:0> L	INTR	MASTER	RESV'd
Source	CMD	ID	FIELD
	M	M	
BI PO L GEN	M	M	RESV'd
CHK	AN	AN	FIELD
BI CNF<2:0> L			>ACK
Source			NO ACK
			Ss

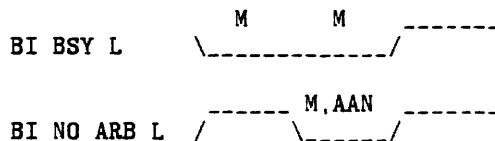
BI BSY L      M      M      -----

BI NO ARB L      ----- M, AAN -----

INTR TRANSACTION FORMAT

FOR INTERNAL USE ONLY

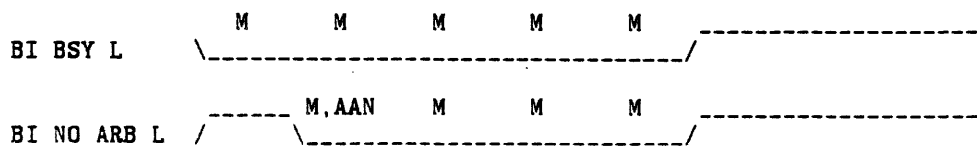
BI CYCLE	C/A	IA	
31			
30			
29			
28			
27			
26			
25	MASTER	DEC'd	
24	DEC'd	ID	
23	ID	LOW	
22		PRIOR	
21			
20			
19			
18			
17			
16			RESV'd
D<31:00> L			FIELD
15			
14			
13			
12			
11			
10			
9	IP	DEC'd	
8	INTR	ID	
7	DEST	HIGH	
6	MASK	PRIOR	
5			
4			
3			
2			
1			
0			
Source	M	AAN	
BI I<3:0> L	IPINTR	MASTER	RESV'd
Source	CMD	ID	FIELD
	M	M	
BI PO L	M	M	RESV'd
GEN	AN	AN	FIELD
CHK			
BI CNF<2:0> L			>ACK
Source			NO ACK
			Ss



IPINTR TRANSACTION FORMAT

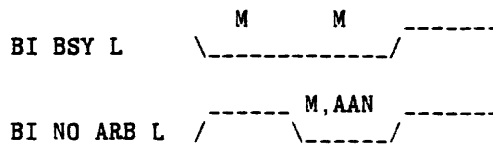
FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	D1	D2	D3	D4		
31	LENGTH							
30	<1:0>							
29								
28								
27								
26								
25		DEC'd						
24		ID						
23	RESV'd	LOW						
22	FIELD	PRIOR						
21								
20								
19								
18								
17								
BI								
D<31:00> L			DATA1	DATA2	DATA3	DATA4		
15								
14								
13								
12								
11								
10								
9		DEC'd						
8	BDCST	ID						
7	MASK	HIGH						
6		PRIOR						
5								
4								
3								
2								
1								
0								
Source	M	AAN	M	M	M	M		
BI								
I<3:0> L	BDCST	MASTER	WRITE	WRITE	WRITE	WRITE		
Source	CMD	ID	MASK	MASK	MASK	MASK		
	M	M	M	M	M	M		
BI PO L								
GEN	M	M	M	M	M	M		
CHK	AN	AN	Ss	Ss	Ss	Ss		
BI								
CNF<2:0> L			>ACK	>ACK	>ACK	>ACK	>ACK	>ACK
			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
Source			Ss	Ss	Ss	Ss	Ss	Ss



BROADCAST TRANSACTION FORMAT  
FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	
31			
30			
29			
28			
27			
26			
25		DEC'd	
24	RESV'd	ID	
23	FIELD	LOW	
22		PRIOR	
21			
20			
19			
18			
17			
16			RESV'd
BI D<31:00> L			FIELD
15			
14			
13			
12			
11			
10			
9		DEC'd	
8	DEST	ID	
7	MASK	HIGH	
6		PRIOR	
5			
4			
3			
2			
1			
0			
Source	M	AAN	
BI I<3:0> L	STOP	MASTER	RESV'd
Source	CMD	ID	FIELD
	M	M	
BI PO L GEN	M	M	RESV'd
CHK	AN	AN	FIELD
BI CNF<2:0> L			>ACK
Source			NO ACK
			Ss



STOP TRANSACTION FORMAT

FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	
31	LENGTH		
30	<1:0>		
29			
28			
27			
26			
25		DEC'd	
24		ID	
23		LOW	
22		PRIOR	
21			
20			
19			
18			
17			
BI	30 BIT		RESV'd
D<31:00> L	ADDR		FIELD
16			
15			
14			
13			
12			
11			
10			
9		DEC'd	
8		ID	
7		HIGH	
6		PRIOR	
5			
4			
3			
2			
1			
0			
Source	M	AAN	
BI	INVAL	MASTER	RESV'd
I<3:0> L	CMD	ID	FIELD
Source	M	M	
BI PO L	M	M	RESV'd
GEN	AN	AN	FIELD
CHK			
BI			>ACK
CNF<2:0> L			NO ACK
Source			Ss

BI BSY L      M      M      -----

BI NO ARB L      ----- M, AAN -----

INVALIDATE TRANSACTION FORMAT

FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	
31	LENGTH		
30	<1:0>		
29			
28			
27			
26			
25		DEC'd	
24		ID	
23		LOW	
22		PRIOR	
21			
20			
19			
18			
17			
BI	30 BIT	UNDEF	
D<31:00> L	ADDR	FIELD	
16			
15			
14			
13			
12			
11			
10			
9		DEC'd	
8		ID	
7		HIGH	
6		PRIOR	
5			
4			
3			
2			
1			
0			
Source	M	AAN	
BI	INVAL	MASTER	UNDEF
I<3:0> L	CMD	ID	FIELD
Source	M	M	
BI PO L	M	M	UNDEF
GEN	AN	AN	FIELD
CHK			
BI			ACK
CNF<2:0> L			>NOACK
Source			STALL
			RETRY

BI BSY L      M      M      M

BI NO ARB L      M, AAN      M

QUADWORD READ WITH NOACK RESPONSE



BI CYCLE	C/A	IA	STALL	D1	D2		
31	LENGTH						
30	<1:0>						
29							
28							
27							
26							
25		DEC'd					
24		ID					
23		LOW					
22		PRIOR					
21							
20							
19							
18							
17							
BI	30 BIT						
D<31:00> L	ADDR		UNDEF	DATA1	DATA2		
15			FIELD				
14							
13							
12							
11							
10							
9		DEC'd					
8		ID					
7		HIGH					
6		PRIOR					
5							
4							
3							
2							
1							
0							
Source	M	AAN	S	S	S		
BI	READ	MASTER	UNDEF	READ	READ		
I<3:0> L	CMD	ID	FIELD	STAT	STAT		
Source	M	M	S	S	S		
BI PO L	M	M	S	S	S		
GEN	AN	AN	M	M	M		
CHK							
BI			ACK	>ACK	>ACK	>ACK	>ACK
CNF<2:0> L			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
			>STALL	STALL	STALL		
Source			RETRY	RETRY	STALL	M	M
			S	S	S		

BI BSY L      M      M      M,S      S

BI NO ARB L      /      M,AAN      M,S      S      /

QUADWORD READ TRANSACTION WITH STALL

BI COMMAND DESCRIPTIONS

BI CYCLE	C/A	IA	D1	D1		
31	LENGTH					
30	<1:0>					
29						
28						
27						
26						
25		DEC'd				
24		ID				
23		LOW				
22		PRIOR				
21						
20						
19						
18						
17						
BI	30 BIT					
D<31:00> L	ADDR		DATA1	DATA1		
15						
14						
13						
12						
11						
10						
9		DEC'd				
8		ID				
7		HIGH				
6		PRIOR				
5						
4						
3						
2						
1						
0						
Source	M	AAN	M	M		
BI	WRITE	MASTER	UNDEF	UNDEF		
I<3:0> L	CMD	ID	FIELD	FIELD		
Source	M	M	M	M		
BI PO L	GEN	M	M	M		
CHK	AN	AN	S	S		
BI			ACK	ACK		
CNF<2:0> L			NO ACK	NO ACK		
Source			>STALL	>STALL		
			RETRY	>RETRY		
			S	S		

BI BSY L      M      M      M,S      M      M

BI NO ARB L      M,AAN      M,S      M      M

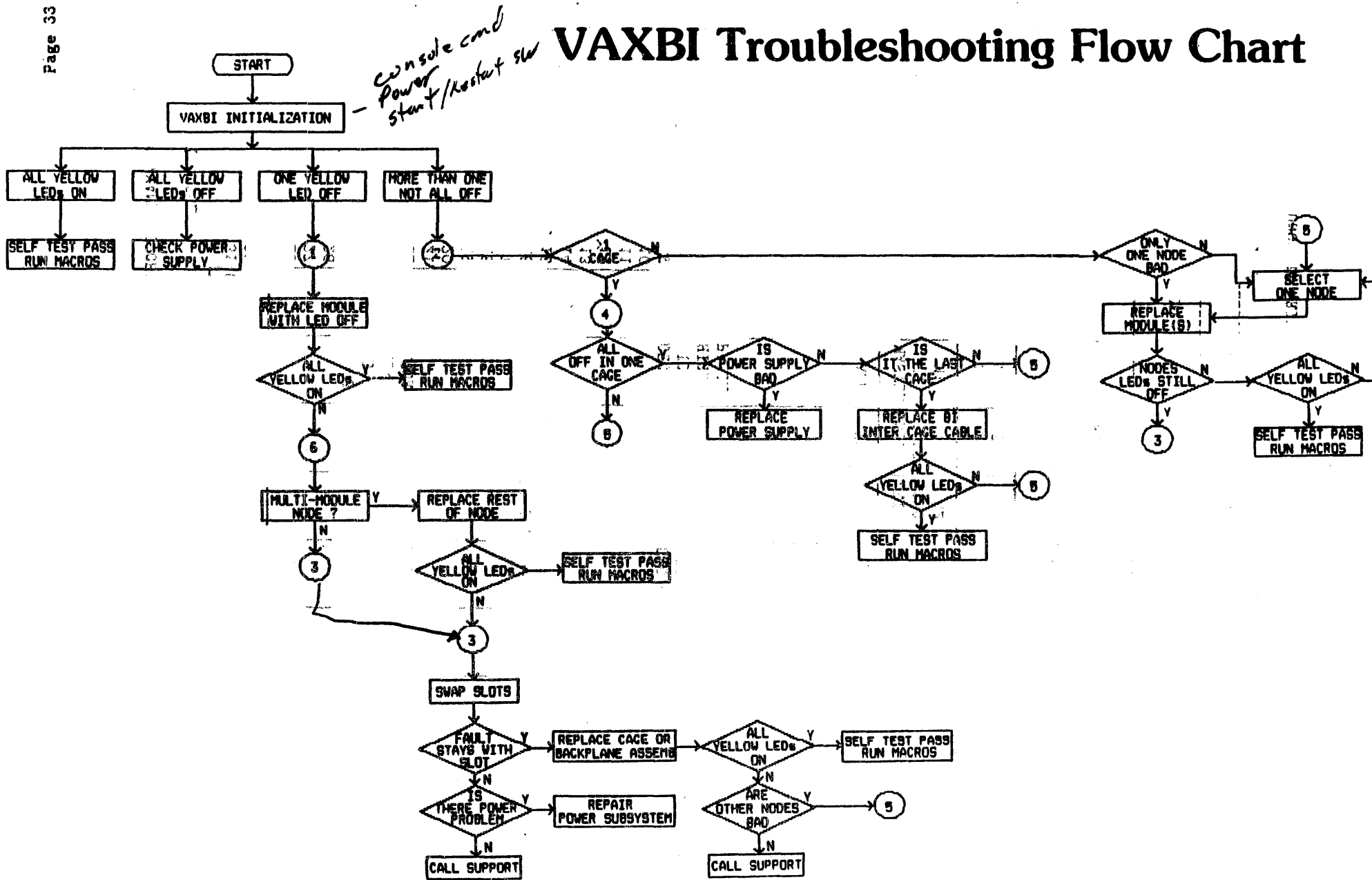
OCTAWORD WRITE TRANSACTION STALLED, THEN RETRIED

FOR INTERNAL USE ONLY

BI CYCLE	C/A	IA	D1	C/A	IA	D1		
31	LENGTH			LENGTH				
30	<1:0>			<1:0>				
29								
28								
27								
26								
25		DEC'd			DEC'd			
24		ID			ID			
23		LOW			LOW			
22		PRIOR			PRIOR			
21								
20								
19								
18								
17								
16	30 BIT			30 BIT				
15	ADDR		DATA1	ADDR		DATA1		
14								
13								
12								
11								
10								
9		DEC'd			DEC'd			
8		ID			ID			
7		HIGH			HIGH			
6		PRIOR			PRIOR			
5								
4								
3								
2								
1								
0								
Source	M1	AAN	M1	M2	AAN	M2		
BI I<3:0> L	WRITE	MASTER	UNDEF	WRITE	MASTER	UNDEF		
Source	CMD	ID	FIELD	CMD	ID	FIELD		
	M1	M1	M1	M2	M2	M2		
BI PO L GEN	M1	M1	M1	M2	M2	M2		
CHK	AN	AN	S1	AN	AN	S2		
BI CNF<2:0> L			>ACK	>ACK	>ACK	>ACK	>ACK	>ACK
Source			NO ACK	NO ACK	NO ACK	NO ACK	NO ACK	NO ACK
			STALL			STALL		
			RETRY			RETRY		
			S1	S1	S1	S2	S2	S2
BI BSY L	M1		M2		M2			
BI NO ARB L	M1, AAN		M2	M2, ANN				

TWO LONGWORD WRITE TRANSACTIONS WITH SECOND WRITE ARBING IN IMBEDDED ARB

# VAXBI Troubleshooting Flow Chart





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