pdp11

# DV11 communications multiplexer user's manual

digital

EK-DV11-OP-001

# DV11 communications multiplexer user's manual

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## CONTENTS

## CONTENTS (Cont)

## CONTENTS (Cont)



## ILLUSTRATIONS



## TABLES

## TABLES (Cont)

# CHAPTER 1
# INTRODUCTION AND GENERAL DESCRIPTION

## 1.1 PURPOSE AND SCOPE

This manual is intended to provide operational programming information for the DV11 Communications Multiplexer. The manual consists of three chapters plus appendices:

Chapter 1 provides an introduction and overall functional and physical descriptions of the DV11;

Chapter 2 contains site preparation, interfacing, and installation information;

Chapter 3 includes all information necessary for operation of the DV11 via the PDP-11 program;

Appendices contain reference data, communications introductory data, and an extensive glossary of terms and abbreviations.

The reader unfamiliar with communication line protocols should read Appendix B before attempting Chapters 1 and 3.

Terms unique to the DV11 are generally defined at their first appearance. However, should the reader encounter a word that is not fully understood, refer to the glossary provided in Appendix C before proceeding.

## 1.2 DV11 COMMUNICATIONS MULTIPLEXER

The DV11 is a communications multiplexer for the PDP-11 family of computers. By means of the DV11, 8 or 16 serial data lines can be multiplexed directly to PDP-11 core memory for bidirectional data transfer. The DV11 is intended for use with a PDP-11 program that provides the rules or protocol which govern the data transfers and the generation and interpretation of data link control and character codes.

Protocols require processing to (1) monitor transmitted and received characters in order to identify and respond to control characters, (2) maintain a record of control and data transmission and reception sequences, and (3) compute the error checking code (block check calculation) on each character transmitted or received. The DV11 performs these functions, thus relieving the processor of this overhead. A Core Memory Control Table, set up by the PDP-11 program, is used by the DV11 to direct the processing of received and transmitted characters. The control table is comprised of control bytes, which form a one-to-one correspondence with each character transmitted or received.

### 1.2.1 DV11 Overview Block Diagram

Figure 1-1 is a DV11 overview block diagram, showing the principal functional units, and data and control lines for the DV11. The DV11 consists of two primary functional subsystems, as indicated on the block diagram: a *Modem Control Unit,* and a *Data Handling Section.* The Modem Control Unit monitors and controls operations of the line modems as directed by the PDP-11 program. The Data Handling Section sequences and synchronizes transfer of data between the modems and the PDP-11 Unibus (effectively, core memory).

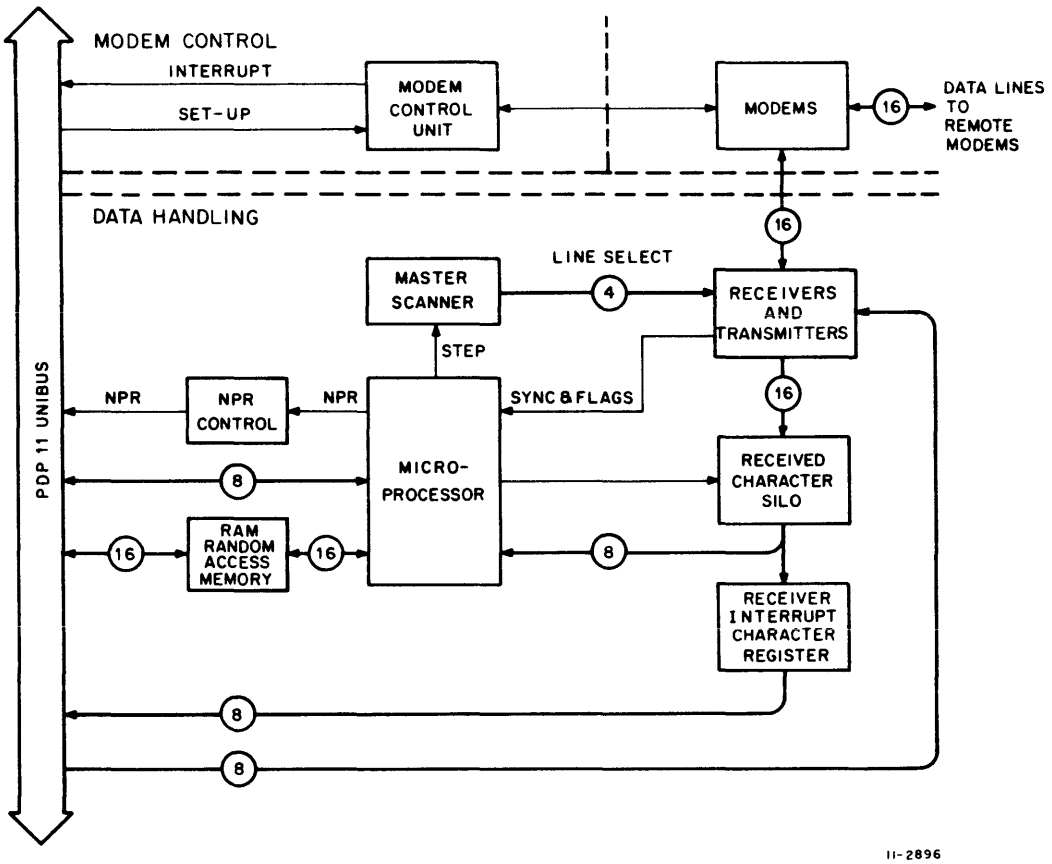



Figure 1-1 DV11 Overview Block Diagram

**1.2.1.1 Establishing the Data Link** – Data transfer is enabled whenever

1. An operator manually initiates a call to a remote modem, or the PDP-11 program dials the remote number via the DN11 Automatic Calling Unit; when the data link is established by the remote modem answering the call, the DV11 Modem Control Unit signals the PDP-11 program via an interrupt.

2. In response to a RING signal from a remote modem, the DV11 Modem Control Unit interrupts the PDP-11 program, to initiate an exchange of signals that establishes the data link.

**1.2.1.2 DV11 Operation** – With the data link established, the PDP-11 program sets up the DV11 Data Handling Section to enable the data transfer between the selected local modem and core memory.

The serial/parallel interface is accomplished in the receivers and transmitters. The receivers assemble characters received from the serial data lines and set a flag each time a character is assembled. The transmitters disassemble parallel characters for transmission on the serial data lines and set a flag each time another character can be accepted for transmission.

The Master Scanner cyclically enables the receivers and transmitters to route their flags to the Microprocessor.

The Microprocessor is controlled by a Read-Only Memory (ROM), which handles character transfers and steps the Master Scanner. Once started by the PDP-11 program, the Microprocessor runs continuously.

The Received Character (RC) Silo is a first-in, first-out storage buffer with a capacity of 128 characters. When a character is received by the DV11 and the RC Silo is empty (usual condition), the character propagates to the bottom of the RC Silo. The Microprocessor then inspects the character code to compute the core memory address of the control byte for that character. A Non-Processor Request (NPR) instruction is issued by the Microprocessor to fetch the control byte, which is then interpreted.

In most cases, the control byte will specify character storage, and the character will be transferred from the bottom of the RC Silo to core memory via an NPR transfer. Should the control byte identify the character as an interrupt character, the character will be propagated into the Receiver Interrupt Character (RIC) register for further attention, and the PDP-11 program will be signalled via an interrupt. The RICr-egister is used to display interrupt characters to the PDP-11 program, along with the line number and any error flags.

Processing instructions for the character in the RIC register are sent to the Microprocessor by the PDP-11 program. The RC Silo continues to accumulate received characters while waiting for the PDP-11 program to complete its response to the interrupt; however, inspection and storage of any additional characters from the RC Silo to PDP-11 core memory by the Microprocessor is inhibited. (The Microprocessor continues to perform data transmission tasks.)

NPR Control is used by the Microprocessor to access core memory, to store received characters, fetch characters for transmission, and fetch control bytes to direct character processing. Table addresses in core memory are stored in the Random Access Memory (RAM) for character storage and retrieval, and byte counts for controlling the quantity of data transferred. The RAM also contains registers for controlling protocol functions for each data line.

Character transmission is similar to the reception process just described. When the Master Scanner finds a transmitter flag, the Microprocessor uses NPR Control to fetch the next character for that line from core memory, it then uses the character code to compute the address of the corresponding control byte, and does an NPR to fetch the control byte. The Microprocessor responds as directed by the control byte and then loads the character into the transmitter for transmission.

### 1.2.2 Reference Documents

Table 1-1 contains a list of pertinent documents, i.e., documents covering concepts and systems peculiar to the DV11, plus documents covering equipment with which the DV11 interfaces.

## 1.3 PHYSICAL DESCRIPTION

The DV11 Communications Multiplexer is housed in a 9-slot, double system unit and includes a separate rack-mounted distribution panel for each group of eight modems in a system. Figure 1-2 shows a DV11 system for supporting eight lines or modems. Other configurations are discussed in Chapter 2.

### 1.3.1 General Specifications

**Environment**

Temperature: 10° to 50° C
Humidity: 0 to 90% non-condensing

**Power Requirements**

A DV11 system with 16 synchronous lines:

17.5 A @ +5 V
1.0 A @ -15 V
0.5 A @ +15 V

A DV11 system with 16 asynchronous lines:

20.5 A @ +5 V
1.0 A @ -15 V
0.6 A @ +15 V

A DV11 with 8 synchronous and 8 asynchronous lines:

19.0 A @ +5 V
1.0 A @ -15 V
0.55 A @ +15 V

**Character Length**

5, 6, 7, or 8 bits

**Internal Baud Rates Provided**

Synchronous (via switch settings):
1200, 2400, 4800, 9600

Asynchronous (via PDP-11 program):
50, 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, 7200, 9600, 38,400

**Operating Modes**

Full- or Half-Duplex

**Table 1-1**
**Reference Documents**

| Title | Description |
|---|---|
| GENERAL | |
| PDP-11 Peripherals Handbook | Discussion of overall system, addressing modes, and basic instruction set from a programming point of view. Some interface and installation data. |
| PDP-11 Instruction List | Pocket-size list of instructions. List group names, functions, codes, and bit assignments. Includes ASCII codes and the bootstrap loader. |
| Logic Handbook | Presents functions and specifications of the M-Series logic modules and accessories used in PDP-11 interfacing. Includes other types of logic produced by DEC but not used with the PDP-11. |
| Introduction to Minicomputer Networks | Principles of computer-based data communications technology. |
| Binary Synchronous Communications | Introduction to IBM's Binary Synchronous Communications Protocol (BISYNC or BSC). |
| A Message-Oriented Protocol for Interprocessor Communication | Introduction to DEC's Digital Data Communication Message Protocol (DDCMP). |
| Data Set 201A and 201B Interface Specifications | Description of interface leads in synchronous modems. |
| Data Set 201C Interface Specification | Interface Specification |
| Data Set 208A Interface Specification | Interface Specification |
| Data Set 208B Interface Specification | Interface Specification |
| SOFTWARE | |
| Paper-Tape Software Programming Handbook | Detailed discussion of the PDP-11 software system used to load, dump, edit, assemble, and debug PDP-11 programs. Also included is a discussion of input/output programming and the floating-point and math package. |

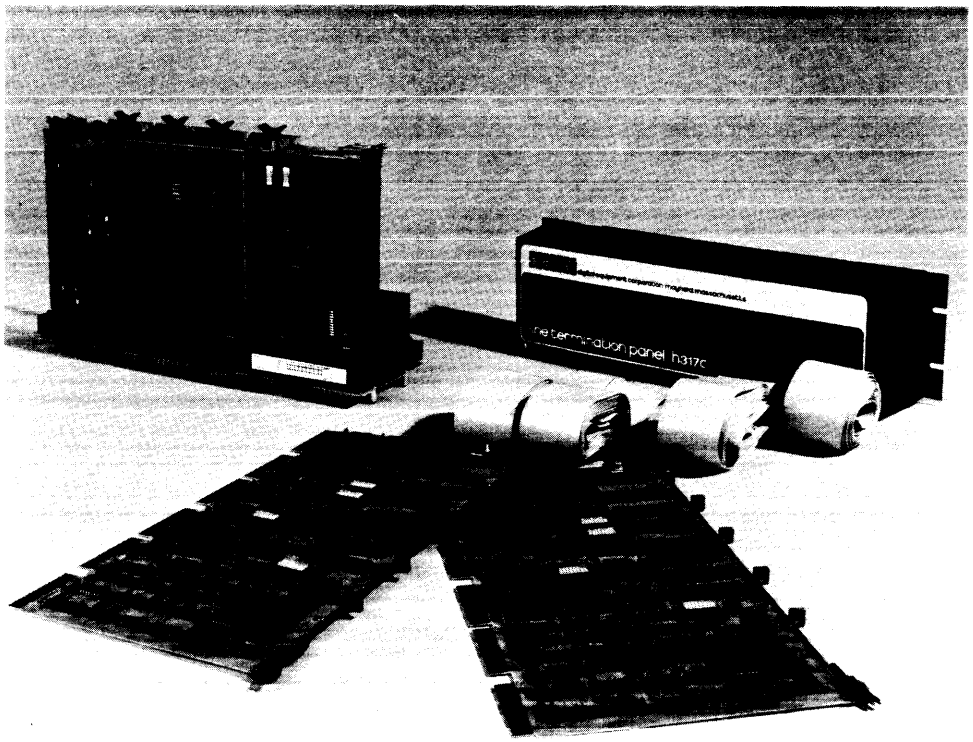


Figure 1-2 DV11 Communications Multiplexer

**Parity Generation and Detection**
Odd, Even, or None

**Modems Accommodated**
Synchronous modems (Bell System 201, 208, 209, or equivalent)

Asynchronous modems (Bell System 202 series, 103 series or equivalent)

**Bus Loading**
Two PDP-11 Unibus Loads

**Protocols Implemented**
The DV11 specifically implements (but is not limited to) Digital's DDCMP and IBM's BISYNC protocols.

**Maximum Throughput**
38,400 characters/second

**Sync Character Facility**
Synchronization of a line can be selected to be on the basis of the receipt of either one sync character or two consecutive, identical sync characters. For each 4-line group, two sync codes may be manually preset in switches. The PDP-11 program may select either of those two sync codes for use on a selected line.

NOTE

**Since the DV11 requires 21 A of +5 V power, only three DV11s can be placed on a typical 21-in. expander box. Expander boxes usually contain three H744 regulators, each of which has a capacity of 25 A. A device cannot be powered partially from one regulator and partially from another regulator; the number of DV11s must equal the number of regulators. Therefore, three DV11s is the maximum for one expander box.**

# CHAPTER 2
# INSTALLATION

This chapter provides information for interfacing, installing, and testing the DV11 Communications Multiplexer. Interfacing considerations are discussed in Section 2.1, Site Preparation and Planning. Installation, customizing, and checkout procedures are discussed in Sections 2.2 through 2.7.

## 2.1 SITE PREPARATION AND PLANNING

### 2.1.1 Minimum Through Maximum Configurations

The DV11 provides multiplexing capability to PDP-11 core memory for up to 16 modems. The DV11 is housed in a nine-slot, double system unit and includes one rack-mounted distribution panel for each group of eight modems in a system. Five of the nine slots are occupied by functions required in any system configuration. The remaining four slots are occupied by four hex-printed circuit boards (M7839 or M7833), designated as the line cards. Each line card is capable of supporting data transfers to and from four modems. The M7839 line card supports synchronous data transfers while the M7833 supports asynchronous data transfers (these line cards contain the receivers and transmitters).

The 5-module unit common to all DV11 configurations is designated the DV11-AA. Two of the M7839 module, plus one distribution panel and associated cables, form an eight line synchronous unit designated the DV11-BA. An eight line asynchronous unit, the DV11-BB, is generated by replacing the M7839 modules in the DV11-BA unit with two M7833 modules. Similarly, a mixture of one of each line card forms a synchronous/asynchronous unit designated the DV11-BC. The minimum DV11 system configuration consists of one DV11-AA unit plus one line card option, DV11-BA, DV11-BB or DV11-BC; a maximum configuration consists of one DV11-AA unit plus two line card options.

### 2.1.2 Compatibility Considerations and Precautions

The DV11 with synchronous line cards is directly compatible with Bell synchronous modems 201, 208, 209, or equivalent. It is also compatible with Bell asynchronous modems 202 series, 103 series or equivalent when asynchronous line cards are used. The DV11 provides internaal clock rates of 1200, 2400, 4800, and 9600 baud at 0.005% accuracy for synchronous operation; modems operating at other rates must supply their own clock signals. It is recommended that modem-supplied clocking be used where available.

The DV11 is compatible with all members of the PDP-11 family of computers. PDP-11 standard software address allocations provide for the implementation of as many as four DV11s in a PDP-11 system. DV11 throughput rate, however, forms a more severe limitation on the number of DV11s in a system, as will now be demonstrated.

A single DV11 multiplexing 16 modems at 9600 baud, each in full duplex mode, is capable of transferring 38,400 8-bit characters per second (1200 characters per line × 16 lines × 2 directions). Although this is well within the capabilities of the DV11, on the average, the PDP-11 is provided with only 26 $\mu$s to handle each character. Although most characters are handled by NPR transfers, program and protocol efficiencies still need to be relatively high to maintain this rate; this would be for a single DV11. Some 76,800 NPR c/s would be required, or about 10 percent of Unibus capacity. With all lines operated in DDCMP mode (control byte fetch inhibited), 38,400 NPR c/s would be required, or about 5 percent of Unibus capacity.

DV11s should be connected ahead of all Massbus devices on the Unibus and behind unbuffered NPR devices such as RK05s. DV11s have placement requirements similar to those for DQ11s. If both DQ11s and DV11s are used, place the units with the highest baud rate first. If all DV11s have 16 lines at a 9600 baud rate, a maximum of 1 DV11 can be connected with the following exceptions:

a. Two DV11s can be used on a PDP-11/40, PDP-11/45, or PDP-11/50 with no disks.

b. Two DV11s can be used on a PDP-11/70 with no Unibus disks.

For lower speed lines, the maximum number can be increased proportionally. (Example: a PDP-11/40 with 2400 baud rate lines can use four DV11s.) A maximum of four DV11s can be placed on any system because of address space limitations; the limitations are based on NPR access. Interrupt performance depends on the operating system, protocol, and buffer lengths.

### 2.1.3 Interface Specifications and Signals

The DV11 presents two unit loads to the PDP-11 Unibus and also provides modem control and data leads compatible with EIA RS-232-C and CCITT-V24 specifications. EIA RS-232-C electrical specifications are listed in Table 2-1.

### 2.1.4 Interrupt Priorities and Address Assignments

**2.1.4.1 Interrupt Priorities** – The DV11 uses three interrupt vector addresses. Interrupt priorities for the Data Handling Section are selectable by means of a priority plug on the M7837 module. The priority plug is preset to select BR5 priority; it may be changed to select BR6 priority, but the diagnostic programs expect BR5. The Modem Control Unit is permanently wired to BR4 priority.

**2.1.4.2 Interrupt Vector Address Assignment** – Communications devices are assigned floating interrupt vector addresses as follows:

1. The vector space starts at location 300 and proceeds upward to 776.
2. The devices are assigned in order by type: DC11; KL11/DL11-A, -B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Reader; PA611 Punch; DT11; DX11; DL11-C, -D, -E; DJ11; DH11; GT40; LPS11; VT20; DQ11; KW11-W; DU11; DUP11; DV11 Data Handling Section/DV11 Modem Conrol Unit.
3. If any type device is not used in a system, vector assignments move down to fill the vacancies.
4. If additional devices are to be added to the system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required. (For example, the vector for another DV11 would be after the existing DV11, but addition of a DC11 would cause all other vector addresses to move upward.)

Each device interrupt vector requires four address locations (two words). A further constraint is that all vector addresses must end in 0 or 4. The vector address is specified as a three-digit, binary-coded octal number using Unibus data bits 0–8. Because the vector must end in 0 or 4, bits 1 and 0 are not specified (they are always 0) and bit 2 determines the least significant octal digit of the vector address (0 or 4).

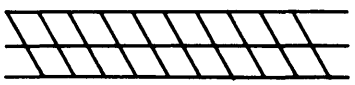
**2.1.4.3 Address Assignments** – The DV11 is assigned an address of 775000. Additional DV11s would be at 775040, 775100, 775140, etc. If any DM11-AAs are in use, the DV11 will follow them.

### 2.1.5 Environment

The DV11 will operate in temperature environment from 10° to 50° C with a relative humidity up to 90%, non-condensing. Power requirements are as follows:

| Voltage | Current (Amperes) |
|---|---|
| +5 | 21 |
| -15 | 1 |
| +15 | 0.5 |

**Table 2-1**
**EIA Electrical Specifications**

| | |
|---|---|
| Driver output logic levels with 3K to 7K load | $15\ V > _{oh} > 5\ V$<br>$-5\ V > _{ol} > -15\ V$ |
| Driver output voltage with open circuit | $/V_o/ < 25\ V$ |
| Driver output impedance with power off | $20 > 300$ ohms |
| Output short circuit current | $/I_o/ < 0.5\ A$ |
| Driver slew rate | $\frac{dv}{dt} < 30\ V\mu s$ |
| Receiver input impedance | $7K\Omega > R_{in} > 3K\Omega$ |
| Receiver input voltage | ± 15 V compatible with driver |
| Receiver output with open circuit input | Mark |
| Receiver output with +3 V input | Space |
| Receiver output with -3 V input | Mark |
| +15<br>+5<br>  | LOGIC "0" = SPACE – CONTROL ON<br>Noise margin |
| +3<br>0<br>-3<br>  | Transition region<br>Noise margin |
| -5<br>-15<br>  | LOGIC "1" = MARK = CONTROL OFF |

## 2.2 UNPACKING AND INSPECTION

After unpacking, check that the following parts are present for the basic DV11-AA unit:

1 D-AD-7010834-0-0 Logic Assembly
1 M7807 Bus Control and Mux Board
1 M7808 Modem Control Scan and Mux Board
1 M7836 ALU and Transfer Bus Board
1 M7837 Unibus Data and NPR Control Board
1 M7838 ROM, RAM, and Branch Board
1 M920 Unibus Connector

Also check that the following parts are present for each line card option ordered:

2 H8612 Line Card Test Connectors
1 H317C Distribution Panel
4 BC08R-15 Cables
1 H325 Test Connector

DV11-BA: 2 M7839 Sync Mux Line Card

DV11-BB: 2 M7833 Async Mux Line Card

DV11-BC: 1 M7839 Sync Mux Line Card; 1 M7833 Async Mux Line Card

## 2.3 INSTALLATION OF BASIC ASSEMBLIES

Drawing D-UA-DV11-0-0 shows the physical arrangement of the wired backplane, distribution panel(s) and cables in a typical installation. Figure 2-1 is the DV11 interconnection schematic. Install the 9-slot, double system unit in the expander box or processor box as space and power are available. With power off, test the resistances between all pins of the power harness Mate-N-Lok connector. Only pins of the same wire color should be connected. Secure the ground wire to one of the mounting screws. Plug in the Mate-N-Lok connector of the power harness. Apply power and check for proper voltages on the logic pins (not the cable) as follows:

| Voltage | Pin |
|---|---|
| +5 ± 0.25 V | C1A2 |
| -15 ± 0.75 V | C1B2 |
| +15 ± 0.75 V | C1U1 |

This will ensure that the cable and the Mate-N-Lok connector were correctly installed. Turn power off. (Note that the DV11 is not yet connected to the Unibus, nor are any modules installed.)

Install the distribution panel(s) as indicated in Figure 2-1. Refer to Figure 2-7 for the proper jumper configuration of the distribution panel. To install an add-on DV11, see Paragraph 2.4.4.

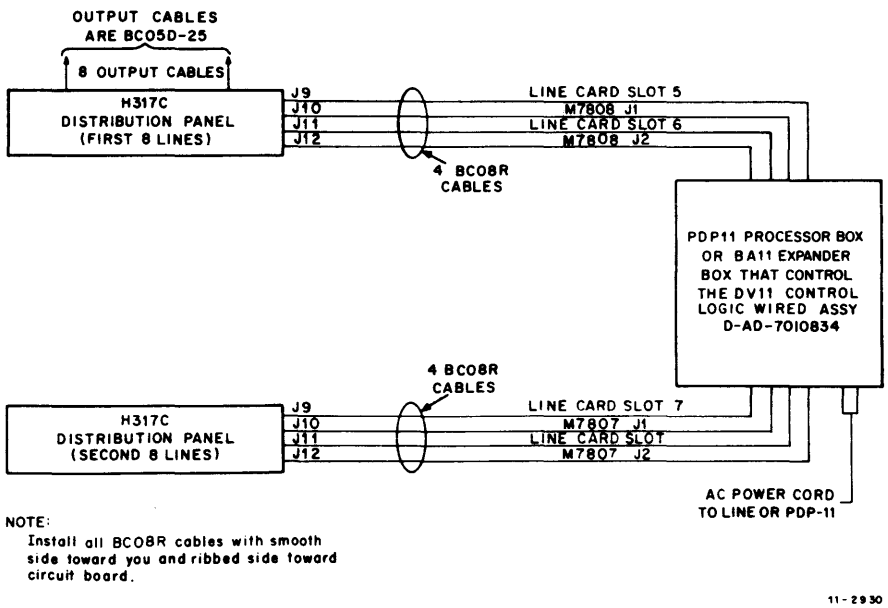



Figure 2-1 DV11 Interconnection Diagram

### 2.3.1 Unibus Cable Interconnections

The DV11 is shipped with one M920 Unibus Connector (placed in slot 9 as shown in the module utilization program, Figure 2-2), which provides for electrically connecting the unit to the PDP-11 Unibus. For processor box installation where the unit is to be electrically placed in mid-bus (i.e., somewhere between the first and last devices on the PDP-11 Unibus), the M920 from the next higher device (closer to the processor) on the bus is plugged into slot 1 of the DV11, and the M920 in slot 9 of the DV11 is plugged into slot 1 of the next lower device on the bus.

For an end-of-bus installation of the DV11, proceed as follows:

1. Remove the M930 Unibus Terminator from the last slot of the current end-of-bus device.
2. Remove the M920 from slot 9 of the DV11 and place in slot 1 of the DV11.
3. Install the M930 (removed in step 1) in slot 9 of the DV11.

Unibus interconnections are made via BC11-A cables where the DV11 is installed in expander box or is physically the first or last unit in any box. Cable requirements in these cases are as described in Figure 2-2.

## 2.4 MODULE INSTALLATION AND CUSTOMIZING

Figure 2-2 is the module utilization diagram. Set the address assignment and parameter selection switches as described in Paragraphs 2.4.1 and 2.4.2 before installing modules.

### 2.4.1 Unibus and Interrupt Vector Address Assignments

The Unibus and interrupt vector addresses for the DV11 must be set manually before operating the DV11. Two Unibus addresses (also called device addresses) and two interrupt vector addresses are provided on the DV11 as follows:

1. DV11 Data Handling Section address,
2. DV11 MCU address,
3. DV11 Data Handling Section interrupt vector address,
4. DV11 MCU interrupt vector address.

Because the DV11 has ten registers directly addressable by the PDP-11 program, it must be assigned a Unibus address that is a multiple of 32 (octal 40). All DV11s in a system should have consecutive addresses.

The Unibus addresses for the DV11 Data Section are controlled by a rocker DIP switch package, located on module M7836, and by jumper straps on module M7807 for the DV11 MCU. (Locations of all address selection switches and jumpers are shown in Figures 2-3 through 2-5.) The position of these switches determines bits 03–12 of the Unibus address. If a rocker switch is set to ON or a jumper on the M7807 board is in, an address bit of zero in the corresponding bit position serves to address the DV11 Data Handling Section. DEC standard software requires that the DV11 address be set as specified in Paragraph 2.1.4. Switch settings for device address selection are shown in Table 2-2.

The interrupt vector address for the Data Handling Section is controlled by a DIP switch package on the M7837 module, which selects vector address bits 08–03. The switches should be set to select vector addresses between 300 and 776. Switch settings for interrupt vector address selection for the Data Handling Section are shown in Table 2-3. Vector address selection for the Modem Control Unit is done by jumpers on the M7807 module (Table 2-4).

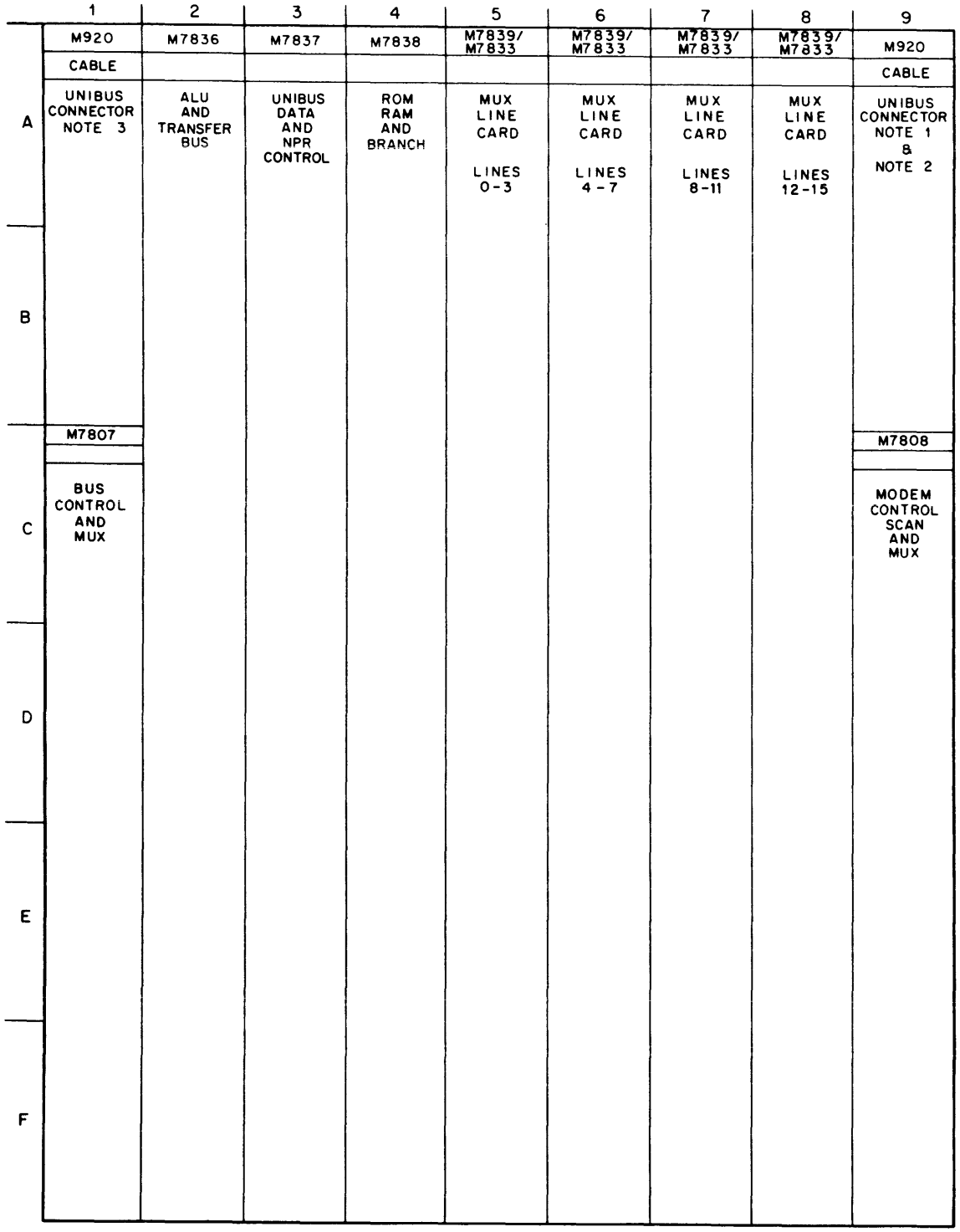



Figure 2-2 Module Utilization Diagram

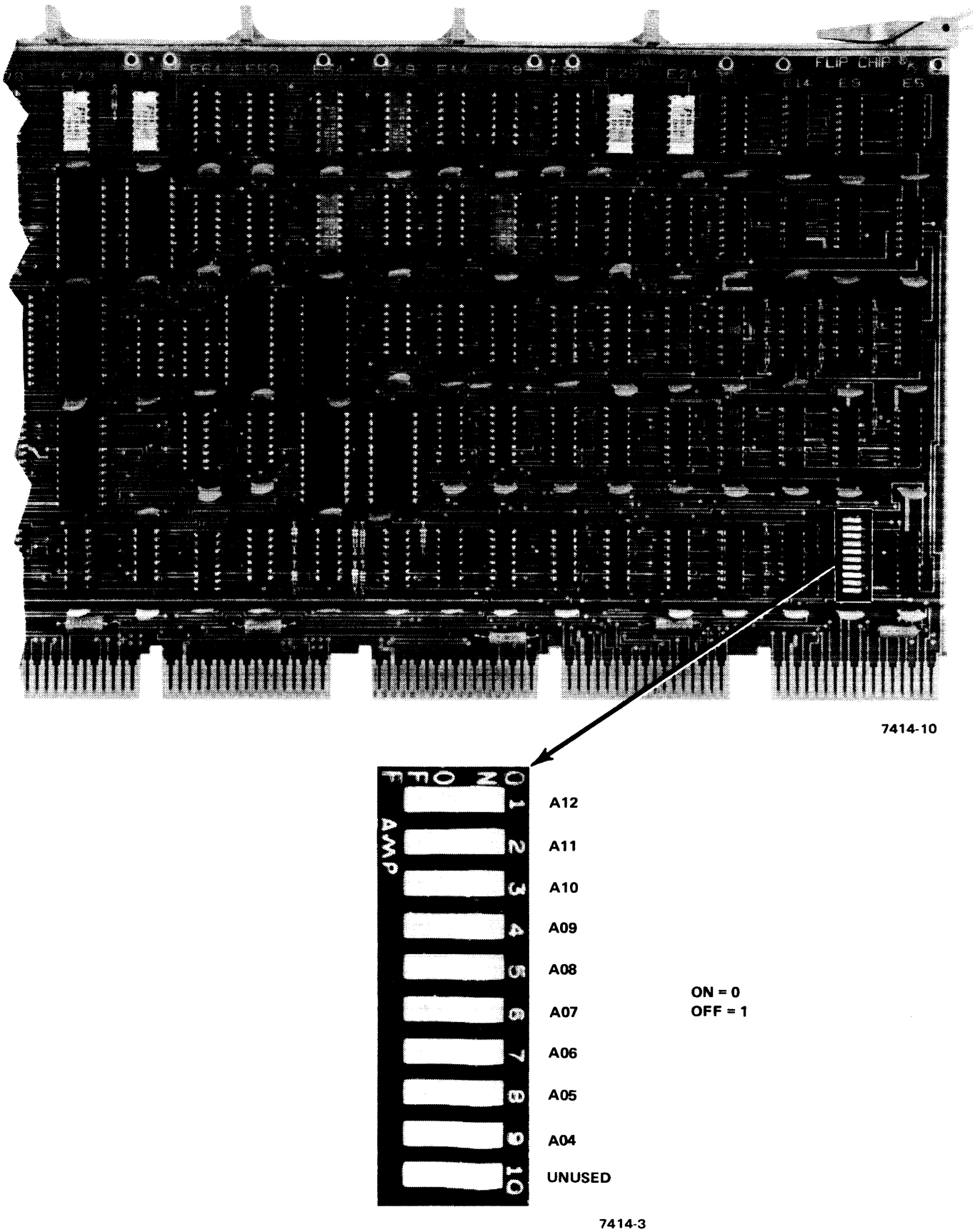
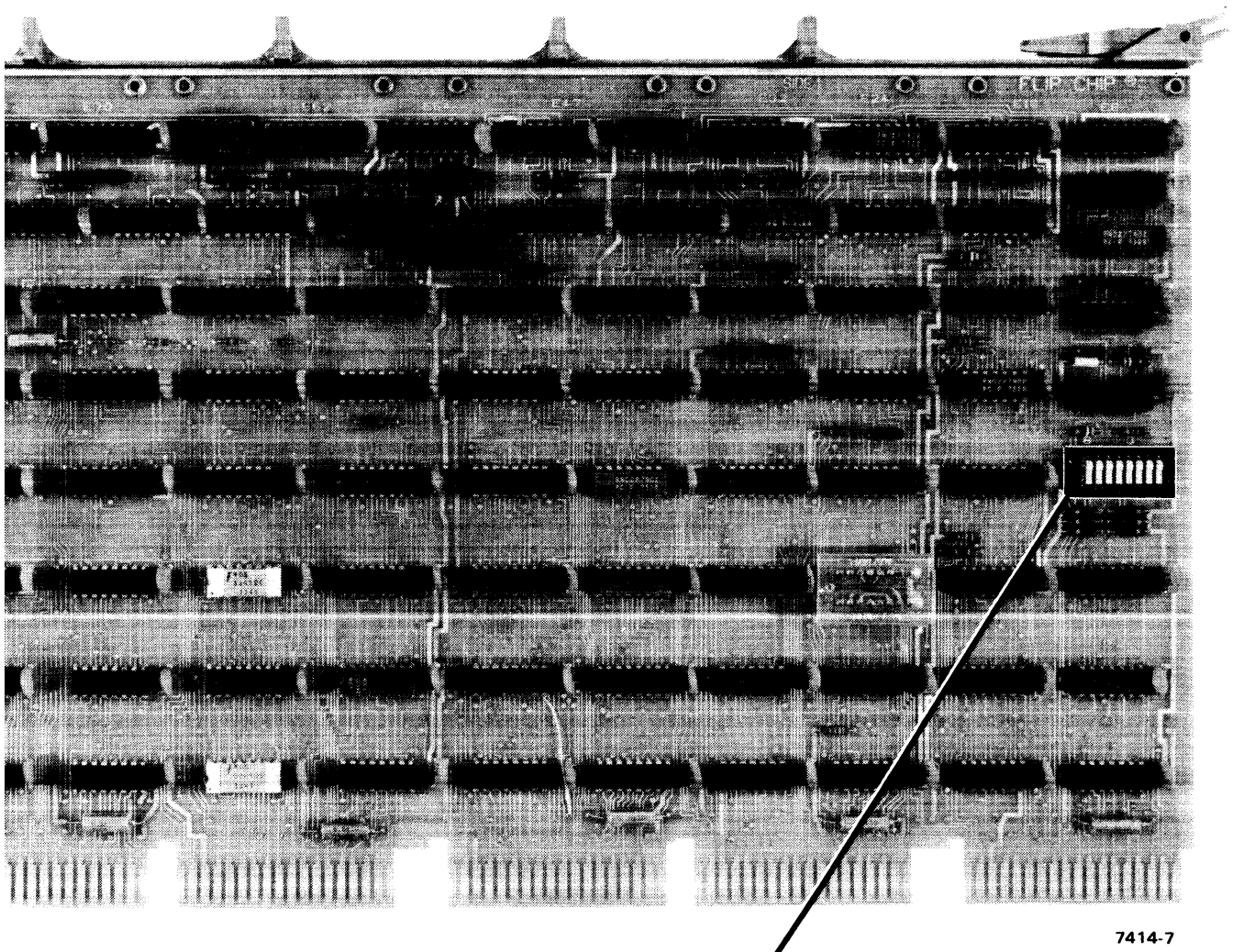



Figure 2-3 DV11 M7836 Module – Device Address Selection Switches



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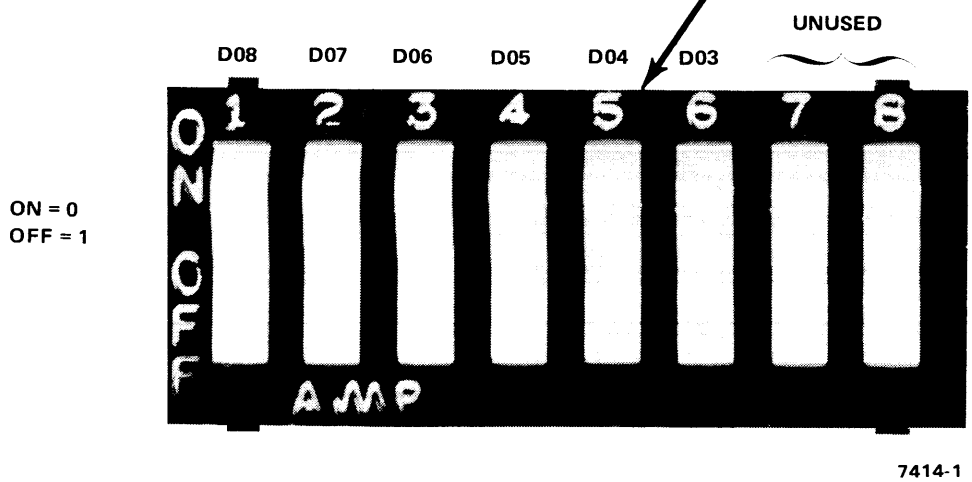


ON = 0
OFF = 1

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Figure 2-4 DV11 M7837 Module – Interrupt Vector Address Selection Switches for DV11 Data Handling Section

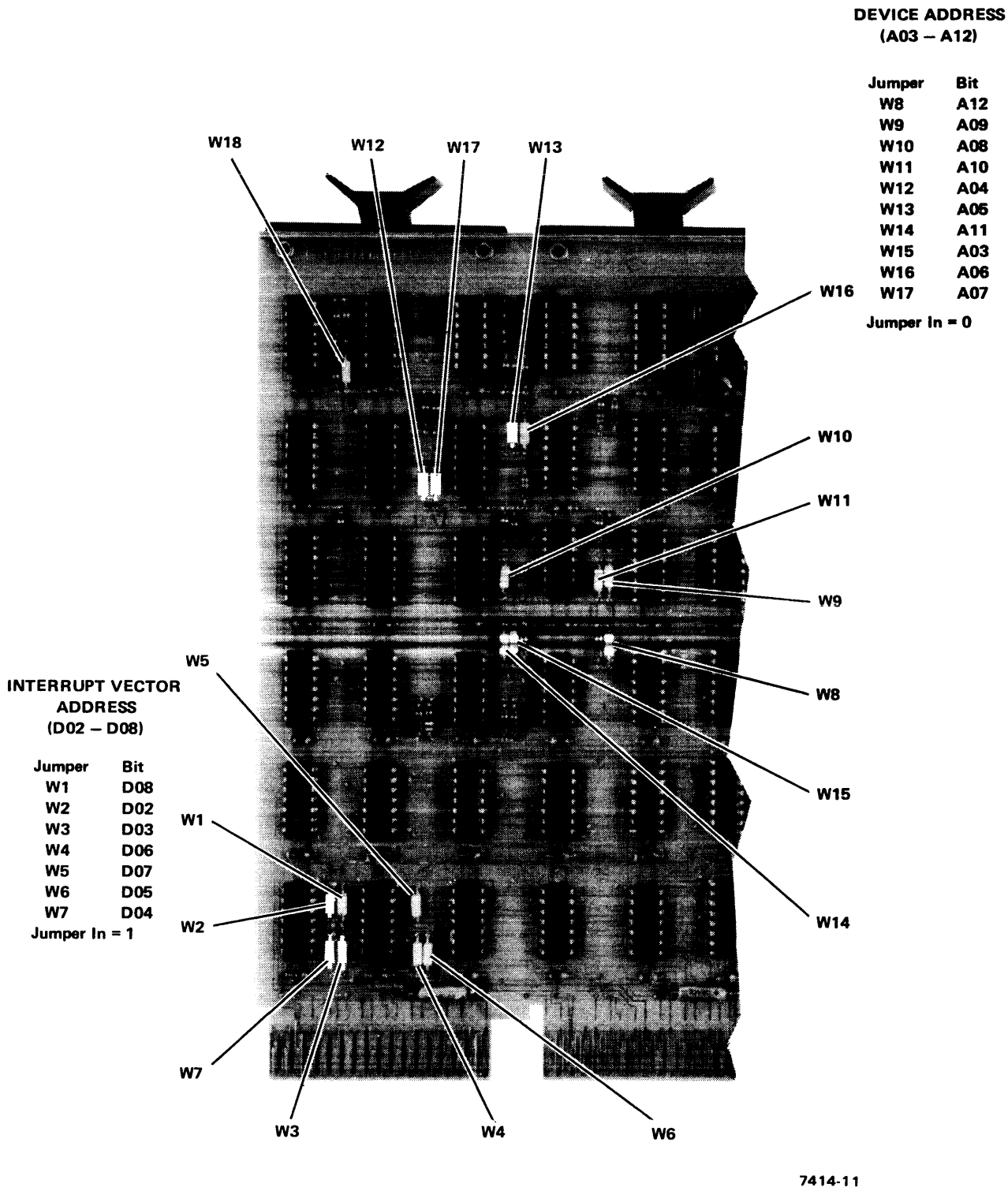



Figure 2-5 DV11 M7807 Module – Device Address Selection Jumpers and Interrupt Vector Address Selection Jumpers for DV11 Modem Control Unit

**Table 2-2**
**Device Address Switches**

| M7807 Jumper | W8 | W14 | W11 | W9 | W10 | W16 | W17 | W13 | W12 | W15 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M7836 Switch | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | | Device | |
| Address Bit | A12 | A11 | A10 | A09 | A08 | A07 | A06 | A05 | A04 | A03* | Address | Notes |
| | X | X | | X | | | | | | | 775000 | First DV11 |
| | X | X | | X | | | | | X | | 775020 | First DV11 MCU |
| | X | X | | X | | | | X | | | 775040 | Second DV11 |
| | X | X | | X | | | | X | X | | 775060 | Second DV11 MCU |
| | X | X | | X | | | X | | | | 775100 | Third DV11 |
| | X | X | | X | | | X | | X | | 775120 | Third DV11 MCU |
| | X | X | | X | | | X | X | | | 775140 | Fourth DV11 |
| | X | X | | X | | | X | X | X | | 775160 | Fourth DV11 MCU |

Note: X means switch off (M7836) or Jumper out (M7807).

*Bit 3 selection applies to M7807 only. No bit 3 switch is provided on M7836 module.

Table 2-3
Vector Address Switches for Data Handling Section
(Vector Addresses are Modulo 10)

| M7837 Switch | 1 | 2 | 3 | 4 | 5 | 6 | Vector |
|---|---|---|---|---|---|---|---|
| Address Bit | D08 | D07 | D06 | D05 | D04 | D03 | Address |
| | X | | | X | X | X | 300 |
| | X | | | X | X | | 310 |
| | X | | | X | | X | 320 |
| | X | | | X | | | 330 |
| | X | | | | X | X | 340 |
| | X | | | | X | | 350 |
| | X | | | | | X | 360 |
| | X | | | | | | 370 |
| | | X | X | X | X | X | 400 |
| | | X | X | X | X | | 410 |
| | | X | X | X | | X | 420 |
| | | X | X | X | | | 430 |
| | | X | X | | X | X | 440 |
| | | X | X | | X | | 450 |
| | | X | X | | | X | 460 |
| | | X | X | | | | 470 |
| | | X | | X | X | X | 500 |
| | | X | | X | X | | 510 |
| | | X | | X | | X | 520 |
| | | X | | X | | | 530 |
| | | X | | | X | X | 540 |
| | | X | | | X | | 550 |
| | | X | | | | X | 560 |
| | | X | | | | | 570 |
| | | | | | | | etc. to |
| | | | | | | | 770 |

Notes: 1. X means switch ON

2. Set only the switches shown.

3. Vector Address Bit D02 is controlled by DV11 logic dependent on whether a Receiver Interrupt (Bit D02 = 0 = Vector A) or a Transmitter Interrupt (Bit D02 = 1 = Vector B) is being requested.

Table 2-4
Vector Address Jumpers for Modem Control Unit
(MCU Vector Addresses are Modulo 4)

| M7807 Jumper | W1* | W5 | W4 | W6 | W7 | W3 | W2 | Vector |
|---|---|---|---|---|---|---|---|---|
| Address Bit | D08 | D07 | D06 | D05 | D04 | D03 | D02 | Address |
| | X | | | X | X | X | X | 300 |
| | X | | | X | X | X | | 304 |
| | X | | | X | X | | X | 310 |
| | X | | | X | X | | | 314 |
| | X | | | X | | X | X | 320 |
| | X | | | X | | X | | 324 |
| | X | | | X | | | X | 330 |
| | X | | | X | | | | 334 |
| | X | | | | X | X | X | 340 |
| | X | | | | X | X | | 344 |
| | X | | | | X | | X | 350 |
| | X | | | | X | | | 354 |
| | X | | | | | X | X | 360 |
| | X | | | | | X | | 364 |
| | X | | | | | | X | 370 |
| | X | | | | | | | 374 |
| | | X | X | X | X | X | X | 400 |
| | | X | X | X | X | X | | 404 |
| | | X | X | X | X | | X | 410 |
| | | X | X | X | X | | | 414 |
| | | X | X | X | | X | X | 420 |
| | | X | X | X | | X | | 424 |
| | | X | X | X | | | X | 430 |
| | | X | X | X | | | | 434 |
| | | X | X | | X | X | X | 440 |
| | | X | X | | X | X | | 444 |
| | | X | X | | X | | X | 450 |
| | | X | X | | X | | | 454 |
| | | X | X | | | X | X | 460 |
| | | X | X | | | X | | 464 |
| | | X | X | | | | X | 470 |
| | | X | X | | | | | 474 |
| | | X | | X | X | X | X | 500 |
| | | X | | X | X | X | | 504 |

Table 2-4 (Cont)
Vector Address Jumpers for Modem Control Unit
(MCU Vector Addresses are Modulo 4)

| M7807 Jumper | W1* | W5 | W4 | W6 | W7 | W3 | W2 | Vector |
|---|---|---|---|---|---|---|---|---|
| Address Bit | D08 | D07 | D06 | D05 | D04 | D03 | D02 | Address |
| | | X | | X | X | | X | 510 |
| | | X | | X | X | | | 514 |
| | | X | | X | | X | X | 520 |
| | | X | | X | | X | | 524 |
| | | X | | X | | | X | 530 |
| | | X | | X | | | | 534 |
| | | X | | | X | X | X | 540 |
| | | X | | | X | X | | 544 |
| | | X | | | X | | X | 550 |
| | | X | | | X | | | 554 |
| | | X | | | | X | X | 560 |
| | | X | | | | X | | 564 |
| | | X | | | | | X | 570 |
| | | X | | | | | | 574 |
| | | | | | | | | etc. to 774 |

Notes: 1. X means jumper OUT

2. Cut only the jumpers shown.

3. *Jumper W1 is in for the PDP-11/20 with the KH11 and for the PDP-11/40, PDP-11/45, and newer PDP-11s.

### 2.4.2 Synchronous Parameter Selection

Rocker DIP switches are located on each M7839 module for selection of the following synchronous data channel parameters:

1. Internal baud rate (1200, 2400, 4800, 9600)
2. Full/half duplex
3. Parity (odd/even/none)
4. Character length (5, 6, 7, or 8 bits)
5. Sync requirement (whether one sync character or two consecutive, identical sync characters are required to achieve line synchronization).
6. Sync character codes

Switch settings for each synchronous parameter are listed in Table 2-5. Switch locations are shown in Figure 2-6.

**NOTE**

**Whenever possible, the parameters should be configured per customer requirements at this time. If half-duplex or parity operation is required, this configuration can only be done after diagnostics have been run. DV11 diagnostics don't support half-duplex or parity operation.**

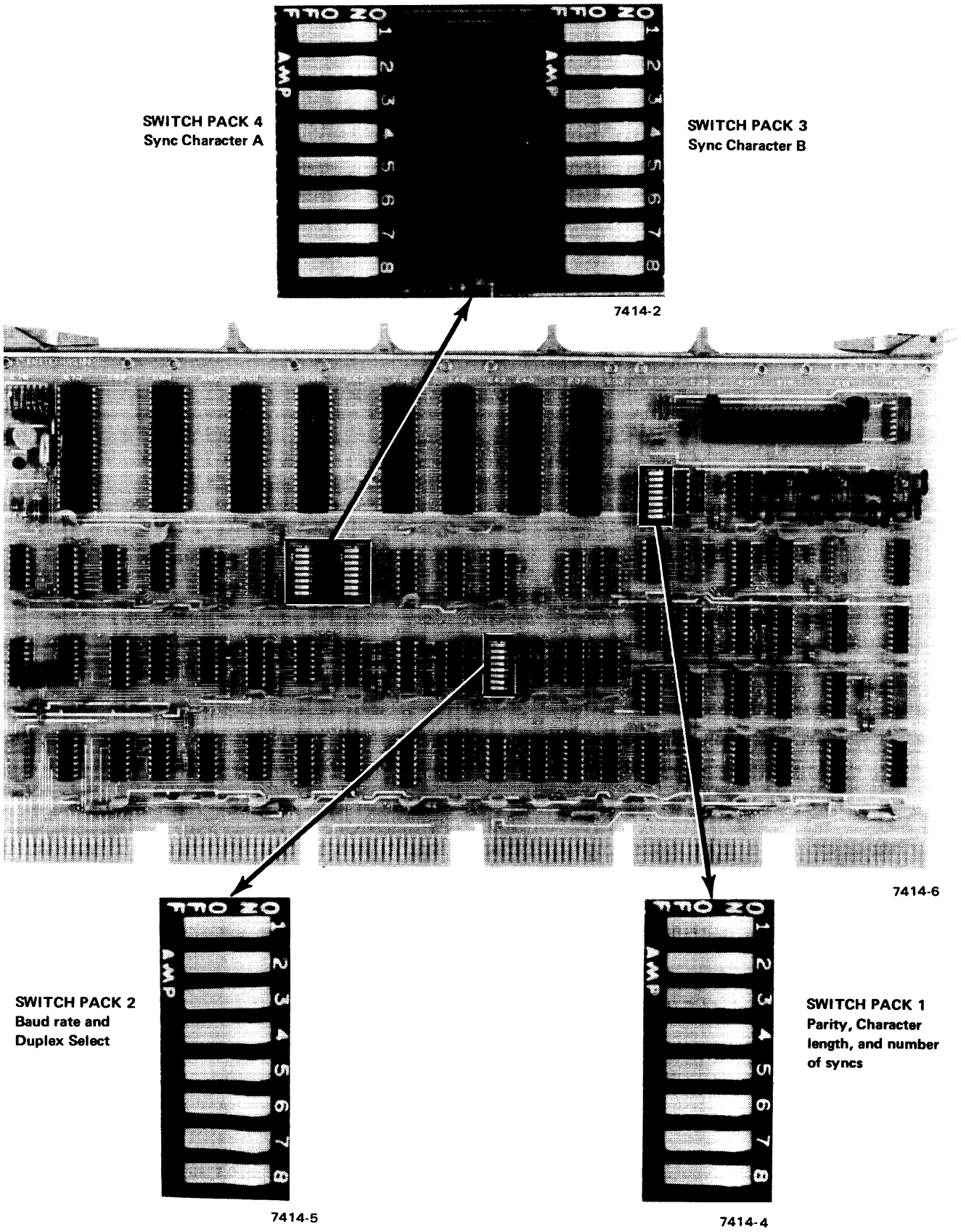



Figure 2-6 Location of Sync Switches on M7839 Module

**Table 2-5**
**Synchronous Parameter Selection Switches**

| Function | Parameter | Switch | | | Setting |
|---|---|---|---|---|---|
| | | Name | Pack | Number | |
| Internal Baud Rate | 1200 Baud | Select B | S2 | 3 | ON |
| | | Select A | S2 | 4 | ON |
| | 2400 Baud | Select B | S2 | 3 | ON |
| | | Select A | S2 | 4 | OFF |
| | 4800 Baud | Select B | S2 | 3 | OFF |
| | | Select A | S2 | 4 | ON |
| | 9600 Baud | Select B | S2 | 3 | OFF |
| | | Select A | S2 | 4 | OFF |
| Full/Half Duplex | Full Duplex* | HD3 | S2 | 5 | ON |
| | | HD2 | S2 | 6 | ON |
| | | HD1 | S2 | 7 | ON |
| | | HD0 | S2 | 8 | ON |
| | Half Duplex | HD3 | S2 | 5 | OFF |
| | | HD2 | S2 | 6 | OFF |
| | | HD1 | S2 | 7 | OFF |
| | | HD0 | S2 | 8 | OFF |
| Parity | No Parity* | PI | S1 | 1 | OFF |
| | | EPE | S1 | 2 | OFF |
| | Odd Parity | PI | S1 | 1 | ON |
| | | EPE | S1 | 2 | ON |
| | Even Parity | PI | S1 | 1 | ON |
| | | EPE | S1 | 2 | OFF |
| Character Length (Excluding Parity) | 8 Bits/Char | WLS1 | S1 | 3 | OFF |
| | | WLS2 | S1 | 4 | OFF |
| | 7 Bits/Char | WLS1 | S1 | 3 | ON |
| | | WLS2 | S1 | 4 | OFF |
| | 6 Bits/Char | WLS1 | S1 | 3 | OFF |
| | | WLS2 | S1 | 4 | ON |
| | 5 Bits/Char | WLS1 | S1 | 3 | ON |
| | | WLS2 | S1 | 4 | ON |
| SYNC Requirement | 1 SYNC REQ. | 1 SYNC 00 | S1 | 5 | OFF |
| | | 1 SYNC 01 | S1 | 6 | OFF |
| | | 1 SYNC 02 | S1 | 7 | OFF |
| | | 1 SYNC 03 | S1 | 8 | OFF |

*Must be selected to run diagnostics DZDVA to DZDVE.

Table 2-5 (Cont)
Synchronous Parameter Selection Switches

| Function | Parameter | Switch | | | Setting |
|---|---|---|---|---|---|
| | | Name | Pack | Number | |
| Sync Req. (cont) | 2 SYNC REQ. | 1 SYNC 00 | S1 | 5 | ON |
| | | 1 SYNC 01 | S1 | 6 | ON |
| | | 1 SYNC 02 | S1 | 7 | ON |
| | | 1 SYNC 03 | S1 | 8 | ON |
| Sync Character Codes | Desired Code | Sync A | S4 | 1 ↓ 8 | (As required OFF=Logical one) |
| | Desired Code | Sync B | S3 | 1 ↓ 8 | (As required OFF=Logical one) |

Line synchronization can be selected by the receipt of either one sync character or two consecutive, identical sync characters. For each 4-line group, two sync codes (Sync A or Sync B) may be manually preset in the Sync Character Code switches. The PDP-11 program may select either of these two sync codes for use on a selected line.

Internal baud rate is determined by the ON/OFF states of the Select A and Select B switches. This is applicable only when the modem does not supply clocking.

### 2.4.3 Resistance Checks

Measure the resistance between the following pins on the backplane with the white plug of the 7010835 cable hanging free (not plugged in), and with all modules plugged in:

+5 V to GND must be 0.5 Ω or greater
-15 V to GND must be 50 Ω or greater
+15 V to GND must be 10 Ω or greater

If the resistance is less than the lower limit indicated, check for a short. If the resistance exceeds five times the low limit, it may indicate an open circuit. Make each measurement *twice*, once for each polarity of the meter. The lowest reading must not be less than the low limit listed. If the above resistances are correct, connect the white plug in accordance with D-UA-DV11-0-0.

### 2.4.4 Installation of Add-On DV11

Proceed as follows to install an add-on DV11:

1. Install the wired backplane assembly in the mounting box.
2. Measure the resistance between pins of the power harness (see first paragraph of Section 2.3).
3. Plug in the Mate-N-Lok connector of the power harness.
4. Apply power and measure voltages at the logic pins (Paragrah 2.3).
5. Turn power off.
6. Set all address, parameter switches (Paragraphs 2.4.1 and 2.4.2) and distribution panel jumpers (Figure 2-7).
7. Install modules (Figure 2-2).
8. Unplug the power harness.
9. Do resistance checks (Paragraph 2.4.3).
10. Apply power.

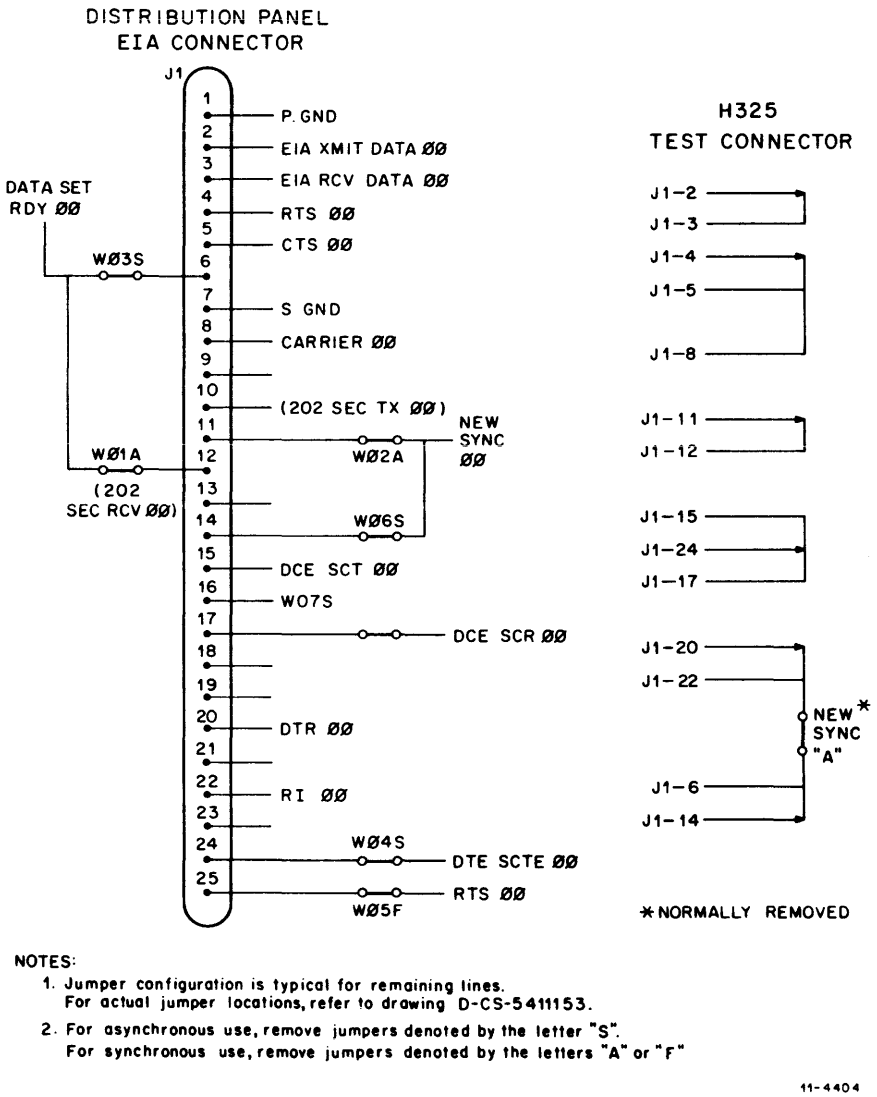
## 2.5 SYSTEM CHECKOUT

Turn on the power. Toggle in the Bootstrap and load the Absolute Loader (if not already done). The addresses and contents of the Bootstrap Loader are listed below.

| | Address | Contents |
|---|---|---|
| Memory size determines the first 3 digits: | ---744 | 016 701 |
| | ---746 | 000 026 |
| ---Equals: | ---750 | 012 702 |
| 017 for 4K | ---752 | 000 352 |
| 037 for 8K | ---754 | 005 211 |
| 057 for 12K | ---756 | 105 711 |
| 077 for 16K | ---760 | 100 376 |
| 117 for 20K | ---762 | 116 162 |
| 137 for 24K | ---764 | 000 002 |
| 157 for 28K | ---766 | ---400 |
| | ---770 | 005 267 |
| | ---772 | 177 756 |
| | ---774 | 000 765 |
| | ---776 | 177 560 (TTY Reader) or 177 550 (High speed reader) |

Place Absolute Loader (MAINDEC-11-LZPA-PO) in the reader, load and start at address ---744. Place the diagnostic tape in the reader, load and start att address ---500. Load and run the DV11 diagnostics as specified in Chapter 5 to verify system operation.

If half-duplex or parity operation is desired, configure the M7839s accordingly (Table 2-5).




NOTES:

1. Jumper configuration is typical for remaining lines.
   For actual jumper locations, refer to drawing D-CS-5411153.
2. For asynchronous use, remove jumpers denoted by the letter "S".
   For synchronous use, remove jumpers denoted by the letters "A" or "F"

11-4404

Figure 2-7 Distribution Panel and Test Connector Jumper Configuration

# CHAPTER 3
# PROGRAMMING

This chapter contains all information required for controlling operation of the DV11 Communications Multiplexer by means of the PDP-11 program. (Chapter 1 should be read prior to this chapter.) The reader should also be familiar with synchronous protocols as discussed in Appendix B. Chapter contents are arranged as follows:

1. Programmable Facilities and Functions: The programmable registers, core memory table references, and functions of the DV11 are discussed (Section 3.1).

2. Complete, detailed descriptions of programmable registers and control bytes (Sections 3.2, 3.3, 3.4).

3. Procedures for DV11 initialization (Section 3.5).

4. Methods for controlling data transfers and implementing protocols (Section 3.6).

Section 3.1 describes DV11 functions in sufficient detail to enable the reader to omit a detailed study of the comprehensive reference data in Sections 3.2, 3.3, and 3.4, and to proceed directly to the procedural data in Sections 3.5 and 3.6.

## 3.1 PROGRAMMABLE FACILITIES AND FUNCTIONS

The DV11 is a core memory-to-synchronous/asynchronous data line multiplexer with special features to facilitate processing of a wide variety of communication protocols. Under the overall direction of the PDP-11 program, the DV11 sets up the data line modems, stores and retrieves data from core memory, monitors and reports error conditions, and examines each transmitted or received character to determine and respond to requirements for auxiliary protocol processing (i.e., block check calculations, data block terminations, control character handling).

The PDP-11 program directs DV11 activities through the programmable registers of the DV11, along with a control table set up in core memory for reference by the DV11.

### 3.1.1 Programmable Registers

The DV11 programmable registers consist of the "primary" system registers, which are directly addressable via the Unibus, plus "secondary" registers, which may be accessed by the PDP-11 program after first loading a primary register. (The primary register selects the secondary register to be accessed.) The directly-addressable registers provide for modem setup and control, data transfer enabling, interrupt enabling and reporting, extended memory addressing, and access to secondary registers. The secondary registers provide for protocol processing and data transfer control.

Ten directly-addressable registers are provided. There are 16 secondary registers provided for each of the 16 multiplexed data channels, for a total of 256 secondary registers. The secondary registers make up a separate Random Access Memory (RAM) within the DV11. Secondary registers store functions that may vary from line to line, and that require the extensive storage capacity of the RAM.

Functions of programmable registers are described in Paragraphs 3.2 and 3.3, following a discussion of the control table. Functions, functional categories, and table references for programmable registers are listed in Table 3-1, which is provided for reference during study of Paragraphs 3.1.3 and 3.1.4.

**Table 3-1**
**Functions of DV11 Programmable Registers**

| Type | Name | Functions | Functional Category | Table |
|---|---|---|---|---|
| Directly Addressable (Modem Control Unit) | Control Status Register (CSR) | Initialization, Modem Enabling, Modem Scanning, Interrupt Enabling, Interrupt Requests. | Modem Set Up and Control | 3-8 |
| | Line Status Register (LSR) | Modem Control, Modem Status Reporting | | 3-9 |
| Directly Addressable (Data Handling Section) | Secondary Register Selection (SRS) | Secondary Register Selection, Line Selection for Line Control Register Bits 9–14. | Secondary Register Accessing | - - - |
| | Secondary Reg. Access Reg. (SAR) | Read or Write Selected Secondary Register | | - - - |
| | System Control Register (SCR) | Initialization, Interrupt Enabling & Requests, Restart after Interrupt, Setting Extended Address Bits. | Data Transfer Enabling, Interrupt Enabling, Extended Memory Addressing | 3-2 |
| | Line Control Register (LCR) | Receiver Enabling, Sync Character Selection, Extended Address Bits Read, Baud Rate Select. Format Select. | | 3-3, 3-4 |
| | Receiver Interrupt Character (RIC) | Receive Interrupt Code and Interrupt Character Storage. | Interrupt Reporting | 3-5, 3-6 |
| | NPR Status Register/Silo (NSR) | Transmit Interrupt Code Storage | | 3-7 |
| | Special Functions Register (SFR) | (Maintenance) | - - - - - - | - - - |
| | Reserved Register (RIR) | (Reserved) | | - - - |
| Indirectly Addressable (Secondary) | Transmitter Principal Current Address | Current Address for Transmitter Principal Data Table | Data Transfer Control | - - - |
| | Transmitter Principal Byte Count | Byte Count for Principal Transmitter Data Table | | - - - |

**Table 3-1 (Cont)**
**Functions of DV11 Programmable Registers**

| Type | Name | Functions | Functional Category | Table |
|---|---|---|---|---|
| Indirectly Addressable (Secondary) (Cont) | Transmitter Alternate Current Address | Current Address for Transmitter Alternate Data Table | Data Transfer Control | |
| | Transmitter Alternate Byte Count | Byte Count for Alternate Transmitter Data Table | | |
| | Receiver Current Address | Current Address for Receiver Data Table | | |
| | Receiver Byte Count | Byte Count for Receiver Data Table | | --- |
| | Transmitter Accumulated BCC | Transmitter Accumulated BCC | | --- |
| | Receiver Accumulated BCC | Receiver Accumulated BCC | | --- |
| | Transmitter Control Table Base Address | Transmitter Control Table Base Address | | --- |
| | Receiver Control Table Base Address | Receiver Control Table Base Address | | --- |
| | Line Protocol Parameters | Block Check Polynomial Type, DLE Storage, Stripping Received Syncs, Idle Select | Protocol Processing | 3-10 |
| | Line State | Transmitter Enabling, Snapshot of line activity. Action required on zero receiver byte count (if marked). | | 3-11 |
| | Transmitter Mode Bits | Transmitter Mode now in use. | | --- |
| | Receiver Mode Bits | Receiver Mode now in use. | | --- |
| | Line Progress | Action Required on zero transmitter byte count (if Marked). | | 3-12 |
| | Receiver Control Byte Holding | Receiver Control Byte Storage | | --- |

### 3.1.2 Control Table

The control table contains the control bytes fetched from core memory by the DV11 each time a character is received or is to be transmitted. The control bytes are used by the DV11 to control processing of the transmitted or received character.

**3.1.2.1 Control Table Format** – The addresses in core memory for each line of the receiver and transmitter control tables are set in secondary registers by the PDP-11 program. The DV11 adds the character code to the base address to form the basic core memory address of the control byte for that character. For example, if the base address of the receiver control table for a given line is 4000 and the character 101 code is received (ASCII letter A), 4101 would be effective core memory address of the associated control byte.

With this scheme, 256 locations ($2_8$) are sufficient to provide control bytes for every possible 8-bit character code. In the usual protocol, however, certain codes are susceptible to more than one mode of interpretation, depending upon the sequence in which they are received and whether the data is transparent or non-transparent. Thus, 3-bit mode specification fields are provided in secondary registers for each line in the transmitter and receiver functions. Sequencing between modes may be effected by the control byte, which specifies the mode in which the DV11 is to operate.

The mode field occupies bits 8, 9, and 10 and is appended to the basic control table address to form the actual address of the control byte. Thus, in the example above, the control bytes for character code 101 would be in location 4101 (mode 0), location 4501 (mode 1), location 5101 (mode 2), etc. The control byte address formation sequence is graphically depicted in Figure 3-1. Control byte formats are shown in Figure 3-2.

**3.1.2.2 Receive Control Byte** – Whenever a character is input to the DV11 from the data link receiver, the associated control byte is obtained from core memory by a Non-Processor Request (NPR) to specify the next mode and to dictate character disposition. The following character dispositions are provided:

1. Generate (or do not generate) an interrupt.
2. Store (or discard) the character.
3. Accumulate (or do not accumulate) the character in the Block Check Character (BCC).
4. Expect the BCC (treat the next character as a BCC).

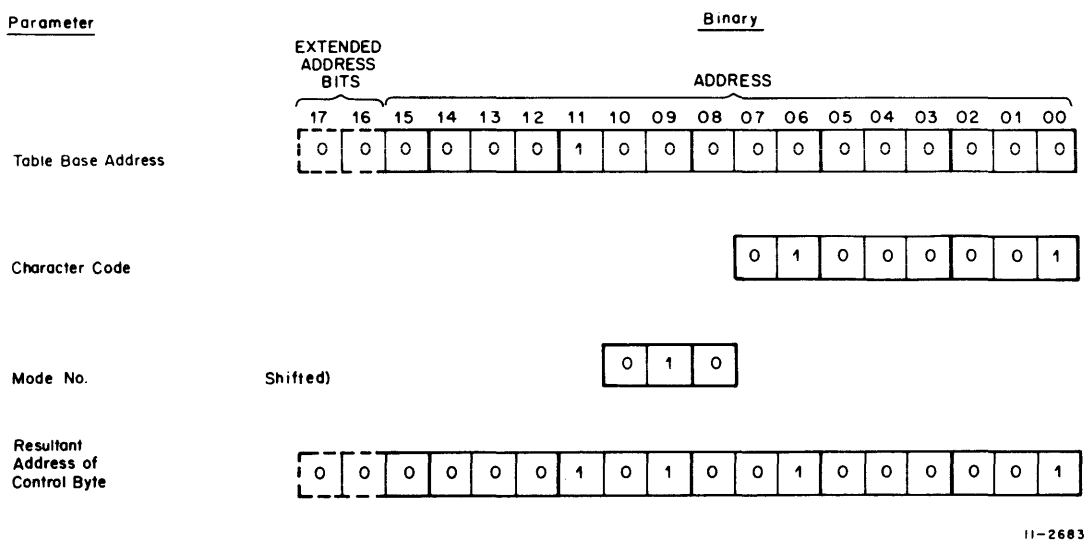



Figure 3-1 Control Byte Address

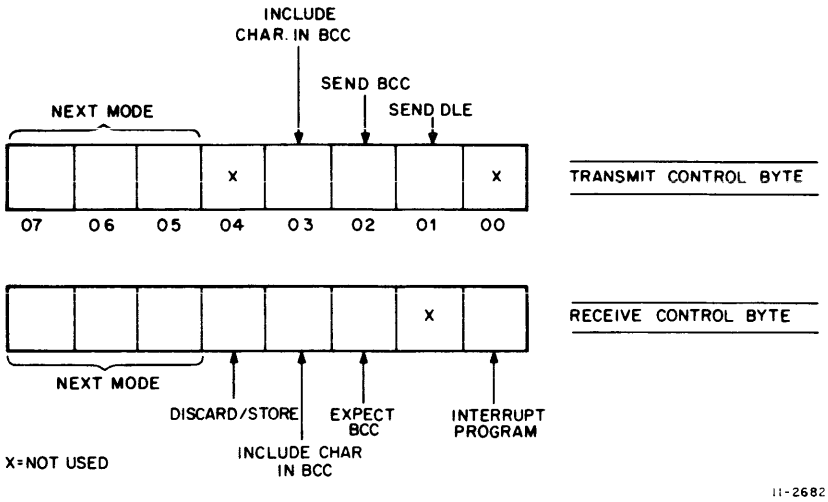



Figure 3-2 Control Byte Formats

The interrupt disposition provides for signalling the program in the event of error conditions, or data link control characters requiring special handling. The character that caused the interrupt is loaded into the RIC register. The program responds by sending a special control byte to the DV11, which would then override the previous dispositions set for received characters. The *discard* disposition provides for inhibiting storage of data link control and other unwanted characters. The *do-not-accumulate* disposition provides for the exclusion of non-data; BCC anticipation signals characters from the error-checking process. BCC anticipation signals the DV11 to initiate data block termination procedure.

**3.1.2.3 Transmit Control Byte** - Whenever a character is input to the DV11 from PDP-11 core memory, the associated control byte is obtained from core memory by a NPR to specify the next mode and any other processing instructions. The following instructions are provided:

1. Accumulate (or do not accumulate) the character in the BCC.

2. Send the BCC after the character.

3. Send the DLE before the character.

As in the case of the receive control byte, the do-not-accumulate disposition provides for the exclusion of non-data characters from the error-checking process. The BCC transmission command signals the DV11 to initiate data block termination procedure. The DLE transmission command causes the DV11 to retrieve the DLE character from secondary register storage and "stuffs" the DLE in front of the character to be transmitted.

**3.1.2.4 Control Byte Symmetry** - The receive and transmit control bytes are configured so that a single control table will provide for both transmit and receive functions for a given line if the following functional limitations are observed:

1. The protocol must progress from mode to mode in a symmetrical fashion for both transmit and receive;

2. the same characters must be included in the BCC for both transmit and receive.

For protocols that do not meet these requirements, separate control tables may be used.

### 3.1.3 Operations With Directly-Addressable Registers

The directly-addressable registers provide for modem setup and control data transfer enabling, interrupt enabling and reporting, extended-memory addressing and access to secondary registers (see Table 3-1).

**3.1.3.1 Modem Setup and Control** - Modem enabling, monitoring, and control are provided by the Control Status Register (CSR) and the Line Status Register (LSR) of the Modem Control Unit. Step-by-step procedures for accomplishing these functions are contained in Paragraphs 3.5 and 3.6.

**3.1.3.2 Accessing Secondary Registers** - The Secondary Register Selection Register (SRS) provides for PDP-11 program access to the secondary registers in the DV11 RAM. To address a secondary register, the PDP-11 program sets the 8-bit RAM address, consisting of the 4-bit line number, plus the 4-bit register selection code, in SRS 00–03 and SRS 08–11, respectively. Loading or reading the SRS is then accomplished by loading or reading the Secondary Register Access Register (SAR). The contents of the SRS must be saved by interrupt service routines.

**3.1.3.3 Data Transfer Enabling** - The System Control Register (SCR) provides for clearing the Data Handling Section (SCR 11) and starting the Microprocessor (SCR 00) to enable the Data Handling Section. Individual receivers are then enabled by setting the line number in bits 00–03 of the SRS, then setting Receiver Enable in Line Control Register (LCR bit 13), coincident with the Control Strobe (LCR 15). Individual transmitters are enabled by setting Transmitter Go (bit 02) in the Line State Secondary Register.

**3.1.3.4 Interrupt Enabling and Response** - Data Handling Section interrupts may occur as a result of *receive* function interrupt conditions or *transmit* function interrupt conditions. Receive function interrupts occur as a result of error conditions, encounter of data block boundaries, or upon fetching a control byte for a received control character that specifies an interrupt. Receive function interrupt information is stored in the RIC register.

Transmit function interrupts occur as a result of error conditions or data block boundaries being encountered. Transmit functions interrupt information is stored in a first-in, first-out buffer; the output of this buffer forms the NPR Status Register (NSR). The buffer (or "silo") is monitored ot detect overflow.

Receive function interrupts, transmit function interrupts, and NSR silo overflow interrupts, when enabled by SCR 06, 13, 12, set SCR 07, 15, 10, respectively.

The PDP-11 program should set SCR 08 in response to a receiver interrupt, enabling the DV11 to process the character in the RIC register and resume withdrawing characters from the RC Silo.

**3.1.3.5 Extended Memory Addressing** - If the DV11 is to access a core memory tables at extended memory locations, the basic 16-bit table address is set in the appropriate secondary register. The extended address bits are the set in SCR 04, 05. The DV11 appends the extended address bits to the 16-bit table address and stores the resultant 18-bit in the SRS (the RAM is 18 bits wide).

LCR bits 04, 05 display the extended memory address bits for the secondary register selected by the SRS, for reading by the PDP-11 program.

**3.1.4 Protocol Processing**

Processing and control of protocol functions is accomplished almost exclusively with secondary registers, as indicated in Table 3-1.

**3.1.4.1 BCC Polynomial Selections** - The code set in bits 03, 04 of the Line Protocol Parameters Secondary Register selects the type of block check polynomial to be applied to the transmitted and received data for error-checking purposes. Longitudinal redundancy checks (LRC), cyclic redundancy checks (CRC-16), and CRC/CCITT checks are provided for.

**3.1.4.2 Processing Block Terminations** - Mode changes and BCC anticipations or transmission may be effected at the end of a data block if the PDP-11 program sets a marked byte count into a byte count secondary register. The mode change and/or BCC command is then set by the PDP-11 program into the appropriate secondary register before or during the data block receive or transmit interval. When the byte count reaches zero, the "mark" is detected by the DV11, which responds to the mode change and/or BCC command.

Byte counts are set in 2's complement form in bits 00–14 of byte count secondary registers; the registers are incremented with each byte transferred to count them up to zero. Thus, a byte count may be marked by setting bit 15 to zero at byte count set time. When the marked byte count reaches zero (00–14=0), bit 15 is set to one, enabling the DV11 to detect the mark.

**3.1.4.3 Control Byte Inhibit** – For protocols such as DDCMP, which do not require arbitrary mode changes within a data block, provision has been made to inhibit the control byte fetch cycle. All characters are included in BCC, and all are stored. The PDP-11 program sets the inhibit bit in the Line Protocol Parameters secondary register (bit 05 for receive, bit 06 for transmit). The inhibit is effective only when the DV11 is in mode 0. If DDCMP is implemented with control tables, but the Control Byte Inhibit feature is desired, the control table must provide space for mode 0, despite the fact that the hardware does not actually reference that part of the table.

**3.1.4.4 Sync Character Selection** – Two sync characters (A and B) may be manually set for each four-line group (00–03, 04–07, 08–11, 12–15). Selection of the sync character for a line is then accomplished by setting the Sync A/B Selection bit (LCR 10) coincident with the Control Strobe (LCR 15). The bit is initialized to sync A (zero).

**3.1.4.5 Sync/Mark State Select** – The selected sync character is also used as the transmitted Fill character. In lieu of syncs, the data line can be set to idle the MARK state upon both byte counts reaching zero by setting Line Protocol Parameters bit 00 to 1. Idling of syncs takes place for a definite number of character times. Idling of the MARK state occurs for an indeterminate period (i.e., synchronization is lost).

**3.1.4.6 Stripping Received Syncs** – Setting Line Protocol Parameters bit 01 to 1 causes sync characters arriving after the achievement of synchronization, but before the first non-sync character, to be stripped from the incoming data stream (i.e., not stored in the RC Silo). Sync characters with which the receiver achieves sync are stripped in any case.

**3.1.4.7 Line Activity Snapshot** – The PDP-11 program can monitor conditions on a selected line by examining bits 00–07 of the Line State Register, which provide a snapshot of line activity. Of particular interest in Line State 03 (Transmitter Underrun). This is set to one by the DV11 whenever data is not available in time for the synchronous transmitter, and indicates that one or more idling syncs have been sent. In byte count-oriented protocols or in IBM's BISYNC transparency operation, idling of a sync causes a bad BCC and hence a NAK from the remote terminal. Thus, the Transmitter Underrun bit indicates whether the NAK is the result of line errors or idling syncs.

### 3.1.5 Data Transfer Operations

To establish a data transfer operation between core memory and a selected data line for either transmission or reception, the PDP-11 program must communicate the following basic information to the DV11:

a. The identification of the selected data line.

b. The quantity of data to be transferred, and

c. the address of the table of locations in memory (the "data table") for data read or write.

The PDP-11 program specifies the selected data line number in bits 00–03 of the SRS. The quantity of data to be transferred is specified by loading a byte count into the appropriate DV11 secondary register. Similarly, the program loads the base address of the core memory table into the DV11 secondary register provided.

Using the data table address to access the corresponding location in core memory, the DV11 starts the data transfer. As each byte is transferred, the DV11 increments both the byte count and the data table address (termed the "current address"). When the byte count reaches zero, the DV11 initiates data block termination procedure and halts data reception for the corresponding line. (Data transmission is handled somewhat differently, as will now be described).

**3.1.5.1 Provision for Alternate Data Transmission Tables** – By means of the data sequencing method just described, data can be transferred between core memory and the selected data line at the maximum DV11 throughput rate. However, if more than one data table is to be transmitted, the program would have only the transmission time of the last byte of the previous table in which to establish a current address and byte count for the next message, unless a double-register system was provided.

The DV11 provides such a double-register system in the form of two registers for storage of transmitter current addresses and two registers for storage of transmitter byte counts. The registers are called principal current address, alternate current address, principal byte count, and alternate byte count. Thus, while the DV11 is transferring data from the table defined by the principal current address and byte count, the PDP-11 program may establish and load the alternate current address and byte count. When the principle byte count reaches zero, the DV11 continues the data transfer operation, without interruption, by switching to the alternate registers and notifies the PDP-11 program, which may then load the primary registers. This seesaw activity continues until both byte counts are zero, at which time transmission stops.

**3.1.5.2 Table Size and Location** – Any memory location, including those with extended address, may be used and data tables may cross extended address boundaries. Messages to be transmitted or received may comprise data tables of up to 16,384 bytes.

## 3.2 DIRECTLY-ADDRESSABLE REGISTERS

The DV11 contains 10 registers which may be directly addressed by the PDP-11 program. Formats, designations, addresses and mnemonic codes for these registers are displayed in Figure 3-3. The System Control Register (SCR) and the Line Control Register (LCR) are used by the PDP-11 program principally to set up data transfers. The Control Status Register (CSR) and the Line Status Register (LSR) are used to set up the line modems. Other directly-addressable registers are provided to enable interrupt interpretation and handling, access to DV11 secondary registers, and for maintenance functions.

The register bit description tables contain a read/write column to indicate whether bits are read only, write only, or may be both read and written by the PDP-11 program. If a bit may be physically read by the program but the datum read is not valid, it is listed as "write" with the "only" omitted; the converse case is similarly treated.

### 3.2.1 System Control Register (SCR)

The System Control Register is a byte-addressable register for use by the PDP-11 program in order to:

1. Initialize the Data Handling Section of the DV11 Master Clear
2. Start the DV11 Microprocessor
3. Enable DV11 data interrupts and detect interrupt requests
4. Restart DV11 Data Handling Section after receiver interrupt and
5. Set the extended address bits to the DV11 for core memory addressing by the DV11.

The SCR also provides PDP-11 program control of Microprocessor ROM functions and provides simulated transmission interrupts for maintenance purposes.

Format of the SCR is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-2.

### 3.2.2 Line Control Register (LCR)

The Line Control Register is intended for use by the PDP-11 program in order to:

1. Enable reception on a selected line
2. Read the extended address bits used for core memory addressing by DV11 secondary registers, and
3. Select the sync character(s) for each line.

The LCR also implements the principal DV11 maintenance functions.

The following LCR bit descriptions apply only to those lines associated with a synchronous line card.

The enabling of reception is controlled by separate storage for each line. This is accomplished by using LCR 15 as a strobe pulse generator to load LCR 13 (Receiver Enable) into control storage for the line set in SRS 00–03 at the time that LCR is set to 1 by the PDP-11 program. The Sync Character Selection bit (LCR 10) and Maintenance bits LCR 09, 11, 12, and 14 are set in separate storages for each four-line group (00–03, 04–07, 08–11, and 12–15, as selected by SRS 02–03) by LCR 15 strobe. Consequently, LCR bits 09–14 are not valid for a line selected at a random point in time and so are designated as write bits. Since LCR 15 strobes 09–14, programs must update all of the bits 09–14 when it is desired to update any one of these bits. The LCR format for synchronous line cards is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-3.

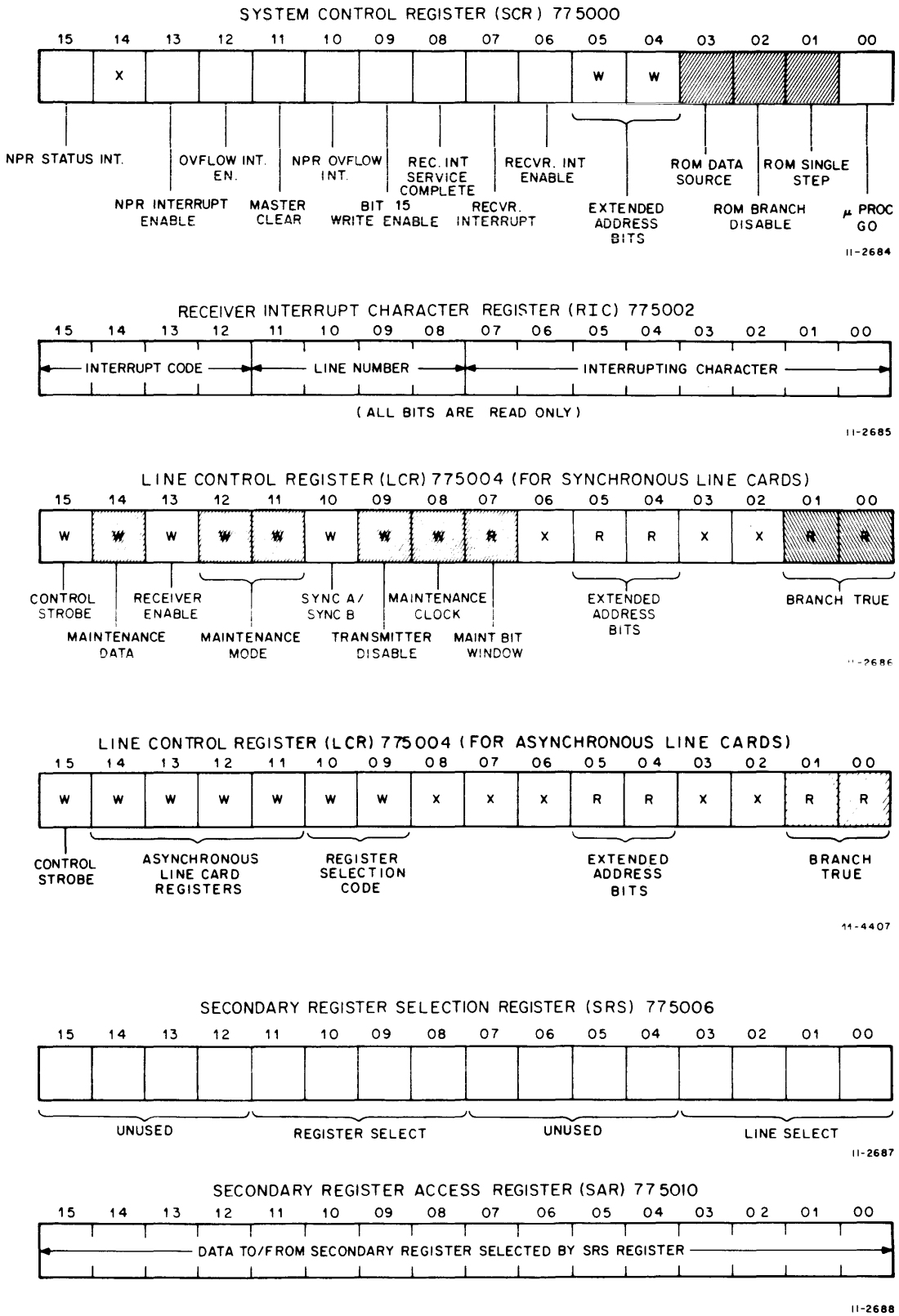



Figure 3-3 DV11 Primary Registers (Sheet 1 of 3)

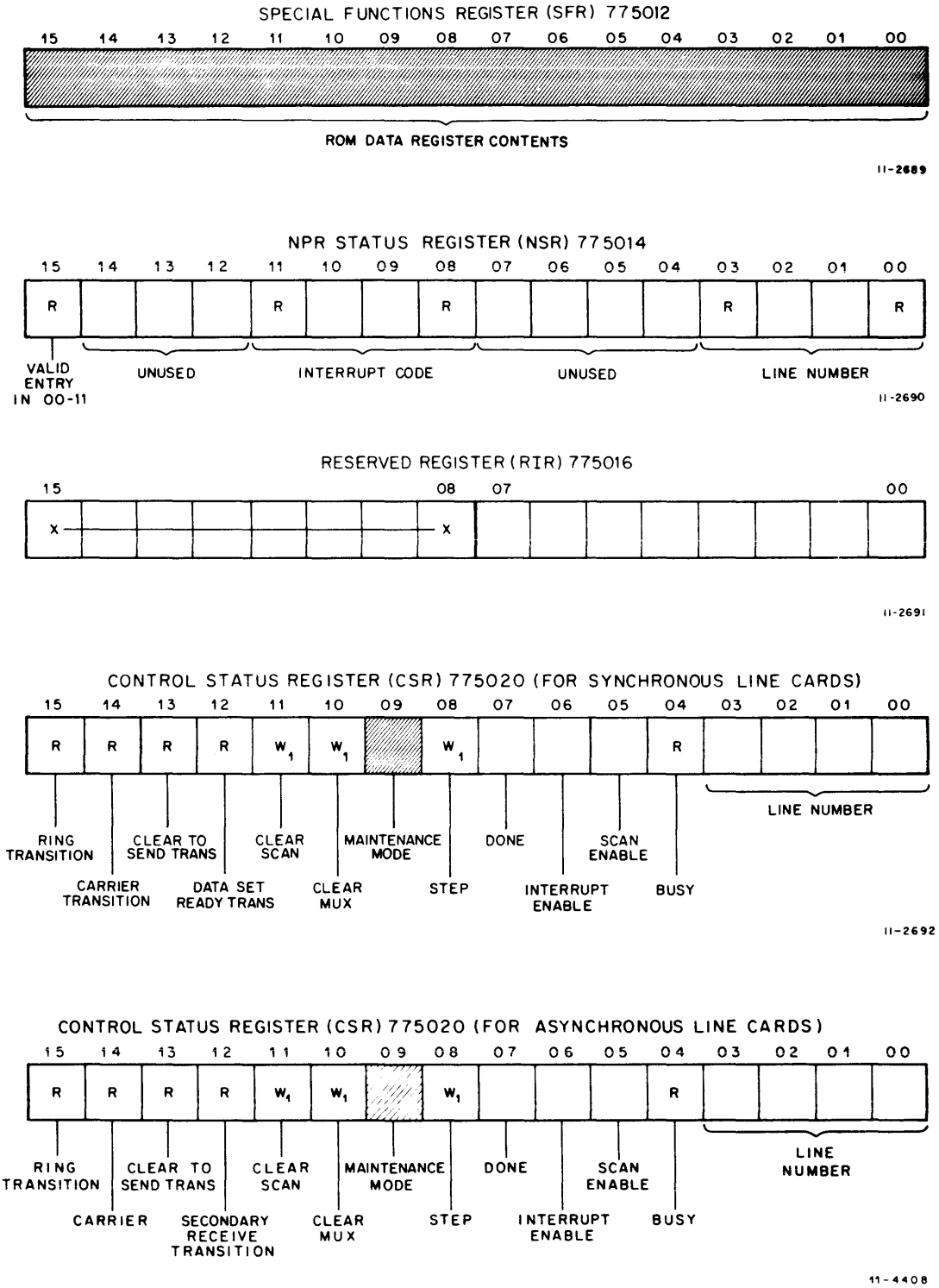



Figure 3-3 DV11 Primary Registers (Sheet 2 of 3)

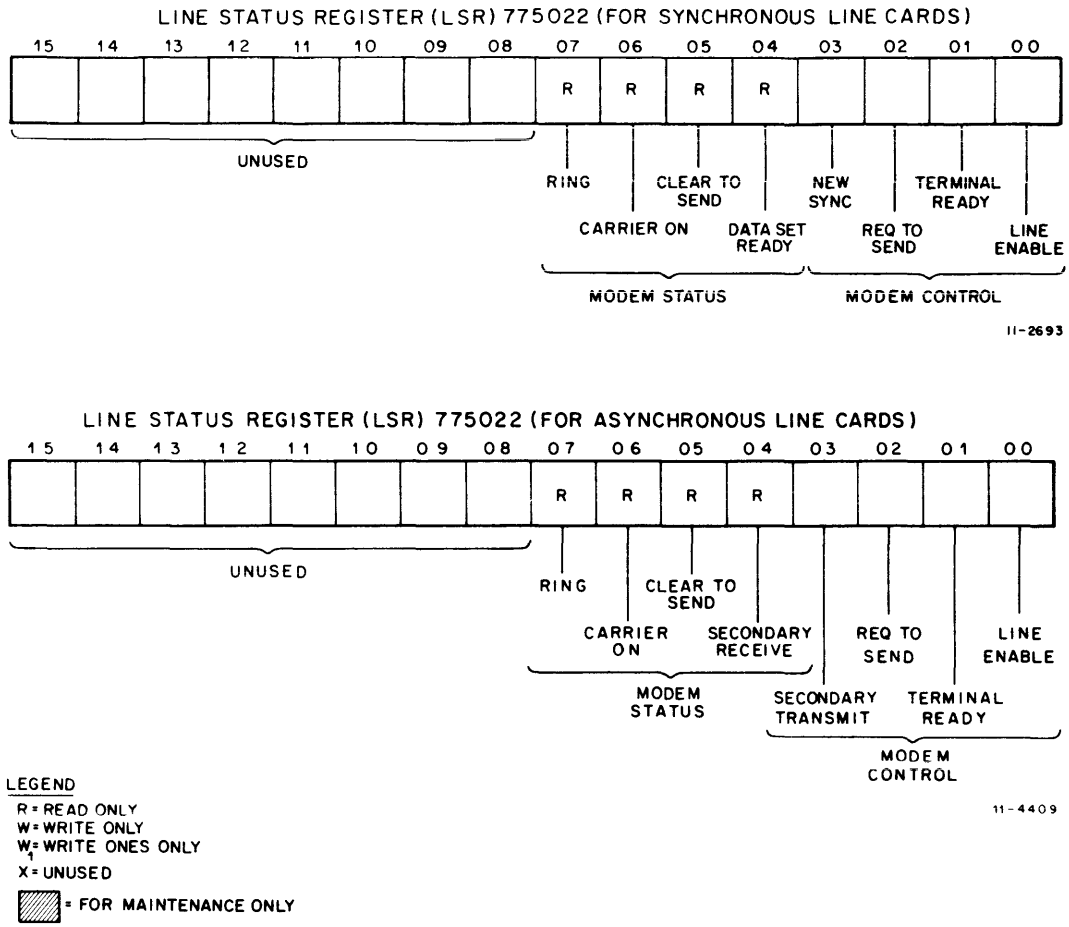



Figure 3-3 DV11 Primary Registers (Sheet 3 of 3)

Table 3-2
System Control Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00 | Microprocessor GO | When set to one, enables the Microprocessor to operate the DV11 Data Handling Section. Must be set to one to enable DV11 to perform any functions other than modem control. Cleared by Initialize. | Read or Write |
| 01–03 | (Maintenance) . | | |
| 04–05 | Extended Address | The contents of these bits as set by the PDP-11 program form bits 16 and 17, respectively, of any current address or control table base address loaded by the PDP-11 program into a secondary register for the line selected by SRS 00–03. These bits must be set before loading the Secondary register. These bits are read/write, but when read reflect only the values of SCR 04–05, and not the values of address bits 16 and 17 for the selected line. (Refer to the discussion of Line Control Register bits 04–05.) Thus, an interrupt service routine saving the contents of these bits will store bits 04–05 exactly as set by the PDP-11 program. Cleared by Initialize. | Write |
| 06 | Receiver Interrupt | When set to one by the PDP-11 program, enables the Microprocessor to interrupt the PDP-11 program by setting a one in SCR 07. Cleared by Initialize. | Read or Write |
| 07 | Receiver Interrupt (Vector A) | Set to one by the DV11 to request a PDP-11 program interrupt occurring during data reception. The reception conditions that cause the DV11 to request an interrupt are listed in Table 3-3. The PDP-11 program should respond to the interrupt by reading the Receiver Interrupt Character Register to identify the condition and may then load the Receiver Control Byte secondary register with a new control byte. The PDP-11 program should then set SCR 08. SCR 07 does not cause an interrupt unless SCR 06 has been set to one by the PDP-11 program. Cleared by Initialize. This bit is read only except when SCR 09 is set, in which case it is read/write. | Read or R/W |
| 08 | Receiver Interrupt Service Complete | Set to one by the PDP-11 program when it has completed an interrupt service routine and desires Microprocessor servicing of the character in the Receiver Interrupt Character register. Setting of this bit clears SCR 07. Cleared by Initialize. | Read or Write |

**Table 3-2 (Cont)**
**System Control Register Bit Assignments**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 09 | (Maintenance) | | |
| 10 | NPR Status Overflow (Vector B) | Set to one by the Microprocessor whenever the NPR Status Register/silo is full. Failure occurs whenever the PDP-11 program does not promptly read the NPR Status Register contents following a SCR 15 interrupt, and 64 NPR status entries have occurred. SCR 10 does not cause an interrupt unless SCR 12 has been set to one by the PDP-11 program. Cleared by Initialize. | Read or Write |
| 11 | Master Clear | When set to one, clears the following bits in the DV11:<br>SCR bits 0–3,6,7,9,10,11,12,13,15<br>RIC bits 0–15<br>LCR bits 7–14<br>NSR bit 15<br><br>The Received Character Silo is also cleared. This bit is self-clearing. | Read or Write |
| 12 | NPR Status Overflow Interrupt Enable | When set to one, enables the setting of SCR 10 to generate an interrupt request. Cleared by Initilize. | Read or Write |
| 13 | NPR Status Interrupt Enable | When set to one, enables the setting of SCR 15 to generate an interrupt request. Cleared by Initialize. | Read or Write |
| 14 | — | Unused. | |
| 15 | NPR Status Interrupt (Vector B) | Set to one whenever the Microprocessor loads data into the NPR Status Register to report an interrupt condition occurring during data transmission. Set to zero whenever the PDP-11 program reads the NPR Status Register. This bit is read only except when Bits 07 and 15 Write Enable (SCR 09) are set to one, in which case it is read/write. SCR 15 does not cause an interrupt unless SCR 13 has been set to one by the PDP-11 program. Cleared by Initialize. | Read or R/W |

Table 3-3
Line Control Register Bit Assignments
(For Synchronous Line Cards)

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00–01 | (Maintenance) | | – |
| 02–03 | – | Unused | – |
| 04–05 | Extended Address Read | For the secondary register selected by SRS 00–03 and 08–11, these bits display the contents of bits 16 and 17, respectively. This enables the program to read the extended address bits of the current address and control table base address secondary registers. | Read only |
| 06 | – | Unused | – |
| 07–09 | (Maintenance) | | – |
| 10 | Sync Select | For the line selected by SRS 00–03, this bit sets Sync A character or Sync B character, depending on whether this bit is set to zero or one, respectively, at LCR 15 set time. Cleared by Initialize.<br><br>Sync character encoding is discussed in Chapter 2. | Write |
| 11,12 | (Maintenance) | | – |
| 13 | Receiver Enable | When set to one at LCR 15 set time, causes the receiver for the line set in SRS 00–03 to search for the synchronization character(s) in the input bit stream. When the synchronization character(s) is found, the Microprocessor sets the Receiver Active bit in the Line State secondary register. LCR 13 must be set to one to enable reception on a line following Initialize. This bit is not used for resynchronization during reception.<br><br>To resynchronize during reception, the Receiver Resynchronize bit in the Line State secondary register is set to one.<br><br>To shut down reception in a line, the line number is set in SRS 00–03 and LCR 13 is set to zero at LCR 15 set time. The Receiver Resynchronization bit in the Line State secondary register is then set.<br><br>Cleared by Initialize. | Write |
| 14 | (Maintenance) | | – |

**Table 3-3 (Cont)**
**Line Control Register Bit Assignments**
**(For Synchronous Line Cards)**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 15 | Control Strobe | When set to one, strobes LCR 13 into control storage for the line set in SRS 00–03 and strobes LCR 09, 10, 11, 12, 14 into control storage for the 4-line group set in SRS 02–03, then clears itself. May be set at the same time as the LCR bits that it strobes into storage for the selected line or line group. | Write |

The following LCR bit descriptions apply only to those lines associated with an asynchronous line card.

For asynchronous line cards, each line has four 4-bit registers associated with it, each of which may be loaded by addressing the LCR with appropriate register selection bits set in LCR 09 and 10, in addition to the line selection bits set in SRS 00–03. The four registers associated with each line are called the "Primary," "Format," "Baud Rate," and "Maintenance" registers and are selected by LCR 10–09 codes of 00, 01, 10, and 11 respectively. While the bit assignments are described in detail in Table 3-4, it can be noted here that LCR 15 (Line Control Strobe) functions the same for asynchronous line cards as it does for synchronous line cards and that the cautions expressed above with regard to LCR bits 09–14 are similarly valid for the asynchronous case. The LCR format for asynchronous line cards is displayed in Figure 3-3. Bit assignments are described in detail in Table 3-4.

### 3.2.3 Receiver Interrupt Character Register (RIC)

The Receiver Interrupt Character Register is a read-only register which stores the character that caused the PDP-11 program interrupt, the line number on which the character was received, and the code specifying the reason for the interrupt. This register is cleared by Initialize.

The format of the RIC is shown in Figure 3-3. Specific bit assignments for the RIC are as follows:

*Bits 00–07:* This field contains the interrupting character, right-justified. Bit 00 is the least significant bit. On parity-equipped synchronous characters of less than eight bits, the parity bit will appear immediately to the left of the highest order bit in the character.

*Bits 08–11:* This field contains the line number on which the interrupting character was received. Bit eight is the least significant bit.

*Bits 12–15:* This field contains the code specifying the reason for the interrupt. Refer to Tables 3-5 and 3-6 for code meanings.

### 3.2.4 NPR Status Register (NSR)

The NPR Status Register is a 64-level "read-once" silo; that is, a read of this silo "empties" it of its oldest entry (destructive read), and any new data "falls" into the silo output if new data is waiting when a read is completed. The NSR is read-only register which identifies (1) interrupt-causing conditions that occur during character transmission and (2) the line number on which the interrupt occurred.

Table 3-4
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00, 01 | (Maintenance) | | – |
| 02, 03 | – | Unused | – |
| 04, 05 | Extended Address Read | For the secondary register selected by SRS 00–03 and 08–11, these bits display the contents of bits 16 and 17, respectively. This enables the program to read the extended address bits of the current address and control table base address secondary registers. | Read only |
| 06, 07, 08 | – | Unused | – |
| 09, 10 | Register Selection Code | For the line number selected by SRS 00–03, the code bits determine which Asynchronous Line Card register is written into at LCR 15 set time. There are four registers associated with each line and they are called "Primary," "Format," "Baud Rate," and "Maintenance" registers. Descriptions of the register bits are found in LCR 11–14. Cleared by Initialize. | Write |
| 11–14 | Asynchronous Line Card Registers | This is the path provided for access to the line card registers. Loading of a register occurs at LCR 15 set time and is dependent on the line number selected by SRS 00–03, and the register selection code set in LCR 09–10. Each line has four 4-bit registers associated with it, designated as: "Primary," "Format," "Baud Rate," and "Maintenance." These registers are cleared by Initialize. Bit assignment description of the registers follows LCR 15 functional description. | Write |
| 15 | Control Strobe | When set to a one, strobes LCR 11, 12, 13, 14 into control storage for the register selection code set in LCR 09–10 and the line specified by SRS 00–03, then clears itself. May be set at the same time as the LCR bits that it strobes into storage for the selected register. | Write |

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| | | **Asynchronous Line Card Primary Register** | |
| 09, 10 | Primary Register Selection Code 00 | For the line number selected by SRS 00–03, the code of 00 specifies writing into the Primary register at LCR 15 set time. | Write |
| 11 | Half Duplex/ Full Duplex | This bit, when set, conditions the line to operate in half duplex mode. If this bit is cleared, the line is conditioned to operate in full duplex mode. When operating in half duplex mode, the selected receiver is blinded during transmission of a character. | Write |
| 12 | Even Parity | This bit, when set, generates characters with even parity on the line and expects received characters to have even parity. If this bit is cleared, characters of odd parity are generated on the line and received characters are expected to have odd parity. The state of this bit is immaterial if the Parity Enable bit (Format register bit 14) is not set. This bit must be conditioned prior to loading the Format Register. | Write |
| 13 | Receiver Enable | This bit must be set before the receiver logic can assemble characters from the serial input line. When this bit is set, Receiver Active (Line State Bit 00) is subsequently set. To shut down reception on a line, the program should first clear Receiver Enable and the set Receiver Resynchronize (Line State Bit 01). The program must wait one character interval after shutdown before restarting a line. | Write |
| 14 | Break | This bit, when set, forces a space on that line's output causing a break condition. The break condition may be timed by sending characters during the break interval, since these characters never reach the EIA line. | Write |
| 15 | Control Strobe | When set to a one, strobes the Primary Register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage. | Write |

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| | | **Asynchronous Line Card Format Register** | |
| 09, 10 | Format Register Selection Code 10 | For the line number selected by SRS 00–03, the code of 10 specifies writing into the Format register at LCR 15 set time. LCR 09 = 1, LCR 10 = 0. | Write |
| 11, 12 | Character Length | These bits are set to transmit and receive characters of the length (excluding parity) as shown below.<br><br>**12 11 Selected Character Length**<br>0 0 5 bits<br>0 1 6 bits<br>1 0 7 bits<br>1 1 8 bits | Write |
| 13 | Two Stop Bits | This bit, when set, conditions the line transmitting with 5, 6, 7, or 8 bit code to transmit characters having two stop bits. One stop bit is sent when this bit is cleared. | Write |
| 14 | Parity Enable | If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have parity checked. Parity sense is determined by the state of Primary Register bit 12. | Write |
| 15 | Control Strobe | When set to a one, strobes the Format register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage. | Write |
| | | **Asynchronous Line Card Baud Rate Register** | |
| 09, 10 | Baud Rate Register Selection Code 01 | For the line number selected by SRS 00–03, the code of 01 specifies writing into the Baud Rate register at LCR 15 set time. LCR 09 = 0, LCR 10 = 1. | Write |
| 11–14 | Speed Code | The state of these bits determine the operating speed for the transmitter and receiver of the selected line. | Write |

**Table 3-4 (Cont)**
**Line Control Register Bit Assignments**
**(For Asynchronous Line Cards)**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| | | **Asynchronous Line Card Baud Rate Register (Cont)** | |
| 11–14 (Cont) | | **14 13 12 11 Baud Rate**<br>0 0 0 0 50<br>0 0 0 1 75<br>0 0 1 0 110<br>0 0 1 1 134.5<br>0 1 0 0 150<br>0 1 0 1 300<br>0 1 1 0 600<br>0 1 1 1 1200<br>1 0 0 0 1800<br>1 0 0 1 2000<br>1 0 1 0 2400<br>1 0 1 1 3600<br>1 1 0 0 4800<br>1 1 0 1 7200<br>1 1 1 0 9600<br>1 1 1 1 38,400* | |
| 15 | Control Strobe | When set to a one, strobes the Baud Rate register bits 11, 12, 13, 14 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bits that it strobes into storage. | Write |

*Special Interface Leads For High Speed Operation

**DV11 Busy** – A response that originates from an asynchronous receiving line to indicate that the character servicing rate for that line is not being sustained. To insure received data integrity, external hardware must interpret and implement this response in such a fashion to provide a restraining feature on the remote transmitter. The "ON" condition of DV11 Busy is indicated by a negative voltage in the 3 to 15 volt range. The "OFF" condition of DV11 Busy is indicated by a positive voltage in the 3 to 15 volt range. DV11 Busy is in the off state following a Unibus Initialize, DV11 Master Clear, or Receiver Enable cleared (LCR Primary Register bit 13). The ON duration of this lead is dependent on the servicing rate of the DV11 Character Processor. Therefore, DV11 Busy may be of any minimal period. DV11 Busy is asserted a maximum of 10/16th of a bit time following reception of the first stop bit. For an operating speed of 38,400 baud, the DV11 Busy feature *must* be used.

**Data Set Busy** – The capability of an asynchronous transmitting line to have continual transmission remotely started and stopped. This is the complementary feature of DV11 Busy. Data Set Busy must be implemented with external supporting hardware and must be used with an operating speed of 38,400 baud. Line card modification is required for implementing Data Set Busy at a baud rate other than 38,400 baud. The "ON" condition of Data Set Busy is interpreted by a negative voltage in the 3 to 15 volt range. The "OFF" condition of Data Set Busy is interpreted by a positive voltage in the 3 to 15 volt range. Data Set Busy, when on, is defined as a remote stop request. To inhibit continual character transmission, Data Set Busy must be received prior to 15/16th of the last stop bit interval. Data Set Busy is invalid when the line is being operated in either internal maintenance mode or at an operating speed less than 38,400 baud, assuming no line card modification was performed.

Table 3-4 (Cont)
Line Control Register Bit Assignments
(For Asynchronous Line Cards)

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| | | Asynchronous Line Card Maintenance Register | |
| 09, 10 | Maintenance Register Selection Code 11 | For the line number specified by SRS 00–03, the code of 11 specifies writing into the Maintenance register at LCR 15 set time. | Write |
| 11 | Maintenance Internal Mode | This bit, when set, loops the transmitter's serial output lead to the receiver's serial input lead. While operating in maintenance mode, the EIA transmit data leads, EIA received data leads, and the remote Data Set busy features are disabled. Normal operating mode is assumed when this bit is cleared. | Write |
| 12–14 | – | Unused | – |
| 15 | Control Strobe | When set to a one, strobes the Maintenance register bit 11 into storage for the line specified in SRS 00–03, then clears itself. May be set at the same time as the bit that it strobes into storage. | Write |

Interrupt-causing conditions and associated line numbers are stacked in the 64 entry first-in, first-out silo buffer and dropped into the NSR output as each prior entry is read by the PDP-11 program. Each time a new entry is dropped into NSR output, NSR 15 is set to indicate the presence of valid data and SCR 15 is set to request an interrupt. Each time an NSR entry is read by the PDP-11 program, NSR 15 and SCR 15 are reset to zero. NSR 15 is also set to zero by Initialize. (The other NSR bits are not reset to zero by initialize.)

The NSR format is shown in Figure 3-3. Transmission interrupt codes are described in Table 3-7.

### 3.2.5 Reserved Register

Reserved for future system requirements.

### 3.2.6 Special Functions Register (SFR)

The Special Functions Register is used for maintenance only.

### 3.2.7 Secondary Register Selection Register (SRS)

The Secondary Register Selection Register provides for PDP-11 program access to the secondary registers in the DV11 RAM. To address a secondary register, the PDP-11 program sets the 8-bit RAM address, consisting of the 4-bit line number, plus the 4-bit register selection code, in SRS 00–03 and SRS 08–11, respectively. Loading or reading the SRS is then accomplished by loading or reading the SAR. Interrupt service routines must save the contents of the SRS.

The 4-bit line selection code in SRS 00–03 provides for selection of the 16 data lines. The 4-bit register selection code in SRS 08–11 provides for selection of the 16 secondary registers supplied for each data line.

**Table 3-5**
**Receive Function Interrupt Conditions**
**(For Synchronous Line Cards)**

| Code Set in RIC 12–15 | | | | Meaning |
|---|---|---|---|---|
| 15 | 14 | 13 | 12 | |
| 0 | 0 | 0 | 0 | Special Character Received:<br>Bit 00 of the control byte for the character in RIC 00–07 is set to one (generate interrupt), indicating that the received character is a special character. |
| 0 | 0 | 0 | 1 | Parity Error:<br>The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the parity sense switches on the M7839 module (Figure 2-6). |
| 0 | 0 | 1 | 0 | Overrun:<br>The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo. |
| 0 | 0 | 1 | 1 | Parity Error and Overrun:<br>As described above for error codes 0001 and 0010. |
| 0 | 1 | 0 | 0 | Byte Count Warning:<br>The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero. |
| 0 | 1 | 0 | 1 | Block Check Complete:<br>The block check character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07. |
| 0 | 1 | 1 | 0 | Undefined |
| 0 | 1 | 1 | 1 | Undefined |
| 1 | 0 | 0 | 0 | Byte Count Zero:<br>The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available. |
| 1 | 0 | 0 | 1 | Undefined |
| 1 | 0 | 1 | 0 | Undefined |
| 1 | 0 | 1 | 1 | Undefined |
| 1 | 1 | 0 | 0 | Processing Error 00:<br>A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07. |
| 1 | 1 | 0 | 1 | Processing Error 01:<br>A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07. |

Table 3-5 (Cont)
Receive Function Interrupt Conditions
(For Synchronous Line Cards)

| Code Set in RIC 12–15 | | | | Meaning |
|---|---|---|---|---|
| 15 | 14 | 13 | 12 | |
| 1 | 1 | 1 | 0 | Processing Error 10:<br>The DV11 received a signal on the memory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations. |
| 1 | 1 | 1 | 1 | Processing Error 11:<br>A memory parity error occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07. |

Table 3-6
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

| Code Set in RIC 12–15 | | | | Meaning |
|---|---|---|---|---|
| 15 | 14 | 13 | 12 | |
| 0 | 0 | 0 | 0 | Special Character Received:<br>Bit 00 of the control byte for the character in RIC 00–07 is set to a one (generate interrupt), indicating that the received character is a special character. |
| 0 | 0 | 0 | 1 | Parity Error:<br>The character in RIC 00–07 has a parity sense opposite to that selected for this line (the line specified in RIC 08–11) by the programmable Format registers of the Asynchronous Line Card. |
| 0 | 0 | 1 | 0 | Overrun Error:<br>The received character(s) preceding the character set in RIC 00–07 have been lost because of overflow of the Received Character Silo. |
| 0 | 0 | 1 | 1 | Framing Error:<br>The character set in RIC 00–07 lacked a stop bit present at the proper time. This code is usually interpreted as indicating the reception of a break. |
| 0 | 1 | 0 | 0 | Byte Count Warning:<br>The character set in RIC 00–07 has been stored in core memory. No more characters may be stored for this line as the byte count is now zero. |
| 0 | 1 | 0 | 1 | Block Check Complete:<br>The block character(s) for the data block received on this line have arrived and have been included in the Accumulated BCC. The Accumulated BCC is now in the Receive Accumulated Block Check Character secondary register; the OR of the high and low bytes of the accumulated BCC is set in RIC 00–07. |

Table 3-6 (Cont)
Receive Function Interrupt Conditions
(For Asynchronous Line Cards)

| Code Set in RIC 12–15 | | | | Meaning |
|---|---|---|---|---|
| 15 | 14 | 13 | 12 | |
| 0 | 1 | 1 | 0 | Undefined |
| 0 | 1 | 1 | 1 | Undefined |
| 1 | 0 | 0 | 0 | Byte Count Zero:<br>The receive byte count for this line was zero prior to receipt of the character set in RIC 00–07. Thus, the character was not stored as no assigned storage was available. |
| 1 | 0 | 0 | 1 | Undefined |
| 1 | 0 | 1 | 0 | Undefined |
| 1 | 0 | 1 | 1 | Undefined |
| 1 | 1 | 0 | 0 | Processing Error 00:<br>A non-existent memory time-out occurred when the DV11 attempted to store the character set in RIC 00–07. |
| 1 | 1 | 0 | 1 | Processing Error 01:<br>A non-existent memory time-out occurred when the DV11 attempted to fetch the control byte corresponding to the character set in RIC 00–07. |
| 1 | 1 | 1 | 0 | Processing Error 10:<br>A DV11 received signal on the memory parity error line from the PDP-11 when the DV11 attempted to store the character set in RIC 00–07. This condition indicates a defect in the memory parity logic, as the PDP-11 generates parity error signals only on core memory read operations. |
| 1 | 1 | 1 | 1 | Processing Error 11:<br>A memory parity occurred when the DV11 attempted to obtain the control byte corresponding to the character in RIC 00–07. |

**NOTE** A priority encoding scheme is used by an asynchronous line to present a multiple error code condition. Any error flag combination that contains an overrun error is presented as an Overrun Error (code 0010) in the RICR register. A framing error and parity error combination is presented as a Framing Error (code 0011) in the RICR register. A multiple error condition that displays a Parity Error (code 0001) does not exist. This priority scheme is used only by the Asynchronous Line Card. Existing error code bits that are generated on a synchronous line are not affected by this scheme.

Table 3-7
**Transmit Function Interrupt Conditions**

| Code Set in NSR 08–11 | | | | Meaning |
|---|---|---|---|---|
| 11 | 10 | 09 | 08 | |
| 0 | 0 | 0 | 0 | Transmitter principal current address specified a non-existent memory location (NXM). |
| 0 | 0 | 0 | 1 | Transmitter principal byte count is equal to zero. |
| 0 | 0 | 1 | 0 | Transmitter alternate current address specified a non-existent memory location (NXM). |
| 0 | 0 | 1 | 1 | Transmitter alternate byte count is equal to zero. |
| 1 | 0 | 0 | 0 | An attempted control byte fetch by the DV11 produced a non-existent memory condition or a memory parity error. (The specific error is set in the Line State secondary register.) |

SRS 00–03 are also used to select line control storage for loading from the Line Control Register.

CAUTION

**Do not change the contents of SRS without checking that LCR 15 is cleared, indicating that any outstanding LCR load to the line cards has been completed.**

### 3.2.8 Secondary Register Access Register (SAR)

The Secondary Register Access Register provides the PDP-11 program with direct access to the secondary register selected by the SRS register. Loading or reading the SAR is equivalent to loading or reading the secondary register addressed by SRS 00–03 and 08–11.

### 3.2.9 Modem Control Registers

PDP-11 program control of the line modems is accomplished through the Control Status Register (CSR) and the Line Status Register (LSR) in the Modem Control Unit (MCU) of the DV11. The CSR controls data line or modem selection and operating mode (interrupt or non-interrupt) of the MCU, and enables the detection of changes in modem status by the PDP-11 program. The LSR routes control bits provided by the PDP-11 program to the modems and transfers modem status bits to the Unibus for the modem(s) selected via the CSR. To enable any one of the 16 lines, the PDP-11 program sets the selected line number in the CSR, then sets the Line Enable bit in the LSR.

Formats for the CSR and LSR are displayed in Figure 3-3. Bit assignments are described in detail in Tables 3-8 and 3-9, respectively. Some bit assignments have dual definitions to reflect the type of modem that is being controlled (i.e., synchronous vs asynchronous). Tables 3-8 and 3-9 define each bit assignment as it applies to both modem types.

The interrupt mode is set for all enabled lines by setting CSR 05 and 06 each to one. CSR 05 (Scan Enable) causes the MCU to scan the enabled modems cyclically to detect a change or transition in one of the modem status bits. When a transition is detected, scanning is stopped, the condition causing the transition is set in the CSR 12–15 field, the line number for the signalling modem is available in CSR 00–03, CSR 07 (Done bit) is set to one, and the PDP-11 program is interrupted.

The non-interrupt mode is feasible if only *one* modem is to be monitored for activity at one time. The line number for the modem is set in the CSR and modem status bits LSR 04–07 are continuously sampled by the PDP-11 program. When one of these status bits becomes set to one, the PDP-11 program may respond by setting a 03.

Table 3-8
Control Status Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00–03 | LINE (Line Number) | Binary address of one of 16 modems:<br><br>Bit 3 2 1 0 Line No.<br>0 0 0 0 0<br>0 0 0 1 1<br>. . . . .<br>. . . . .<br>. . . . .<br>1 1 1 1 15<br><br>Cleared to 0000 by Initialize or Clr Scan (bit 11 of CSR). Sixteen microseconds ±10% settling time is required.<br><br>This portion of the CSR is a presettable binary counter; thus, it may be loaded directly by the PDP-11 program to address a selected data line, or advanced by SCAN EN (CSR bit 5) or STEP (CSR bit 8) to address sequential data lines. | Read or Write |
| 04 | BUSY | Set to 1 whenever modems are being cyclically scanned or a Clr Scan (CSR bit 11) is being executed. | Read only |
| 05 | SCAN EN (Scan Enable) | Causes cyclical scanning of status lines from all enabled modems when set to 1 if Done (CSR bit 7) is set to 0. Scanning stops and Done is set to 1 when a status transition is detected. A 1.2 microsecond period is required for scanning to come to a halt when the PDP-11 program changes this bit from 1 to 0; therefore, Busy (CSR bit 4) must be tested for its zero state before changing the line number (CSR bits 0–3) to ensure that all detected transitions are serviced. Cleared by Initialize and Clr Scan (CSR bit 11). | Read or Write |
| 06 | INTER EN (Interrupt Enable) | Enables Done signal from CSR bit 7 to cause a PDP-11 interrupt on priority four when set to 1. Cleared by Initialize and Clr Scan (CSR bit 11). | Read or Write |

Table 3-8 (Cont)
**Control Status Register Bit Assignments**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 07 | DONE | Set to one whenever a transition occurs on a status line (RING, CO, CS, DSR) from an enabled modem during the modem scanning process, as initiated by Scan En (CSR bit 5). When Done is set to one, the scan stops and the status transition(s) are set in CSR bits 12–15. The line number of the modem with the new status is in CSR bits 0–3, and the current states of that modem's status lines are reflected in LSR bits 4–7. Cleared by Initialize and Clr Scan (CSR bit 11). | Read or Write |
| 08 | STEP | When set to 1, causes the line number in CSR bits 0–3 to be incremented by 1. If a status transition is detected for the new line, Done (CSR bit 7) is set to 1. Done does not inhibit Step. This bit is used principally for maintenance and requires 1.2 microseconds ±10% to execute. This bit is write ones only. | |
| 09 | (Maintenance) | | |
| 10 | CLEAR MUX | Clears bits 4–7 of the LSR (RS, Term Rdy, NS, Line En) for all lines when set to 1. This bit is write ones only. | Write ones |
| 11 | CLR SCAN | Clears bits 0–3, 5, 6, 7, 9, and 12–15 of the CSR when set to 1, and clears MCU "Scan Memory" in 18.8 microseconds ± 10%.<br><br>(The MCU detects modem status transitions by storing the conditions of the several modems' status lines in Scan Memory, then continuously comparing the updated status conditions with the previous status conditions during the modem scanning process. Thus, if Scan En (CSR bit 5) is set to 1 following a Clear Scan and the interrupt mode is set, an interrupt will occur for all modems which have ON status lines (DSR, CS, CO, RING), as these will appear as OFF to ON transitions to the MCU.) | Write ones |

Table 3-8 (Cont)
Control Status Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 12 | DSR<br>(Data Set Ready transition)<br>(Synchronous modem definition) | Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the DSR status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan. | Read only |
| 12 | SEC RX<br>(Secondary Receive transition)<br>(Asynchronous modem definition) | Set to a 1 whenever an ON to OFF or OFF to ON transition occurs on the SEC RX status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan. | Read only |
| 13 | CS<br>(Clear to Send transition) | Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the CS status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan. | Read only |
| 14 | CO<br>(Carrier On transition) | Set to 1 whenever an ON to OFF or OFF to ON transition occurs on the CO status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan. | Read only |
| 15 | RING<br>(Ring Signal) | Set to 1 whenever an OFF to ON transition occurs on the RING status line from the selected modem. Not valid if the PDP-11 program has changed the line number in CSR bits 0–3 and the scan has not been cycled for one or more lines by Scan En (CSR bit 5) or Step (CSR bit 8). Cleared by Initialize or Clr Scan. | Read only |

Table 3-9
Line Status Register Bit Assignments

| Bit | Designation | Function | Read/Write |
|---|---|---|---|
| 00 | LINE EN<br>(Line Modem Enable) | When set to 1 for the line selected by bits 0–3 of the CSR, causes status conditions DSR, CS, CO, and RING from the corresponding modem to appear in bits 4–7 of the LSR and causes status transitions from the same modem to set the Done bit (CSR bit 7) to 1 during the scanning process. To set the Line En bit for a line, the line number is set in the CSR, then the Line En bit is set in the LSR. Cleared by Initialize and Clear Mux (CSR bit 10). | Read or Write |
| 01 | TERM RDY<br>(Terminal Ready) | When set to 1 for the line selected by bits 0–3 of the CSR, maintains line seizure ("off-hook" condition) for the corresponding modem. To set the TERM RDY bit for a line, the line number must be in the CSR, then the TERM RDY bit is set in the LSR. Cleared by Initialize and Clear Mux. | Read or Write |
| 02 | RS<br>(Request to Send) | When set to 1 for the line selected by bits 0–3 of the CSR, conditions the corresponding modem to transmit data. To set the RS bit for a line, the line number must be in the CSR, then the RS bit is set in the LSR. Cleared by Initialize and Clear Mux. | Read or Write |
| 03 | NS<br>(New Sync)<br>(Synchronous modem definition) | When set to 1 for the line selected by bits 0–3 of the CSR, signals the corresponding modem to resynchronize on the carrier. To set the NS bit for a line, the line number must be in the CSR, then the NS bit is set in the LSR. Cleared by Initialize and Clear Mux. | Read or Write |
| 03 | SEC TX<br>(Secondary Transmit)<br>(Asynchronous modem definition) | When set to a 1 for the line selected by bits 0–3 of the CSR, signals the corresponding modem to transmit on the reverse channels. To set the SEC TX bit for a line, the line number must be in the CSR, then the SEC TX bit is set in the LSR. Cleared by Initialize and Clear Mux. | Read or Write |
| 04 | DSR<br>(Data Set Ready)<br>Synchronous modem definition) | Set to 1 whenever the DSR line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates the modem has seized the line. | Read only |
| 04 | SEC RX<br>(Secondary Receive)<br>(Asynchronous modem definition) | Set to 1 whenever the SEC RX line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates a remote modem is signaling the local modem on the reverse channels. | Read only |
| 05 | CS<br>(Clear to Send) | Set to 1 whenever the CS line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for the modem has been set. Indicates the modem is ready to transmit data. Occurs in response to an RS (LSR bit 2). | Read only |

Table 3-9 (Cont)
Line Status Register Bit Assignments

| Bit | Designation | Function | Read/Write |
|---|---|---|---|
| 06 | CO<br>(Carrier On)<br>(detected) | Set to 1 whenever the CO line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem is present and that the received signal is present for demodulation. | Read only |
| 07 | RING | Set to 1 whenever the RING line from the modem selected by bits 0–3 of the CSR is ON, provided that the Line En bit for that modem has been set. Indicates a remote modem is signalling the local modem. | Read only |

## 3.3 INDIRECTLY ADDRESSABLE (SECONDARY) REGISTERS

The secondary registers make up the RAM of the DV11 and may be accessed by the PDP-11 program via the SRS and the SAR, as described in Section 3.2. The PDP-11 program must clear (or properly set up) all secondary registers before setting SCR 00 (Microprocessor GO). Because the RAM is volatile, secondary register contents must be re-established in the event of power failure.

Sixteen secondary registers, summarized in Table 3-1, are provided for each of the 16 data lines, making a total of 256 secondary registers. Secondary register formats are shown in Figure 3-4.

**NOTE**
**The Secondary Registers are NOT cleared by Initialize.**

### 3.3.1 Transmitter Principal Current Address (0000)

The Transmitter Principal Current Address secondary register contains the 18-bit core memory address of the next character to be transmitted on the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State secondary register bit 07 set to zero).

When the transmitter Principal Byte Count (secondary register 0001) for the same line reaches zero, an interrupt code is set in the NPR Status register. Transmission continues, using the Transmitter Alternate Current Address for this line (secondary register 0001), provided that the Transmitter GO bit in the Line State secondary register for this line is still set to one.

### 3.3.2 Transmitter Principal Byte Count (0001)

The Transmitter Principal Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission, based on reaching a zero byte count during transmission. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line Progress secondary register for this line will control the transmission mode when the principal byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the principal message table is being used (Line State 07 set to zero). When this register reaches zero, transmission continues (using the Transmitter Alternate Byte Count for this line) if the Transmitter GO bit in the Line State secondary register is still set to one.

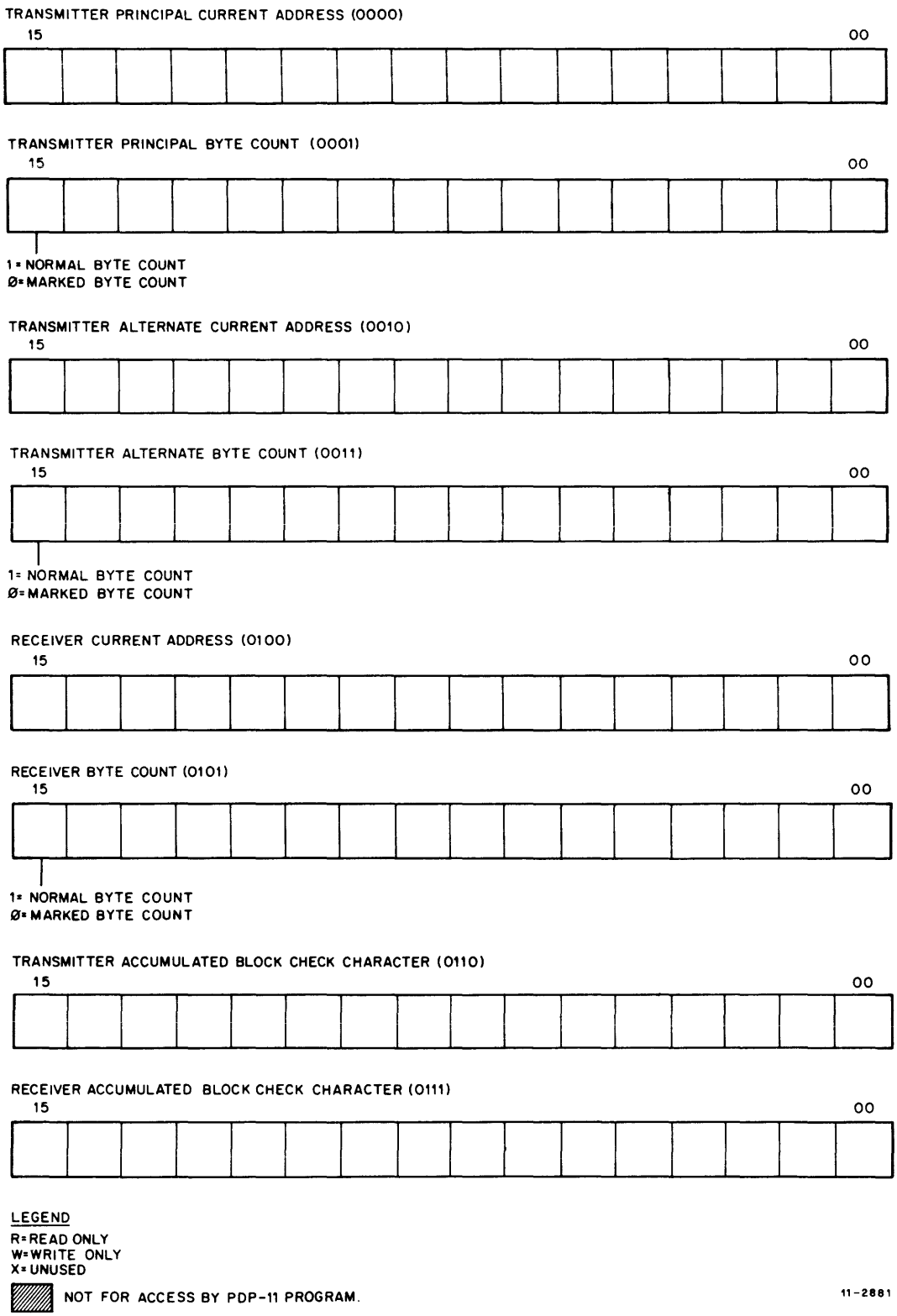



Figure 3-4 DV11 Secondary Registers (Sheet 1 of 2)

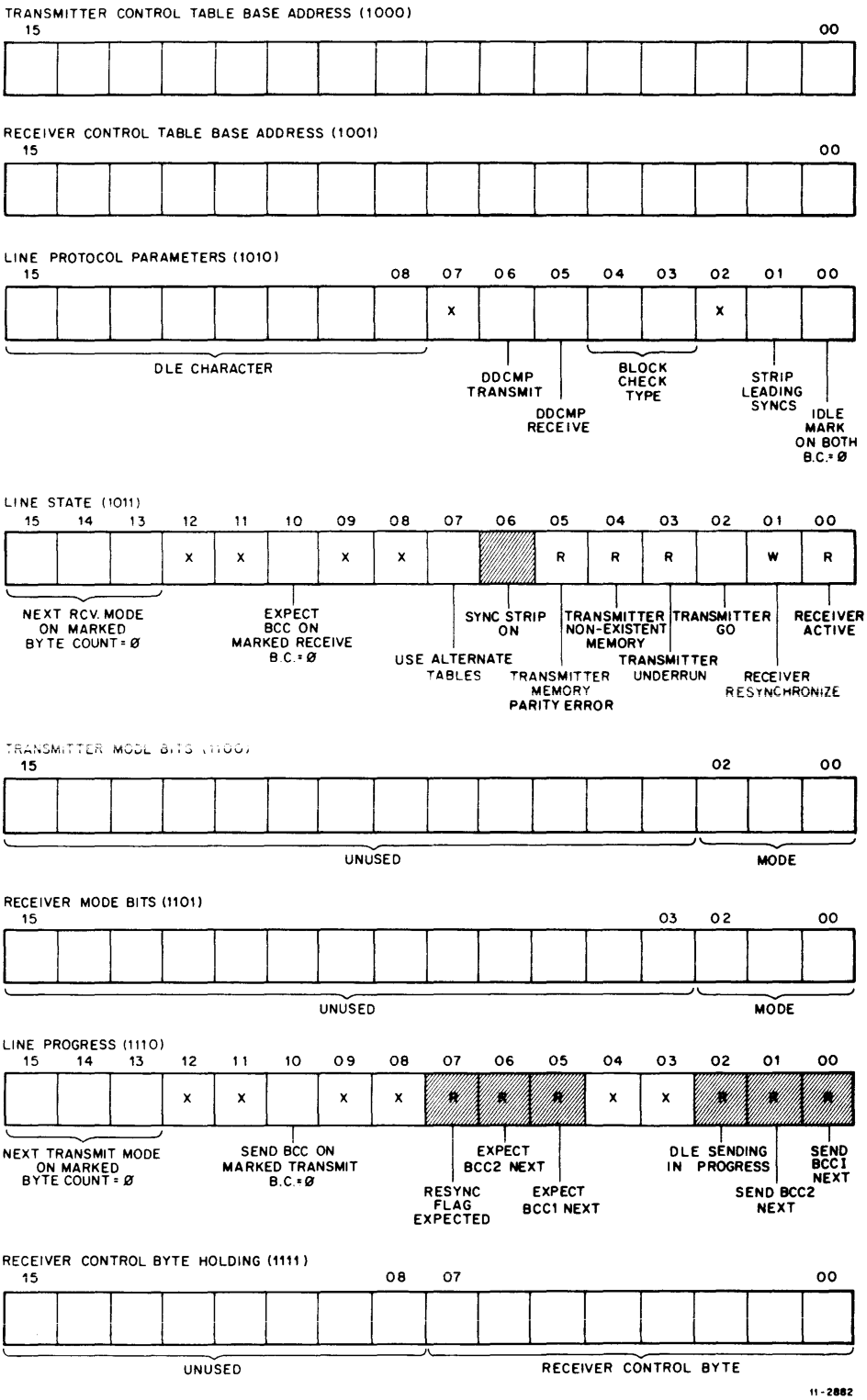



Figure 3-4 DV11 Secondary Registers (Sheet 2 of 2)

### 3.3.3 Transmitter Alternate Current Address (0010)

The Transmitter Alternate Current Address register has exactly the same function as the Transmitter Principal Current Address register described in Paragraph 3.3.1. This register is incremented by one with each character transmitted by the DV11 on the associated line if the alternate message table is being used (Line State secondary register bit 07 set to one).

When the Transmitter Alternate Byte Count (secondary register 0011) for the associated line reaches zero, an interrupt code is set in the NPR Status register. Transmission continues using the Transmitter Principal Current Address for this line (secondary register 0001), provided that the Transmitter GO bit in the Line State secondary register for the same line is still set to one.

### 3.3.4 Transmitter Alternate Byte Count (0011)

The Transmitter Alternate Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be transmitted on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC transmission, based on reaching a zero byte count during transmission. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line Progress secondary register for this line will control the transmission mode when the alternate byte count reaches zero; also, the BCC will be transmitted if Line Progress bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Transmitter Mode Bits secondary register continue to control the line transmission mode. A byte count with bit 15 set to zero (at the time that the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count.

This register is incremented by one with each character transmitted on the associated line by the DV11 if the alternate message table is being used (Line State secondary register bit 07 set to one). When this register reaches zero, transmission continues using the Transmitter Principal Byte Count for this line if the Transmitter GO bit in the Line State secondary register is still set to one.

### 3.3.5 Receiver Current Address (0100)

The Receiver Current Address register contains the 18-bit core memory address for storage of the next character to be received on the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. This register is incremented by one with each character received on the associated line by the DV11.

### 3.3.6 Receiver Byte Count (0101)

The Receiver Byte Count secondary register contains a 15-bit word that is the 2's complement of the number of bytes (characters) remaining to be received on the associated line. The 16th bit (bit 15) is used by the PDP-11 program to enable change of mode and/or BCC anticipation, based on reaching a zero byte count during reception. When bit 15 is set to zero by the PDP-11 program, bits 13–15 of the Line State secondary register for this line will control the reception mode when the byte count reaches zero; also, the BCC will be expected if Line State bit 10 is set to one. When bit 15 is set to one by the PDP-11 program, bits 00–02 of the Receiver Mode Bits secondary register continue to control the line reception mode. A byte count with bit 15 set to zero (at the time the byte count is loaded by the PDP-11 program) is referred to as a "marked" byte count. When this register reaches zero, an interrupt code is set in the RIC register and the DV11 stops transferring received characters to core memory.

### 3.3.7 Transmitter Accumulated Block Check Character (0110)

The Transmitter Accumulated Block Check secondary register contains the continuously-computed BCC (specified by the Line Protocol Parameters secondary register) to enable destination stations to check integrity of transmission on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the Transmitter Control Bytes for each character. The contents of this register are transmitted as two sequential bytes, low-order eight bits first (except when LRC-8 is the selected block check type, in which case a single byte is transmitted). The DV11 automatically clears this register to zero after transmitting its contents.

**NOTE**

**The DV11 computes CRC-16 and CRC-CCITT on a byte-at-a-time basis (parallel), thus the character length must be eight bits. LRC-8 may be selected for characters of 5, 6, 7, or 8 bits.**

### 3.3.8 Receiver Accumulated Block Check Character (0111)

The Receiver Accumulated Block Check secondary register contains the continuously-computed BCC (specified by the Line Protocol Parameters secondary register) for checking integrity of data received on the associated line. Characters to be included in the block check calculation are specified by bit 03 of the Receiver Control Byte for that character. The PDP-11 program should clear this register if the accumulated block check at the end of the message is non-zero.

### 3.3.9 Transmitter Control Table Base Address (1000)

The Transmitter Control Table Base Address secondary register contains the 18-bit address of the transmitter control table for the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. The contents of this register are used by the Microprocessor in the computation of the control byte addresses for transmitted characters.

### 3.3.10 Receiver Control Table Base Address (1001)

The Receiver Control Table Base Address secondary register contains the 18-bit address of the receiver control table for the associated line. The extended address bits are initially loaded from SCR 04–05 to provide the 18-bit address capability. The contents of this register are used by the Microprocessor in the computation of the control byte addresses for the received characters.

### 3.3.11 Line Protocol Parameters (1010)

The Line Protocol Parameters secondary register contains the transmitter Data Link Escape (DLE) character when required by the associated line protocol, plus control bits to implement protocol requirements and handling of sync characters. The PDP-11 program writes the data in this register for reference by the microprogram. Bit assignments are described in detail in Table 3-10.

### 3.3.12 Line State (1011)

The Line State secondary register is used by the PDP-11 program and the Microprocessor to control and monitor line activities in executing the selected protocol. This register is also used by the PDP-11 program to store mode change and BCC anticipation bits for reference by the Microprocessor when a marked Receiver Byte Count reaches zero, as discussed in Section 3.1. Bit assignments are described in detail in Table 3-11.

### 3.3.13 Transmitter Mode Bits (1100)

The Transmitter Mode Bits secondary register contain the 3-bit mode selection field (in bits 00–02) which determines the transmitter control table to be used for controlling transmission on the associated line.

### 3.3.14 Receiver Mode Bits (1101)

The Receiver Mode Bits secondary register contains the 3-bit mode selection field (in bits 00–02) which determines the receiver control table to be used for controlling reception on the associated line.

### 3.3.15 Line Progress (1110)

The Line Progress secondary register contains bits set and referenced by the Microprocessor to control and monitor activities on the associated line in executing the selected protocol (these bits are not intended for access by the PDP-11 program). This register also stores mode change and BCC transmission control bits, as set by the PDP-11 program, for use by the Microprocessor when a marked Transmitter Byte Count reaches zero, as discussed in Section 3.1. Line Progress register bit assignments are described in detail in Table 3-12.

### 3.3.16 Receiver Control Byte Holding (1111)

The Receiver Control Byte Holding secondary register provides storage for the Receiver Control Byte in bits 00–07. The PDP-11 program may set a control byte into this register while responding to a DV11 receiver special character interrupt. When the PDP-11 program signals the DV11 that its interrupt response is complete (SCR 08=1), the Microprocessor uses the control byte in this register to control the disposition of the interrupting character in the RIC register.

The Microprocessor may also use this register to write control bytes that specify character discard only, if an error condition or data block boundary condition caused the interrupt; the existing mode specified in the control byte is not altered. The PDP-11 program should not write this register except during initialization or interrupt response cycles. Receiver Control Byte format is shown in Figure 3-4.

If the PDP-11 programmer so desires, the generation of receiver interrupts may be limited to only those cases where the PDP-11 program wishes *notification* that a particular character has arrived, rather than have the PDP-11 program change the character processing directions specified in the control byte. In these circumstances, the PDP-11 program may direct that character processing resume (set SCR 08=1) without changing the control byte stored in the Receiver Control Byte Handling register. This is possible because the control byte is stored with its bit 00 (generate interrupt) cleared.

Table 3-10
Line Protocol Parameters Secondary Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00 | Idle Mark | When set to one, causes the associated data line to go to the MARK state at the conclusion of transmission of the character currently being loaded into the transmitter if both principal and alternate byte counts are zero. When cleared, sync characters will be idled on a synchronous data line or a MARK STATE will be asserted on an asynchronous line. | Read or Write |
| 01 | Strip Leading Syncs | When set to one, causes sync characters arriving on the associated data line after the achievement of synchronization, but before the first non-sync character, to be stripped from the incoming data stream (i.e., not stored in the RC Silo). The sync character(s) with which the receiver achieves sync are stripped in any case. | Read or Write |
| 02 | | Unused | |
| 03–04 | Block Check Type | Set by the PDP-11 program to specify the type of block check calculation to be done for transmissions and receptions on this line:<br>**03 04 BCType**<br>0 0 LRC-8 (XOR)<br>1 0 CRC-16 ($X^{16} + X^{15} + X^2 + 1$)<br>0 1 Unused-16<br>1 1 CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) | Read or Write |
| 05 | DDCMP Receive | When set to one, inhibits the Microprocessor from fetching control bytes during character reception on the associated line if reception mode is 0. Useful for increasing throughput and reducing core storage requirements when using DDCMP protocol. | Read or Write |
| 06 | DDCMP Transmit | When set to one, inhibits the Microprocessor from fetching control bytes during character transmission on the associated line if transmission mode is 0. Useful for increasing throughput and reducing core storage requirements when using DDCMP protocol. | Read or Write |
| 07 | | Unused | |
| 08–15 | DLE Character | Contains the Data Link Escape (DLE) character for the associated line. When a character is to be transmitted and the control byte for that character (as fetched by the DV11) has bit 01 set to one, the DLE character is fetched from this register by the Microprocessor and transmitted just prior to the character being processed. | Read or Write |

Table 3-11
**Line State Secondary Register Bit Assignments**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00 | Receiver Active | Set to one by the Microprocessor when the enabled receiver for the associated line has detected the synchronization character(s) for that line. (Receiver enabling, done via the Line Control Register, is discussed in Paragraph 3.2.2.) | Read |
| 01 | Receiver Resynchronize | Set to one by the PDP-11 program to effect resynchronization during reception or to turn off reception on the associated line, as described in Section 3.5. The Microprocessor searches for the synchronization character(s) for the associated line if the receiver for the line has been enabled (receiver enabling is discussed in Paragraph 3.2.2). When the synchronization character(s) is found, the Microprocessor sets the Receiver Active bit (Line State 00) to one. If any characters for the associated line are stored in the RC Silo when this bit is set, they are discarded (see Line Progress 07 description). | Write |
| 02 | Transmitter Go | Set to one by the PDP-11 program to command the DV11 to transmit data on the associated line. Set to zero by the Microprocessor whenever<br><br>1. transmitter principal and alternate byte counts are both equal to zero, or<br><br>2. transmitter NXM (Line State 04) sets to one, or<br><br>3. transmitter MPE (Line State 05) sets to one.<br><br>This bit may be set to zero by the PDP-11 program to abort transmission. | Read or Write |
| 03 | Transmitter Underrun | Set to one by the Microprocessor when a character has been loaded into the transmitter for the associated line and the transmitter has returned a Data Not Available signal. Should be set to zero by the PDP-11 program after it has been read. Indicates that one or more idling sync characters have been sent by the transmitter.<br><br>**CAUTION**<br>**In byte count oriented protocols or transparency operation in IBM's BISYNC, idling of a sync causes a bad BCC and hence a NAK from the remote terminal. Thus, the Transmitter Underrun bit indicates whether the NAK is the result of line errors or idling syncs.** | Read or Write zero |

Table 3-11 (Cont)
Line State Secondary Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 04 | Transmitter Non-Existent Memory (NXM) | Set to one by the Microprocessor whenever a non-existent memory condition is encountered during transmission (NPR Status Register interrupt codes 0000, 0010, 1000). The PDP-11 program should read the NPR Status Register, then clear this bit. This bit clears Transmitter Go (Line State 02) when set to one. | Read or Write zero |
| 05 | Transmitter Memory Parity Error | Set to one by the Microprocessor whenever a memory parity error is encountered during transmission (NPR Status Register interrupt code 1000). The PDP-11 program should read the NPR Status Register, then clear this bit. This bit clears Transmitter Go (Line State 02) when set to one. | Read or Write zero |
| 06 | Sync Strip On | Set to one by the Microprocessor in response to Strip Leading Syncs command bit (Line Protocol Parameters 01) from PDP-11 program to the associated line. Causes the Microprocessor to strip from the incoming data stream all sync characters arriving after the achievement of synchronization, but before the first non-sync character. Set to zero by the Microprocessor on arrival of the first non-sync character. | Read only |
| 07 | Use Alternate Tables | When set to zero by the PDP-11 program or the Microprocessor, causes the Microprocessor to extract data for transmission on the associated line from the principal tables. When set to one by the PDP-11 program or the Microprocessor, causes the Microprocessor to extract the transmit data from the alternate tables. Set to zero by the Microprocessor when the alternate byte count is equal to zero. Set to one by the Microprocessor when the principal byte count is equal to zero. | Read or Write |
| 08–09 | | Unused | |
| 10 | Expect BCC | When a marked receiver byte count reaches zero, this bit is examined by the Microprocessor. If this bit has been set to one by the PDP-11 program, the Microprocessor interprets the next received character (in the case of LRC-8 block check types) or the next two received characters (in the case of CRC-16 and CRC-CCITT block check types) as block check character(s), and passes them through the BCC calculation logic. The Microprocessor then places the OR of the high and low bytes of the accumulated BCC into the RIC register with the line number and interrupt code 0101. A control byte with bit 04 set to one (character discard) is written into the Control Byte secondary register to inhibit storage of the block check character(s), and SCR 07 is set to one to interrupt the program. | Read or Write |

Table 3-11 (Cont)
**Line State Secondary Register Bit Assignments**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 11–12 | | Unused | |
| 13–15 | Next Receive Mode on Marked Byte Count = 0 | When a marked receiver byte count reaches zero, the Microprocessor transfers these bits to bits 00–02 of the Receiver Mode Bits secondary register to set the mode for the next character(s) to be received. | Read or Write |

Table 3-12
**Line Progress Secondary Register Bit Assignments**

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 00 | Send BCC1 Next | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever:<br><br>1. A marked transmitter byte count has reached zero and bit 10 of this register is set to one.<br><br>2. A transmit control byte with bit 03 set to one has been fetched by the Microprocessor (useful when an ITB, ETB, or ETX has been encountered in BISYNC protocol).<br><br>Cleared by the Microprocessor if LRC or the first BCC has been loaded for transmission by the Microprocessor. | Read |
| 01 | Send BCC2 Next | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor when LRC or the first BCC has been loaded for transmission, but reset to zero again if LRC-8 is selected as the Block Check Type for the associated line in Line Protocol 03–04.<br><br>Set to zero by the Microprocessor when the second BCC byte (BCC2) has been loaded for transmission by the Microprocessor. | Read |
| 02 | DLE Sending In Progress | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor when it loads a Data Link Escape character for transmission on the associated line in response to a control byte command bit (01). Cleared by the Microprocessor when the DLE has been sent. | Read |
| 03–04 | | Unused | |

Table 3-12 (Cont)
Line Progress Secondary Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 05 | Expect BCC1 | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever (1) Line State bit 11 (Expect BCC) has been set to one by the PDP-11 program and a marked byte count has reached zero, or (2) a receive control byte has been fetched with bit 03 (Expect BCC) set to one. The next received character is then interpreted as the first block check character (BCC1) and a BCC calculation is performed. If LRC-8 is the selected block check type, the Microprocessor<br><br>1. places the OR of the high and low bytes of the accumulated BCC into the RIC register with the line number and interrupt code 0101.<br><br>2. writes a control byte with bit 04 (character discard) set to one, into the Control Byte secondary register to inhibit storage of the BCC, and<br><br>3. sets SCR 07 to one to interrupt the PDP-11 program.<br><br>If either CRC-16 or CRC-CCITT is the selected block check type (both BCC1 and BCC2 required), the Microprocessor sets Line Progress 06 (Expect BCC2) and does not perform steps 1, 2, and 3 until after BCC2 is received. | Read |
| 06 | Expect BCC2 Next | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever Line Progress 05 (Expect BCC1) is set from one to zero during a character reception cycle and either CRC-16 or CRC-CCITT is the selected block check type. The next received character is then interpreted as the second BCC (BCC2), a BCC calculation is performed, and the Microprocessor proceeds as described in steps 1, 2, and 3 for Line Progress bit 05. | Read |

Table 3-12 (Cont)
Line Progress Secondary Register Bit Assignments

| Bit(s) | Designation | Function | Read/Write |
|---|---|---|---|
| 07 | Resynchronization Flag Expected | (Not intended for access by the PDP-11 program.) Set to one by the Microprocessor whenever a resynchronization cycle starts for the associated line receiver as commanded by Line State 01. Cleared by the Microprocessor when all characters stored in the RC Silo for the associated line have been removed. This bit inhibits transfer of RC Silo characters designated for the associated line to the Unibus until the Resynchronization Flag character reaches the bottom (output) of the RC Silo. | Read |
| 08–09 | | Unused | |
| 10 | Send BCC | When a marked transmitter byte count reaches zero, this bit is examined by the Microprocessor. If this bit has been set to one by the PDP-11 program, the Microprocessor sets Line Progress 00 (Send BCC1 Next) to one for the associated line. The Microprocessor then transmits the first block character (BCC1) after the character which caused this byte count to go to zero. If either CRC-16 or CRC-CCITT is the selected protocol, the Microprocessor transmits the second block check character (BCC2) after transmission of BCC1. | Read or Write |
| 11–12 | | Unused | |
| 13–15 | Next Transmit Mode on Marked Byte Count = 0 | When a marked transmitter byte count reaches zero, the Microprocessor transfers these bits to bit 00–02 of the Transmitter Mode Bits secondary register to set the mode for the next character(s) to be transmitted. | Read or Write |

## 3.4 CONTROL BYTE FORMAT

Control byte bit assignments (Table 3-13), are based on the structure of the DV11 interpretation logic, and are arranged so that the same control bytes can be used for both transmission and reception, provided that:

1. The protocol progresses from mode to mode in a symmetrical fashion for both transmit and receive, and
2. The same characters are included in the BCC for both transmit or receive.

If the protocol being executed does not have the above characteristics, separate control tables for transmit and receive may be established by setting different values in Receive Control Table Base Address and Transmit Control Table Base Address secondary registers. Control byte formats for transmission and reception are shown in Figure 3-2.

Table 3-13
**Control Byte Bit Assignments**

| Bit(s) | Function | |
|---|---|---|
| | **Transmitter Control Byte** | **Receiver Control Byte** |
| 00 | Unused (to effect symmetry) | Interrupt PDP-11 Program:<br>When set to one, causes the DV11 to request a PDP-11 program interrupt. The DV11 sets the received character being processed in the Receiver Interrupt Character Register and awaits a reset of SCR 08 by the PDP-11 program. |
| 01 | Send Data Link Escape Next:<br>When set to one, causes the DV11 to fetch the Data Link Escape (DLE) character from secondary register 1010 for the selected line and transmit it before transmitting the character being processed. | Unused (to effect symmetry) |
| 02 | Send BCC:<br>When set to one, causes DV11 to transmit the block check character(s) for the selected line following transmission of the character being processed. | Expect BCC:<br>When set to one, causes DV11 to set up for receiving and processing the next received character as the block check character. |
| 03 | Include Character in BCC:<br>When set to one, causes the character being processed to be included in the block check character being accumulated for the selected line. When set to zero, inhibits inclusion. | Include Character in BCC:<br>When set to one, causes the character being processed to be included in the block check character being accumulated for the selected line. When set to zero, inhibits inclusion. |
| 04 | Unused (to effect symmetry) | Discard/Store Character:<br>When set to zero, causes the character being processed to be stored at the receiver current address in core memory for the selected line. When set to one, inhibits character storage. |
| 05–07 | Next Mode:<br>Specifies the mode for the next character to be transmitted on the selected line. Bit 05 is the least significant bit. | Next Mode:<br>Specifies the mode for the next character to be received on the selected line. Bit 05 is the least significant bit. |

## 3.5 DV11 INITIALIZATION

DV11 initialization consists of setting up the DV11 line modems and the DV11 Data Transfer Section.

### 3.5.1 Line Modem Set-Up

Initialization for the line modems consists of setting the line number for the modem to be enabled in CSR 00–03. CSR 06 (Interrupt Enable) may also be set to one at this time to select the interrupt mode. The Line Enable bit (LSR 00) is then set to one to complete the initialization process for the selected line. The process is repeated for each line that is to be enabled.

CSR and LSR are cleared at bus initialization time. Setting CSR 10 and 11 (Clear Mux and Clear Scan) each to one is equivalent to bus initialization, except that the Terminal Ready bits (LSR 01) for each line are also cleared by Clear Mux. If a Clear Scan is issued, the PDP-11 program must wait for the MCU Busy Indicator (CSR 04) to return to zero before sending additional command bits.

### 3.5.2 DV11 Data Transfer Setup

The primary registers should be cleared by a Master Clear (SCR 11), then the secondary registers for all lines must be cleared. Then set Microprocessor GO (SCR 00). The Microprocessor will now loop in an idle mode. The first word to SCR may also contain the extended address bits (SCR 04–05) and interrupt enables (SCR 06, 12, 13), as required.

Following is an illustrative procedure to setup a line for data reception:

1. Set the receiver control table core memory address and the byte count in the appropriate secondary registers.

2. Set the required protocol control bits in the Line Protocol Parameters secondary register.

3. Initialize receiver mode to non-zero in Receiver Mode Bits secondary register (1101) if required by the receiver protocol implementation logic.

4. When the data link is established on the selected line (Paragraph 3.5.1), set LRC 13 and 15 to one to cause the line to sync up and start receiving characters. Set LRC 10 to one at the same time if sync character(s) B is to be selected.

   LCR 10 and 13 are implemented for synchronous reception on a line. When operating on an asynchronous line, character format and baud rate must be set up at this time.

Following is an illustrative procedure to setup a line for transmission:

1. Set the transmitter control table core memory addresses and byte counts in the appropriate principal and alternate secondary registers, setting bit 15 of the byte counts to zero if marked byte counts are required by the protocol.

2. Set the required protocol control bits and the DLE character in the Line Protocol Parameters secondary register.

3. Initialize transmitter mode to non-zero in Transmitter Mode Bits secondary register (1100) if required by the protocol; set other bits in this register as required by the protocol.

4. Set bit 07 of Line State secondary register to one if transmission is to start from the alternate tables.

5. If the data link is established on the selected line, set bit 02 of Line State secondary register to one to start the transmitter for the line.

   If the line is asynchronous, the character format and baud rate in the Line Control register must be setup prior to setting Line State bit 02.

## 3.6 DATA TRANSFER IMPLEMENTATION

With the DV11 initialized as discussed in Section 3.5, calls to or from remote modems may be originated or answered and DV11 data transfers started by the PDP-11 program. The data transfer process or protocol is controlled by the contents of the control bytes and by the service routines for the DV11 interrupts. This section contains descriptions of call origination and answering procedures; resynchronization during reception; termination of transmission and reception; and suggested programming methods for implementing BISYNC and DDCMP protocols.

### 3.6.1 Originating and Answering Calls

The Control Status Register (CSR) and the Line Status Register (LSR) are provided to enable the PDP-11 program to originate and answer calls to/from remote modems. Initially, the local modem is enabled and the operating mode (interrupt or non-interrupt) is set, as described in Paragraph 3.5.1. An interchange then takes place between the PDP-11 program and the MCU to originate a call, as follows:

1. PDP-11 program sends Data Terminal Ready (LSR 01) to cause enabled modem to hold the line once the call is established.

2. PDP-11 program dials remote number via DN11 Automatic Dialing Unit, or an operator manually initiates a call to the remote modem. When the call has been established, the DN11 will hold the line via the Call Request line and Data Terminal Ready. In the manual dialing case, the operator switches to "Data Mode" and Data Terminal Ready holds the call.

3. PDP-11 program waits on Data Set Ready (DSR) transition from the enabled modem (CSR 12). If the MCU is operating in the non-interrupt mode with only one line enabled (as reflected by the contents of CSR 00–03) LSR 04 may be readily used to monitor the DSR line.

4. When DSR is detected, the PDP-11 program sends a Request to Send (LSR 02) to set the data mode for transmission.

5. PDP-11 program waits on Carrier On (CO) and Clear to Send (CS) transitions (CSR 14 and 13) from the enabled modem.

6. When CO and CS are detected, the PDP-11 program starts the DV11 Data Handling Section and initiates data transfer.

Answering a call consists of the PDP-11 program detecting the Ring transition from the enabled modem (CSR 15), then

1. PDP-11 program sends Data Terminal Ready (LSR 01) to cause enabled modem to answer the call.

2. PDP-11 program waits on Data Set Ready (DSR) transition (CSR 12) and the Carrier On (CO) transition (CSR 14) from the enabled modem.

3. When CO is detected, the PDP-11 program starts the DV11 Data Handling Section and initiates data transfers.

### 3.6.2 Resynchronization During Reception

If line synchronization initially fails or is lost, the PDP-11 program can command resynchronization during reception by setting bit 01 of Line State secondary register to one. The DV11 then

1. defines a "Resync Flag Expected interval" (Line Progress secondary register bit 07 set to one), during which any receiver characters for this line already buffered in the DV11 are discarded

2. clears the Resync Command bit (Line State 01) and Receiver Active (Line State 00), and

3. searches for the synchronization character.

When the synchronization character is found, the DV11 sets the Receiver Active bit to one to enable receipt and storage of subsequent characters on the resynchronized line. The program should not request resynchronization again until at least one character has been received since the previous resynchronization request.

### 3.6.3 Termination of Transmission and Reception

The DV11 terminates transmission on a line whenever both principal and alternate byte counts have reached zero, or a non-existent memory or memory parity error condition is encountered. The DV11 sets Transmitter GO (Line State secondary register bit 02) to zero to terminate transmission. The PDP-11 program may set Transmitter GO to zero to abort transmission.

The PDP-11 program shuts down reception on a line by clearing Receiver Enable (LCR 13) and setting Line State secondary register bit 01 (Receiver Resynchronize) to one. The DV11 then

1. clears the Resync Command bit (Line State 01) and the Receiver Active bit (Line State 00), and

2. discards any receiver characters already accumulated for the line.

### 3.6.4 BISYNC Implementation

BISYNC implementation software is considered in three functional groups: control tables, interrupt service routines, and the protocol module.

The control tables contain the control bytes, which control sequencing between modes and accumulation of the BCC. During transmission, the control bytes also control DLE stuffing and BCC transmission. Additionally, during reception, the control bytes enable discard of unwanted characters and reception of this BCC.

The interrupt service routines respond to zero byte count and error interrupts, and, during reception, respond to special character interrupts.

The protocol module initializes the DV11, establishes direction of transfer, sets up and manages the data buffers, and handles error and special character flags set by interrupt service routines. Handling of error flags may take the form of try-again routines, or operator notification. Handling of special characters may require such operations as a switch from receive to transmit, or termination and disconnect (i.e., EOT received).

**3.6.4.1 Transmission Control** - Figure 3-5 shows state flowcharts for the BISYNC transmission control process. There are five states or modes: three for transparent data transmission, and two for non-transparent data transmission.

For *transparent* data, the DV11 mode is initialized to Mode 0, causing the DV11 to stuff a DLE in front of any ACK, RVI, or WACK control characters sent by the PDP-11. The DV11 also stuffs a DLE in front of the first STX sent by the PDP-11 and switches to Mode 1, the transparent data transmission mode. The DV11 stays in Mode 1 until a marked byte count reaches zero (see Section 3.3), and is then switched to Mode 2, the end-of-transparent block mode.

In Mode 2, transmission of the ITB sequence (ITB DLE STX) causes a return to Mode 1 for transmission of the remainder of the data block. Transmission of an ETB or ETX character causes a return to Mode 0 to enable transmission of the next data block.

Table 3-14 shows the transmission sequence and the control byte directives for a block of transparent data that is separated into two intermediate blocks. The DV11 principal and alternate registers would initially be loaded with the base addresses and byte counts for data buffers one and two, respectively. On each zero byte count interrupt, the next buffer address would be loaded into the appropriate registers.

For *non-transparent* data, the DV11 is initialized to Mode 3 for transmission of any header data (see Figure D-3) or the ENQ control character. ITB, ETB, ETX characters are included in the BCC and followed by the BCC in Mode 3. The DV11 is switched to Mode 4, the text transmission mode, on occurrence of the STX or ITB delimiters. Occurrence of a zero byte count causes a return to Mode 3 to send the next data block.

Table 3-15 shows the transmission sequence and the control byte directives for a block of non-transparent data that is separated into two intermediate blocks.

**3.6.4.2 Reception Control** - Figure 3-6 is a state flow chart for the BISYNC reception control process. Four states or modes are required: Modes 0 and 2 are used to handle non-transparent data, Modes 3 and 4 are used to handle transparent data.

**Mode 0 (Waiting for Message)**

The DV11 is initialized to Mode 0, and the address and byte count registers in the DV11 are set to receive one byte. Response to the initial control character is as follows:

*ENQ* - the character is stored to record the request, an interrupt is generated to turn the buffer contents over to the protocol module for printout or other handling, and a new buffer is requested to store the expected data. The data is input in Mode 0 (no mode change).

*DLE* - discard the character and go to Mode 1 (transition to transparent reception).

*STX or SOH* - store the character and go to Mode 2 (non-transparent data reception).

*EOT* - store the character, generate an interrupt to turn buffer contents over to protocol module for termination of reception; stay in Mode 0.

*NACK* - store the negative acknowledgement character, generate interrupt to turn buffer contents over to protocol module for resumption of transmission; stay in Mode 0.

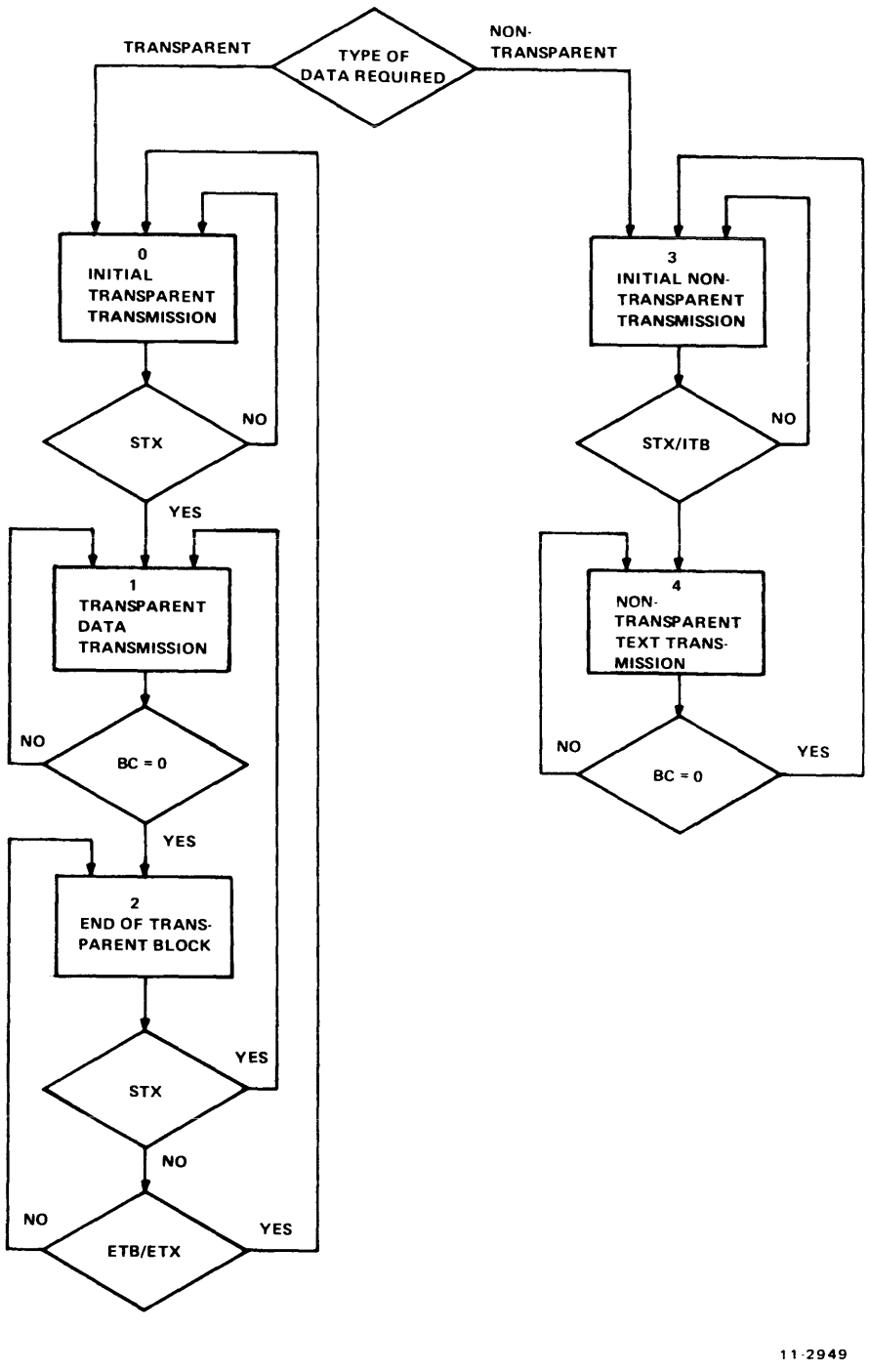



Figure 3-5 BISYNC Transmission Flow Diagram

Table 3-14
Transparent Data Transmission Control

| Data Buffer | | Control Byte Directives | | | | |
|---|---|---|---|---|---|---|
| | | Mode | | Stuff | Send BCC After | |
| No. | Contents | Current | Next | A DLE? | This Character? | INCL. CHAR. IN BCC? |
| 1 | STX | 0 | 1 | YES | – | – |
| 2 | CHAR. 1 | 1 | – | – | – | YES |
| | . | . | . | . | . | . |
| | . | . | . | . | . | . |
| | . | . | . | . | . | . |
| | CHAR. N** | 1 | (2)* | – | – | YES |
| 3 | ITB | 2 | – | YES | YES | YES |
| | DLE | 2 | – | – | – | YES |
| | STX | 2 | 1 | – | – | YES |
| 4 | CHAR. 1 | 1 | – | – | – | YES |
| | . | . | . | . | . | . |
| | . | . | . | . | . | . |
| | . | . | . | . | . | . |
| | CHAR. N** | 1 | (2)* | – | – | YES |
| 5 | ETX/ETB | 2 | 0 | YES | YES | YES |

*On Byte Count Zero Interrupt Not Control Byte Directive
**If Char. is a DLE, Stuff a DLE

Table 3-15
Non-Transparent Data Transmission Control

| Data Buffer | | Control Byte Directives | | | |
|---|---|---|---|---|---|
| | | Mode | | Send BCC After | |
| No. | Contents | Current | Next | This Character? | INCL. CHAR. IN BCC? |
| 1 | STX | 3 | 4 | – | – |
| 2 | CHAR. 1 | 4 | – | – | YES |
| | . | . | . | . | . |
| | . | . | . | . | . |
| | . | . | . | . | . |
| | CHAR. N | 4 | (3)* | – | YES |
| 3 | ITB | 3 | 4 | YES | YES |
| 4 | CHAR. 1 | 4 | – | | YES |
| | . | . | . | . | . |
| | . | . | . | . | . |
| | . | . | . | . | . |
| | CHAR. N | 4 | (3)* | – | YES |
| 5 | ETX/ETB | 3 | – | YES | YES |

*On Byte Count Zero Interrupt – Not Control Byte Directive

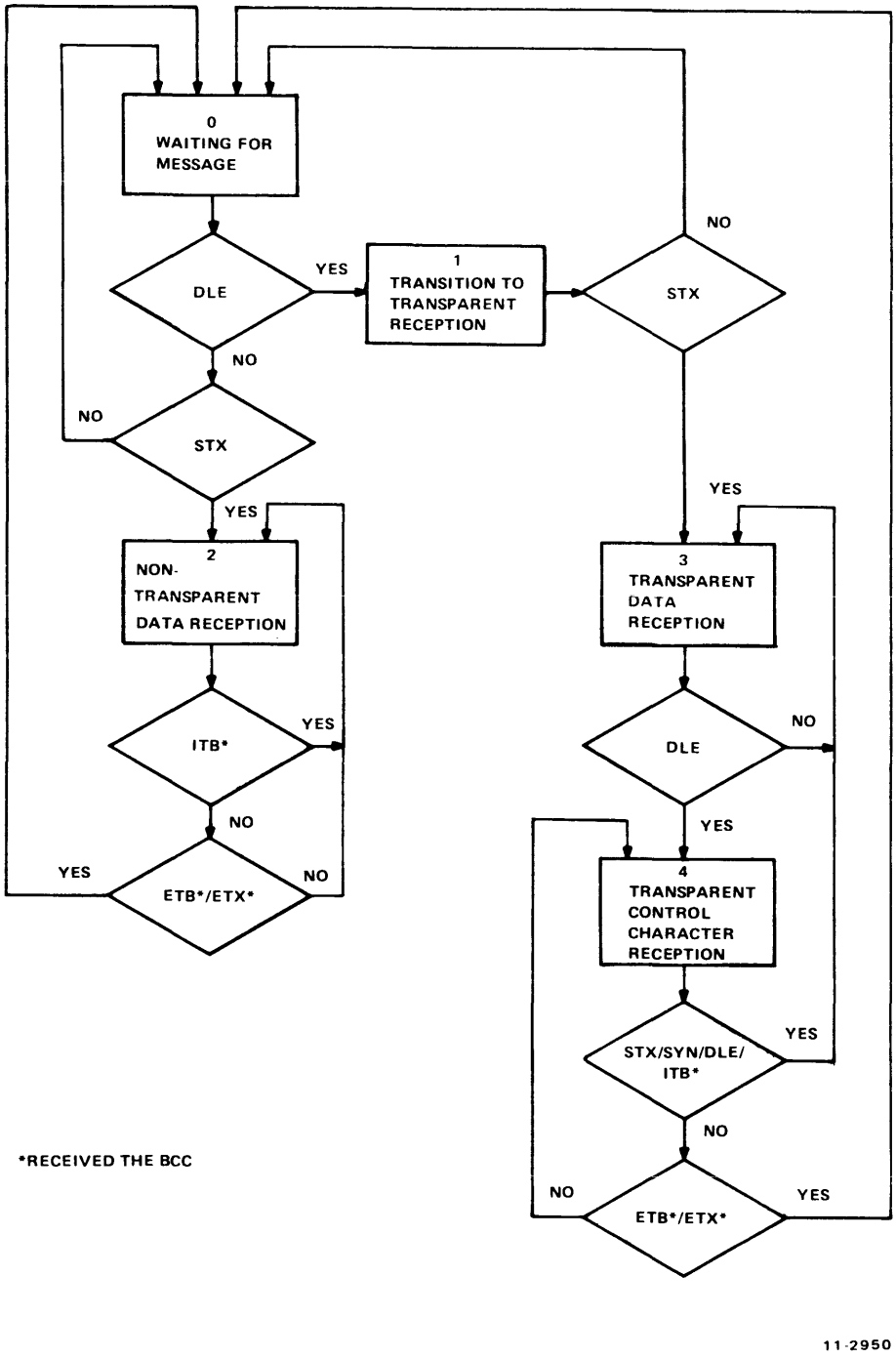



Figure 3-6 BISYNC Reception Flow Diagram

**Mode 1 (Transition to Transparent Reception)**
In this mode, the system initializes for the reception of transparent text. Mode 1 is entered only from Mode 0 following reception of a DLE. An STX is expected; if one is received, it is discarded (an interrupt is generated to set the Transparent Data flag), and Mode 3 is set.

If a positive acknowledgement character (ACK, WACK, RVI) is received, an interrupt is generated to turn the buffer contents over to the protocol module for resumption of transmission, and the DV11 is returned to Mode 0. Receipt of the ENQ repeat request causes an interrupt to set an Error flag and turn buffer contents over to the protocol module.

All other received characters are stored, an interrupt is generated, and the DV11 is returned to Mode 0.

**Mode 2 (Non-Transparent Data Reception)**
The system receives non-transparent text (including header, if sent) in this mode. All characters are stored and included in the BCC, except as follows:

*ITB* - store the character, include in BCC and receive BCC next. Interrupt, turn buffer contents over to protocol module.

*ETB or ETX* - store the character, include in BCC and receive BCC next. Set End-of-Block flag and turn buffer over to protocol module. Go to Mode 0.

*ENQ* - discard the character and set error flag. Interrupt and turn buffer over to protocol module. Return to Mode 0.

*SYN* - discard.

**Mode 3 (Transparent Data Reception)**
Transparent text is received in this mode. All characters except DLE are sorted and included in the BCC. A DLE, if received, is discarded, and Mode 4 (Transparent Control Character Reception) is set.

**Mode 4 (Transparent Control Character Reception)**
Control characters received in the transparent data stream are processed in this mode. The usual control characters would be the block delimiters, ITB, ETB, or ETX; these are included in the BCC, which is received immediately after them. The ITB is stored and requires a change to Mode 5 to strip syncs and then to get the rest of the data block. ETB or ETX is stored and return to Mode 0 is made. An interrupt is generated, the buffer contents are turned over to the protocol module, and address and byte counts are set to receive the 2-byte BCC.

Mode 4 responds to other control characters as follows:

*DLE* - store the character, include in the BCC, return to Mode 2.

*STX* - discard, include in BCC, return to Mode 3.

*ENQ* - interrupt, store the character, set Error flag, return to Mode 0.

*SYN* - discard, return to Mode 3.

*All Other Characters* - store, include in BCC, return to mode 3.

**Mode 5 (Transparent Intermediate Data Reception)**

*SYN* - discard

*DLE* - discard, include in BCC, go to mode 4.

*All Other Characters* - Interrupt, store, return buffer to the protocol module with errors. Go to mode 0.

### 3.6.5 DDCMP Implementation

The method suggested for DDCMP implementation uses a single control table for both send and receive. Buffers are configured so that the only interrupts required are those resulting from zero byte counts. Reference Figure B-4 for DDCMP data message format.

**3.6.5.1 Transmission Control** - Figure 3-7 is a flow chart for the DDCMP transmission process. Initially, the DV11 principal transmit registers are set with the base address and byte count of the data buffer containing the header, with bit 15 of the byte count set to zero, to cause BCC transmission at zero byte count time (reference Paragraph 3.1.4.2).

If a numbered (data) message or bootstrap message is being sent, set the alternate transmit registers with the base address and byte count of the first data buffer containing the actual data. When setting up to transmit the last data buffer, set bit 15 of the byte count to zero to cause BCC transmission at zero byte count time.

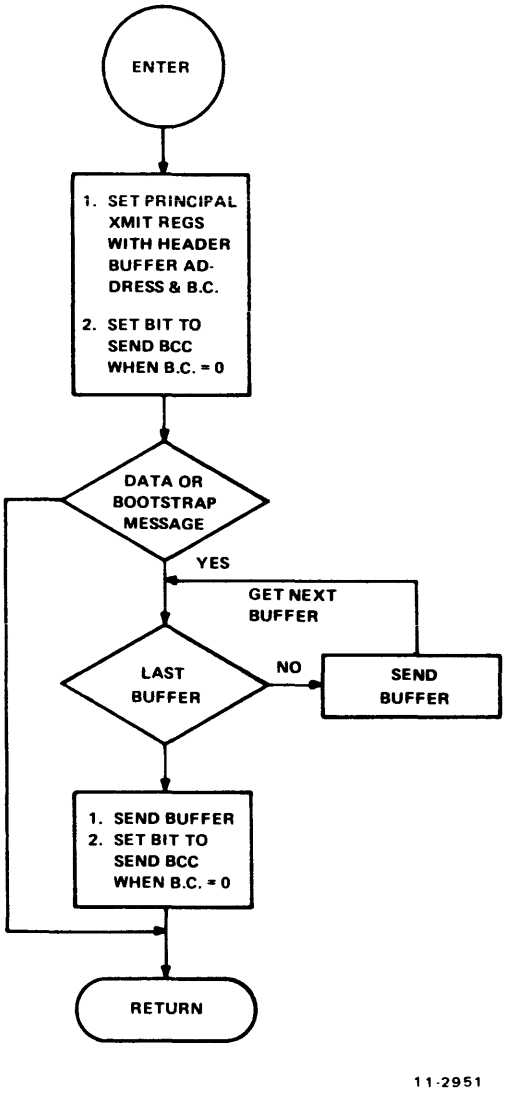



Figure 3-7 DDCMP Transmission Flow Diagram

**3.6.5.2 Reception Control** – Figure 3-8 is a flow chart for the DDCMP reception process. Initially, the DV11 receive registers are set to receive the six bytes of the incoming DDCMP header and bit 15 of the byte count register is cleared to direct reception of the BCC.

The first character in the first buffer is now examined to determine message type. If it is a numbered data message (SOH character) or a bootstrap message (DLE character), the character count in buffer words two and three is used to build a receive buffer of appropriate size. If it is an unnumbered control message (ENQ character), no additional buffering is required.

When the DV11 interrupts to signal BCC reception complete, set the DV11 receive registers to input the data to the receive buffer that has just been built, if any. On the next interrupt, return control to the calling program.

The BCC is checked at the points indicated in Figure 3-8. The BCC Received interrupt occurs as a result of a control byte directive or a marked byte count reaching zero. The BCC characters are included in the BCC. The accumulated BCC, if correct, should be zero.

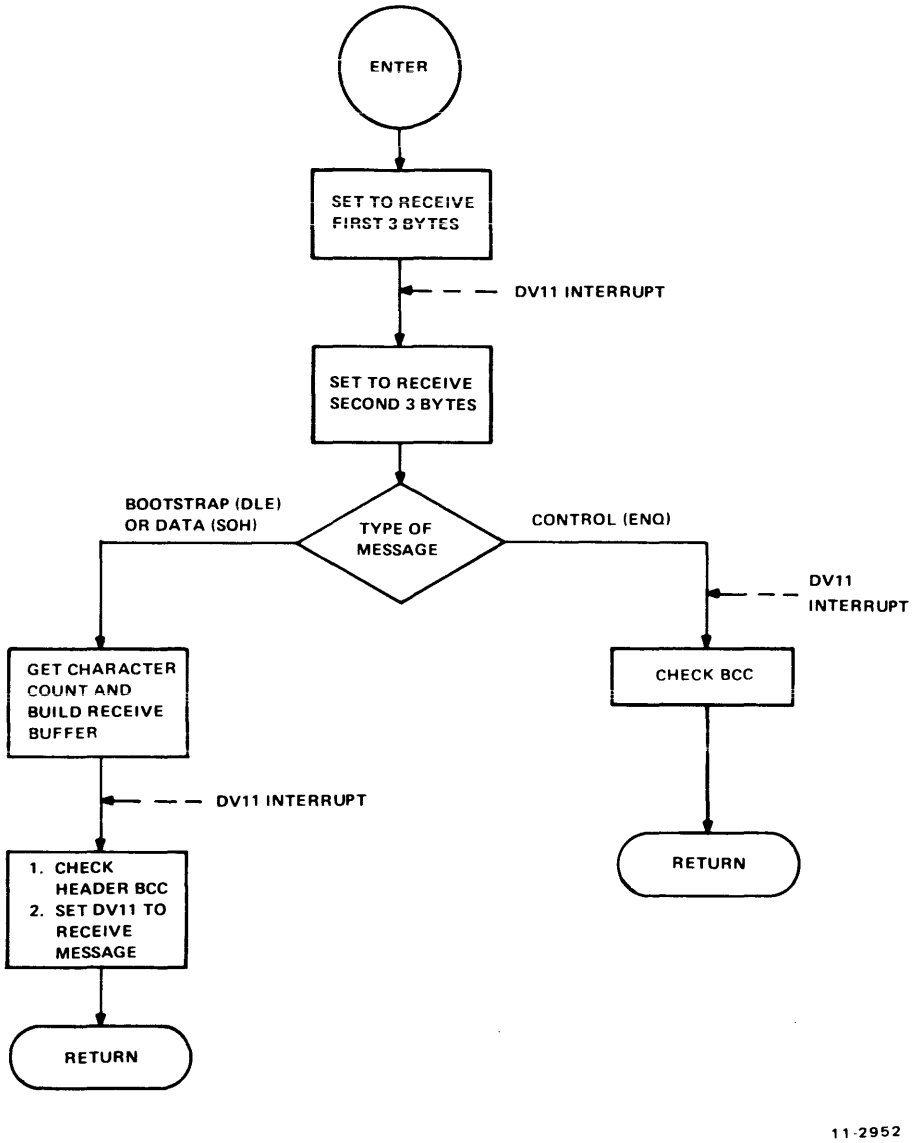



Figure 3-8 DDCMP Reception Flow Diagram

# APPENDIX A
# PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized into 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location: low bytes are even-numbered, high bytes are odd-numbered. Words are addressed at even-numbered locations *only* and the high (odd) byte of a word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even-numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00). These 18 bits provide the capability of addressing 256K memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multiplier *K* equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. This maximum memory size can be used only by a PDP-11 processor with a Memory Management Unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure A-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 218 or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the processor uses, as shown below.

The highest 8K address locations (760000–777777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248K bytes or 124K words to program.

A PDP-11 processor without the Memory Management Unit provides 16 address bits that specify $2^{16}$ or65,536 (64K) locations (Figure A-2). The maximum memory size is 65,536 (64K) bytes or 32,768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s, when the processor is master, to allow generation of addresses in the reserved area with only 16-bit control.

Bits 13, 14, and 15 become all 1s first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777, which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

| 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 | ADDRESS BIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BINARY |
| | | 1 | | | 1 | | | 7 | | | 6 | | | 0 | | | 1 | OCTAL |

11-3176

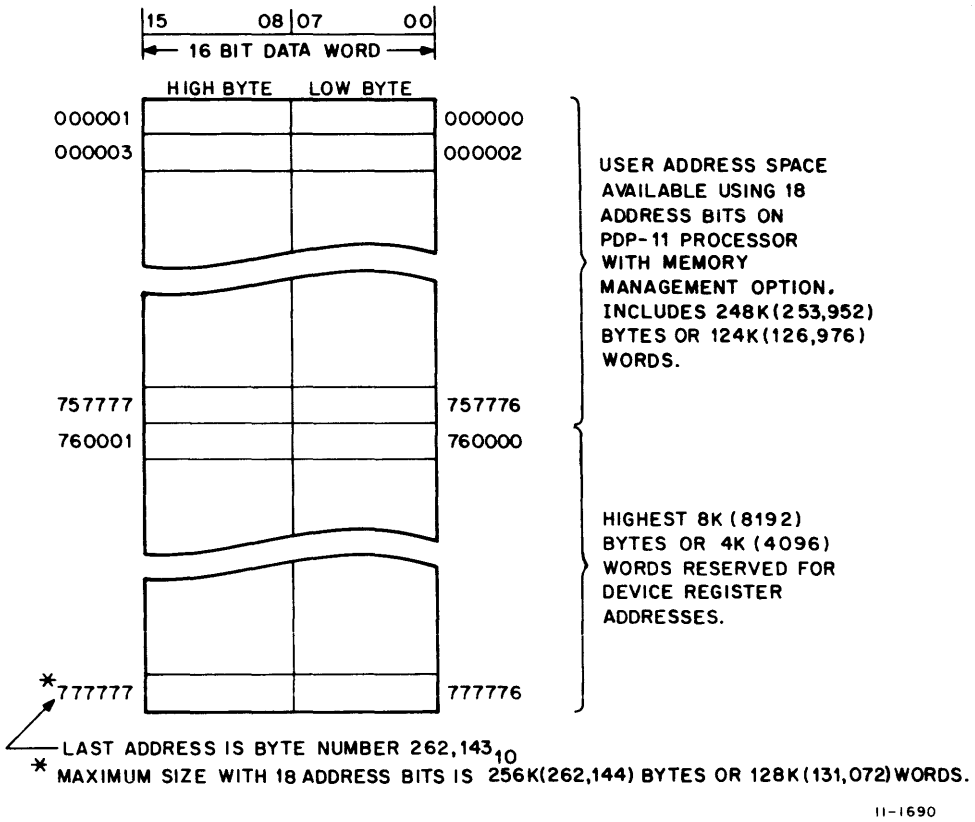



Figure A-1 Memory Organization for Maximum Size Using 18 Address Bits

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possibility of physical memory locations interferring with the reserved space.

PDP-11 core memories are available in 4K, 8K, or 16K increments. The highest location of various size core memories are shown.

| Memory Size K-Words | K-Bytes | Highest Location (Octal) |
|---|---|---|
| 4 | 8 | 017777 |
| 8 | 16 | 037777 |
| 12 | 24 | 057777 |
| 16 | 32 | 077777 |
| 20 | 40 | 117777 |
| 24 | 48 | 137777 |
| 28 | 56 | 157777 |

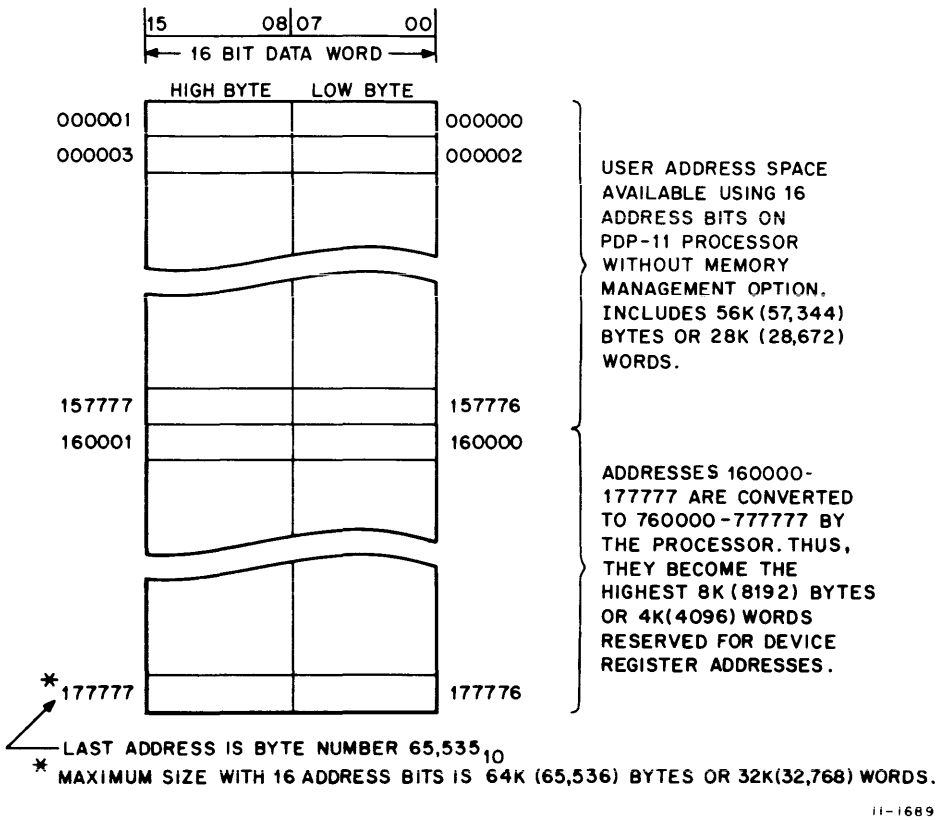



Figure A-2 Memory Organization for Maximum Size Using 16 Address Bits

# APPENDIX B
# PROTOCOLS FOR BINARY SYNCHRONOUS COMMUNICATIONS

A protocol is a set of rules which govern the sequencing, identification, and synchronization of data interchanged between data terminals. This appendix describes the features of two popular protocols to enable the user to select and plan for the implementation of the protocol best suited to his needs. This appendix also provides the necessary background data for understanding the data exchange requirements which the DV11 was specifically designed to accommodate.

## B.1 DATA CHANNEL UTILIZATION

The DV11 interchanges serial, synchronous, bytes or characters with remote terminals via data channels or lines. The maximum efficiency with which a channel may be utilized is determined by the structure of the protocol being used. Four factors inherent in any protocol affect data channel utilization efficiency:

direction utilization
control overhead
acknowledgement handling
number of data terminals or stations per line.

### B.1.1 Direction Utilization

A data channel between two terminals may physically permit one-way or two-way transmission, called simplex or duplex operation, respectively. The two-way transmission may alternate in direction of transmission, called *half-duplex*, or may provide simultaneous two-way transmission, called *full-duplex*. Most physical facilities are full-duplex, however, the protocol being used may not take advantage of the physical facility. It may be a half-duplex protocol (alternate data transmissions), although the physical facility is full-duplex. To make the most efficient use of a full-duplex facility, a full-duplex protocol is required.

### B.1.2 Control Overhead

Data transferred between terminals is comprised of information, control and error-checking bits. All but the information bits are Control Overhead bits. A data terminal is capable of transmitting a fixed number of bits per second in each direction; the control bits reduce the effective rate of information transfer. The ratio of the information bits to the total bits determines the one-way line utilization efficiency. The more control, header and error-checking characters needed by a protocol, the less efficient the line.

### B.1.3 Acknowledgement Handling

Acknowledgement handling can affect line utilization in two ways. First, if the acknowledgement is a separate message, then both the acknowledgement and the gaps between the acknowledgement and the data blocks are part of Control Overhead. Second, more overhead occurs if each message requires a separate acknowledgement. Acknowledgements within blocks containing information reduce the first overhead because it usually takes fewer or no additional characters for normal conditions; only errors are indicated by separate blocks. If the protocol defines a way to acknowledge multiple blocks with one response, the number of overhead bits is further reduced.

### B.1.4 Stations Per Line

When the activity from one station on a line is below full utilization, the extra capacity can be utilized by putting additional stations on the line. This is similar to telephone party lines and is called "multipoint" or "multidrop." When only two stations are involved, it is called "point-to-point." Most protocols support both point-to-point and multipoint arrangements. For multipoint operation, one station in the network is designated as the *Control Station*. The remaining stations are designated as *Tributary Stations*. The Control Station initiates data transfers by "polling" and "selection" of Tributary Stations. Polling is an invitation to send data, transmitted from a Control Station to a Tributary Station. Selection is a request to receive data, to be sent from the Control Station to the Tributary Station.

## B.2 DATA AND CONTROL CODES

The purpose of a data channel is to transfer data, unaltered, from a transmitter station (master) to a receiver station (slave). The data to be transferred is embedded in control codes, which serve to identify the type of data being transferred, and to provide for synchronization and error detection. (Thus, the channel is considered to consist of the physical facility plus control codes. For this reason, the control codes may be referred to as Data Channel or Data Link control codes.) Since both stations are operated in accordance with the same protocol, the receiver station is able to differentiate between the several types of control codes and data codes sent by the transmitter, and can therefore act accordingly.

### B.2.1 Types of Data

In the protocols to be described, all data are classed into two types or categories: Transparent Data, or Character-Encoded Data.

**B.2.1.1 Transparent Data** – It is often necessary to transmit binary data, floating-point numbers, packed-decimal data, unique specialized codes, or machine-language computer programs. In order to do this, all data, including the normally restricted Data-Link Control characters, are treated only as specific bit patterns. Protocols differ in the methods used to permit the use of all possible bit patterns as data while still controlling the data channel. Techniques for achieving transparency are discussed separately for each protocol described herein.

**B.2.1.2 Character Codes** – Several character encoding schemes are available. The codes differ primarily in the number of bits used to represent characters and the bit patterns which correspond to the characters. Characters are divided into graphic characters, representing a symbol, and control characters, which are used to control a terminal or computer function.

Although many codes are in use, the trend is toward the universal 7-bit-plus-parity ASCII (American Standard Code for Information Interchange) code. ASCII was introduced by the U.S.A. Standards Institute and has been accepted as the U.S. Federal Standard. Techniques for transmitting transparent or binary data also exist within the structure of the ASCII code. Special characters are set aside for Data Channel control.

A variation of the ASCII code is the 8-bit Data Interchange Code. Primarily, this code differs from ASCII in that some printing characters are replaced by non-printing control characters and the parity is specified to be odd. This code is readily adaptable to computer-to-computer communications.

Of the other existing codes, the most widely used are the Extended Binary Coded Decimal Interchange Code (EBCDIC), the 5-bit Baudot code, found in old teleprinter equipment, the Four of Eight Code, the IBM punched-card Hollerith code, the Binary Coded Decimal (BCD) code, and the 6-bit Transcode.

EBCDIC is an eight-level code similar to ASCII, except that while ASCII uses its eighth level for parity bits, EBCDIC uses it for information bits, thereby extending the range of characters to 256.

### B.2.2 Synchronization Codes

Preceding the data and control character is a sequence of one or more synchronizing (SYN or SYNC) characters, which have a protocol-defined bit pattern. The synchronization characters are used by the receiver to synchronize, or get in phase with, the characters in the continuous stream of bits, to determine where each character begins and ends. (This is the character-framing process described in Appendix C.)

### B.2.3 Error-Detecting Codes

The protocols to be described use error-detecting codes provided for by the DV11: LRC, CRC-16, and CRC-CCITT.

LRC is a Longitudinal Redundancy Check on the total data bits by message block (see Figure B-1). An LRC character is accumulated in both the sending and receiving terminals during the transmission of a block. This accumulation is called the Block Check Character (BCC). The transmitted BCC is compared with the accumulated BCC at the receiving station for an equal condition. An equal comparison indicates a good transmission of the previous block.

Cyclic Redundancy Checking (CRC) is a more powerful method of block checking than LRC. A CRC is a division performed by both the transmitting and receiving stations, using the numeric binary value of the message as a dividend, which is divided by a constant. In performing the division, borrows are ignored. The quotient is discarded and the remainder serves as the check character, which is then transmitted as the BCC. The receiving station compares the transmitted remainder with its own computed remainder, and finds no error if they are equal.

| Bit Position | P | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Character 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| Character 2 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| Character 3 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Character 4 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| LRC-8 BCC | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |

Figure B-1 Longitudinal Redundancy Checking

An infinite number of constants may be used to perform the CRC division. The DV11 makes available two CRC computations: CRC-16 (which uses a polynomial of the form $x^{16} + x^{15} + x^2 + 1$), and CRC-CCITT (which uses a polynomial of the form $x^{16} + x^{12} + x^5 + 1$). Each generates a 16-bit BCC.

## B.3 BSC PROTOCOL (BISYNC)

One of the most widely used protocols is IBM's Binary Synchronous Communications (BSC). BSC, also known as BISYNC, has been in use since 1968 for transmission between IBM computers and remote terminals of the batch and video display types.

LRC is the modulo 2 sum (exclusive-OR) of the bits in each bit position of all characters in a message block to produce a BCC. The figure shows the BCC computation for four 8-bit characters using LRC. Each character contains seven data bits and an odd-parity bit.

### B.3.1 Controlling Data Transfers

The format of a BSC message is shown in Figure B-2. BSC uses control characters to delimit the fields. The header is optional; if it is used, it begins with SOH (Start of Header) and ends with STX (Start of Text). The contents of the header are defined by the user. Polling and addressing on multipoint lines are handled by a separate control message and not by using the header field. The text portion of the field is variable in length and may contain transparent data. If it is defined as transparent, it is delimited by DLE (Data Line Escape) STX and DLE ET (End of Text), or DLE ETB (End of Text Block). The block is terminated by the BCC.

BSC protocol employs a rigorous set of rules for establishing, maintaining, and terminating a communications sequence. A typical exchange between a data terminal and the DV11/PDP-11 on a point-to-point private line is illustrated in Figure ~~B-2~~ B-3

### B.3.2 Error Checking and Recovery

To detect and correct transmission errors, BSC uses either VRC/LRC or CRC, depending upon the character code. If the code is ASCII, a VRC check is performed on each character and an LRC on the whole message. The LRC becomes one 8-bit BCC. If the code is EBCDIC, CRC-16 ($x^{16} + x^{15} + x^2 + 1$) is used, resulting in a 16-bit BCC.

If the BCC transmitted does not agree with the BCC computed by the receiver, or if there is a VRC error, a NAK sequence (shown in Figure B-3) is sent back to the data source. BSC calls for the retransmission of the block when an error occurs. BSC will typically retry three times before concluding that the line is in an unrecoverable state. BSC checks for sequence errors by alternating positive acknowledgments to successive blocks. ACK0 and ACK1 are the responses to the even-numbered and odd-numbered blocks in the message, respectively. These are sent in separate control messages.

### B.3.3 Character Coding

BSC supports ASCII, EBCDIC, or 6-bit Transcode. Table D-1 lists and describes certain bit patterns in each set that have been set aside for the required BSC control characters. Some BSC control codes are multi-character sequences.

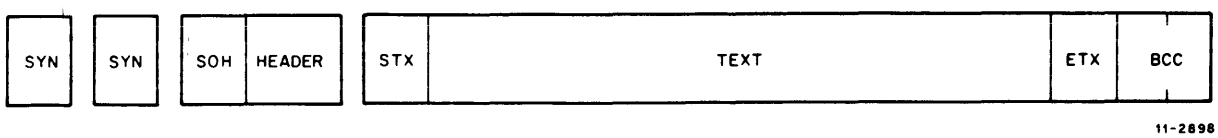



Figure B-2 BSC Data Message Format

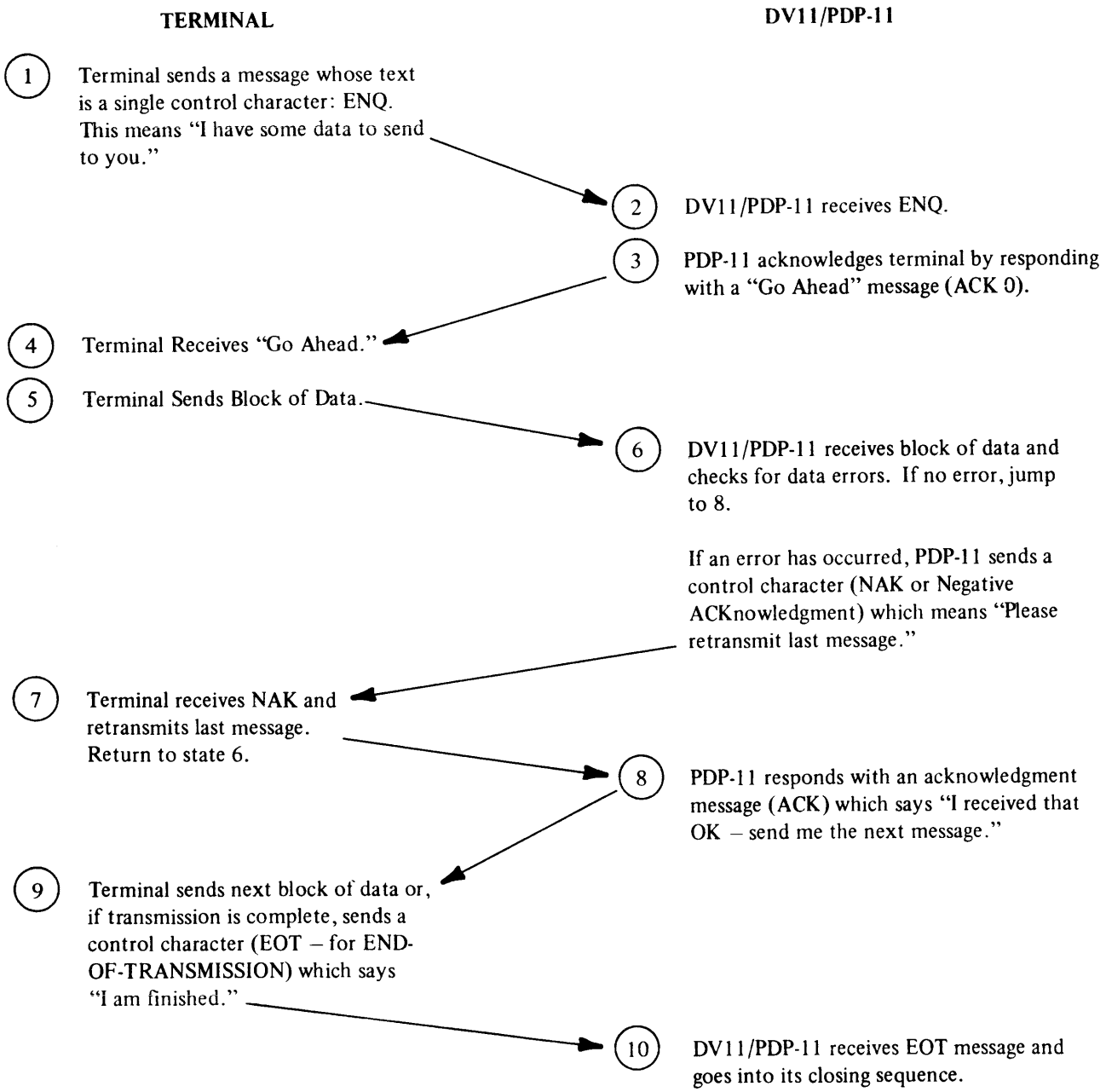



Figure B-3 Typical Data Exchange Using BSC (BISYNC)

**Table B-1**
**BSC Data Channel Control Codes**

| Control Code Mnemonic | Meaning |
|---|---|
| SYN | Synchronous Idle |
| SOH | Start of Heading |
| STX | Start of Text |
| ITB | End of Intermediate Transmission Block |
| ETB | End of Transmission Block |
| ETX | End of Text |
| EOT | End of Transmission |
| ENQ | Enquiry |
| ACK0/ACK1 | Alternating Affirmative Acknowledgments |
| WACK | Wait-Before-Transmit Positive Acknowledgments |
| NAK | Negative Acknowledgment |
| DLE | Data-Link Escape |
| RVI | Reverse Interrupt |
| TTD | Temporary Text Delay |
| DLE EOT | Disconnect Sequence for a Switched Line |

### B.3.4 Data Transparency

In BSC, the transparent mode is defined by starting the text field with DLE STX. Once in transparency, the only control character of significance is DLE. Any Data Link control characters transmitted during the transparent mode must be preceded by a DLE control character to be recognized as a control function. When a bit pattern equivalent to DLE appears within the transparent data, two DLEs are used to permit transmission of DLE as data. When received, one DLE is disregarded; the other is treated as data. This technique is called "character stuffing."

### B.3.5 Data Channel Utilization

BSC transmission is half-duplex. The line must be turned around *twice* between each block (once for the acknowledgment sequence and once for the data block). All fields are delimited by control characters, and acknowledgments are handled by separate control sequences. An acknowledgment sequence is required for each block and for each acknowledgment sequence. A minimum of two character times is required for each synchronization. BSC supports both point-to-point and multipoint lines.

### B.3.6 Synchronization

BSC synchronizes on each block or control sequence by preceding the formatted block with the synchronizing (SYN) characters. Two synchronizing characters are required, but more (usually five) are sent. SYN is defined as a unique bit pattern in each of the three information exchange codes available with BSC. In addition, some BSC applications require that all 1s PAD characters follow messages.

## B.4 DDCMP PROTOCOL

DDCMP (Digital Data Communications Message Protocol) was developed to provide full-duplex message transfer over standard existing hardware.

### B.4.1 Controlling Data Transfers

The DDCMP message format is shown in Figure B-4. A single control character is used in a DDCMP message, and is the first character in the message. Three control characters are provided in DDCMP to differentiate between the three possible types of messages:

SOH - data message follows
ENQ - control message follows
DLE - bootstrap message follows.

Note that the use of a fixed-length header and message size declaration obviates the BSC requirement for extensive message and header delimiter codes.

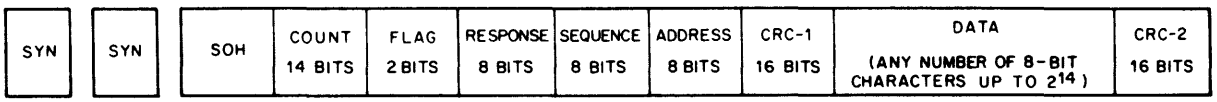



Figure B-4 DDCMP Data Message Format

Figure B-5 shows a simple example of data exchange between the DV11/PDP-11 and a data terminal. More efficient procedures can be derived after a study of DDCMP.

### B.4.2 Error Checking and Recovery

DDCMP uses CRC-16 for detecting transmission errors. When an error occurs, DDCMP sends a separate NAK message. DDCMP does not require an acknowledgment message for all data messages. The number in the response field of a normal header or in either the special NAK or ACK message, specifies the sequence number of the last good message received. For example, if messages 4, 5, and 6 have been received since the last time an acknowledgment was sent and message 6 is bad, the NAK message specifies number 5 which says "message 4 and 5 are good and 6 is bad." When DDCMP operates in full-duplex mode, the line does not have to be turned around; the NAK is simply added to the sequence of messages for the transmitter.

When a sequence error occurs in DDCMP, the receiving station does not respond to the message. The transmitting station detects, from the response field of the messages it receives (or via timeout), that the receiving station is still looking for a certain message and sends it again. For example, if the next message the receiver expects to receive is 5, but 6 is received, the receiver will not change the response field of its data messages, which contains a 4. This says: "I accept all messages up through message 4 and I'm still looking for message 5."

### B.4.3 Character Coding

DDCMP uses ASCII control characters for SYN, SOH, ENQ and DLE. The remainder of the message, including the header, is transparent.

### B.4.4 Data Transparency

DDCMP defines transparency by use of a count field in the header. The header is of fixed length. The count in the header determines the length of the transparent information field, which can be zero to 16,383 bytes long. To validate the header and count field, it is followed by a 16-bit CRC-16 field; all header characters are included in the CRC calculation. Once validated, the count is used to receive the data and to locate the second CRC-16, which is calculated on the data field. Thus, character stuffing is avoided.

### B.4.5 Data Channel Utilization

DDCMP uses either full- or half-duplex circuits at optimum efficiency. In the full-duplex mode, DDCMP operates as two dependent one-way channels, each containing its own data stream. The only dependency are the acknowledgments which must be sent in the data stream in the opposite direction.

Separate ACK messages are unnecessary, reducing the control overhead. Acknowledgments are simply placed in the response field of the next message for the opposite direction. If several messages are received correctly before the terminal is able to send a message, all of them can be acknowledged by one response. Only when a transmission error occurs or when traffic in the opposite direction is light (no data message to send) is it necessary to send a special NAK or ACK message, respectively.

In summary, DDCMP data channel utilization features include:

1. The ability to run on full- or half-duplex data channel facilities.
2. Low control character overhead.
3. No "character stuffing."
4. No separate ACKs when traffic is heavy; this saves on extra SYN characters and inter-message gaps.
5. Multiple acknowledgments (up to 255) with one ACK.
6. The ability to support point-to-point and multipoint lines.

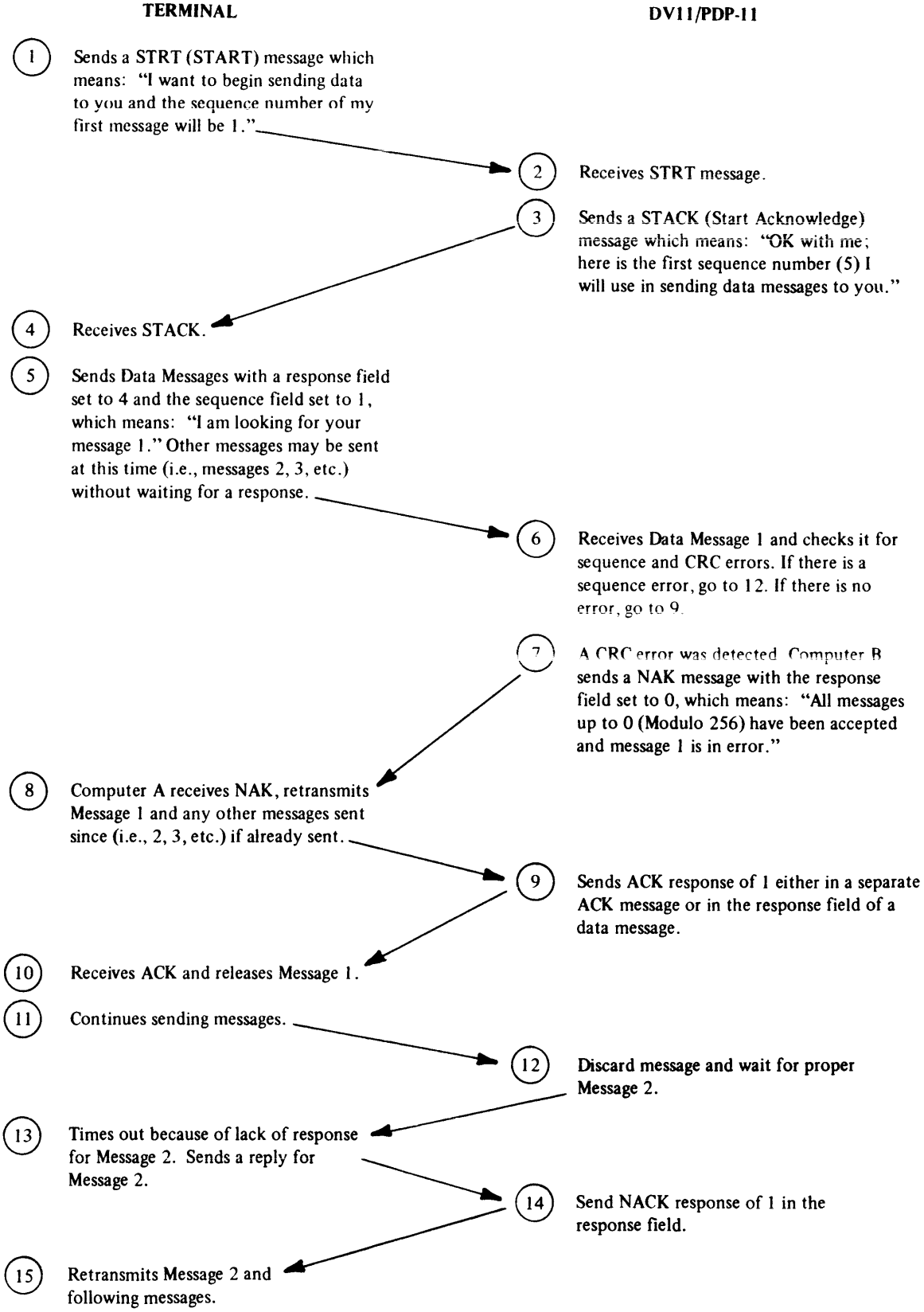



Figure B-5 DDCMP Sample Handshaking Procedure

### B.4.6 Synchronization

DDCMP achieves synchronization through the use of two ASCII SYN characters preceding the SOH, ENQ, or DLE. It is not necessary to synchronize between messages as long as no gap exists. Gaps are filled with SYN characters. Two sync characters are required, but more are usually transmitted. If synchronization between messages is deliberately lost by sending PAD (all 1s) characters, the intermessage interval must be at least 14 character times in length.

### B.4.7 Bootstrapping

DDCMP has a bootstrap message as part of the protocol. It begins with the ASCII control character DLE. The information field contains the system reload programs and is totally transparent.

# APPENDIX C
# GLOSSARY OF TERMS AND ABBREVIATIONS

*ACK* - Acknowledgment

*ACK 0, ACK 1 (Affirmative Acknowledgment)* - These replies (DLE sequence in Binary Synchronous Communications) indicate that the previous transmission block is accepted by the receiver and that it is ready to accept the next block of the transmission. Use of ACK 0 and ACK 1 alternately provides sequential checking control for a series of replies. ACK 0 is also an affirmative (ready to receive) reply to a station selection (multipoint), or to an initialization sequence (line bid) in point-to-point operation.

*ASCII* - American Standard Code for Information Interchange. This is the code established as an American standard by the American Standards Association.

*Automatic Calling Unit (ACU)* - A dialing device (Bell 801 or equivalent) that permits a business machine to dial calls automatically over the communications network.

*Baseband* - In the process of modulation, the baseband is the frequency band occupied by the aggregate of the transmitted signals when first used to modulate a carrier.

*Baud* - A unit of signaling speed. One baud corresponds to a rate of one signal element per second. Thus, with a duration of the shortest signal element of 20 ms, the modulation rate is 50 baud.

*Baudot Code* - A code for the transmission of data in which five bits represent one character. It is named for Emile Baudot, a pioneer in printing telegraphy. The name is usually applied to the code used in many teleprinter systems and which was first used by Murray, a contemporary of Baudot.

*BCC* - Block Check Character (q.v.)

*Binary Synchronous Communications (BSC)* - A uniform discipline, using a defined set of control characters and control sequences, for synchronized transmission of binary coded data between stations in a data communications system. (Also called BISYNC.)

*BISYNC* - Binary Synchronous Communications.

*Block Check Character (BCC)* - The result of a transmission verification algorithm accumulated over a transmission block, and normally appended at the end: e.g., CRC, LRC.

*Byte* - A binary element string operated upon as a unit and usually shorter than a computer word, e.g., six-bit, eight-bit, or nine-bit bytes.

*Carrier* - A continuous frequency capable of being modulated or impressed with a signal.

*CCITT* - Comite Consultatif Internationale Telegraphique et Telephonique. An international consultative committee that sets international communications usage standards.

*Channel* - (a.) A path for electrical transmission between two or more points. Also called a circuit, facility, line, link, or path. (b.) The physical facility or path plus control codes, within which the actual data to be transferred is embedded.

*Character* - The actual or coded representation of a digit, letter, or special symbol.

*CO* - Carrier On.

*Communication Control Character* - In ASCII, a functional character intended to control or facilitate transmission over data networks. There are ten control characters specified in ASCII which form the basis for character-oriented communications control procedures. (See also: Control Character.)

*Concentrator* – A communications device that provides a communications capability between many low-speed, usually asynchronous channels, and one or more high-speed, usually synchronous channels. Usually different speeds, codes, and protocols can be accommodated on the low-speed side. The low-speed channels usually operate in contention, requiring buffering. The concentrator may have the capability to be polled by a computer, and may in turn poll terminals.

*Conditioning* – The addition of equipment to leased voice-grade lines to provide specified minimum values of line characteristics required for data transmission, e.g., equalization and echo suppression.

*Contention* – A condition on a communications channel when two or more stations try to transmit at the same time.

*Control Character* – (1.) A character whose occurrence in a particular context initiates, modifies, or stops a control function. (2.) In the ASCII code, any of the first 32 characters. (See also: Communications Control Character.)

*Control Procedure* – The means used to control the orderly communication of information between stations on a data link. Syn: Line Discipline. (See also: Protocol.)

*CRC* – Cyclic Redundancy Check (q.v.)

*Cross Talk* – Unwanted insertion of signal from an adjacent communication channel.

*CS* – Clear to Send.

*Cyclic Redundancy Check (CRC)* – An error detection scheme in which the check character is generated by taking the remainder after dividing all the serialized bits in a block of data by a predetermined binary number.

*Dataphone* – A trademark of the A.T.&T. Company to identify the data sets (modems) manufactured and supplied by the Bell System for use in the transmission of data over the regular telephone network. It is also a service mark of the Bell System that identifies the transmission of data over the regular telephone network (DATAPHONE Service).

*Data Link* – An assembly of terminal installations and the interconnecting circuits operating according to a particular method that permits information to be exchanged between terminal installations. Note: The method of operation is defined by particular transmission codes, transmission mode, direction, and control.

*Data Set* – A device that converts the signals of a business machine to signals that are suitable for transmission over communication lines and vice versa. It may also perform other related functions. (Same as "modem.").

*DDCMP* – Digital Data Communications Message Protocol. A uniform discipline for the transmission of data between stations in a point-to-point or multipoint data communications system. The method of physical data transfer used may be parallel, serial synchronous, or serial aysnchronous.

*Demodulation* – The process of retrieving an original signal from a modulated carrier wave. This technique is used in data sets to make communication signals compatible with business machine signals.

*Dial-Up* – The use of a dial or push-button telephone to initiate a station-to-station telephone call.

*Dibit* – A pair of binary digits. Used to encode the four carrier phase shifts required for binary modulation by modems.

*Direct Memory Access (DMA)* – A facility that permits I/O transfers directly into or out of memory without passing through the processor's general registers; either performed independently of the processor or on a cycle-stealing basis. (Same as NPR.)

*DLE (Data Link Escape)* – (a.) A control character used in BISYNC to provide supplementary line-control signals (control character sequences or DLE sequences). These are two-character sequences where the first character is DLE. The second character varies according to the function desired and the code used. (b.) A control character used in DDCMP to signal a bootstrap message.

*Duplex* – In communications, pertaining to a simultaneous two-way, independent transmission in both directions, sometimes referred to as full-duplex. (Contrast with half-duplex.)

*EBCDIC* – Extended Binary Coded-Decimal Interchange Code. An 8-bit character code used primarily in IBM equipment. The code provides for 256 different bit patterns.

*Echo* – A portion of the transmitted signal returned from the distant point to the source with sufficient magnitude and delay so as to cause interference.

*ENQ (Enquiry)* – (a.) Used in BISYNC as a request for response to obtain identification and/or an indication of station status. ENQ is transmitted as part of an initialization sequence (line bid) in point-to-point operation, and as the final character of a selection or polling sequence in multipoint operation. (b.) Used in DDCMP to signal a control message.

*EOT (End of Transmission)* – Indicates the end of a transmission, which may include one or more messages, and resets all stations on the line to control mode (unless it erroneously occurs within a transmission block). EOT is also transmitted as a negative response to a polling sequence.

*ETB* – End of Transmission Block.

*ETX (End of Text)* – Indicates the end of a message. If multiple transmission blocks are contained in a message in BSC systems, ETX terminates the last block of the message. (ETB is used to terminate preceding blocks.) The block check character is sent immediately following ETX. ETX requires a reply indicating the receiving station's status.

*Executive Routine* – A program that monitors system activity and transfers control to subordinate programs for handling. When handling is complete, control is returned to the executive. When the system is inactive, the executive spins in an idle mode.

*Facility* – See Channel.

*Full-Duplex* – See Duplex.

*H* – High (positive).

*Half-Duplex* – Pertaining to an alternate, one-way-at-a-time independent transmission. (Contrast with duplex.)

*Header* – The control information prefixed in a message text, e.g., source or destination code, priority, or message type. Syn: Heading, Leader.

*Idle Loop* – See Executive Routine.

*ITB (Intermediate Text In Binary Synchronous Communications, Block)* – A control character used to terminate an intermediate block of characters. The block check character is sent immediately following ITB, but no line turnaround occurs. The response following ETB or ETX also applies to all of the ITB checks immediately preceding the block terminated by ETB or ETX.

*L* – Low.

*Line* – See Channel.

*Link* – See Channel.

*Longitudinal Redundancy Check (LRC)* – A system of error control based on the transmission of a Block Check Character (BCC) based on preset rules. The check formation rule is applied in the same manner to each character.

*LRC* – Longitudinal Redundancy Check.

*Mark* – Presence of a signal. In telegraphy, mark represents the closed condition or current flowing. Equivalent to a binary one condition.

*Modem* – Contraction of modulator-demodulator. A device that modulates and demodulates signals transmitted over communication facilities. (Same as data set.)

*Modulation* – The process by which some characteristic of a high-frequency carrier signal is varied in accordance with another lower frequency "information" signal. This technique is used in data sets to make business-machine signals compatible with communication facilities.

*Multiplexing* – The division of a transmission facility into two or more channels.

*Multipoint Circuit* – A circuit interconnecting several stations.

*NAK (Negative Acknowledgment)* – Indicates that the previous transmission block was in error and the receiver is ready to accept a retransmission of the erroneous block. NAK is also the "not ready" reply to a station selection (multipoint) or to an initialization sequence (line bid) in point-to-point operation.

*Non-Processor Request (NPR)* – High priority data transfers to the PDP-11 Processor. These are direct memory access type transfers, and are honored by the processor between bus cycles of an instruction execution. NPR data transfers can be made between any two peripheral devices without the supervision of the processor. Normally, NPR transfers are between a mass storage device, such as a disk and core memory. An NPR device has very fast access to the bus and can transfer at high data rates once it has control. The processor state is not affected by the transfer; therefore, the processor can relinquish control while an instruction is in progress. (See DMA.)

*Non-Transparent Mode* – Transmission of characters in a defined character format, e.g., ASCII or EBCDIC, in which all defined control characters and control character sequences are recognized and treated as such.

*NS* – New Sync.

*Parallel Transmisson* – Method of information transfer in which all bits of a character are sent simultaneously. Contrast with serial transmission.

*Path* – See Channel.

*Polling* – A centrally controlled method of calling a number of points to permit them to transmit information.

*Priority or Precedence* – Controlled transmission of messages in order of their designated importance; e.g., urgent or routine.

*Private Line or Private Wire* – A channel or circuit furnished to a subscriber for his exclusive use (non dial-up).

*Protocol* – A set of rules which govern the sequencing, identification, and synchronization of data exchanged between data terminals.

*RC* – Received Character.

*Reverse Interrupt (RVI)* – In Binary Synchronous Communications, a control character sequence (DLE sequence) sent by a receiving station instead of ACK1 or ACK0 to request premature termination of the transmission in progress.

*RS* – Request to Send.

*SDLC* – Synchronous Data Link Control. A protocol for the transfer of data between stations in a point-to-point, multipoint, or loop arrangement, using synchronous data transmission techniques.

*Seizure Line* – Terminating a transmission line in a DC path, causing a relay element in the telephone switching network to trigger and complete the circuit between the calling station and the called station. Voice or data is then inductively coupled between the transmission line and the terminal. Equivalent to taking the handset "off the hook" of a conventional telephone instrument or data set.

*Selective Calling* – The ability of a transmitting station to specify which of several stations on the same line is to receive a message.

*Serial Transmission* – A method of information transfer in which the bits composing a character are sent sequentially. (Contrast with parallel transmission.)

*Signal* – In communication theory, an intentional disturbance in a communication system. (Contrast with noise.)

*Silo* – A first-in, first-out hardware buffer, such as the RC Silo and the NSR in the DV11, which use the 3341 Propagable Register I.C., described in Appendix B.

*Simplex Mode* – Operation of a channel in one direction only with no capability of reversing.

*Single-Address Message* – A message to be delivered to one destination only.

*Start of Heading (SOH)* – (a.) In Binary Synchronous Communications (BISYNC), precedes a block of heading characters. (b.) In DDCMP, signals a data message.

*Station* – One of the input or output points on a communications system.

*Stuff a DLE* – Send a Data Link Escape character just prior to the character to be transmitted.

*STX* – Start of Text.

*Synchronous Idle (SYN)* – Character used as a time fill in the absence of any data or control character to maintain synchronization. The sequence of two continuous SYNs is used to establish synchronization (character phase) following each line turnaround.

*System Unit* – Three 8-slot connector blocks mounted end-to-end and capable of accommodating up to four hex modules (printed circuit boards). When two system units are connected to form a double system unit, up to nine hex modules may be accommodated.

*Teletypewriter Exchange Service (TWX)* – An automatic teleprinter exchange switching service provided by Western Union.

*Telex* – An automatic teleprinter exchange switching service provided by Western Union.

*Temporary Text Delay (TTD)* – In Binary Synchronous Communications, a control character sequence (STX...ENQ) sent by a transmitting station to either indicate a delay in transmission or to initiate an abort of the transmission in progress.

*Term* – Terminal

*Terminal* – (a.) A point at which information can enter or leave a communication network. (b.) An I/O device designed to receive or send source data in an environment associated with the job to be performed. Capable of transmitting entries to and obtaining output from the system of which it is a part.

*Text* – That part of the message which contains the substantive information to be conveyed. Sometimes called "body" of the message.

*Transparent Mode* – Transmission of binary data with the recognition of most control characters suppressed. In Binary Synchronous Communications, entry to and exit from the transparent mode is indicated by a sequence beginning with a special Data Link Escape (DLE) character.

*TTD* – Temporary Text Delay (q.v.).

*Unibus* – The single, asynchronous, high-speed bus structure shared by the PDP-11 processor, its memory, and all of its peripherals.

*Unibus Load* – The electrical connection of two 8881 outputs and one 8640 input to a Unibus signal lead.

*Unit Load* – All inputs impose a load on the outputs driving them. A TTL unit load requires 1.6 mA at ground and +40 $\mu$A at +3 V. The load imposed upon an output by an input can be defined as a number of unit loads.

*Vector* – Two words, containing the value of the program counter and processor status word, respectively, that direct the processor to a new routine.

*Vector Address* – The address of the location containing the vector words.

*Vertical Redundancy Check (VRC)* – A check or parity bit added to each character in a message such that the number of bits in each character, including the parity bit, is odd (odd parity) or even (even parity).

*Volatile* – A storage device whose contents may be altered by a power shut-off. The DV11 RAM is a volatile device.

*VRC* – Vertical Redundancy Check.

*WACK* – Wait-Before-Transmit Positive Acknowledgments. In Binary Synchronous Communications, this DLE sequence is sent by a receiving station to indicate that it is temporarily not ready to receive.

DV11 COMMUNICATIONS MULTIPLEXER
USER'S MANUAL
EK-DV11-OP-001

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