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MAINTENANCE MANUAL

DEC-16-HMMMA-A-D

PDP16-M
MAINTENANCE MANUAL

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FOREWORD

All information necessary to service and maintain the PDP16-M minicomputer is contained in this manual. The manual contains five chapters and four appendices:

Chapter 1 provides a general functional and physical description of the PDP16-M and its options. Specifications and configuration data are also detailed in this chapter.

Chapter 2 contains installation and checkout procedures. The basic diagnostic and all relevent option diagnostic programs are performed after installation to verify that the PDP16-M is operating properly.

Chapter 3 covers operating and programming details. In addition to the operating information, a complete description of the basic instruction set for the PDP16-M is included. Instructions that are implemented through options are detailed in the appropriate option descriptions (Appendix A).

Chapter 4 contains the theory of operation of the basic PDP16-M. Theory of operation for the options is included in the appropriate option description (Appendix A).

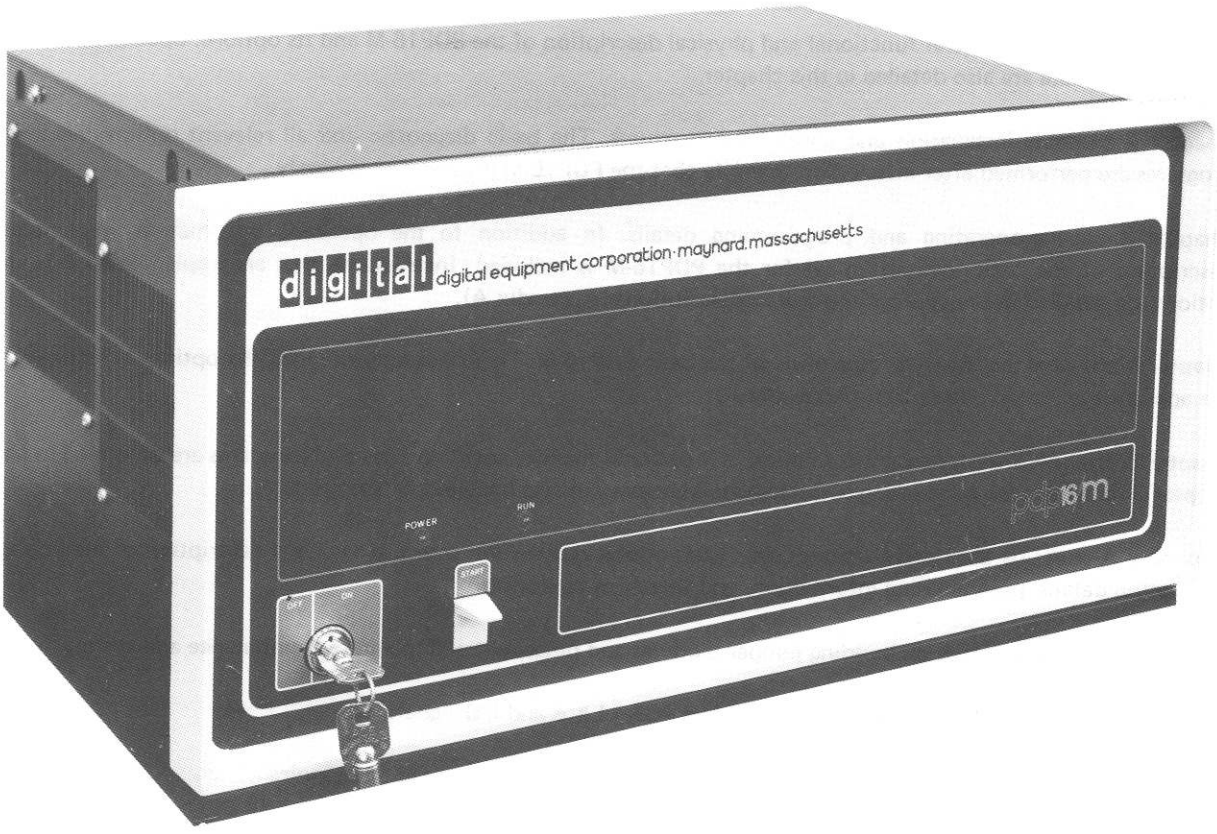
Chapter 5 provides maintenance information. All optional maintenance modules and programs are described in this chapter. Procedures for performing corrective maintenance are also included in this chapter.

Appendix A contains the option descriptions. Each option description provides a general description of the option, installation details, programming information, and theory of operation.

Appendix B presents details on building jumper modules and plugs that will facilitate maintenance and testing.

Appendix C is an alphabetic listing of PDP16-M and PDP-11 bus and I/O signals.

Appendix D lists all PDP16-M instruction machine codes, execution times, and mnemonics.


digital
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POWER
RUN
START
pdp8m

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

The PDP16-M is a programmable minicomputer with built-in flexibility for memory and I/O expansion. It can be used as a stand-alone controller or as a subprocessor in a larger system.

A prewired mainframe facilitates expansion of control memory, data memory, and I/O options simply by inserting the appropriate option module in its assigned slot. Insertion slots are also reserved on the mainframe for standard I/O interfacing cables and PDP16-M maintenance options. The application program is stored in a control PROM which can be reprogrammed at least 100 times. Once a PROM is loaded and installed in a PDP16-M, the machine exhibits the characteristics of a dedicated controller. However, the PROM can be reloaded with a different application program and/or a different application PROM can be installed in the PDP16-M. This feature permits the PDP16-M to be used not only as a dedicated controller, but as a general purpose controller, monitor, or preprocessor.

Application programs can be written for virtually any kind of application within the range of the arithmetic, logic, memory, and I/O capabilities of the PDP16-M. Data logging, waveform analysis, data format and media conversion, preprocessing, and postprocessing are some applications for which a PDP16-M can be implemented.

1.2 FUNCTIONAL DESCRIPTION

The basic PDP16-M consists of a general purpose arithmetic unit (GPA), 256-location control PROM, a high speed transfer register, a 16-bit I/O interface, three programmable flip-flops (Boolean outputs or flags), a 4-word data constant ROM, and six external Boolean inputs (Figure 1-1). Space is reserved within the chassis for prewired memory and I/O options which can expand the machine to 1K of control PROM, 33 registers, 256, 512, 1K, 1.25K or 2K of 16-bit read-write MOS memory, 28 constants, three 16-bit I/O interfaces, two serial I/O interfaces, six programmable flip-flops, a 256-word 8- or 16-bit data PROM, and 22 external Boolean inputs.

The control program is stored in a semiconductor PROM which may be erased and reloaded using ultraviolet light and a special PROM loader interface. Data constants used by the control program are not stored in the control memories. They are stored in either a high speed 4-word ROM, 24-word ROM or a 256-word 8- or 16-bit semiconductor PROM. This feature allows the data to be easily changed without having to reprogram the control memories.

The program may be started by the front panel start switch or by auto start after power on.

1.2.1 Control

The programmable control section of the PDP16-M generates all control signals that cause data transfers and execute the instructions stored in the control PROMs. It includes a control module, a control memory (expandable to 4), 4 evoke decoders (expandable to 6), and a 30-channel Boolean multiplexer (expandable to 2). The control section also contains a 16-level automatic hardwired subroutine push down stack. The CALL and EXIT instructions control the stack operations.

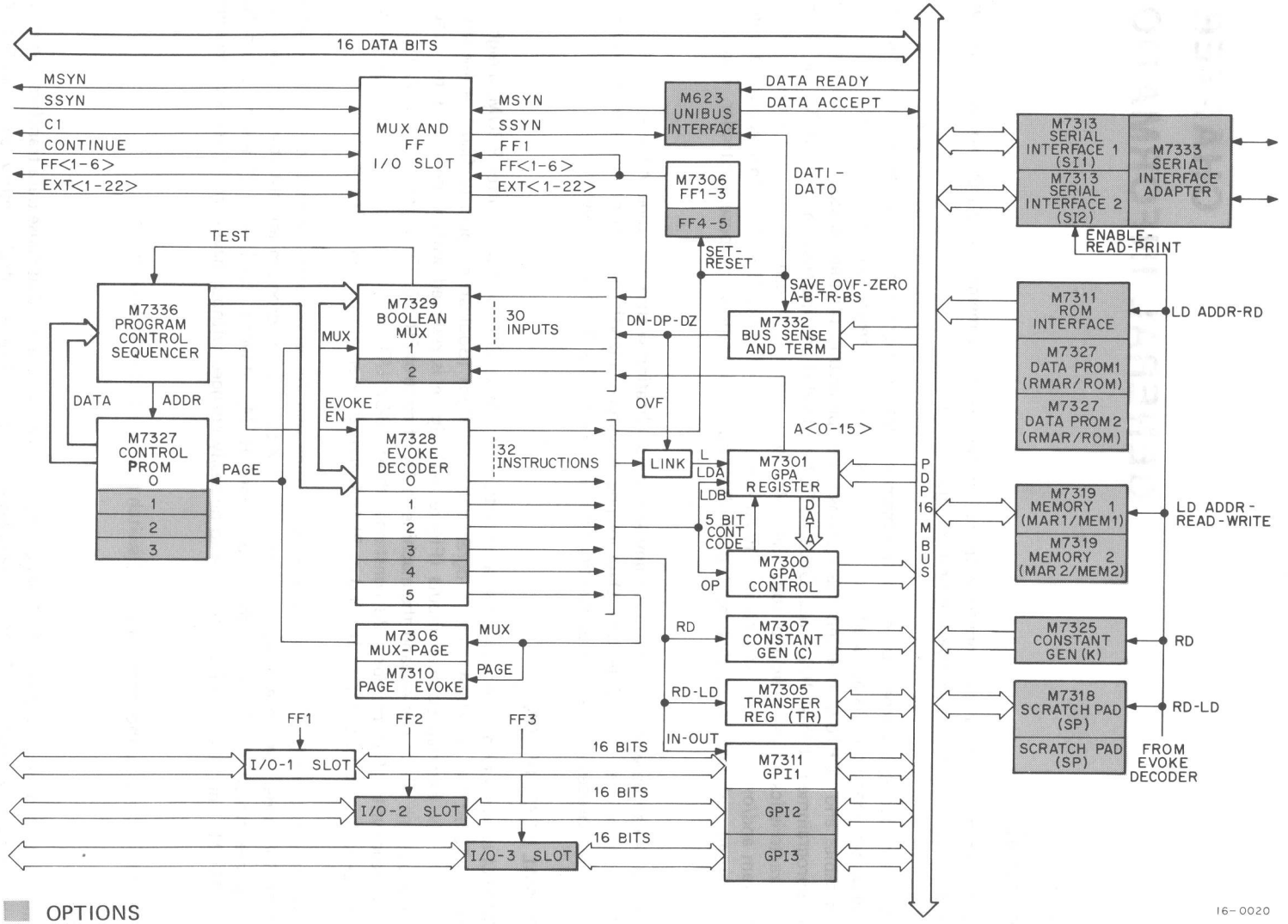


Figure 1-1 PDP16-M Minicomputer, Block Diagram

The control section of the PDP16-M consists of the following modules:

Program Control Sequencer (PCS), M7336

Control PROM, M7327

EVOKE Decoders, M7328

MUX/PAGE Flag Module, M7306

Page Evoke Module, M7310

Boolean Multiplexer, M7329

1.2.1.1 Program Control Sequencer – The M7336 program control sequencer controls the operation and timing of the PDP16-M. It contains the start-stop circuitry, the clock, addressing circuitry, memory request logic, instruction decoder state generator, and evoke enable logic.

1.2.1.2 Control PROM – The M7327 Control PROM stores the control program. One PROM is provided with the basic PDP16-M, while three are optional. A special interface is required to load the control program into the PROM. The PROM may be erased with ultraviolet light and reloaded with a different program.

1.2.1.3 Evoke Decoders – The M7328 Evoke Decoders are used to decode the 8-bit operation codes used in the register transfer instructions. Each decoder will decode 32 instructions. There are six decoders for the 192 instructions. (Two decoders are optional.)

The evoke enable line from the control module allows the selected decoder to generate a control signal for the specified data transfer operation. It will remain asserted until the data operation is completed.

1.2.1.4 Flag (MUX and PAGE) Module – An M7306 Flag Module houses the PAGE flip-flop and the MUX select flip-flop.

The PAGE flip-flop is controlled by the PAGE0 and PAGE1 instructions. It is used to select the upper 512 or lower 512 control memory locations.

The MUX flip-flop is controlled by the MUX0 and MUX1 instructions. It is used to enable one or the other multiplexer for internal or external bit testing, using the IF instruction.

1.2.1.5 Page Evoke Module – The M7310 Evoke Module controls the operation of the PAGE select flip-flop.

1.2.1.6 Boolean Input Multiplexer – The M7329 Boolean Multiplexer serves as a 30-channel input multiplexer for the program control sequencer. It multiplexes external and internal Boolean inputs to be tested in response to the 5-bit operation code used in the conditional and unconditional jump instructions.

1.2.2 Data Processor

The data processor section has a fully implemented 16-bit arithmetic and logic instruction set, a parallel I/O channel, a 4-word data ROM, three programmable flip-flops (Boolean outputs/flags), LINK and six external Boolean inputs. The backplane is prewired to accept a variety of memory and I/O options to allow the basic processor to be expanded as required to fit many different applications.

The processor section of the PDP16-M consists of the following modules:

General Purpose Arithmetic (GPA) Register, M7301

General Purpose Arithmetic (GPA) Control, M7300

LINK (L) flip-flop, M7306

Constant (C) Generator, M7307

Transfer Register (TR), M7305

Boolean Output/Flag (FF1 – FF3) Module, M7306

General Purpose Interface (GPI), M7311

Bus Sense (BS) Module, M7332

1.2.2.1 General Purpose Arithmetic (GPA) Register – The M7301 GPA Register performs arithmetic and logical operations on data in two 16-bit registers designated A and B. The M7301 cannot be used alone; it is only half of a GPA unit. The M7300 GPA control makes up the other half of the GPA unit and must be located in the socket adjacent to the M7301. Control signals are routed from the M7300 to the M7301 by way of an H851 Edge Connector which plugs into the handle end of each unit.

1.2.2.2 General Purpose Arithmetic (GPA) Control – The M7300 GPA control performs the control functions needed to operate the M7301 GPA Register.

1.2.2.3 Link (L) Flip-Flop – The Link flip-flop located in an M7306 Flag Module in slot C9 is connected to the left and right shift inputs (LSI and RSI). (Figure 4-2). When a shift instruction is executed, the link bit is shifted into the vacant bit location. The Link flip-flop is unchanged by the shift operation. The instructions L=1, L=0, L=LNOT, and L=OVF may be used to condition the Link flip-flop.

1.2.2.4 Constant (C) Generator – The M7307 Constant Generator provides a convenient way to store hard-wired constants for a PDP16-M program. Up to four 16-bit constants may be encoded by clipping out jumper wires associated with a diode read-only memory. The constants, normally all 1s and 0s are created by cutting out wires.

1.2.2.5 Transfer Register (TR) – The M7305 Transfer Register is a 16-bit storage register that communicates with the PDP16-M data bus. Command inputs from the evoke decoders load data from the bus to the register, or read data from the register to the bus. The register is divided into lower and upper bytes that can be loaded or read separately (8 bits) or together (16 bits).

1.2.2.6 Boolean Output/Flags (FF1 – FF3) Module – The M7306 module contains three control flip-flops which may be set or cleared under program control. Their outputs are available at the MUX and FF I/O slot for external device control (Boolean output channels) or they may be used as internal 1-bit registers (flags).

1.2.2.7 General Purpose Interface No. 1 (GPI1) – The M7311 General Purpose Interface provides for bidirectional data transfers (parallel I/O) between external equipment and the PDP16-M data bus. The output interface includes a 16-bit register that is loaded by an output command. The register buffers the output data until the next output command. The input interface consists of a gating structure only. An input command samples the input by gating it to the PDP16-M data bus.

1.2.2.8 Bus Sense and Termination Module – The M7332 Bus Sense and Termination Module provides the control for the asynchronous timing circuits; these circuits make all other transfer and flow operations possible. The bus

sense module also terminates the control and data bus. In addition, this unit provides some useful supporting functions. An overflow storage circuit, control switch inputs, a power clear bus output, and detect positive, negative, and zero logic are included in the M7332 Bus Sense and Termination Module.

1.2.3 Memory Options

The PDP16-M is prewired to accept a variety of memory options for data/constant storage. The following memory options can be implemented simply by inserting the option module into its preassigned slot (Paragraph 1.5):

Constant (K) Generator, M7325 (MR16-D)

Data PROM, M7327 (MR16-E)

Scratch Pad (SP) Register, M7318 (MS16-C)

Data R/W MOS Memory (256 words), M7319 (MS16-D)

Data R/W MOS Memory (1024 words), M7324 (MS16-E)

1.2.3.1 Constant Generator MR16-D – The MR16-D Constant Generator provides a convenient way to store hard-wired constants in a PDP16-M. Up to twenty-four 16-bit constants may be encoded by soldering a wire to the appropriate split lug for the constant desired (1–24) at the top of the module. The wire must then be woven through the core of the appropriate bit (1–16) to create a "1." If a "0" is desired, the wire must be woven through the hole of the appropriate bit (1–16).

The module is shipped with a test wire already woven into place. When wiring constants 1–24, care must be taken to pass wires through the cores in the same direction as the test wire.

1.2.3.2 Data PROM MR16-E – This option is implemented by using one or two MR16-E 256-word PROM options. This option provides a convenient way to store 8- or 16-bit data constants such as code conversion tables, text, or numeric data to be used by the program. One MR16-E option will provide 256 8-bit constants; two memories will allow 256 16-bit constants.

The PROM memories are the same type that are used to store the control program. They may be erased with ultraviolet light and reprogrammed using a special interface.

1.2.3.3 Scratch Pad (SP) Register MS16-C – The MS16-C High-Speed SP Register is a 16-word X 16-bit storage register that is organized to operate like 16 independent registers for temporary storage.

Space for two of these options is reserved in the basic machine. An evoke decoder must be added to the PDP16-M for each MS16-C Register option that is implemented. (NOTE: The basic machine has four decoders. Space is provided for a total of six.)

1.2.3.4 Data R/W MOS Memory MS16-D – The MS16-D R/W MOS Memory is a 256-word by 16-bit read/write memory with built-in address and memory buffers. It is interchangeable with the 1024-word R/W MOS Memory (MS16-E) option.

1.2.3.5 Data R/W MOS Memory MS16-E – The MS16-E R/W MOS Memory is a 1024-word by 16-bit read/write memory with built-in address and memory buffers. It is interchangeable with the 256-word R/W MOS Memory option.

1.2.4 I/O Options

The PDP16-M is prewired to accept several additional I/O options. The following I/O options can be implemented simply by inserting the option module into its preassigned slot (Paragraph 1.5).

General Purpose Interface No. 2 (GPI2), M7311 (DB16-A)

General Purpose Interface No. 3 (GPI3), M7311 (DB16-A)

Serial Interface No. 1 (SI1), M7313 (DC16-A)

Serial Interface No. 2 (SI2), M7313 (DC16-A)

Boolean Input Multiplexer 1 (MUX1), M7329 (PCS16-D)

Boolean Output/Flag (FF4 – FF6) Module, M7306 (KFL16)

PDP-11 Peripheral Interface, M623 (DA16-F)

1.2.4.1 General Purpose Interface DB16-A – Two additional 16-bit parallel I/O channels may be added to the basic PDP16-M. Each interface contains a 16-bit flip-flop output register and a 16-bit input register. All inputs and outputs are TTL levels. A separate cable socket is provided for each interface at the rear of the logic assembly.

The DB16-A General Purpose Interface provides for bidirectional data transfers between external equipment and the PDP16-M data bus. The output interface includes a 16-bit register that is loaded by an output command. The register buffers the output data until the next output command. The input interface consists of a gating structure only. An input command samples the input data by gating it to the PDP16-M data bus.

1.2.4.2 Serial Interface DC16-A – The DC16-A Serial Interface allows the PDP16-M to interface with teleprinters and serial data communication lines through the SI Adapter DC16-B option. Two serial I/O channels can be implemented. The DC16-A option contains a transmitter, a receiver, and built-in crystal clock. Data rates available are 110, 150, 300, 600, 1200, and 2400 baud. The number of bits/character can be 5, 6, 7, or 8 and the number of stop bits can be 1 or 2.

Standard 20 mA current loops are available on a connector mounted on the side of the SI Adapter. This connector is compatible with the standard PDP-11 teleprinter. TTL compatible input and output is available on the MUX and FF I/O connector socket.

The TAPE1 or TAPE2 instruction causes one character to be read from the paper tape reader on a teleprinter. To continue reading, more TAPE commands must be issued.

Bit configuration and baud rate are selected by jumpers on the SI Adapter option. Space is reserved in the basic processor for up to two DC16-A Serial Interface options.

1.2.4.3 Boolean Input Multiplexer PCS16-D – The optional multiplexer may be used to expand the number of external inputs from 6 to a total of 22. Bit 0 and 15 of the B Register, the link, and remaining A Register bits may also be tested when this option is implemented.

The power OK level from the power supply is also available for testing by the programmer if ac power fail procedures are necessary.

1.2.4.4 Boolean Output/Flag Module KFL16 – Three additional programmable flip-flops may be implemented in the basic PDP16-M with the KFL16 option. Each flip-flop may be tested by MUX0 and their outputs are available at the MUX and FF I/O socket at the rear of the logic assembly.

1.2.4.5 PDP-11 Peripheral Interface DA16-F – The PDP-11 peripheral interface option provides the necessary logic for interfacing the PDP16-M with a PDP-11 low-speed peripheral device. Three slots on the PDP16-M logic assembly provide the control, address, and data signals required by the peripheral device. Since the PDP-11 I/O connections are distributed between only two slots (double height), a special interface is required. Refer to DA16-F option description for details.

1.2.5 Interfacing Details

1.2.5.1 Peripheral Interface – The basic processor is wired to allow PDP-11 peripherals that do not need to become the master device to be interfaced to the PDP16-M control and data bus. Two instructions, DATI and DATO, allow the PDP16-M to use the peripheral as a slave device. Interfacing requires three cable connections on the PDP16-M.

1. GPI1 cable carries a 16-bit address. Bits 17 and 18 must be hard wired at the controller to +3V.

2. MUX and FF I/O cable carries MSYNC and SSYNC control signals and C1 signal from FF1.

3. The third cable connects the 16-bit PDP16-M data bus to the PDP-11 peripheral data bus.

Cable lengths must not exceed 5 feet and the data bus cable must be terminated with a KTM16 option at the peripheral controller.

For longer distances, a module interface must be constructed to drive the long lines. A maximum of one additional terminator may be added to the PDP16-M data bus.

1.2.5.2 Interface Sockets – All parallel and Boolean I/O are implemented with standard TTL inputs and outputs. All signals are high for assertion. Signals must be buffered with K or M series modules if distances greater than 5 feet are to be driven or received by the interface. Each parallel I/O interface has a cable socket assigned to it at the rear of the logic assembly. The output of one programmable flip-flop is also available at each interface socket to be used for I/O synchronization or control. FF1 is available with GPI1, FF2 with GPI2, and FF3 with GPI3.

The outputs of these three flip-flops as well as FF4, FF5, and FF6 are also available at the MUX and FF I/O socket. The MUX and FF I/O socket is located at the rear of the logic assembly and contains the following signals.

External Inputs: EXT1 through EXT22 are available for inputting Boolean logic levels to be tested by IF instruction in the control program.

MSYNC and SSYNC: PDP-11 control signals MSYNC and SSYNC are available (if option DA16-F is implemented) for the control of PDP-11 low-speed peripherals.

CONTINUE: A low for assertion TTL pulse on this input will continue the program after the last programmed HALT instruction. The front panel START switch will restart the program at location 000 on the current page.

SI1 <SI>, SI2 <SI>: TTL serial inputs for serial interface 1 and 2.

SI1 <SO>, SI2 <SO>: TTL serial outputs for serial interface 1 and 2.

1.2.5.3 DC16-B Serial Interface Adapter – This module is used to define the characteristics of serial interfaces 1 and 2. Lugs are provided for the user to specify the baud rate, stop bits, and data bits for each serial interface. Two Mate-N-Lok plugs are provided on the module to be used to connect standard 20 mA current loop devices such as Teletype, VT05, and LA30 directly to the PDP16-M.

1.3 PHYSICAL DESCRIPTION

The PDP16-M (Figure 1-2) is packaged in a small table-top or rack-mountable cabinet with a self-contained power supply, two cooling fans, an air filter, and a simple front panel.

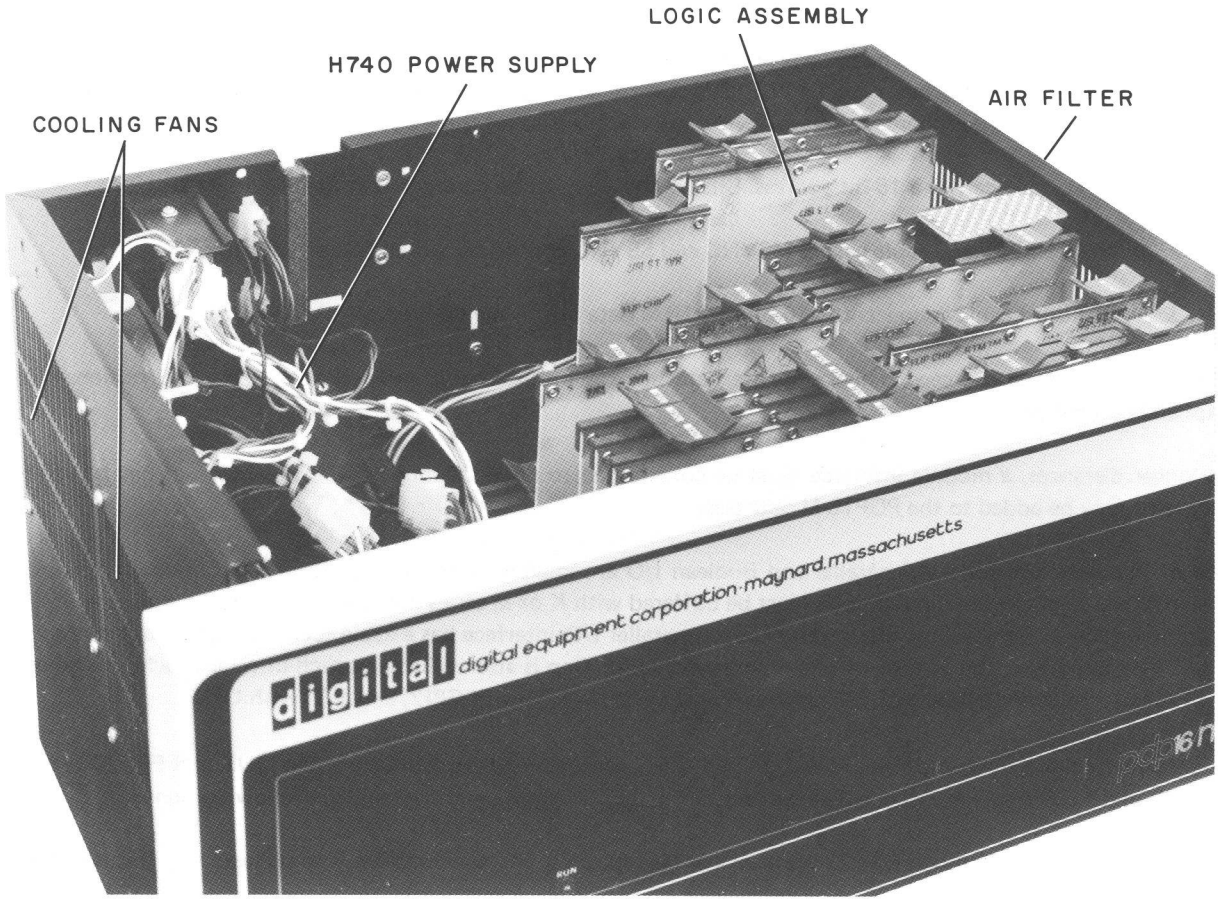


Figure 1-2 PDP16-M Oblique View (top cover removed)

Each slot of the logic assembly has been wired to accept only a specific module type.

CAUTION

Damage may result to the machine if a module is inserted into the wrong slot.

Figure 1-3 and Table 1-1 illustrate the prewired configuration and describe each module of the PDP16-M. Four additional optional modules are available from DEC. These modules are designed to facilitate maintenance and program debugging. Refer to Maintenance Chapter 5 and *PDP16-M Users Guide* for details.

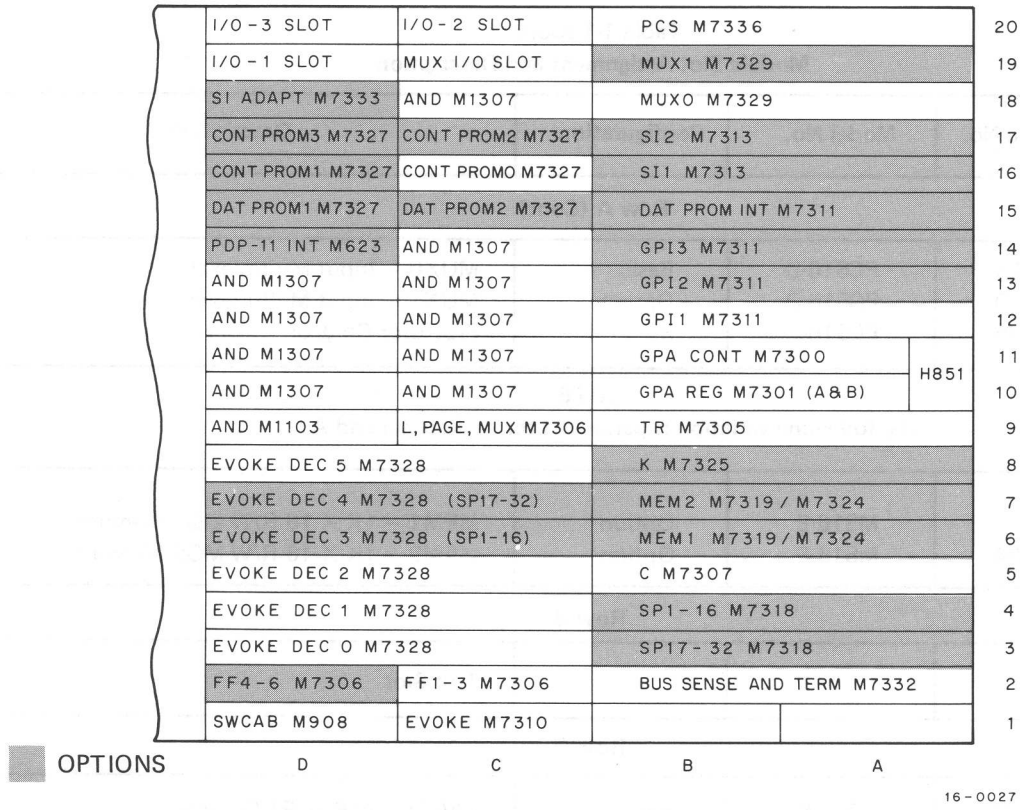


Figure 1-3 Logic Assembly Configuration Diagram

Table 1-1
Module Slot Assignment and Description

Slot	Module No.	Model No.	Configuration	Description
			Row A	
1				Test Slot
2	M7332	KBS16-A	Basic	Timing Control, Data Testing, Bus Terminator
3	M7318	MS16-C	Option	16-Bit Registers, SP17 through SP32
4	M7318	MS16-C	Option	16-Bit Registers, SP1 through SP16
5	M7307	MR16-A	Basic	4-Word Constant Generator
6	M7319	MS16-D	Option	MEM1 – 256 X 16 R/W MOS Memory
7	M7319	MS16-D	Option	MEM2 – 256 X 16 R/W MOS Memory
8	M7325	MR16-D	Option	24-Word Constant Generator
9	M7305	MS16-A	Basic	16-Bit Register with Byte Control
10	M7301	KAR16	Basic	ALU and Registers A and B
11	M7300	KAC16	Basic	ALU Control Unit
12	M7311	DB16-A	Basic	GPI1 – 16-Bit I/O TTL Interface
13	M7311	DB16-A	Option	GPI2 – 16-Bit I/O TTL Interface
14	M7311	DB16-A	Option	GPI3 – 16-Bit I/O TTL Interface
15	M7311	DB16-A	Option	Interface for 8 or 16 X 256 data PROM
16	M7313	DC16-A	Option	SI1 – Asyn Serial I/O Interface
17	M7313	DC16-A	Option	SI2 – Asyn Serial I/O Interface

Table 1-1 (Cont)
Module Slot Assignment and Description

Slot	Module No.	Model No.	Configuration	Description
			Row A (Cont)	
18	M7329	PCS16-D	Basic	MUX0 – Input Multiplexer
19	M7329	PCS16-D	Option	MUX1 – Input Multiplexer
20	M7336	PCS16-E	Basic	Processor Control
			NOTE **The following variation is permitted for sockets A6 and A7.**	
6	M7324	MS16-E	Option	MEM1 – 1K X 16 R/W MOS Memory
7	M7324	MS16-E	Option	MEM2 – 1K X 16 R/W MOS Memory
			Row B	
1				Test Slot
			Row C	
1	M7310	KEV16	Basic	PAGE0 and PAGE1 Control
2	M7306	KFL16	Basic	FF1, FF2 and FF3
3	M7328	PCS16-C	Basic	Evoke Decoder 000–037_8
4	M7328	PCS16-C	Basic	Evoke Decoder 040–077_8
5	M7328	PCS16-C	Basic	Evoke Decoder 100–137_8
6	M7328	PCS16-C	Option	SP1–SP16 Evoke Decoder 140–177_8
7	M7328	PCS16-C	Option	SP17–SP32 Evoke Decoder 200–237_8
8	M7328	PCS16-C	Basic	Evoke Decoder 240–177_8
9	M7306	KFL16	Basic	Link, MUX Select, PAGE Select
10	M1307	KOR16-B	Basic	Control Logic
11	M1307	KOR16-B	Basic	Control Logic
12	M1307	KOR16-B	Basic	Control Logic
13	M1307	KOR16-B	Basic	Control Logic
14	M1307	KOR16-B	Basic	Control Logic
15	M7327	MR16-E	Option	8 X 256 Data PROM (lower 8 bits)
16	M7327	PCS16-B	Basic	Control PROM Loc 0000–0377_8
17	M7327	PCS16-B	Option	Control PROM Loc 1000–1377_8
18	M1307	KOR16-A	Basic	Control Logic
19		I/O Socket	Basic	EXT1–EXT23, FF1–FF6, SI1, SI2, MSYNC and SSYNC
20		I/O Socket	Basic	GPI2 I/O and FF2
			Row D	
1	M908	Panel Socket	Basic	Front Panel and Autostart (SWCAB)
2	M7306	KFL16	Option	FF4, FF5 and FF6
9	M1103	KOR16-A	Basic	Control Logic

Table 1-1 (Cont)
Module Slot Assignment and Description

Slot	Module No.	Model No.	Configuration	Description
			Row D (Cont)	
10	M1307	KOR16-B	Basic	Control Logic
11	M1307	KOR16-B	Basic	Control Logic
12	M1307	KOR16-B	Basic	Control Logic
13	M1307	KOR16-B	Basic	Control Logic
14	M623	DA16-F	Option	PDP-11 MSYNC & SSYNC Interface
15	M7327	MR16-E	Option	8 X 256 Data PROM (upper 8 bits)
16	M7327	PCS16-B	Option	Control PROM Loc $0400-0777_8$
17	M7327	PCS16-B	Option	Control PROM Loc $1400-1777_8$
18	M7333	DC16-B	Option	Serial I/O Interface Adapter
19		I/O Socket	Basic	GPI1 I/O and FF1
20		I/O Socket	Basic	GPI3 I/O and FF3

1.4 SPECIFICATIONS

1.4.1 Processor

Word Length

Control Program:	8 bits
Memory Address:	9 bits (10th bit is programmable)
Program Data:	16 bits

Memory

Programmed Instruction:	256-word reprogrammable control ROM (PROM) – Expandable to 1024 in 256-word increments.
Program Data (Constants):	4-word diode ROM – Expandable by 24 words and/or 256 8- or 16-bit words.
Auxiliary Data Storage:	256 to 2048 words of 16-bit Read/Write MOS memory.

Control PROM

Type:	Electrically alterable quartz window ROM.
Organization:	256 8-bit words
Minimum Prop. Delay:	300 ns
Maximum Prop. Delay:	1 μsec

Voltage Spec:	+5V ± 5% −9V ± 5%
Outputs:	1 TTL unit load drive. Tri-state output or open collector drivers.
Address:	8-bit TTL address. Internally decoded. Two memory select inputs.
Programming:	The semiconductor PROM control memories are programmed by using a special electrical interface. The Quartz Window PROM can be erased with ultraviolet light and reprogrammed at least 100 times.
Scratch Pad Register	1 (byte addressable) — Expandable by 16- or 32-word addressable registers.
Accumulators	1 (A)
Argument Register	1 (B)
I/O Channels	
Flags (Boolean Outputs):	3 — Expandable to 6
Boolean Inputs:	6 — Expandable to 22
Parallel:	1 (PDP-11 Unibus compatible) — Expandable by 2 straight data I/O channels.

NOTE

The three standard flags are available at the channel interface for I/O synchronization.

Serial: 2 (optional)

NOTE

The serial channels will accommodate baud rates of 110, 150, 300, 600, 1200, or 2400; one or two stop bits; and 5, 6, 7, or 8 data bits.

Instructions	Maximum Execution Time	Machine Code
LET:	2.4 μsec	$0–277_8$
GOTO:	3.2 μsec	300_8 and 301_8
IF:	2 μsec if false 3.2 μsec if true	$302_8 – 373_8$
CALL:	3.2 μsec	374_8 and 375_8
EXIT:	3.2 μsec	376_8 or 377_8

NOTE

The LET and EXIT instructions require one 8-bit memory location each and the GOTO, IF, and CALL instructions use two 8-bit locations each; one for the operation code and the other for the jump address. The GOTO and IF instructions are the same electronics with the condition for the GOTO instruction always true.

Bus

Pin Assignments:
(Slots A1–A17)

Bit	Pin	Bit	Pin
0	AA1 (LSB)	8	AK1
1	AB1	9	AL1
2	AC1	10	AM1
3	AD1	11	AN1
4	AE1	12	AP1
5	AF1	13	AR1
6	AH1	14	AS1
7	AJ1	15	AU1 (MSB)

Control	Pin
Overflow	BA1
Power Clear	BB1
Data Accept	BC1
Done	BD1
Data Ready	BE1

Voltage: Logic 1 = 0 to 0.4V
Logic 0 - 3.0 to 4.0V

Current: Logic 1 = 24 to 31 mA with one terminator
Logic 0 = 1.5 to 4.0 mA

1.4.2 Mechanical

Chassis

Dimensions: 19 X 13 X 10.44 inches; 48 X 33 X 26.5 cm

Fans: Two fans exhaust from left side of cabinet. Filter is located on right side of cabinet.

Weight: 55 lb (approx); 25 kg (approx)

Mounting: Chassis slides for rack mounting in standard 19 in. cabinet. Without slides the cabinet may be used as a table-top unit.

Front Panel

Run Light: LED Indicator is on when the program is running.

Power Light: LED Indicator is on when +5V is available from internal power supply.

Start Switch: Initiates program execution.

Panel Lock: Disables the START switch.

1.4.3 Electrical

Primary Power:	PDP16-MA: 115 Vac 47–63 Hz 2A maximum PDP16-MB: 230 Vac 47–63 Hz 1A maximum
H740 Power Supply:	(+5V @ 17A, -15V @ 2A)

1.4.4 Environmental

Temperature:	0 to 60°C ambient
Relative Humidity:	95% maximum (without condensation)
Altitudes:	10K ft; 3000m
Vibration:	1.89G rms overall from 0–70 Hz. Acceleration spectral density – 0.029 G^2/Hz from 10–50 Hz with an approximate 8 dB/octave roll-off from 50 to 70 Hz.

1.5 CONFIGURATION DATA

The basic PDP16-M can be expanded simply by inserting the desired option module into its preassigned slot. To implement some options, some prerequisites to the basic machine are required. These prerequisites, the resident slot in the logic assembly, the module number, the option number and name and the purpose of each option are detailed in Table 1-2.

Table 1-2
Configuration Data

Purpose	Option Name	Option Model No.	Module No.	Slot	Prerequisite
Increase storage for Control program to 512 words	Control PROM 1	PCS16-B	M7327	D16	None
Increase storage for Control program to 768 words	Control PROM 2 or 3	PCS16-B	M7327	C17 or D17	PCS16-B in slot D16

NOTE
If only 768 words are implemented, it is desirable to insert the 3rd control PROM in slot D17 (thereby defining it as the 4th PROM with the 3rd PROM not implemented) to avoid complicated page linking code.

Increase storage for Control program to 1024 words	Control PROM 3	PCS16-B	M7327	D17	PCS16-B in slots D16 and C17
Increase storage for Program Data (constants) from 4 to 28 words	Constant Generator (K)	MR16-D	M7325	AB8	None

Table 1-2 (Cont)
Configuration Data

Purpose	Option Name	Option Model No.	Module No.	Slot	Prerequisite
Increase storage for Program Data (constants) from 4 to 260 words	Data PROM 1 and Data PROM 2	MR16-E MR16-E	M7327 M7327	D15 C15	DB16-A in slot AB15

NOTE

Both Data PROM 1 and 2 must be used if 16-bit data is required. If only 8-bit data is to be stored (such as characters for messages), then only one or the other need be implemented. Both the constant generator (K) and the Data PROMs can be implemented to extend data storage to 288 words.

Increase Scratch Pad Registers from 1 to 17 or 1 to 33	Fast Registers (SP1 to 16)	MS16-C	M7318	AB4	PC16-C in slot CD6
	Fast Registers (SP17 to 32)	MS16-C	M7318	AB3	PCS16-C in slot CD7

NOTE

One Scratch Pad Register, designated the Transfer Register (TR), is implemented in the basic machine. If additional Scratch Pad Registers are required either or both of the above option can be implemented.

Add Read/Write MOS Memory for Aux Data Storage	MEM 1 and 2				
256 words	MEM 1	MS16-D	M7319	AB6	None
512 words	MEM 2	MS16-D	M7319	AB7	MS16-D in slot AB6
1024 words	MEM 1	MS16-E	M7324	AB6	None
1280 words	MEM 2	MS16-D	M7319	AB7	MS16-E in slot AB6
2048 words	MEM 2	MS16-E	M7324	AB7	MS16-E in slot AB6

NOTE

MEM 2 can be implemented without MEM 1. The listing above serves only to illustrate what is required to expand the R/W memory from the minimum through all available sizes to the maximum.

Table 1-2 (Cont)
Configuration Data

Purpose	Option Name	Option Model No.	Module No.	Slot	Prerequisite
Expand Boolean Inputs (EXT) from 6 to 22; or test even bits of A Register, test LSB and MSB of B Register, test LINK or test PWOK using IF instruction	MUX 1	PCS16-D	M7329	AB19	None
Expand flags from 3 to 6	Flags FF4–6	KFL16	M7306	D2	None
Add 2nd Parallel I/O	GPI2	DB16-A	M7311	AB13	None
Add 3rd Parallel I/O	GPI3	DB16-A	M7311	AB14	DB16-A in slot AB13
Add one serial I/O	SI1	DC16-A	M7313	AB16	DC16-B
Add 2nd serial I/O	SI2	DC16-A	M7313	AB16	DC16-A in slot AB16
DATA PROM option Interface	GPI	DB16-A	M7311	AB15	None
Decode EVOKES for SP1–16	EVOKE Decoder	PCS16-C	M7328	CD6	None
Decode EVOKES for SP17–32	EVOKE Decoder	PCS16-C	M7328	CD7	None
Maintenance Configuration	See Maintenance Chapter 5				

CHAPTER 2
INSTALLATION

2.1 GENERAL

Installation of a PDP16-M requires no special tools or equipment. Normal hand tools are all that is necessary.

2.2 UNPACKING

Unpack the equipment, using the following procedure.

1. Remove the shipping straps.
2. Open the outer carton.
3. Lift out the inner carton.
4. Open the inner carton.
5. Slide the computer out, using care not to damage the switch.
6. Check that all equipment is included, as specified on the inventory checklist.
7. Install the chassis slides using the hardware, if necessary.

2.3 INSPECTION

After removing the equipment packing material, inspect the equipment.

1. Inspect the external surfaces of the chassis for surface, bezel, switch, and light damage, etc.
2. Internally inspect the cabinet for console and processor damage; loose or broken modules; fan damage, loose nuts, bolts, screws, etc.
3. Inventory all hardware against key sheet.
4. Inventory all prints against drawing directory.

2.4 INSTALLATION PROCEDURE

Install the equipment, using the following procedure.

1. Turn off power switch. Do not plug in the PDP16-M until step 4 of this procedure.

WARNING

Do not touch the computer after plugging in power until the computer is checked for proper ground.

2. Ensure that all ac power is received from the same source, if the PDP16-M is a part of a system.

3. Disconnect the dc harness at the rear of the logic assembly.

WARNING

Ensure that lugs on end of dc harness are not touching anything.

4. Plug in power.

5. Before touching the computer, check frame to ground voltage.

6. Unplug power.

7. Turn on computer power key switch and push the circuit breaker on the rear panel.

8. Repeat steps 4 and 5.

9. Check that the dc voltages at the dc harness are in accordance with those specified in Table 2-1.

Table 2-1
DC Voltages

Wire (Color)	Voltage (dc)
Red	+4.8 to 5.2 Vdc
Blue	-14.5 to -15.5 Vdc
Gray	+2.8 to 5.5 Vdc
Blk	Ground
Orn	+1.0 to 2.0 Vdc

10. Turn off power

11. Connect the dc harness at the rear of the logic assembly.

12. If the AUTO RUN option is desired, install a jumper between pins D01S1 and D01U1 on module M908. This jumper should not be installed to start the machine using the START switch.

13. Check that modules are in their assigned slot in accordance with Table 1-1.

WARNING

Sockets have been preassigned for all options. Modules may be damaged if inserted into the wrong socket. (Figures 1-3 and 5-7).

2.5 CHECKOUT PROCEDURE

2.5.1 Equipment Required

1 set PDP16-M Diagnostic PROMs

Basic Test PROMS

PROM 2: M7327 YC
PROM 3: M7327 YD

Option Test ROMS

PROM 0: M7327 YA
PROM 1: M7327 YB

1 – KBM16 Bus Monitor (M7322)
1 – KSM16 Service Module (M7335)
1 – KSL16 Option Switch Module (M7334)
2 – Extender Cables (7007222)
2 – Extender Module (Double Height) W984

NOTE

The jumpers for the following modules and plugs must be installed by the user. Refer to Appendix B for details.

2 – Mate-N-Lok jumper plugs
1 – Interface Jumper Module 1 (W971)
1 – Interface Jumper Module 2 (W971)

2.5.2 Procedures

1. Install Diagnostic PROMs 0, 1, 2 and 3 in sockets C16, D16, C17, and D17, respectively.

2. Plug in KBM16 Bus Monitor M7322 in socket A01 and KSM16 Service Module M7335 in socket B01. Both modules should be on 7007222 extender cables. Insert Mate-N-Lok serial I/O jumper plugs in module M7333 located in slot D18.

3. Install W971 Interface Jumper Module 1 in socket CD19 and W971 Interface Jumper Module 2 in CD20. Set SI and BP switches on service module to OFF position.

4. Turn on power. Check the power light for ON condition.

5. If autostart jumper is installed, proceed to step 9.

6. Check RUN light for OFF condition, and DATA READY and DATA ACCEPT lights on Bus Monitor for ON condition.

7. Turn panel switch to panel lock position, push START switch, and check RUN light for OFF condition.

8. Turn panel switch to ON position and push START switch.

9. Check RUN light for ON condition. The basic diagnostic should be running. If the program halts, refer to Chapter 5 for service information.

10. Perform the acceptance test for the basic PDP16-M for 30 minutes. If abnormal conditions are encountered, the program will halt with the RUN light off. Refer to Chapter 5 for maintenance information if required.

11. Turn off power and replace the M7311 module in location AB12 with the KSL16 option switch module M7334 on the extender module.

12. Refer to Table 2-2 and set the switch on the M7334 module to select the option to be tested. Only one switch may be selected at a time.

13. Turn on power and push START. Run the diagnostic for the time period indicated in Table 2-2.

14. Turn off power.

15. Repeat steps 12 and 13, selecting a different option switch until all implemented options have been tested.

NOTE

If no switch is selected, the basic diagnostic will be executed. This will result in a false error indication because the M7311 in socket A12 has been replaced by the M7334 option switch module.

Table 2-2
Diagnostic Option Select Switches

Switch	Option	Slot No.	Module Tested	Run Mode	Symptoms of Correct Operations	Option Acpt Time
0	DB16-A	AB13	M7311	Single Step & Auto	Using single step, watch the bus monitor up count the data bus to a count of (10_8). Put into Auto Run and watch up count. Runs until error or power down.	1 min.
1	DB16-A	AB14	M7311	Single Step & Auto	Same as switch 0. Up count starts at 2_8.	1 min.
2 & 15	DB16-A	A15 C/D15	M7311 M7327 M7327	Auto	RUN light OFF. Proper data displayed in the light register on the M7334 module. Press START switch to display next location. 257th push displays checksum. Push again for high speed checksum. Check for equal.	Check all 256 locations.

Table 2-2 (Cont)
Diagnostic Option Select Switches

Switch	Option	Slot No.	Module Tested	Run Mode	Symptoms of Correct Operations	Option Acpt Time
3	MR16-D	AB8	M7325	Single Step	Each constant will be displayed in the M7322 Bus Monitor. Refer to diagnostic listing for program operation. Checksum displayed in M7334 at end of test.	Check each const. (NOTE): ALL constants must be wired.
4	MS16-D	A6	M7319	Auto	RUN light ON. Bus monitor lights - all on and flickering.	5 min.
5	MS16-E	A7	M7324	Auto	RUN light ON. Same as switch 4.	5 min.
6	MS16-C	A4	M7318	Auto	RUN light ON. Shows an up count in the bus monitor.	5 min.
7	MS16-C	A3	M7318	Auto	Same as switch 6.	5 min.
8	DC16-A	A16	M7313	Auto	RUN light OFF and 400_8 is displayed in the light switch register (M7334) after the program halts in loc 0313. Test shows an up count to 400_8 in the bus monitor M7322.	10 times
9	DC16-A	A17	M7313	Auto	Same as switch 8.	10 times
10	KFL16	D2	M7306	Auto	RUN light ON and bits 4 and 5 are on the bus monitor. 177777 displayed in the lights on M7334.	1 min.
11	–	–	–	–	Not used.	–
12	DATI & DATO	D14	M623	Single Step & Auto	RUN light is ON and all data lights in the bus monitor are ON. Single step until the data bus seems to complement.	1 min.
13–14	–	–	–	–	Not used.	–
15					Used with switch 2.	

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 CONTROLS AND INDICATORS

Once started, the PDP16-M will be under complete control of the program stored in the control PROM. The operator cannot intervene except to stop the machine by turning the power off. Therefore, an elaborate front panel is not required. The front panel of the PDP16-M houses only a power key switch, a POWER indicator, a START switch, and a RUN light. A pushbutton circuit breaker is located on the rear panel of the PDP16-M.

The PDP16-M can be started automatically upon power up or manually by depressing the START switch. A jumper must be installed/removed to select one or the other start method (see Installation Chapter, Paragraph 2.4).

3.2 INSTRUCTION FORMAT

There are five basic types of instructions in the PDP16-M. They are:

LET	Used for Arithmetic/Logical operations and Data Transfers
GOTO	Unconditional Jump
IF	Conditional Jump
CALL	Jump to Subroutine on Same Page
EXIT	Return from Subroutine on Same Page

The LET and EXIT instructions each require one 8-bit memory location and the GOTO, IF, and CALL instructions use two 8-bit locations each (Figure 3-1). The GOTO and IF instructions use the same electronics with the condition for the GOTO instruction always true.

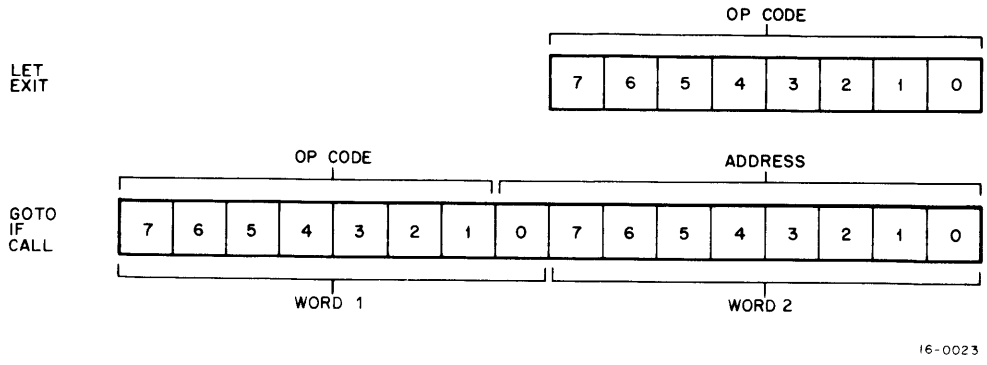


Figure 3-1 Instruction Format

3.2.1 LET Instruction

Codes: 0 to 277_8

Each data operation that the PDP16-M is capable of performing has been assigned an 8-bit machine code. These codes (object codes) are stored in the control PROM and are decoded by the instruction and evoke decoders in the control section and executed by the data section as 16-bit operations.

Control signals from the evoke decoders are wired to the control inputs (source and destination registers) of the data sections to implement the instruction set of the machine.

Examples:

```
LET   A = 0          /Clear the A Register
LET   A = A + 1      /Increment the A Register
LET   B = C1         /Load the B Register with constant 1
LET   A = A + B      /Add A and B together
LET   TR = A         /Save results in Transfer Register
```

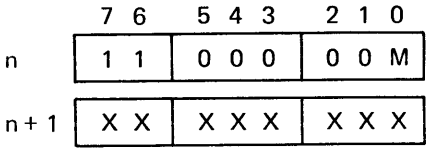
NOTE

The assembler will allow the word "LET" to be used optionally by the programmer.

3.2.2 GOTO Instruction

Codes: 300_8 and 301_8

Address: $0–377_8$

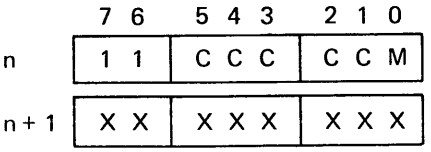


Bit M and the 8 bits in the next PROM location (n + 1) form a 9-bit address for a location on the current page. The next instruction executed will be at the specified address.

3.2.3 IF Instruction

Codes: 302_8 to 373_8

Address: $0–377_8$



CCCCC: MUX Channel codes 1 to 35_8

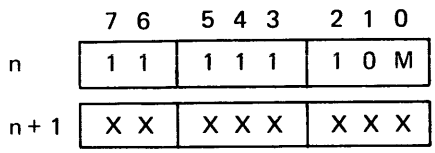
Bit M and the 8 bits in the next PROM location (n + 1) form a 9-bit address for a location on the current page.

The next instruction executed will be at the specified address if the condition tested is true, otherwise the next sequential instruction (n + 2) will be fetched.

3.2.4 CALL Instruction

Codes: 374_8 and 375_8

Address: $0–377_8$



Bit M and 8 bits in the next PROM location (n + 1) form a 9-bit address for a location on the current page. The next instruction will be at the specified address and the 9-bit return address will be saved in the 16-level hardware pushdown stack.

3.2.5 EXIT Instruction

Code: 376_8 or 377_8

7 6	5 4 3	2 1 0
1 1	1 1 1	1 1 1

The next instruction executed will be at the 9-bit address specified at the top of the subroutine pushdown stack. The return point will be on the same page as the EXIT instruction.

3.3 BASIC INSTRUCTION SET

Only the basic instruction set is discussed in this chapter. Instructions implemented through options are discussed in the option description. The following paragraphs define the octal machine code, execution time in microseconds, instruction mnemonic, and description of all the instructions implemented in the basic machine.

3.3.1 Arithmetic Group

All arithmetic operations are executed by the General Purpose Arithmetic (GPA) Control (M7300) and Registers (M7301). The following arithmetic operations have been implemented in the basic PDP16-M:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
000	2.4	A = 0	Clear A
001	2.4	A = B	A gets B
002	2.4	A = A + 1	Increment A
003	2.4	A = A - 1	Decrement A
004	2.4	A = A + B	A gets A + B
005	2.4	A = A - B	A gets A - B
012	2.4	A = A/2	A gets A/2 (shift right)
013	2.4	A = AX2	A gets AX2 (shift left)
014	2.4	A = A + 1(S)	Same as above except overflow (OVF) bit is saved so it can be tested.
015	2.4	A = A - 1(S)	
016	2.4	A = A + B(S)	
017	2.4	A = A - B(S)	
020	2.4	A = A/2(S)	
021	2.4	A = AX2(S)	
022	2.4	B = 0	Clear B
023	2.4	B = A	B gets A
024	2.4	B = A + B	B gets A + B
025	2.4	B = A - B	B gets A - B
032	2.4	B = B/2	B gets B/2 (shift left)
033	2.4	B = A + B(S)	B gets A + B and save OVF
034	2.4	B = A - B(S)	B gets A - B and save OVF
035	2.4	B = B/2(S)	B gets B/2 (shift right) and save OVF
074	1.8	L = 0	Reset LINK
075	1.8	L = 1	Set LINK
257	2.4	B = A + 1	B gets A incremented
260	2.4	B = A + 1(S)	B gets A incremented with OVF saved
261	2.4	B = A - 1	B gets A decremented
262	2.4	B = A - 1(S)	B gets A decremented with OVF saved
263	2.4	B = AX2	B gets AX2 (shift left)
264	2.4	B = AX2(S)	B gets AX2 (shift left) and save OVF
265	2.4	B = A/2	B gets A/2 (shift right)
266	2.4	B = A/2(S)	B gets A/2 (shift right) and save OVF

Evoke (Octal Code)	Time (μsec)	Instruction	Description
267	1.8	L = OVF	LINK gets OVF
270	1.8	L = LNOT	Complement LINK
272	2.4	A = B/2	A gets B/2 (shift right)
273	2.4	A = B/2(S)	A gets B/2 (shift right) and save OVF

NOTE

The Destination Register overflow bit is saved when the instructions suffixed with (S) are executed. This bit (OVF) can then be tested using the conditional test instruction (Paragraph 3.3.8).

3.3.2 Logical Group

All logical operations are also executed by the General Purpose Arithmetic (GPA) Control (M7300) and Registers (M7301). The following logical operations have been implemented in the basic PDP16-M.

Evoke (Octal Code)	Time (μsec)	Instruction	Description
006	2.4	A = AXORB	A gets A ∀ B
007	2.4	A = AORB	A gets A V B
010	2.4	A = AB	A gets A ∧ B
011	2.4	A = ANOT	Complement A
026	2.4	B = AXORB	B gets A ∀ B
027	2.4	B = AORB	B gets A V B
030	2.4	B = AB	B gets A ∧ B
031	2.4	B = BNOT	Complement B

3.3.3 Register Group

The A Register of the GPA and the Transfer Register module (M7305) are involved in executing these instructions. The following register instructions have been implemented in the basic PDP16-M:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
130	2.3	TR = A	Transfer Register gets A
131	2.1	A = TRU	A upper gets upper byte of TR A lower = 0
132	2.1	A = TRL	A lower gets lower byte of TR A upper = 0
133	2.1	A = TR	A gets Transfer Register
250	2.0	TR = 0	Clear Transfer Register
276	2.3	TRU = A	Transfer Register upper gets upper byte of A
277	2.3	TRL = A	Transfer Register lower gets lower byte of A

3.3.4 Constant Generator Group

The B Register of the GPA and the Constant Generator module (M7307) are involved in executing these instructions. The following constant instructions have been implemented in the basic PDP16-M:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
046	2.4	B = C1	B gets Data constant 1
047	2.4	B = C2	B gets Data constant 2
136	2.4	B = C3	B gets Data constant 3
137	2.4	B = C4	B gets Data constant 4

3.3.5 I/O Group

The basic PDP16-M is equipped to handle Boolean inputs, Boolean outputs, and 16-bit parallel I/O. Optionally, two serial I/O channels and two additional parallel I/O channels can be added. Conditional jump instructions are implemented for the Boolean input channels (Paragraph 3.3.8). The Boolean output channels can also serve as program flags. Module M7306 contains the three flip-flops that serve as the flags and the source of the Boolean output channels. As for the parallel I/O channel, both registers of the GPA (A and B Registers) and the General Purpose Interface module (M7311) are involved in executing the parallel I/O channel instructions. The following I/O instructions for the Boolean output channels/flags and the parallel I/O channels have been implemented in the basic PDP16-M:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
040	2.2	GPI1 = A	GPI1 gets A (Data out)
041	2.0	A = GPI1	A gets GPI1 (Data in)
056	1.8	FF1 = 0	Reset Flag 1
057	1.8	FF1 = 1	Set Flag 1
060	1.8	FF2 = 0	Reset Flag 2
061	1.8	FF2 = 1	Set Flag 2
062	1.8	FF3 = 0	Reset Flag 3
063	1.8	FF3 = 1	Set Flag 3
255	2.2	GPI1 = B	GPI1 gets B (Data out)
256	2.0	B = GPI1	B gets GPI1 (Data in)

Conditional Jump instructions are also implemented in the basic PDP16-M for testing the Boolean output channels and for testing the odd bits of the A Register (Paragraph 3.3.8). Option PCS16-D (Boolean input multiplexer option) can be installed to implement additional conditional jump instructions for testing the even bits of the A Register and the MSB and LSB of the B Register. Installing this option also implements conditional jump instructions for testing the LINK bit and the power OK signal.

3.3.6 Command Group

The command instruction group facilitates the switching of control memory pages, switching Boolean input multiplexers and stopping the program. The instructions for switching pages and multiplexers serve their function only if more than two control PROMs and/or the optional Boolean input multiplexer have been implemented. The command instructions are:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
072	1.8	PAGE 0	Get next instruction from PAGE 0
073	1.8	PAGE 1	Get next instruction from PAGE 1
076	1.8	MUX0	Select test group 0 for IF instruction
077	1.8	MUX1	Select test group 1 for IF instruction
271	–	HALT	Stops program

3.3.7 Test Group

Any time data is transferred via the PDP16-M data bus, a test for positive, negative, or zero data is automatically performed. The result is stored in one of three registers (DP, DN and DZ) in the M7332 Bus Sense and Termination Module. One of three conditional jump instructions can then be programmed (Paragraph 3.3.8) to jump to another part of the program based on the stored test result. Some register-transfer instructions do not transfer data on the bus and therefore the result from the previous test is cleared since no data (zero data) is on the bus. To facilitate retesting the contents of the A or B Register for a subsequent conditional jump, the following two test instructions have been implemented in the basic PDP16-M:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
036	2.4	EXA	Examine A and set DP, DN, or DZ
037	2.4	EXB	Examine B and set DP, DN, or DZ

3.3.8 Conditional Jump Group

The GOTO and IF instructions are considered to be conditional jump instructions in the PDP16-M. A 30-channel Boolean input multiplexer is employed to provide the condition to be tested in response to the object code (machine code) of the programmed jump instruction. The GOTO instruction selects channel 00 of the multiplexer. This channel is connected to +3V and therefore the GOTO instruction will always cause a jump resulting in an unconditional jump. The other channels of the multiplexer are connected to internal and external Boolean conditions. These conditions may be true or not true. The program control sequencer (M7336) performs the test for true or not true to determine which program sequence to execute. The following conditional jump instructions have been implemented in the basic PDP16-M:

Machine Code (Octal)*		Time (μsec)		Instruction	Description
MEM0	MEM1	False	True		
300	301	2.0	3.2	GO TO	Test channel 0 input (+3V)
302	303	2.0	3.2	IF EXT1, LABEL	Test channel 1 input (EXT1)
304	305	2.0	3.2	IF EXT2, LABEL	Test channel 2 input (EXT2)
306	307	2.0	3.2	IF EXT3, LABEL	Test channel 3 input (EXT3)
310	311	2.0	3.2	IF EXT4, LABEL	Test channel 4 input (EXT4)
312	313	2.0	3.2	IF EXT5, LABEL	Test channel 5 input (EXT5)
314	315	2.0	3.2	IF EXT6, LABEL	Test channel 6 input (EXT6)
316	317	2.0	3.2	IF DZ, LABEL	Test channel 7 input (DZ)
320	321	2.0	3.2	IF DP, LABEL	Test channel 8 input (DP)
322	323	2.0	3.2	IF DN, LABEL	Test channel 9 input (DN)

Machine Code (Octal)*		Time (μsec)		Instruction	Description
MEM0	MEM1	True	False		
324	325	2.0	3.2	IF OVF, LABEL	Test channel 10 input (OVF)
326	327	2.0	3.2	IF A<1>, LABEL	Test channel 11 input (A<1>)
330	331	2.0	3.2	IF A<3>, LABEL	Test channel 12 input (A<3>)
332	333	2.0	3.2	IF A<5>, LABEL	Test channel 13 input (A<5>)
334	335	2.0	3.2	IF A<7>, LABEL	Test channel 14 input (A<7>)
336	337	2.0	3.2	IF A<9>, LABEL	Test channel 15 input (A<9>)
340	341	2.0	3.2	IF A<11>, LABEL	Test channel 16 input (A<11>)
342	343	2.0	3.2	IF A<13>, LABEL	Test channel 17 input (A<13>)
344	345	2.0	3.2	IF A<15>, LABEL	Test channel 18 input (A<15>)
346	347	2.0	3.2	IF FF1, LABEL	Test channel 19 input (FF1)
350	351	2.0	3.2	IF FF2, LABEL	Test channel 20 input (FF2)
352	353	2.0	3.2	IF FF3, LABEL	Test channel 21 input (FF3)
354	355	2.0	3.2	IF FF4, LABEL	Test channel 22 input (FF4)
356	357	2.0	3.2	IF FF5, LABEL	Test channel 23 input (FF5)
360	361	2.0	3.2	IF FF6, LABEL	Test channel 24 input (FF6)
362	363	2.0	3.2	IF KF1, LABEL	Test channel 25 input (KF1)
364	365	2.0	3.2	IF PF1, LABEL	Test channel 26 input (PF1)
366	367	2.0	3.2	IF KF2, LABEL	Test channel 27 input (KF2)
370	371	2.0	3.2	IF PF2, LABEL	Test channel 28 input (PF2)
372	373	2.0	3.2	IF CLK, LABEL	Test channel 29 input (clock)

*Codes are given for jumps into or within memory 1 and into or within memory 2. The least significant bit of the machine code is in M (memory) bit.

3.3.9 Subroutine Group

The hardware stack in the program control sequencer (M7336) automatically keeps track of the return address when a subroutine is called. Sixteen return addresses can be stored in the stack. Therefore, up to sixteen subroutines can be called before returning to the main program. The following instructions have been implemented in the basic PDP16-M to facilitate jumping to and returning from subroutines:

Machine Code (Octal)	Time (μsec)	Instruction	Description
374	3.2	CALL LABEL	Jump to a subroutine in memory 0 of the current page
375	3.2	CALL LABEL	Jump to a subroutine in memory 1 of the current page
377	3.2	EXIT	Return from a subroutine

3.4 A AND B REGISTERS

The A and B Registers are used to perform arithmetic and logical operations (Paragraph 3.3) on 16-bit data. Program data is *not* stored in the control PROM but in separate Constant or Data ROMs. The A Register is the accumulator and the B Register is the argument register. The status of bits 1, 3, 5, 7, 9, 11, 13 and 15 of the A Register can be tested with the IF instruction if MUX0 is selected. When the MUX1 option is implemented, the remaining bits of the

A Register and bits 0 (LSB) and 15 (MSB) of the B Register can also be tested with the IF instruction by declaring MUX1 in the program. An example of how to write the IF instruction for the A and B Registers follows:

```
        IF A<3>, TRUE
        Instruction for false condition        /A<3> is logic 0
              .
              .
              .
              .
              .
TRUE    Instruction for true condition         /A<3> is logic 1
```

Notice that a comma separates (delimits) the MUX condition (A<3>) to be tested and the program label (TRUE), and a space (or tab) separates the instruction word (IF) and the MUX condition (A<3>).

3.5 LINK (OVERFLOW)

The Link bit is connected to the left and right shift inputs of the A and B Registers. It is affected only by the four Link instructions:

```
L = 0          /Clear Link
L = 1          /Set Link to Logic "1"
L = LNOT       /Complement Link
L = OVF        /Set Link Equal to Overflow
```

The Link is set to zero during power on. Its state may be tested by an IF instruction if the MUX1 option is implemented, and MUX1 is declared in the source program. Refer to PCS16-D option description in Appendix A.

3.6 BOOLEAN I/O

Three programmable control flip-flops (FF1 – FF3) and six external Boolean inputs (EXT1 – EXT6) are provided in the basic PDP16-M. Space is reserved for expansion to 6 programmable flip-flops and 22 external inputs. These inputs and outputs may be used for I/O synchronization or for testing external TTL logic levels under program control. All signals are available through the MUX and FF I/O socket located at the rear of the logic assembly.

Each input presents one TTL unit load and each flip-flop output can drive seven TTL unit loads.

These inputs and outputs are unbuffered TTL logic levels. If distances greater than five feet are to be driven and received, it will be necessary to use a K or M series module interface to buffer the signals. Refer to the DIGITAL Control and Logic Handbooks (C110 and C105).

3.7 GPI1 (GENERAL PURPOSE INTERFACE) – PARALLEL I/O

The basic PDP16-M contains one 16-bit parallel I/O interface designated GPI1. Space is reserved on the data bus for two additional parallel I/O options. The interface consists of a 16-bit flip-flop output register and 16 input gates for placing external data on the PDP16-M bus under program control. Flags FF1 – FF3 are available at the interface of GPI1 – GPI3, respectively, for use in I/O synchronization.

Once data is loaded into the output register, it will remain unchanged until the next time data is transferred to the interface. The output register is set to zero during power on.

3.8 CONSTANT GENERATOR (C)

The basic PDP16-M contains a ROM Constant Generator (C) capable of storing four 16-bit data constants. Since data constants that may be required for the program cannot be stored in the control PROM, the constant generator is included in the basic machine to store these constants.

3.9 TRANSFER REGISTER (TR)

The Transfer Register is a byte addressable Read-Write General Register for manipulating data or for temporarily storing results.

3.10 BUS SENSE AND TERMINATOR

The bus sense and terminator module contains three 1-bit registers (DP, DN, and DZ), the bus terminator, and some timing logic. Every time a data transfer is evoked, a test for positive, negative, and zero is automatically performed and the result is automatically stored in one of the three 1-bit registers. Since no data is transferred on the bus when a FF, PAGE, MUX, LINK, or HALT instruction is executed, the bus is zero and the DZ Register will then be set. The EXA and EXB instructions are therefore provided to permit the previous data transfer to be re-examined for a subsequent conditional jump (IF DP, LABEL).

For example:

```
          LET A = A + 1                    /A is incremented
          MUX0                             /MUX0 is selected
          EXA                              /A Register is retested for DP, DN, or DZ
          IF DP, POSITIVE
          Instruction for not positive condition
POSITIVE  Instruction for positive condition
```

3.11 MUX SELECTION

NOTE

This feature of the PDP16-M applies only to those machines that have the MUX1 option (PCS16-D) implemented.

The instructions MUX0 and MUX1 are used to select the input multiplexer to be used for executing the IF instruction. Channel 0 (instruction code 300_8 and 301_8) on both multiplexers are hard wired to +3V for the GOTO instruction. Once a multiplexer is selected, it will remain selected until the other multiplexer is specified by a MUX0 or MUX1 instruction. The MUX0 and MUX1 instructions also zero the bus. Therefore, a detect zero (DZ) conditional jump instruction (IF DZ, LABEL) will always be true if it is preceded by a MUX instruction.

For example:

```
MUX1                    /change multiplexer
IF DZ, LABEL            /this test will be true
```

NOTE

At the time the PDP16-M is turned on, MUX0 is selected and remains selected until a MUX1 command is executed.

3.12 PAGE SELECTION

NOTE

This feature of the PDP16-M applies only to those machines that have more than two control PROMs (>512 words) implemented. At the time the PDP16-M is turned on, PAGE0 is selected and remains selected until a PAGE1 command is executed.

The 1024 X 8 control memory (maximum that can be implemented) is divided into two pages with 512 locations on each page. Any location within a page, can be directly addressed, however, locations in the other page are not directly addressable. Two instructions, PAGE0 and PAGE1, are used to control the PAGE select flip-flop to switch from one page of instructions to the other.

When the paging instructions are used, the next instruction executed will be in the page requested at an address one greater than the address of the instruction.

Instructions cannot be sequentially executed from one page to the next. The next location after the last location on the page is the first location on the same page.

The page instructions also zeros the bus. Therefore, a detect zero (DZ) instruction will always be true if it is preceded by a page instruction. (See Paragraph 3.10 for example.)

3.13 PAGE LINKAGES

The programmer must write some code (page linkages) for switching pages and calling subroutines on the other page This code is illustrated in examples A and B that follow:

A. Switching Pages

1. The program will start at Location 0 in Page 0 and run until it reaches the GOTO P1 instruction.

2. At label P1 (location 775), Page 1 will be selected and the next instruction will be fetched from location 1776. This will cause a jump to the location labeled XYZ in Page 1.

3. The program will run until it reaches the GOTO P0 instruction.

4. At label P0 (location 1775), Page 0 will be selected and the next instruction will be fetched from location 776. This will cause a jump to the location labeled ABC in Page 0.

```
0000                .
                    .
                    .
                    GOTO P1
          ABC       .
                    .
                    HALT

                    ORG 0775
0775      P1        PAGE1
0776                GOTO ABC
0777
```

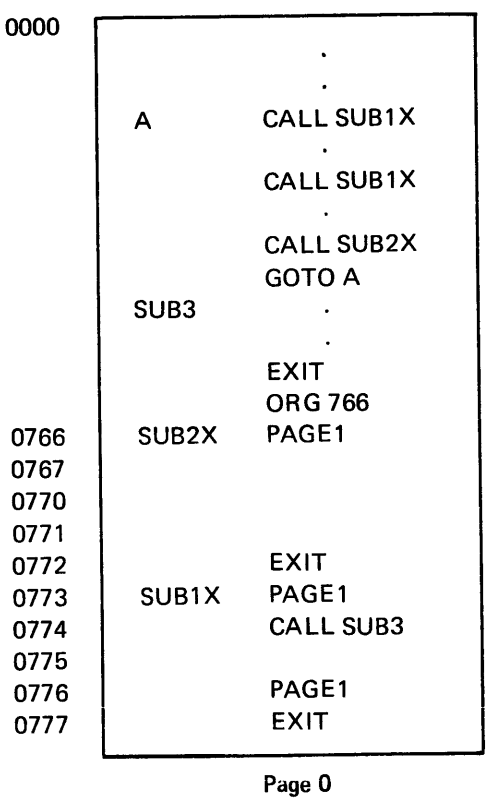
Page 0

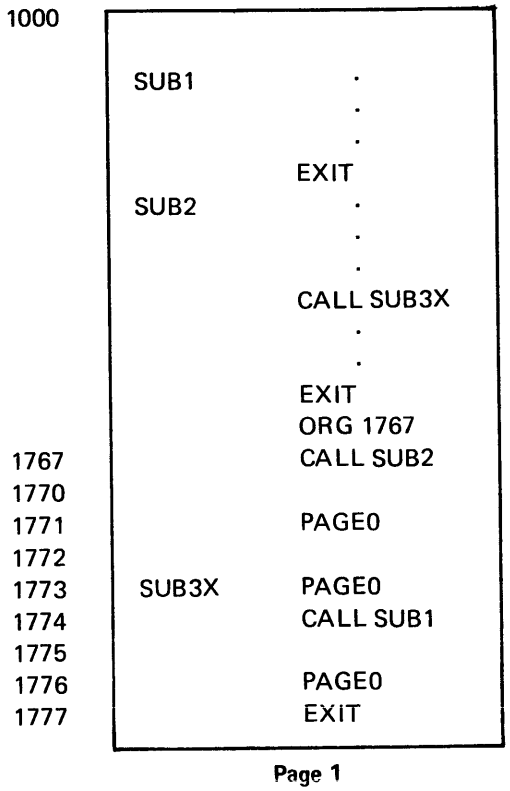
```
1000
          XYZ       .
                    .
                    .
                    GOTO P0

                    ORG 1775
1775      P0        PAGE0
1776                GOTO XYZ
1777
```

Page 1

B. Calling Subroutines on the other Page





1. Call SUB1 on Page 1 from Page 0 twice.
2. Call SUB2 on Page 1 from Page 0.
3. SUB2 calls SUB3 on Page 0.
4. Repeat.

Notes For Examples A and B:

1. Use origin statement (ORG n) to position linkage. For example, the statement following ORG 177_8 will be stored in location 200_8.
2. No linkage is required in calling subroutines on the same page.
3. Remember that the next instruction that is executed after a PAGE instruction will be that instruction which appears in the next sequential location on the specified page.
4. GOTO, conditional jumps (IF), CALLs and EXITs cannot jump across page boundary. The PAGE0 and PAGE1 instruction must be used for this purpose.

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

Two types of instructions are implemented in the PDP16-M:

Evoke Data Transfer
Jump (Control)

A data transfer between the PDP16-M data modules is evoked by any of the following instructions/commands involving the specified data module registers.

Instructions (LET)

Arithmetic and Logical Set

A Register
B Register
L (LINK)

Boolean Set

FF1
FF2
FF3

Data Memory Set

TR Register
C Constant Generator

I/O Set

GPI1

Commands

PAGE0, PAGE1
MUX0, MUX1
HALT

The 192 data transfer instructions are assigned octal codes 0–277. Individual evoke signals are produced by the evoke decoders in response to these codes. The transfer is made between a module Source Register and a module Destination Register via a 16-bit data bus (Figure 4-1). A 5-line control bus carries DATA READY, DATA ACCEPT, and DONE timing signals to ensure proper interlock for all data transfers. The control bus also carries the POWER CLEAR signal and the OVERFLOW (OVF) bit. All data modules are connected to the control and data bus. The data bus of the PDP16-M is bidirectional. High impedance receivers and open-collector drivers are employed in each data module to transfer data between the module Source and Destination Registers. A bus terminator (load and pull-up resistors) is located in the bus sense and termination module to terminate each bus line with a TTL level and to provide the necessary current for the bus receivers.

The evoke data transfer instructions are implemented by the wire-wrap connections from the evoke decoder outputs to the control inputs of the data modules. For example, the evoke decoder output for the instruction A ← A + B (LET A = A + B) is wired to the control input A + B of a module Source Register (resulting in a data transfer of BUS ← A + B) and to the control input LDA (load the A Register) of a module Destination Register (resulting in a data transfer of A ← BUS). After the data transfer of BUS ← A + B, the DATA READY control signal is asserted which allows the data transfer A ← BUS to be completed. After the data transfer A ← BUS, the DATA ACCEPT control signal is asserted. The DONE signal is asserted after both DATA READY and DATA ACCEPT have been asserted. The DONE signal restarts the clock and causes the next instruction to be fetched.

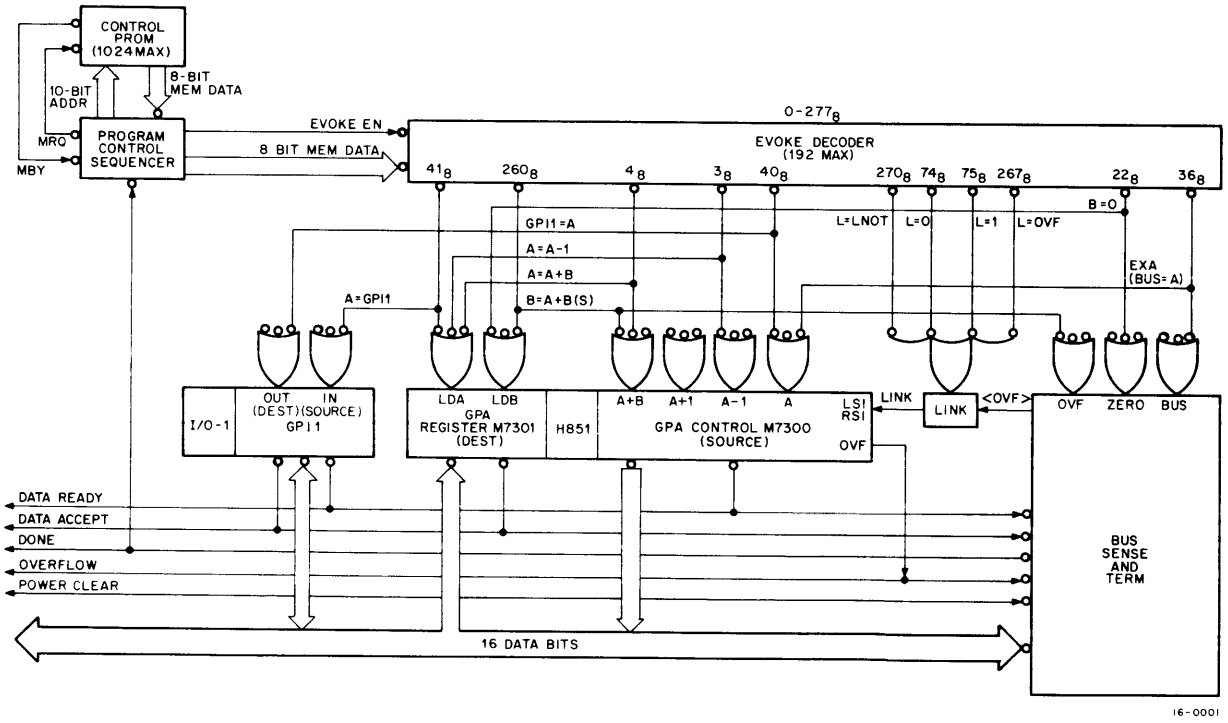


Figure 4-1 Evoke Data Transfer Scheme

A jump (control) is caused whenever any of the following instructions is executed:

GOTO
IF
CALL
EXIT

These instructions are not involved with data transfers on the data bus (Figure 4-2). The GOTO and IF instructions effect a test of a particular input to Boolean multiplexer 0. Octal codes 300 through 373 have been assigned to these instructions (this amounts to 60 combinations). However, the least significant bit of the instruction code is the M (Memory) address bit, resulting in only 30 possible test instruction codes. The M bit is tested every time a GOTO, a true IF, or a CALL instruction is executed. This bit is then stored and added as the most significant bit to the jump address fetched from the control memory. Before the inputs to Boolean multiplexer 0 can be tested with the IF instruction, the MUX0 command must be declared in the control program. MUX0 is selected when the PDP16-M is turned on. It remains selected until MUX1 is declared in the program. Then, the only way a MUX0 condition can be tested is to redeclare MUX0 in the program. The IF instruction (octal codes 302–373) causes either a skip (increment PC) to the next instruction (test is not true) or a memory request to fetch the eight least significant bits of the jump address (test is true). The most significant bit of the address is the M bit of the instruction code. The GOTO instruction (octal code 300–301) will always cause a memory request to fetch the eight least significant bits of the jump address because this test will always be true. It will be true because the multiplexer channel for the GOTO instruction is hard wired true.

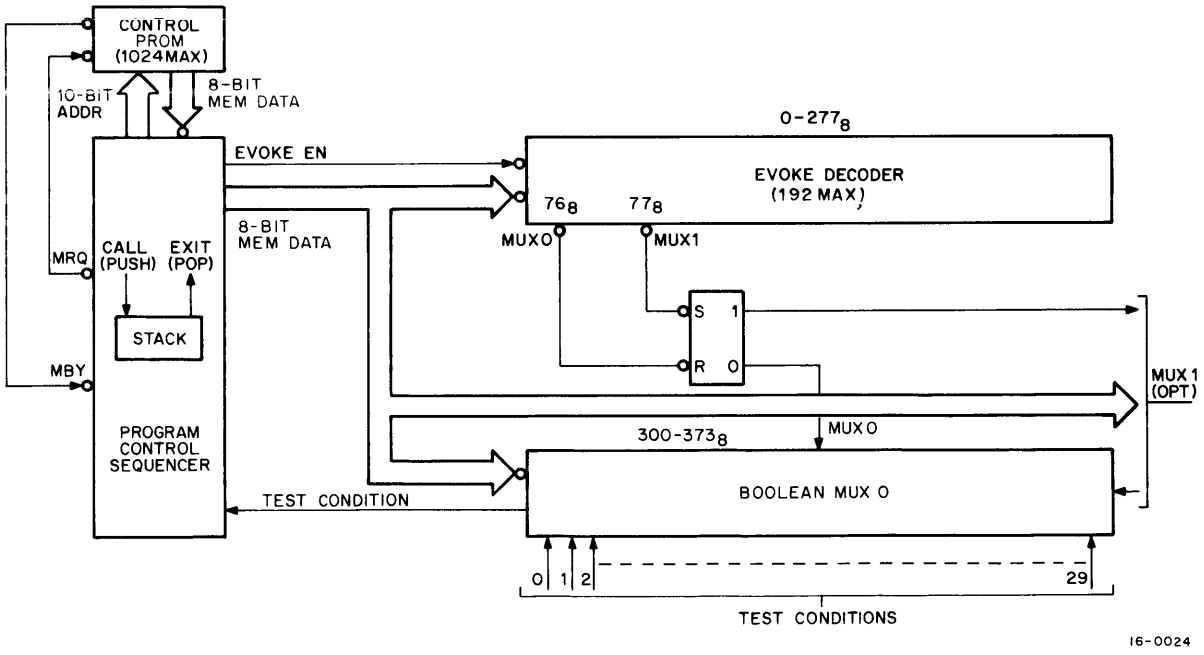


Figure 4-2 Control Scheme

The CALL and EXIT instructions (octal codes 374–377) use neither the data bus nor the Boolean multiplexer. These instructions use the stack in the program control sequencer to store the 9-bit return address. The stack is 16 words deep, allowing up to 16 calls before returning.

4.2 CONTROL SECTION

4.2.1 Program Control Sequencer

As the name implies, the program control sequencer is the controlling element in the PDP16-M. The following operations are performed by the program control sequencer.

- Decodes Instruction
- Generates timing states for executing instructions
- Keeps track of the program count (PC) or address
- Keeps track of the return address for a subroutine call

4.2.1.1 Start, Clock, and Evoke Enable Logic – When the PDP16-M is started, it is initialized by resetting the program counter (PC) and the state generator (Figure 4-3). After a small delay, the RUN light is turned on and the clock is enabled. However, the clock remains off until the MBY (memory busy) single-shot recovers.

This single-shot is triggered when the machine is started or when the state generator is in state 0 or 6. After the MBY single-shot recovers, the state generator is clocked to execute the instruction. If the instruction is an evoke data transfer instruction (LET instruction or command), the Evoke flip-flop is set to enable the evoke decoders. Upon completion of the data transfer, the DONE signal will reset the Evoke flip-flop. Termination of the DONE pulse will restart the clock.

4.2.1.2 Instruction Decoder – Simple combinational logic (Figure 4-4) is used to decode the 8-bit instructions fetched from the control PROM. Besides the seven bits of the Memory Data (MD1–MD7), the combinational logic receives INST DEC EN from the state generator and TEST CONDITION from the Boolean input multiplexer. The instruction decoder is enabled when the machine is started and after each instruction is executed. It is enabled for only one-half clock period when the state generator is in state 0. Only one output from the instruction decoder is asserted when the decoder is enabled. This output then jam sets the state generator to a specific count.

4.2.1.3 State Generator – The state generator (Figure 4-5) consists of three input gates, a 3-bit register, a binary-to-octal decoder and feedback logic. The input gates receive the output from the instruction decoder to jam set the state generator. The state generator is reset (state 0) when the machine is started and after each instruction is executed. A memory request (MRQ) is issued and the instruction decoder is enabled by state 0. Flip-flop A is set by the state 0 output of the state generator and reset the next time the clock goes low. Therefore, the instruction decoder is enabled for only one-half clock period. From the jam set count, the state generator will progress through a series of states (Figure 4-6) as it is clocked. The sequence is defined by the jam set state and the feedback logic. All operations required to execute the decoded instruction are performed during these states.

The state generator has 8 states (0 through 7). Each state is assigned a particular function. These functions are described in state Table 4-1. The table also identifies the jam state for each instruction, current state, and next state. A general timing diagram is given in Figure 4-7.

By examining Figure 4-5, one will notice that the feedback logic is arranged so that a return to state 0 can only be achieved from state 3 or state 7. The clock loads the 3-bit register with whatever the feedback logic receives and then enables the binary-to-octal decoder. The register is clocked on the positive clock transition and the binary-to-octal decoder is enabled for the negative clock period.

Table 4-1
State Table

Instruction	Current/Jam State	Description	Next State
START	0	Memory Request (MRQ). Instruction is decoded between state 0 and the next state (state generator is disabled while clock is high)	Depends on Instruction Decoded
IF not true	1	Increment PC	3
CALL	2	Stack return address	5
LET	3	Decode evoke, transfer data, and increment PC	0
EXIT	4	Get Return address and load into PC	1
IF true	5	Test and store M bit of instruction code and increment PC	6
—	6	Memory Request	7
—	7	Load PC with M bit and jump address	0

4.2.1.4 Program Counter (PC) and Stack – The PC is a 9-bit register that points to the memory location within a page of the control PROM from which the current instruction was fetched. The PC can be incremented to point to the next sequential memory location or it can be loaded with the jump address from the control PROM or from the stack. The jump address from the control PROM is only 8 bits. These 8 bits are loaded into the 8 least significant bit positions of the PC. The ninth bit, which is taken from the least significant bit position of the instruction code, is stored in the M flip-flop. A 9-bit address can address up to 512 words of storage. The PAGE flip-flop, which is programmable with the PAGE0 and PAGE1 commands, serves as the tenth bit of the address extending the addressing capability to 1024 words. The stack is a read-write memory with 16 9-bit locations. A 4-bit up/down counter serves as a pointer to address the stack. The stack can be loaded with the contents of the PC or the PC can be loaded with the contents of the stack. Each time the stack is loaded with a word, the pointer is incremented to select another stack location for the next entry. When the stack is to be read, the pointer is decremented before the stack is read to get the correct return address. Each of the following types of instruction operate on the PC in a different way:

LET – evoke data transfer

GOTO/IF (true) – unconditional/conditional jump

IF (not true) – conditional jump

CALL – subroutine jump

EXIT – subroutine return

After the memory request (state 0), which occurs when the program is started or after an instruction is executed, the state generator will progress in a fashion described by the instruction code itself and the feedback logic of the state generator. The memory request is not directly involved with fetching the instruction from the control PROM. It is only issued to stop the state generator clock long enough to transfer the data from the control PROM to the instruction decoder or the PC if it is a jump address.

If the PC points to a memory location containing an evoke data transfer (LET) instruction state 3 is asserted, an interlocked data transfer (Figure 4-7) is effected and the PC is incremented to point to the next instruction (Figure 4-8).

If the PC points to a GOTO or an IF instruction that is true, the following occurs:

a. State 5 is asserted after state 0 (Figure 4-9). This is because the instruction decoder found that the test is true (Figure 4-4). The M bit of the instruction code is tested and stored. The PC is also incremented to advance to the jump address location.

b. The state generator advances to state 6, causing another memory request to be issued. This stops the state generator clock long enough to transfer the data (in this case it will be the 8-bit jump address) to the receivers for the PC.

c. State 7 is then asserted to load the PC with the M bit and the 8-bit jump address.

d. After state 7, state 0 is asserted to fetch and decode the next instruction.

If the PC points to an IF instruction that is not true, the following occurs:

a. State 1 is asserted after state 0 (Figure 4-10). The PC is incremented in state 1 and incremented again in state 3. Incrementing the PC twice for this instruction results in a skip over the jump address and leaves the PC pointing to the next instruction.

b. State 0 is then asserted to fetch and decode the next instruction.

If the PC points to a CALL instruction, the following occurs:

a. State 2 is asserted after state 0 (Figure 4-11). The contents of the PC is loaded into the stack and the pointer is incremented.

NOTE
The contents of the PC is not changed.

b. The M bit of the CALL instruction code is tested and stored. The PC is also incremented to advance to the jump address location.

c. The state generator advances to state 6, causing another memory request to be issued. This stops the state generator clock long enough to transfer the data (in this case it will be an 8-bit jump address) to the receivers for the PC.

d. State 7 is then asserted to load the PC with the M bit and the 8-bit jump address.

e. After state 7, state 0 is again asserted to fetch and decode the next instruction.

If the PC points to an EXIT instruction, the following occurs:

a. Following state 0 and before state 4 (instruction is decoded while the clock is high and the state generator is disabled), the stack is decremented to point to the most recent subroutine return address.

b. When state 4 is asserted (Figure 4-12), the contents of the addressed stack location is loaded into the PC.

c. State 1 is then asserted. The PC is incremented in state 1 and again in state 3. The PC is incremented twice because the address received from the stack is the address of the CALL and the location following the call was the jump address. Therefore, to continue with the program, the stacked address must be incremented twice.

d. After state 3, state 0 is again asserted to fetch and decode the next instruction.

4.2.2 Memory and Page Select

The control program for the PDP16-M is stored in a programmable Read-Only-Memory (PROM). Any constants or data that may be required by the program are stored in a separate ROM constant generator. Up to four control PROM modules (Figure 4-13) can be implemented in the PDP16-M. One is supplied with the basic PDP16-M and the remaining three are optional. Each PROM module can store 256 8-bit words. Fully implemented, the 1024-word control memory is divided into two 512 word pages; each containing a memory 0 and a memory 1 of 256-words each (Figure 4-13). Eight address bits (MA00–07) are required to address every location in a given memory. The ninth bit (MA8) is used to select the desired memory (0 or 1) in a given page. This bit is the M bit (LSB) of the control code for a jump (GOTO, IF, and CALL) instruction. The tenth address bit (PAGE bit) is used to select the desired page. This bit is not stored in the control PROM but is programmable.

Whenever PAGE0 or PAGE1 is declared in the control program, the BS ← 0 and the PAGE ← n evoke logic is activated. The clock in the program control sequencer is also stopped when either PAGE command is declared. The clock is stopped while both data transfers are evoked and is restarted only by the CONTINUE signal – not the DONE signal. Two evoke circuits are used in series to allow the page select logic to stabilize before asserting the CONTINUE signal to reactivate the clock.

4.2.3 Boolean Input Multiplexers

The Boolean multiplexers (Figure 4-14) are used only with the GOTO and IF instructions – not with the evoke data transfer nor the CALL instruction. The basic PDP16-M is supplied with one Boolean input multiplexer, designated MUX0. The other Boolean input multiplexer (MUX1) is optional. Each multiplexer is capable of selecting one of 30 data inputs for test. The test for the GOTO and IF instruction is performed by the instruction decoder in the program control sequencer. Table 4-2 lists the conditions that can be tested.

NOTE

Octal machine codes are given for jumps into or within memory 0 and in () into or within memory 1. The least significant bit of the code is the M (Memory) address bit.

The commands MUX0 and MUX1 must be declared in the application program to test the corresponding data set. Once a multiplexer is selected, it will remain available until the other multiplexer is selected. MUX0 is automatically selected during power-up.

Table 4-2
Boolean Multiplexers Inputs

Condition	MUX0	MUX1	Octal Machine Code
0	+3V (GOTO)	+3V (GOTO)	300 (301)
1	EXT 1	A <0>	302 (303)
2	EXT 2	A <2>	304 (305)
3	EXT 3	A <4>	306 (307)
4	EXT 4	A <6>	310 (311)
5	EXT 5	A <8>	312 (313)
6	EXT 6	A <10>	314 (315)
7	DZ	A <12>	316 (317)
8	DP	A <14>	320 (321)
9	DN	B <0>	322 (323)
10	OVF	B <15>	324 (325)
11	A <1>	EXT 7	326 (327)
12	A <3>	EXT 8	330 (331)
13	A <5>	EXT 9	332 (333)
14	A <7>	EXT 10	334 (335)
15	A <9>	EXT 11	336 (337)
16	A <11>	EXT 12	340 (341)
17	A <13>	EXT 13	342 (343)
18	A <15>	EXT 14	344 (345)
19	FF1	EXT 15	346 (347)
20	FF2	EXT 16	350 (351)
21	FF3	EXT 17	352 (353)
22	FF4	EXT 18	354 (355)
23	FF5	EXT 19	356 (357)
24	FF6	EXT 20	360 (361)
25	KF1	EXT 21	362 (363)
26	PF1	EXT 22	364 (365)
27	KF2	L	366 (367)
28	PF2	PWOK	370 (371)
29	CLK	GND	372 (373)

4.2.4 Evoke Decoders

The evoke decoders (Figure 4-15) are used only with the evoke data transfer instructions – not with the jump (GOTO, IF, CALL, or EXIT) instructions. The basic PDP16-M is supplied with four evoke decoders. Two are optional and are required if the Scratch Pad (SP) memories are implemented. Each evoke decoder module is capable of decoding 32 unique evoke signals for data transfers. Each decoder receives the 8-bit memory data (MD00–07). The three most significant bits of the memory data (machine control code) are used to select the proper decoder.

The five least significant bits (MD00–04) are used to select one of the 32 possible output states. The decoder address (MD05–07) is decoded by the three exclusive OR gates. Each decoder socket is prewired to provide the Exclusive OR gate a unique combination of ground and +5V (see table of Figure 4-15). Therefore, all evoke decoders are interchangeable within the range of their assigned sockets without modification.

4.3 DATA SECTION

4.3.1 General Purpose Arithmetic (GPA) Unit, LINK and OVERFLOW

The GPA unit (Figure 4-16) is formed by two adjacent modules: GPA Control M7300 and GPA Register M7301. The M7300 contains the operation encoder, the right shift logic, and drivers while the M7301 contains the A Register (accumulator), the B Register (argument register), the Arithmetic and Logic Unit (ALU), and the data ready and accept logic. The Link flip-flop is located on a separate module. All arithmetic and logical operations that have been implemented in the PDP16-M are executed by the GPA unit. The LINK Register permits simpler algorithms to be employed in performing arithmetic.

The output from the evoke decoders evoke the arithmetic or logical operation and the transfer of data between the registers of the GPA unit and LINK. By using the proper instructions, data transfers can also be evoked between GPA registers A or B and other data module registers (TR, GPI1, etc.). As mentioned earlier, a data module may have a Source Register, a Destination Register or both. The GPA unit has two registers (A and B). Either of these registers can serve as Source or Destination Registers.

The ALU and the right shift/driver logic (output logic) serve as a function generator when an arithmetic or logical operation is specified in the instruction. A summary of the implemented arithmetic and logical operations and associated encoder outputs for the ALU and output logic is given in Table 4-3. The operations can only be performed on the contents of the A or B Register (source) and the result can only be stored in the A or B Register (destination) – not the TR or GPI1 etc.

Table 4-3
GPA Units Operations Summary

Source Evokes						
Operation	**Encoder Output**					
	S/2	**M**	**S3**	**S2**	**S1**	**S0**
A	0	1	1	1	1	1
B	0	1	1	0	1	0
A + 1	0	0	0	0	0	0
A - 1	0	0	1	1	1	1
A + B	0	0	1	0	0	1
A - B	0	1	0	1	1	1
A X 2	0	0	1	1	0	0
A/2	1	1	1	1	1	1
B/2	1	1	1	0	1	0
NOTA	0	1	0	0	1	1
NOTB	0	1	1	0	1	0
AORB	0	1	0	1	1	0
AB	0	1	1	0	1	1
AXORB	0	1	0	1	1	0

Destination Evokes	
A (LDA)	See Above
B (LDB)	See Above

Once the arithmetic or logical operation is executed and the result is stored in A or B, the data can be transferred to another data module Destination Register (TR or GPI1 in the basic machine) using the appropriate instructions. The TR can receive data only from the A Register. Options are available to expand the Destination Registers. Constants/Data required in performing arithmetic or logical operation are stored in a 4-word constant generator (C Register) ROM. Since a ROM can only be read, it can therefore only serve as a Source Register. Constants in this register must be transferred to the B Register using the appropriate instruction. Besides the A, B, and C Registers, additional Source Registers in the basic machine are the TR and GPI1. Using the appropriate instructions, data from these registers can be read into the GPA unit. The result from an arithmetic or logical operation that is temporarily stored in the TR can be read back into the A Register but not the B Register. Data from the "outside world" (GPI1) can be read into either the B or the A Register.

For each arithmetic or logical operation and for each data transfer involving the GPA, a DATA READY and a DATA ACCEPT is generated by the Source and Destination Registers, respectively. Bits 01, 03, 05, 07, 09, 11, 13, and 15 of the A Register are routed to input channels of Boolean multiplexer 0. These bits can be tested using the IF instruction. The remaining bits of the A Register and bits 00 and 15 of the B Register can be made available for test if the multiplexer 1 option is incorporated into the basic machine. Examples of the test instruction follow:

```
IF A <1>, LABEL 1
IF A <3>, LABEL 2
IF A <15>, LABEL 3
```

If the condition tested is true (logical 1), then a jump to the specified program label is executed; otherwise, the next instruction is executed.

The OVF is a 1-bit register (in the bus sense and termination module) which is used to extend the arithmetic capability of the GPA unit. It is used as a Carry Register for 2's complement arithmetic or as a Holding Register for shift operations. Under program control, the OVF bit can be checked and loaded into the LINK Register. LINK can then be rotated as part of the A or B Register to simplify arithmetic algorithms. The LINK Register can also be cleared, set, and complemented. The following instruction evoke data transfers to the LINK bit register:

INSTRUCTION

Destination		Source	Remarks
L	=	OVF	OVF is stored in bus sense (BS) module if saved (S)
L	=	1	imaginary source
L	=	0	imaginary source
L	=	LNOT	imaginary source

4.3.2 Transfer Register (TR)

The TR (Figure 4-17) is a one-word byte and word addressable register. It can be used for temporarily storing results of arithmetic or logical operations appearing in the A Register or storing data from the outside world via GPI1 and the A Register. The stored data can be read back into the A Register when needed, using the appropriate instruction. The following instructions evoke data transfers between the TR and the A Register via the data bus.

STORE			READ			
Destination		**Source**	**Destination**		**Source**	**Remarks**
TR	=	A	A	=	TR	word
TRU	=	A	A	=	TRU	upper byte
TRL	=	A	A	=	TRL	lower byte

To complete the data transfers specified by the above instructions, a DATA READY is issued by the Source Register and a DATA ACCEPT is issued by the Destination Register.

4.3.3 Constant Generator (C)

The constant generator (C) is a four-word diode ROM (Figure 4-18). The desired constants/data are selected by removing or not removing the jumpers associated with a given word. With the jumper left in place, logic 1s are placed on the bus (bus lines are asserted – LOW) when the constant is transferred. If a 0 is desired for a particular bit position of a word (bus is not asserted – HIGH), the corresponding jumper must be cut. Constants can be transferred only to the B Register. The following instructions evoke data transfers between the constant generator and the B Register via the data bus:

INSTRUCTION

Destination		Source	Remarks
B	=	C1	Word 1
B	=	C2	Word 2
B	=	C3	Word 3
B	=	C4	Word 4

To complete the data transfers specified by the above instructions, a DATA READY is issued by the constant generator and a DATA ACCEPT is issued by the GPA unit.

4.3.4 General Purpose Interface No. 1 (GPI1)

The GPI1 (Figure 4-19) is a one-word I/O interface. It can be used for transferring data between the A or B Registers and the outside world. The following instructions evoke data transfers between the A or B Registers and the outside world via the GPI1.

SEND			RECEIVE		
Destination		**Source**	**Destination**		**Source**
GPI1	=	A	A	=	GPI1
GPI1	=	B	B	=	GPI1

To complete the data transfer specified by the above instruction, a DATA READY is issued by the Source Register and a DATA ACCEPT is issued by the Destination Register.

Details for interfacing with the PDP-11 low-speed peripherals are presented in the DA16-F option description (refer to Appendix A).

4.3.5 Bus Sense and Termination Module (BS)

The bus sense and termination module (Figure 4-20) performs a variety of functions:

a. The module terminates the data bus and provides the source current for the open-collector drivers of all Source Registers in the data modules.

b. The module serves as a Destination Register (3-bits) to recapture the test result (positive, negative, or zero) from the previous data transfer. This may be required if a conditional test (IF instruction) on the transferred data is to be made after a FF, PAGE, MUX, LINK, or HALT instruction is executed. These instructions zero the bus (no data is transferred on the bus) and activate the DZ Register in the bus sense and termination module. Therefore, the test result from the previous data transfer is lost and must be recaptured in order to execute the conditional test successfully.

c. The module serves as a Destination Register (1 bit) to store the overflow (if any) from the GPA unit.

d. The module serves as a pseudo Source and Destination Register to zero the bus (BS), and a pseudo Source Register to zero the GPA unit A or B Registers or the Transfer Register (TR).

e. The module generates the DONE signal whenever a Destination Register (in any data module connected to the bus) accepts the data – DATA ACCEPT is asserted. The DONE signal restarts the clock after a data transfer instruction.

f. The module generates the START signal (AUTO/MANUAL) and POWER CLEAR signal.

The bus terminators and current sources are not shown in Figure 4-20. Refer to circuit schematic D-CS-M7332 for the circuit details.

Every data transfer instruction causes an automatic test of the data being transferred. The test is for positive, negative, or zero data. The following instructions evoke data transfers between the A or B Register and the bus sense and termination (BS) module just to test the data without any actual transfer of data between any data registers.

```
EXA
EXB
```

To complete the data transfers specified by the above instructions, a DATA READY is issued by the GPA unit register (A or B) and a DATA ACCEPT results by asserting the BUS gate of the bus sense and termination module. The DATA ACCEPT signal clocks flip-flops DN, DZ, and DP and generates the DONE signal. Each of the three flip-flops receives, as its data input, a logic level derived from the bus through combinational logic. The following logic definitions prevail on the data bus because the bus is driven by open-collector drivers that are turned on by logic 1s (HIGH):

```
HIGH = LOGIC 0
LOW = LOGIC 1
```

When data bit 15, the most significant data bit (sign bit in 2's complement representation), is low (logic 1) the DN flip-flop will be reset when clocked. This causes the output from this flip-flop ("zero" side) to go high. The DZ flip-flop is reset only when all data inputs are high (no data bits are low). The DP flip-flop is reset when both of the above two conditions are not true. The outputs from the "zero" side of these flip-flops are brought to three input channels of Boolean multiplexer 0 to permit these conditions to be tested using the IF instruction.

For example:

```
IF DN, LABEL
IF DZ, LABEL
IF DP, LABEL
```

If the condition tested is true (logic 1), then a jump to the specified program label is executed. If the condition is not true, the next instruction is executed.

Arithmetic operations performed by the A and B Registers can result in a carry (overflow). It is important to keep track of this overflow whenever arithmetic routines are written for the PDP16-M. Therefore, the following instructions are implemented to keep track, test, and manipulate the overflow bit:

```
x = y (S)
IF OVF, LABEL
L = OVF
```

Any data transfer instruction suffixed with (S) asserts the OVF gate and causes the overflow bit to be tested and clocked into the OVF flip-flop of the bus sense and termination module. The output from this flip-flop is applied to an input channel of Boolean multiplexer 0 and the 1-bit LINK Register. The IF instruction is used to determine whether an overflow occurred. If it did, then the L = OVF instruction can be used to add the carry to the contents of the GPA unit register.

Data Register A, B, and TR can be zeroed using the following instructions.

Destination		Source
A	=	0
B	=	0
TR	=	0

No Source Register is evoked when these instructions are executed. However, a DATA READY signal is generated by the ZERO gate of the bus sense and termination module to make it appear as if data was placed on the bus. Since no Source Register is evoked, the data bus is zero and the Destination Register will therefore be cleared.

The following evoke data transfer instructions/commands zero the data bus.

PAGE1	L = OVF
PAGE2	L = 0
HALT	L = 1
$FF_n = 1$	L = LNOT
$FF_n = 0$	
MUX0	
MUX1	

This causes a pseudo data transfer of zero because a DATA READY is issued by the ZERO gate and a DATA ACCEPT results from asserting the BUS gate (for PAGE and HALT commands), both of which are in the bus sense and termination module, or because a DATA ACCEPT is issued by the flag module (FF_n, L, or MUX).

Therefore, whenever any of these instructions/commands are used and the data from the previous data transfer is needed for a decision, the data of interest in the A or B Register must be examined again. For example:

```
EXA
EXB
```

This operation permits the data of interest to be tested after switching pages or multiplexers, setting or resetting flags, or operating on the LINK.

The DONE signal is generated every time a Destination Register accepts the data by issuing an ACCEPT signal. The clock is then restarted to fetch and decode the next instruction.

The bus sense and termination module also generates the POWER CLEAR and the START signals. An RC network between +5V and ground initiates the POWER CLEAR signal every time power is turned on. The START signal is generated automatically upon power up by the power clear RC network if the jumper in the switch cable is installed or by the front panel START switch if this jumper is not installed.

4.3.6 Data Transfer Timing

As emphasized throughout this chapter, every data transfer evoked causes a DATA READY, a DATA ACCEPT, and a DONE signal to be generated and placed on the control bus. The DATA READY is always generated by a Source Register and the DATA ACCEPT is always generated by the Destination Register. In summary, Table 4-4 lists the Source and Destination Registers and functions that are part of the basic PDP16-M.

Table 4-4
Basic PDP16-M Registers and Functions

Destination	Source
Registers	
A	A
B	B
TR	TR
TRL	TRL
TRU	TRU
GPI1	C1, C2, C3, C4
DN, DZ, DP	GPI1
(Examine A or B)	
(S) – Save OVF	0 (Pseudo Source)
FF_n	1 (Pseudo Source)
Functions	
MUX_n	A - 1
$PAGE_n$	A + 1
HALT	A - B
	A + B
	A X 2
	A / 2
	B / 2
	NOTA
	NOTB
	A OR B
	AB
	AXORB

In all cases, the EVOKE signal wired to the evoke control input of the source and destination modules asserts the DATA READY and DATA ACCEPT signals, respectively. After both DATA READY and DATA ACCEPT are asserted, the result from the data test is stored in the DN, DZ, and DP flip-flops of the bus sense and termination module, and the DONE signal is asserted to reset the Program Control Sequencer.

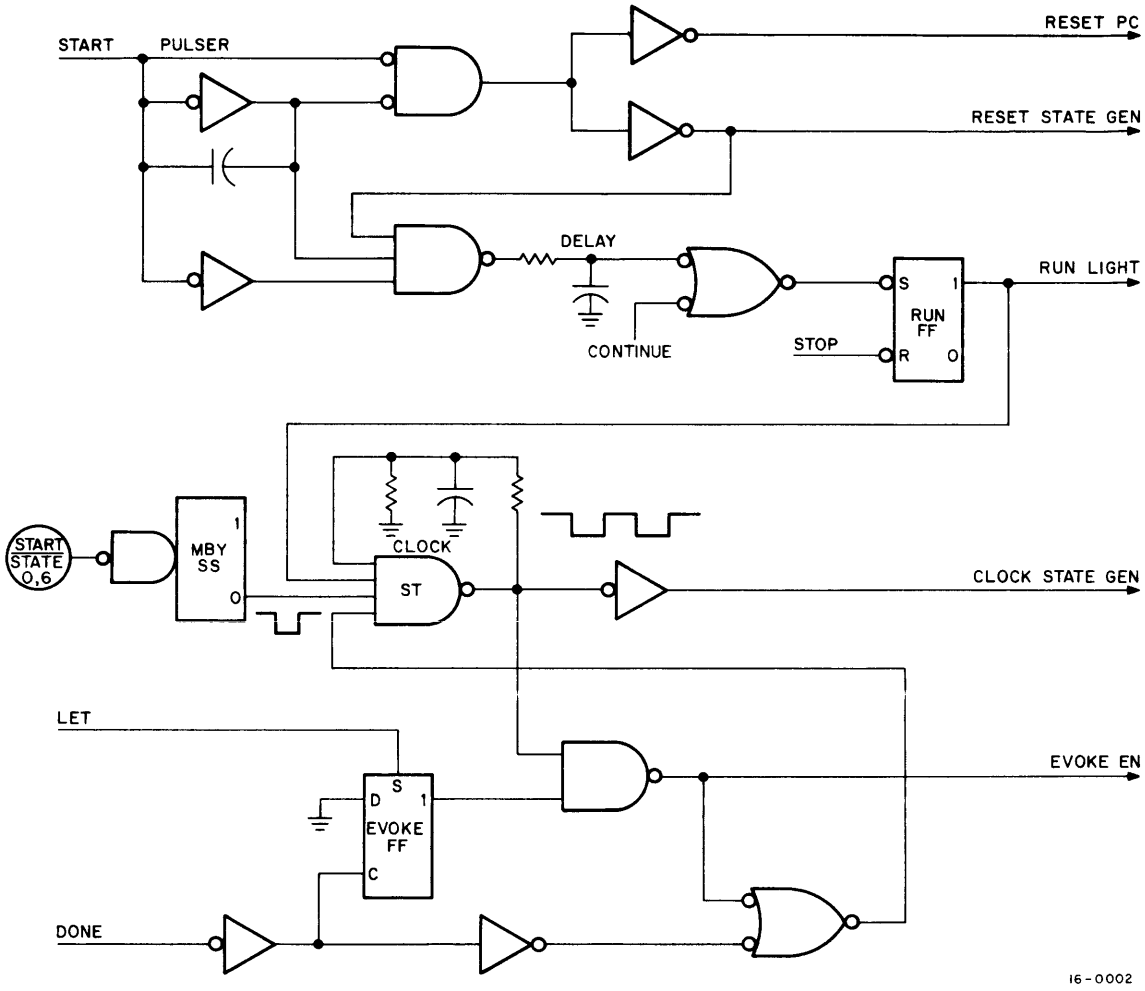


Figure 4-3 Start, Clock, and Evoke Enable Logic

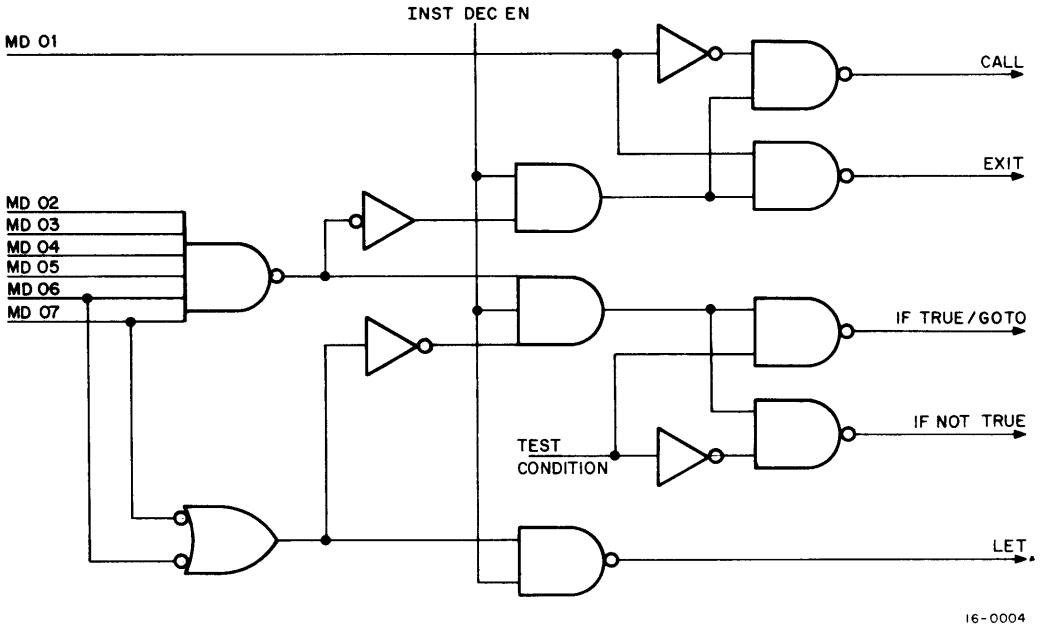


Figure 4-4 Instruction Decoder

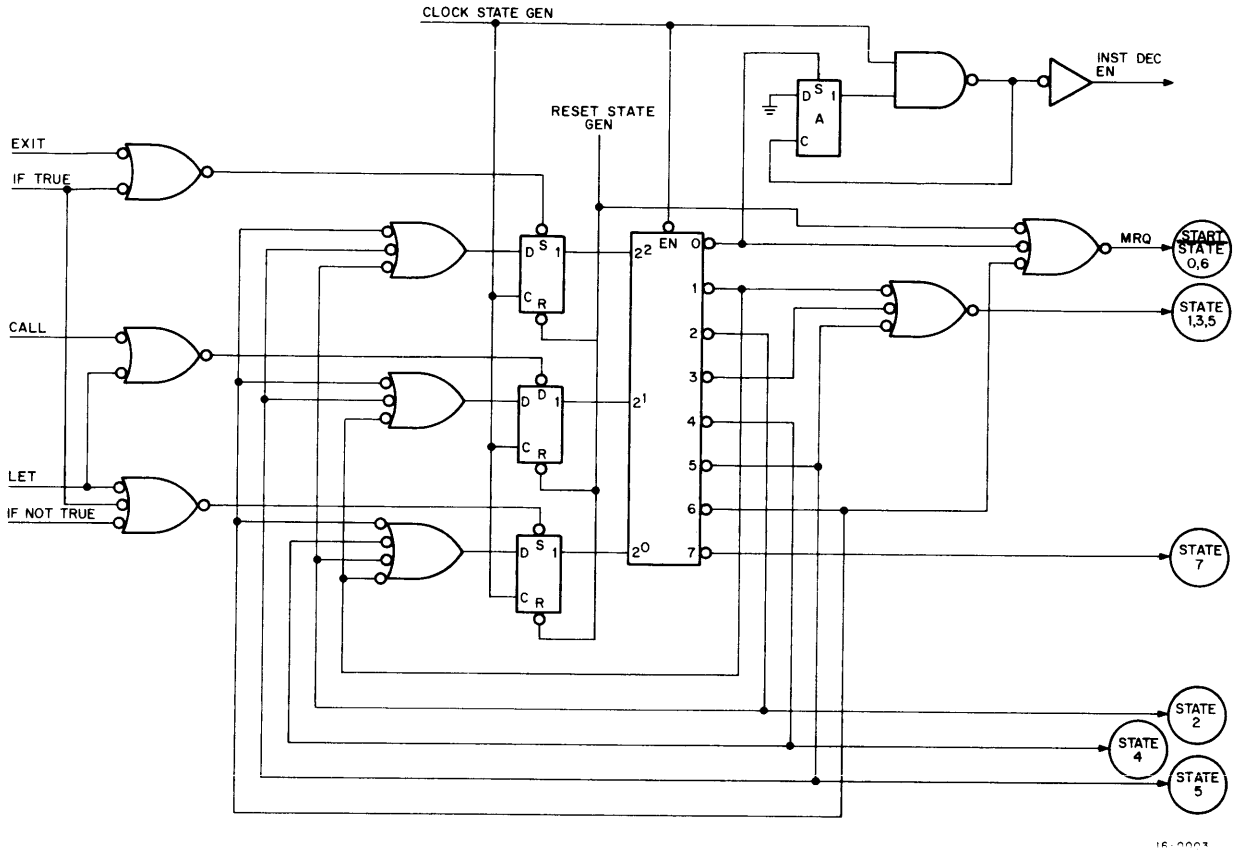


Figure 4-5 State Generator

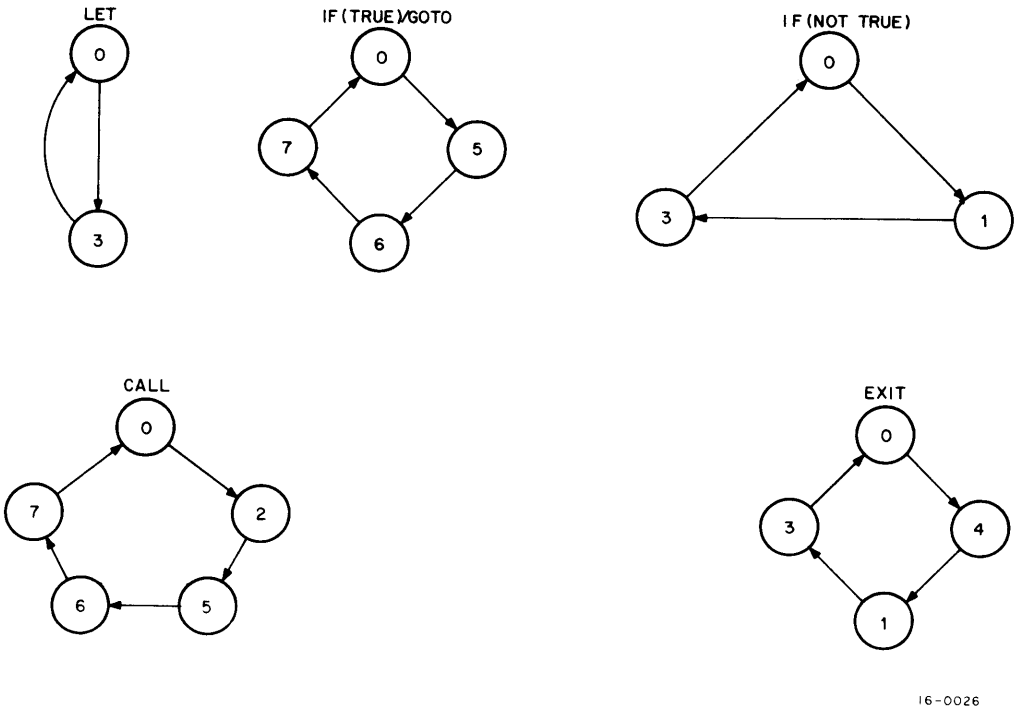


Figure 4-6 State Generator State Diagram

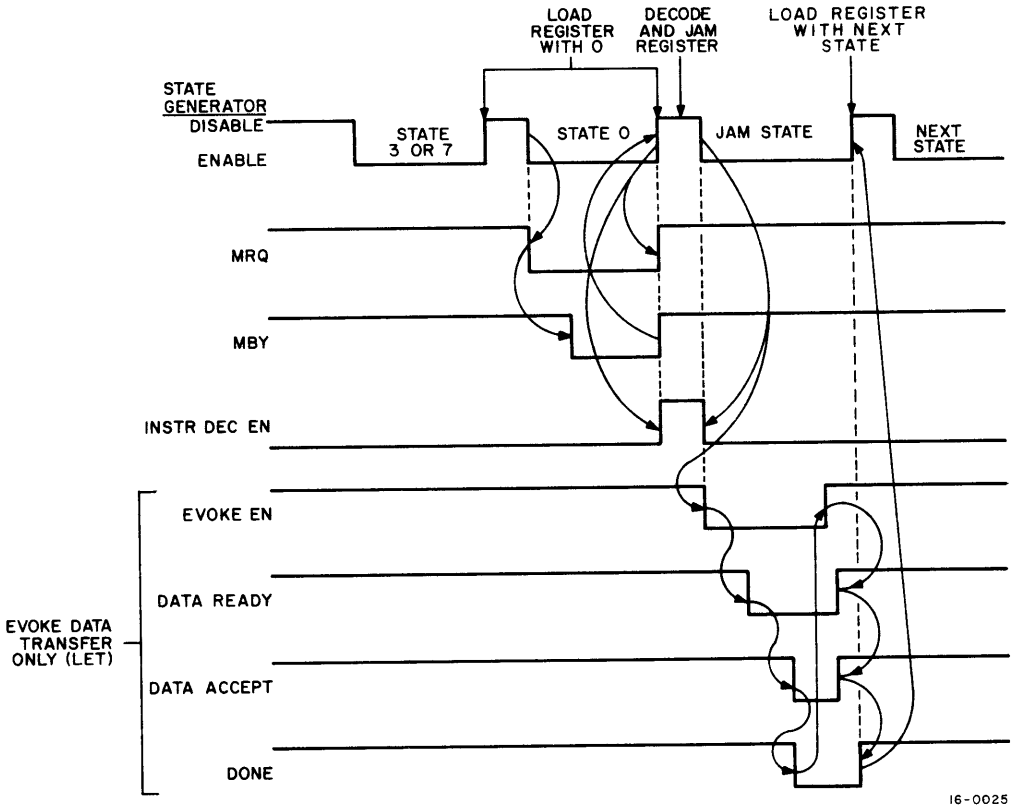


Figure 4-7 State Generator Timing Diagram

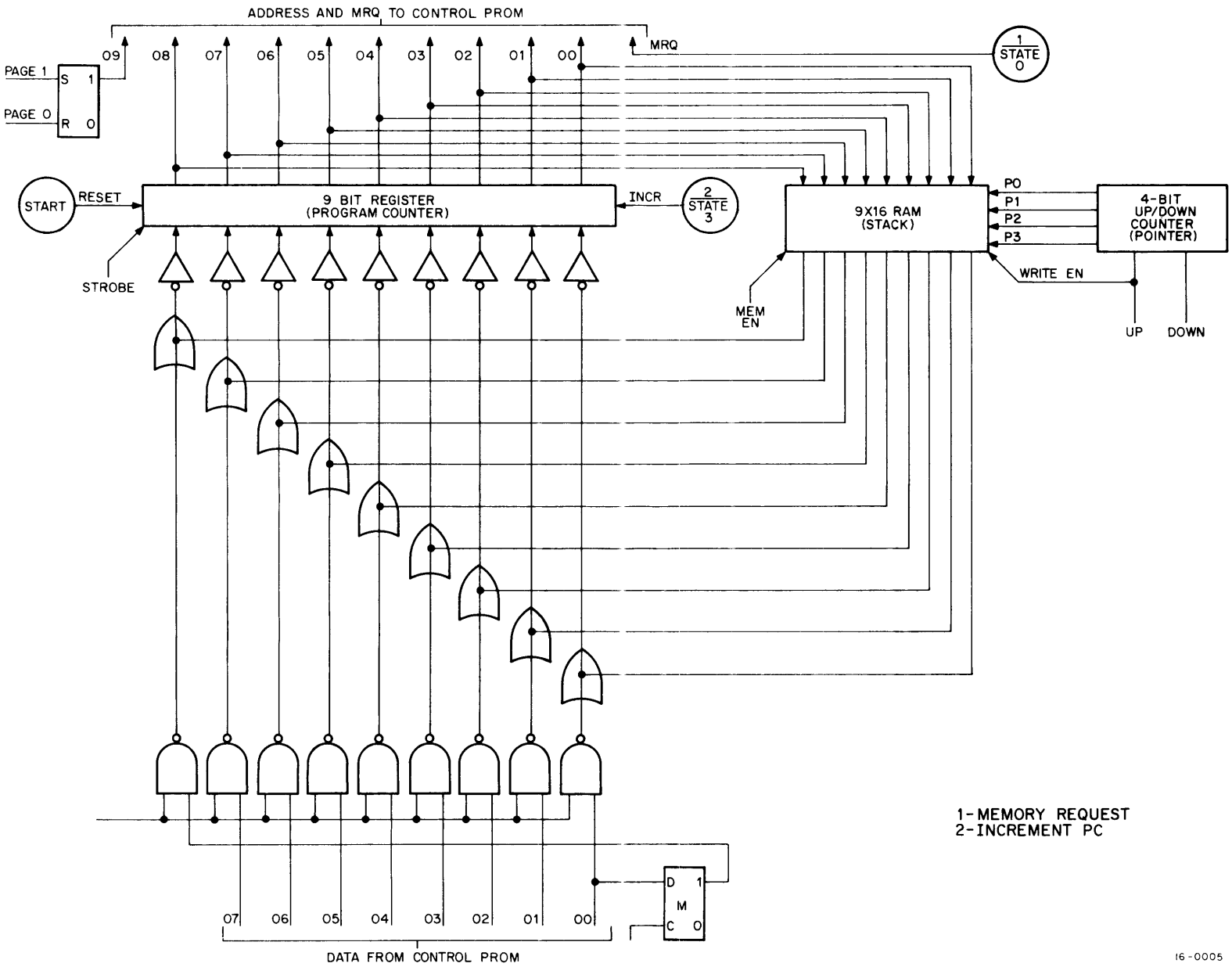


Figure 4-8 Program Counter and Stack – LET Instruction

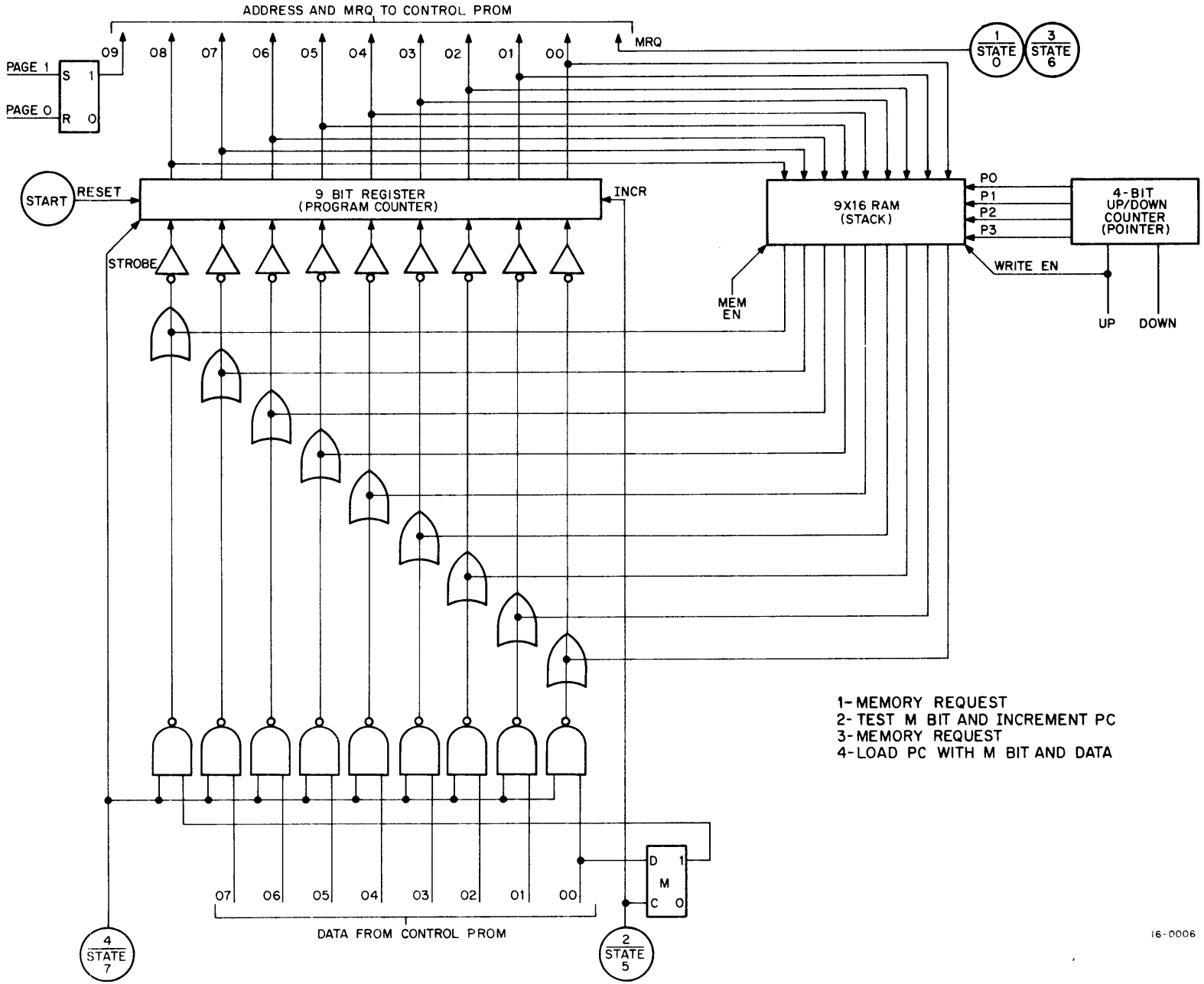


Figure 4-9 Program Counter and Stack – GOTO/IF (true) Instruction

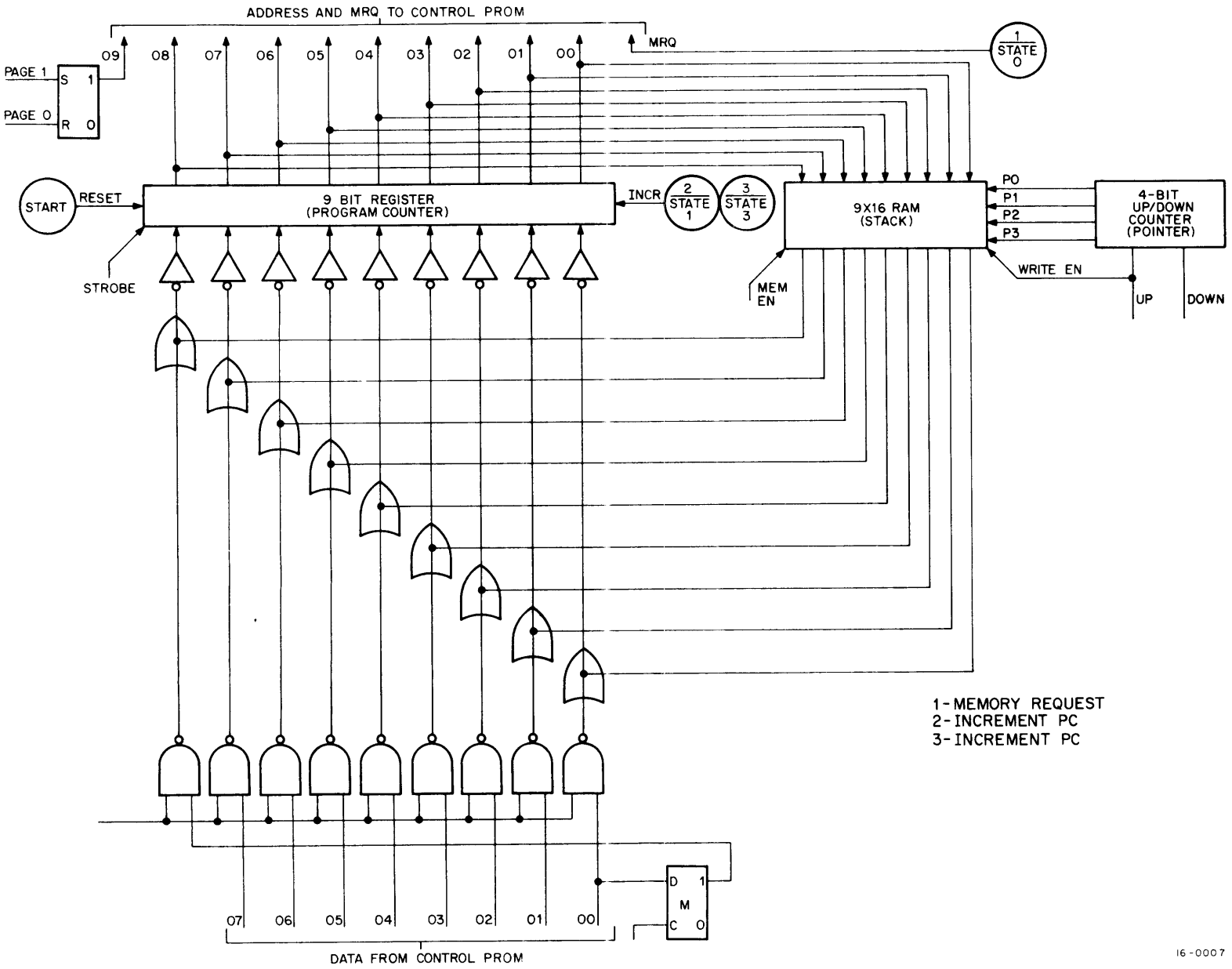


Figure 4-10 Program Counter and Stack – IF (not true) Instruction

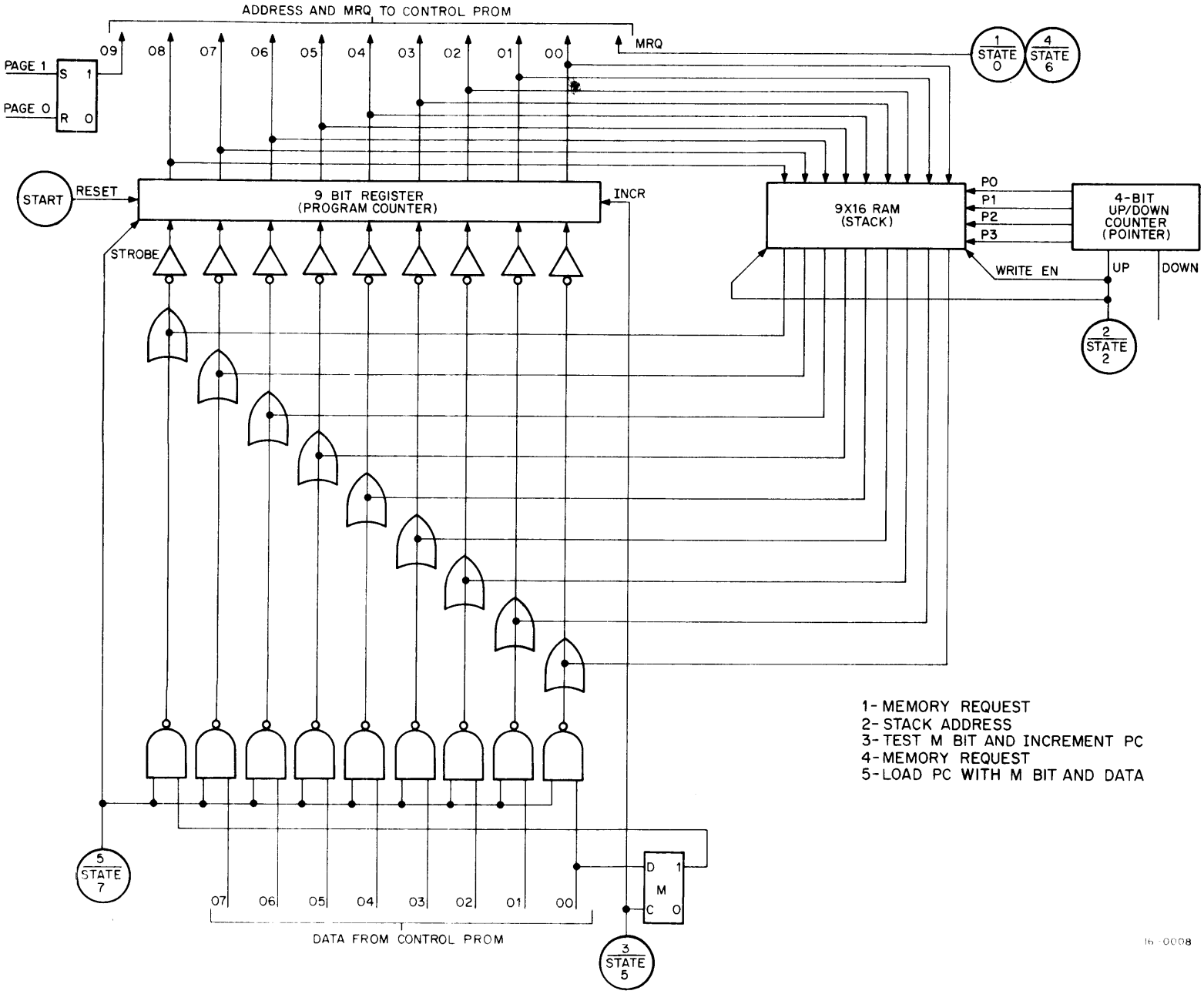


Figure 4-11 Program Counter and Stack – CALL Instruction

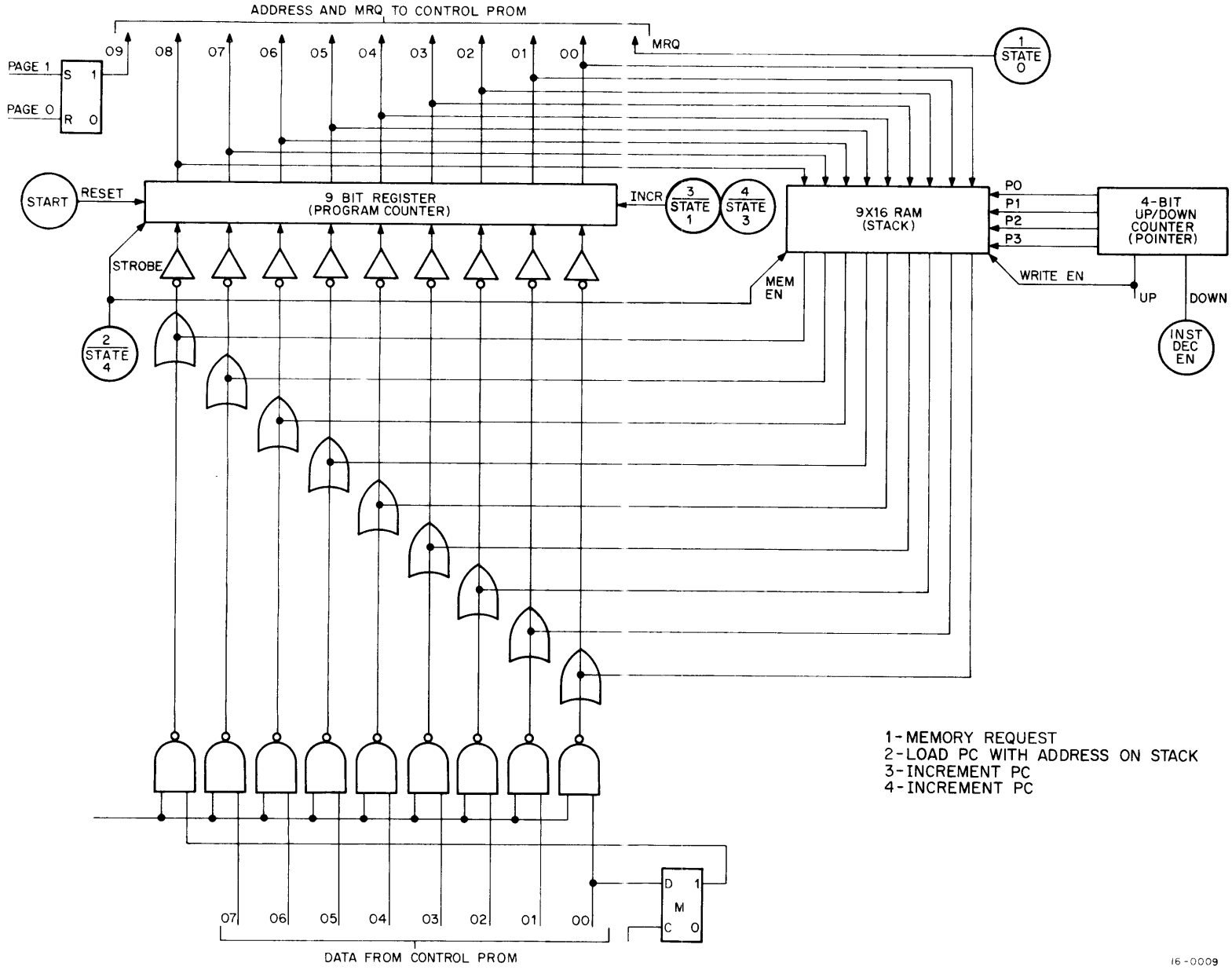


Figure 4-12 Program Counter and Stack – EXIT Instruction

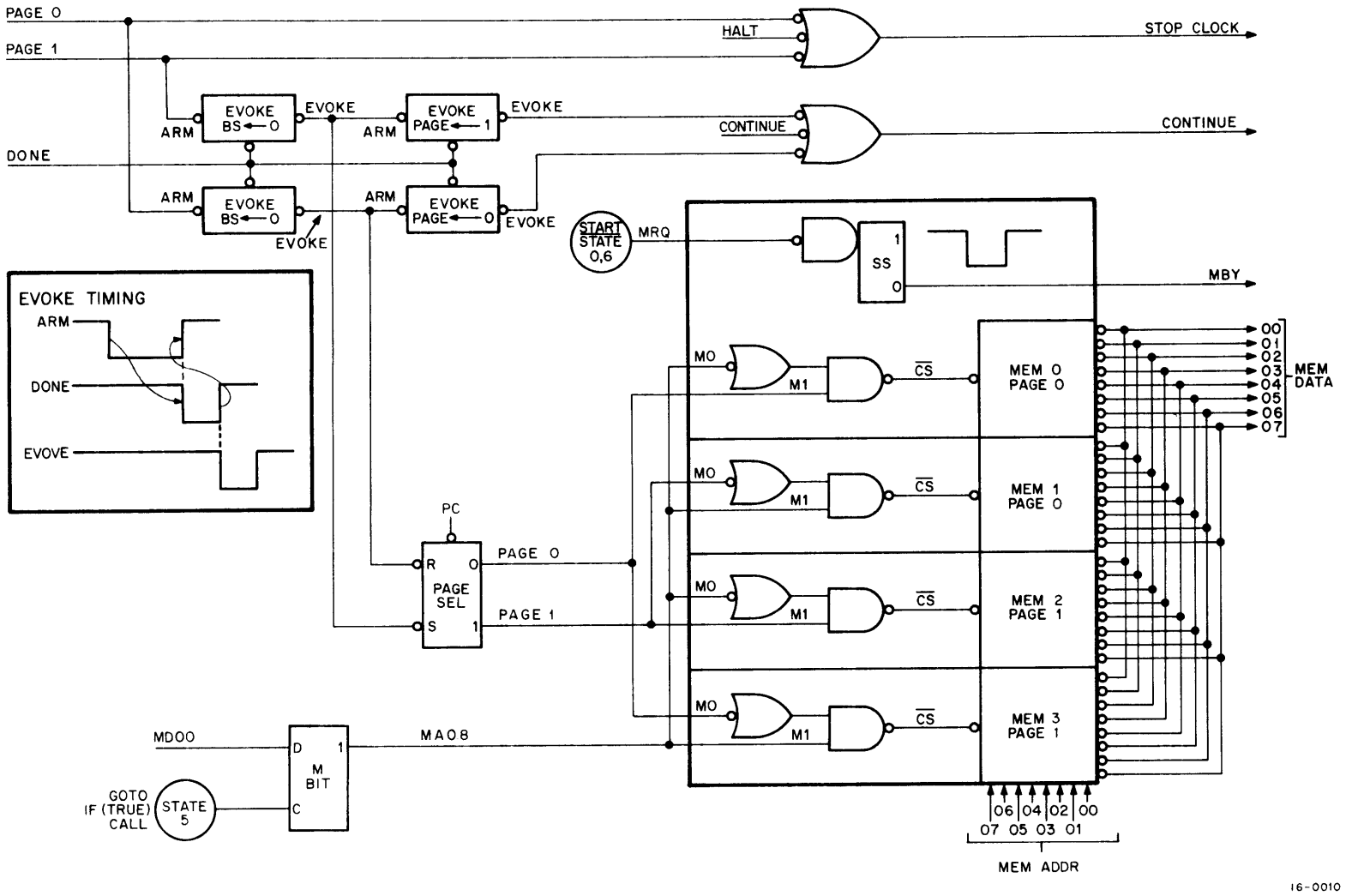


Figure 4-13 Memory and Page Select Logic

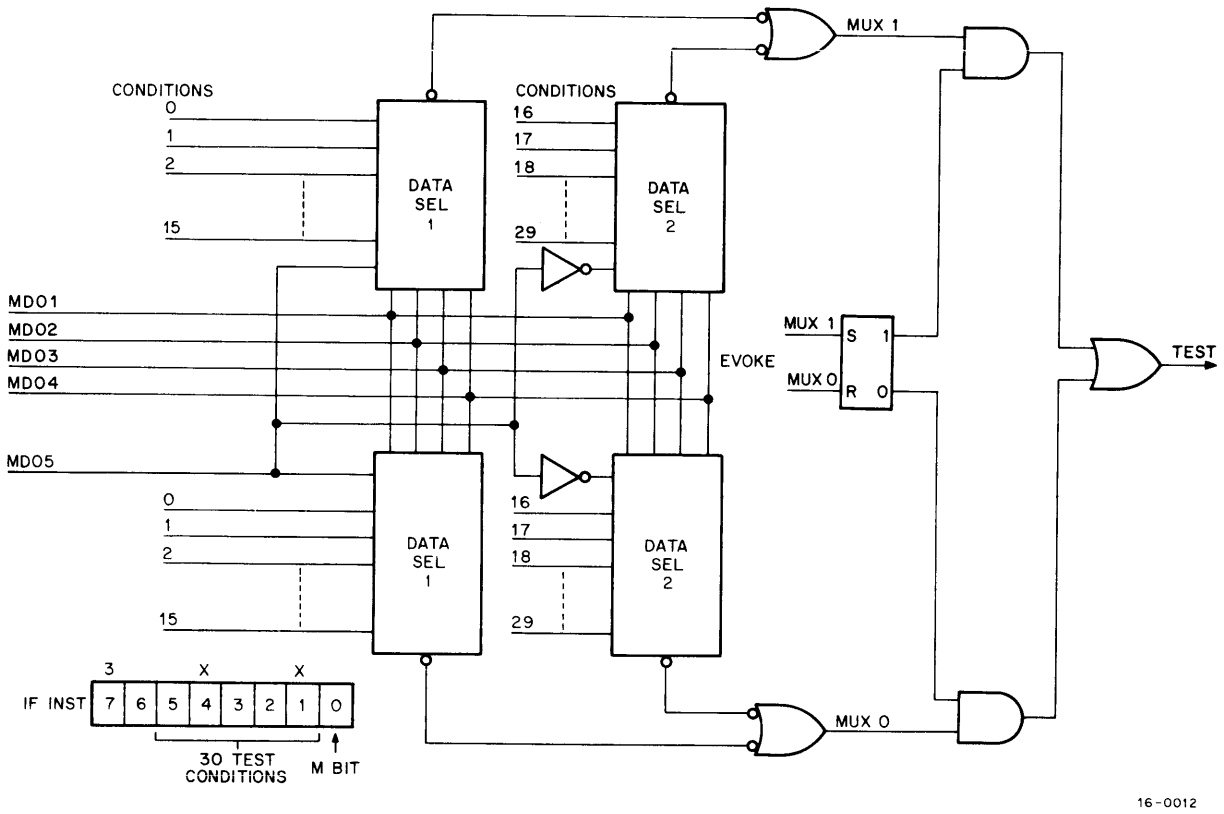
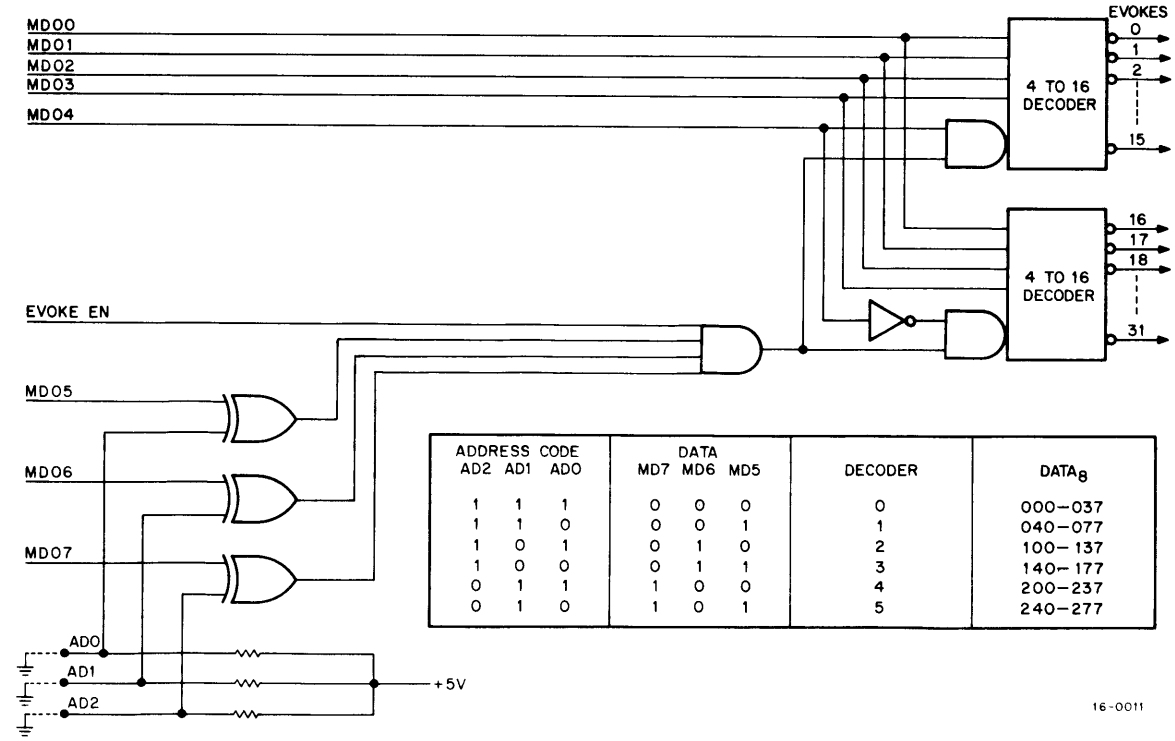


Figure 4-14 Boolean Multiplexers



ADDRESS CODE AD2	AD1	AD0	DATA MD7	MD6	MD5	DECODER	$DATA_8$
1	1	1	0	0	0	0	000–037
1	1	0	0	0	1	1	040–077
1	0	1	0	1	0	2	100–137
1	0	0	0	1	1	3	140–177
0	1	1	1	0	0	4	200–237
0	1	0	1	0	1	5	240–277

Figure 4-15 Evoke Decoder

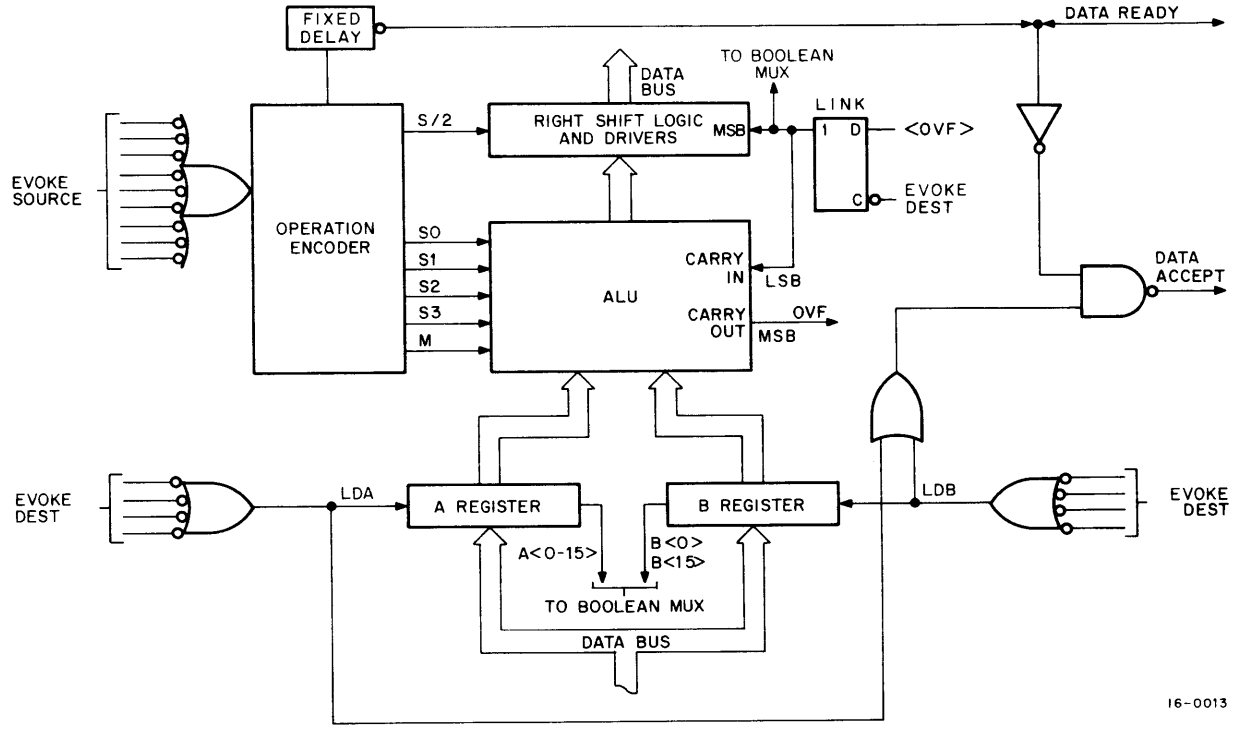


Figure 4-16 GPA Registers and Control

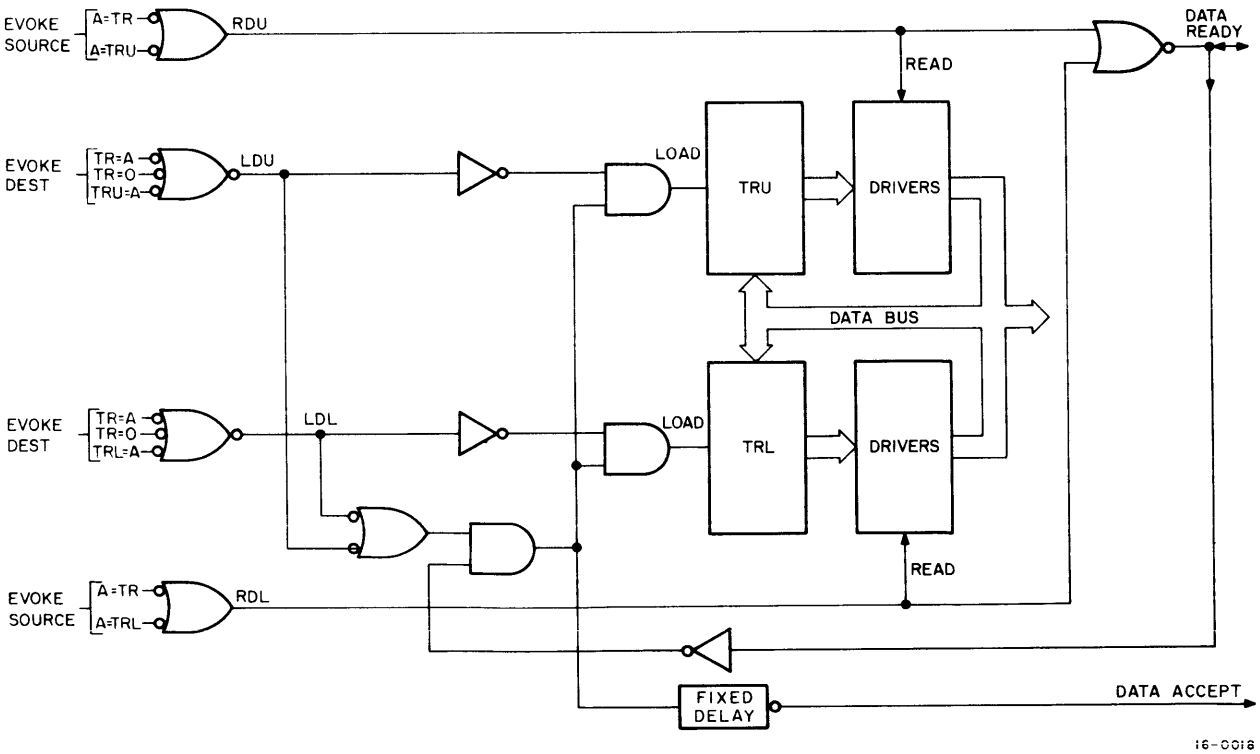


Figure 4-17 Transfer Register

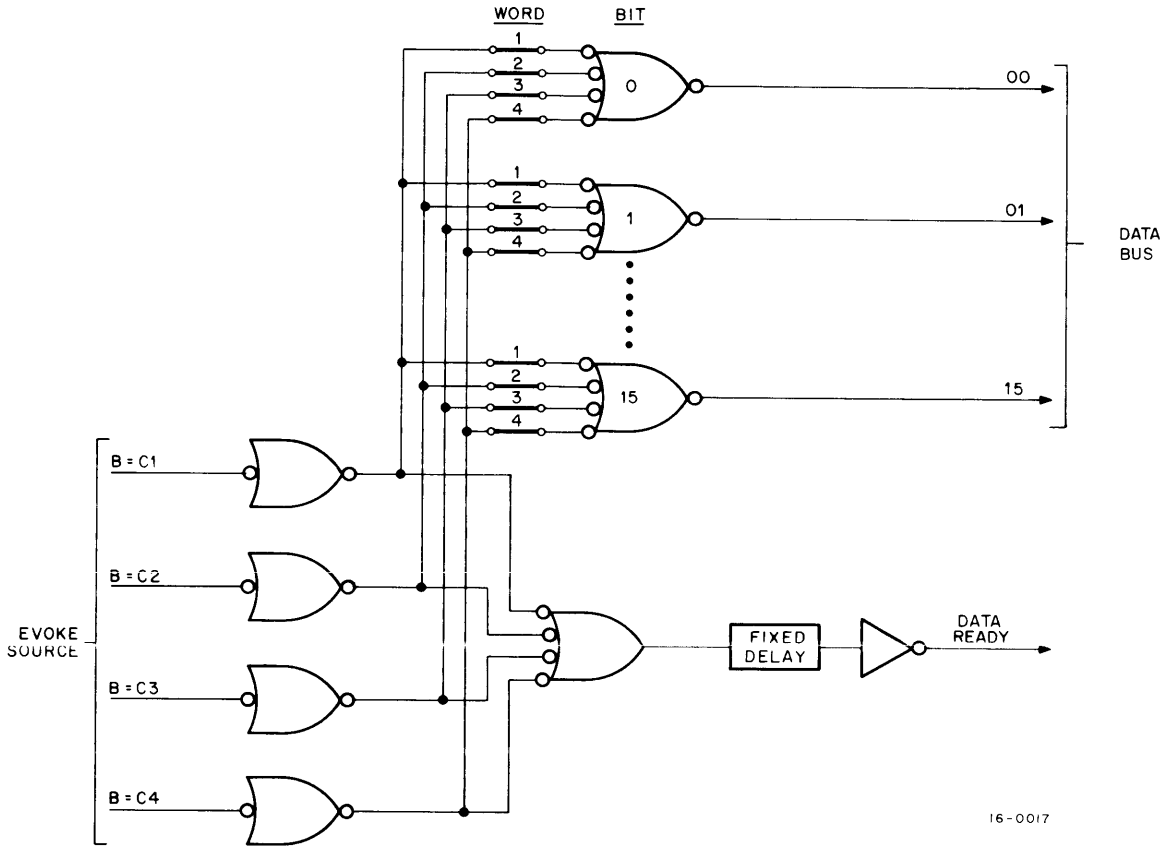


Figure 4-18 4-Word Constant Generator

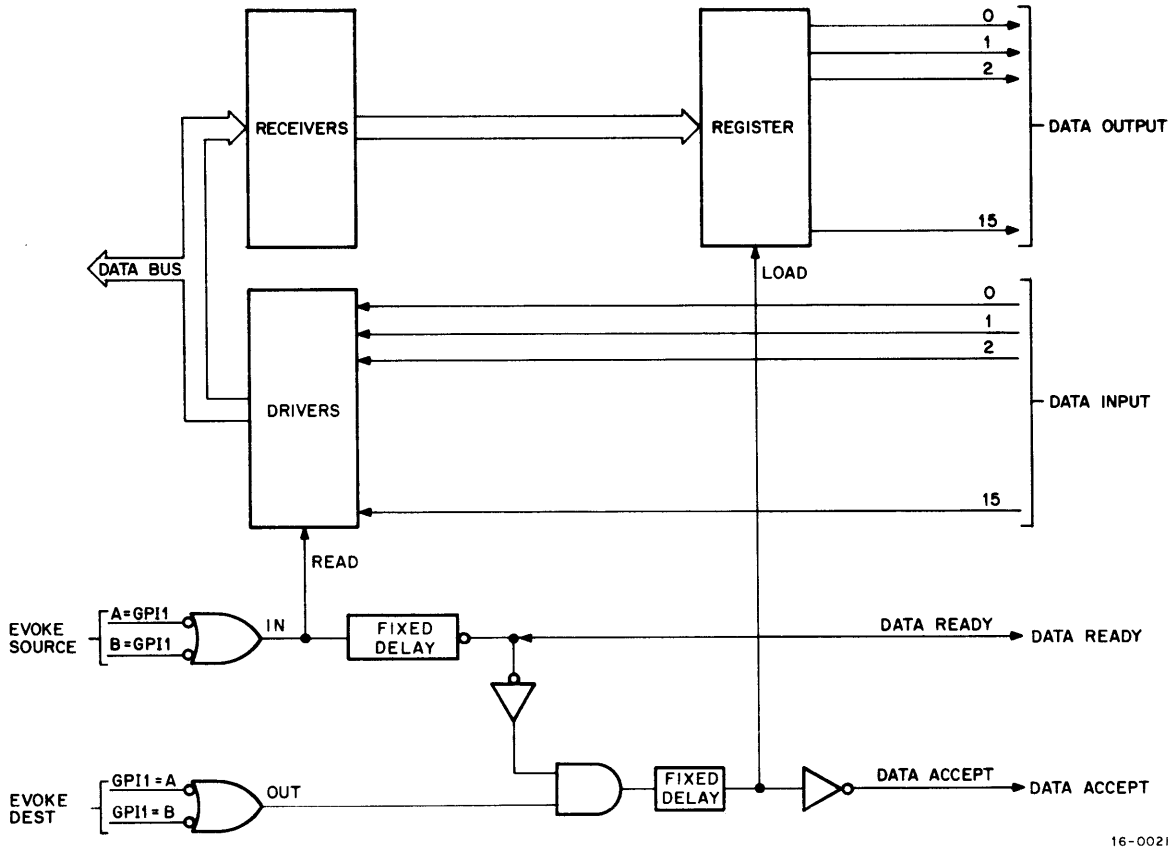
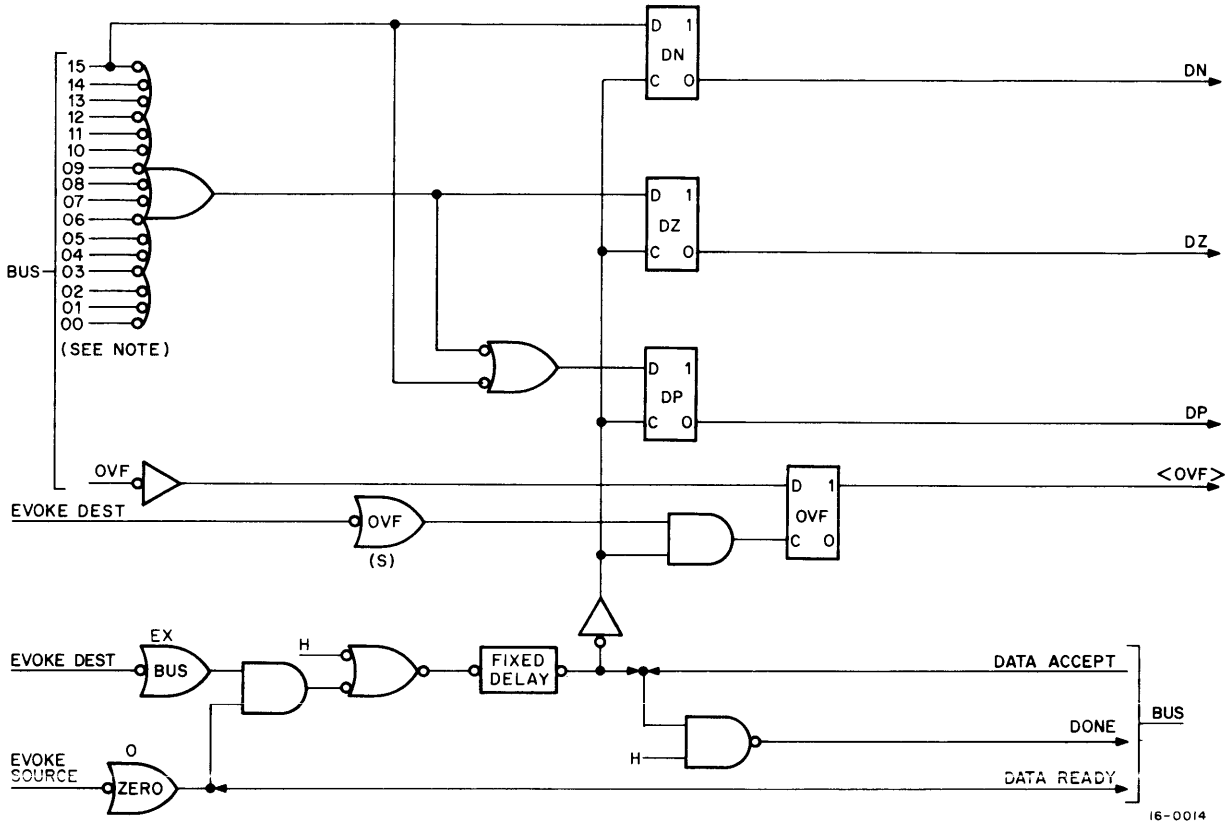


Figure 4-19 General Purpose Interface



NOTE:
Each data input line is terminated with a load and a current source.
(See schematic D-CS-M7332)

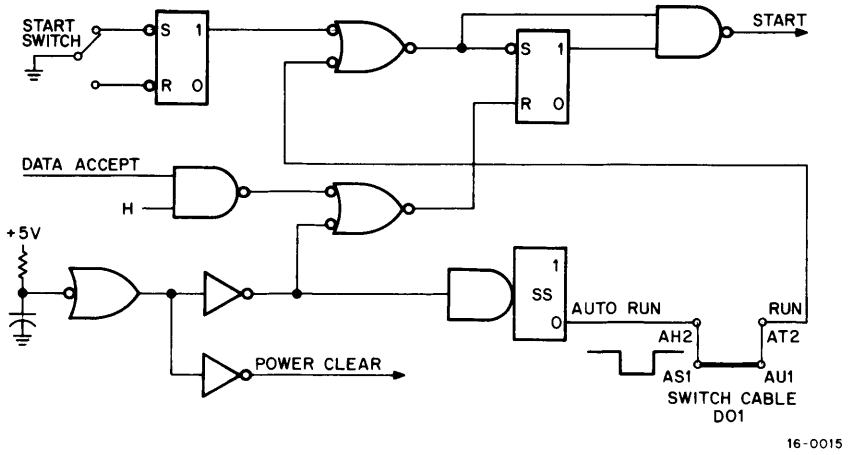


Figure 4-20 Bus Sense and Termination Module

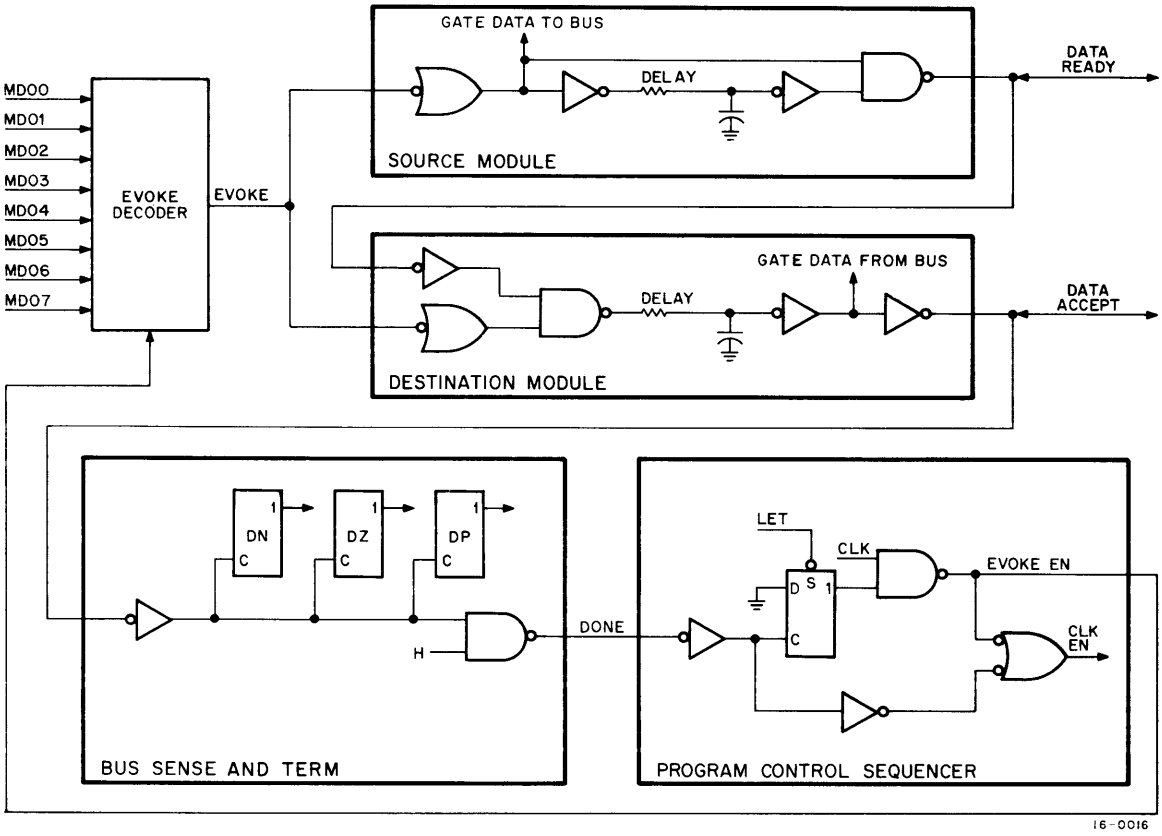


Figure 4-21 Data Transfer Timing Logic

CHAPTER 5
MAINTENANCE

5.1 PREPARATION FOR MAINTENANCE

The maintenance philosophy for the PDP16-M is to isolate the defective module by selective substitution in response to diagnostic program results.

5.1.1 Equipment Required

The following equipment is required to perform preventive and corrective maintenance on the PDP16-M.

a. PDP16-M Field Service Repair Kit (Table 5-1)

b. Oscilloscope – Tektronix type 453 or equivalent

c. Multimeter, Radio Shack J22846 or equivalent

d. Scope probes

e. Vacuum Cleaner

f. Nonflammable solvent

g. Clean soft cloth

Table 5-1
PDP16-M Field Service Repair Kit

Purpose	Description	Quantity	Part No.
Maintenance Module	Service Module KSM16	1	M7335
Maintenance Module	Option Switch Module KSL16	1	M7334
Maintenance Module	Bus Monitor KBM16	1	M7322
Maintenance Module	Interface Jumper Module	2	W971
Module	KAC16 GPA CONT	1	M7300
Module	KAR16 GPA REG	1	M7301
Module	MS16-A TR	1	M7305
Module	KFL16 FF4–6	1	M7306
Module	AND Gates	1	M1307
Module	AND Gates	1	M1103

Table 5-1 (Cont)
PDP16-M Field Service Repair Kit

Purpose	Description	Quantity	Part No.
Module	KEV16 EVOKE	1	M7310
Module	DB16-A GPI	1	M7311
Module	DCS16-A	1	M7313
Module	MS16-C SP	1	M7318
Module	MS16-D MEM	1	M7319
Module	MR16-D K	1	M7325
Module	PCS16-C EVOKE DEC	1	M7328
Module	PCS16-D MUX1	1	M7329
Module	KBS16-A BS	1	M7332
Module	PCS16-E PCS	1	M7336
Diagnostic ROM	PCS16-B DIAG PROM0	1	M7327 YA
Diagnostic ROM	PCS16-B DIAG PROM1	1	M7327 YB
Diagnostic ROM	PCS16-B DIAG PROM2	1	M7327 YC
Diagnostic ROM	PCS16-B DIAG PROM3	1	M7327 YD
Miscellaneous Parts			
Extender Module		1	W984
Mate-N-Lok Jumper Plugs		2	—
Extender Cables		2	7007222
Edge Connector		1	H851
Diagnostic Listings		2	

5.1.2 Maintenance Modules

Three special modules (options) have been designed by DEC to facilitate maintenance of the PDP16-M. These modules are:

a. Bus Monitor Module, M7322 (KBM16)

b. Service Module, M7335 (KSM16)

c. Option Switch Module, M7334 (KSL16)

5.1.2.1 Bus Monitor Module M7332 – The bus monitor (Figures 5-1 and 5-2), which plugs into slot A01 via extender cable 7007222, shows the operator what is on the 16-bit data bus and also if timing signals DA (DATA ACCEPT) and DR (DATA READY) are present. At power-on time, the DATA READY and DATA ACCEPT lights (LEDs) should be lit. No lights on the data bus should be lit. When the basic diagnostic is running correctly, the data bus lights will exhibit a down counter. Spare 1 and spare 2 lights represent the overflow and Link bits respectively under certain program conditions. When operating the PDP16-M under single step control, visual inspection of the LINK, OVERFLOW, DATA ACCEPT, and DATA READY signals is possible; the content of the bus can also be visually inspected.

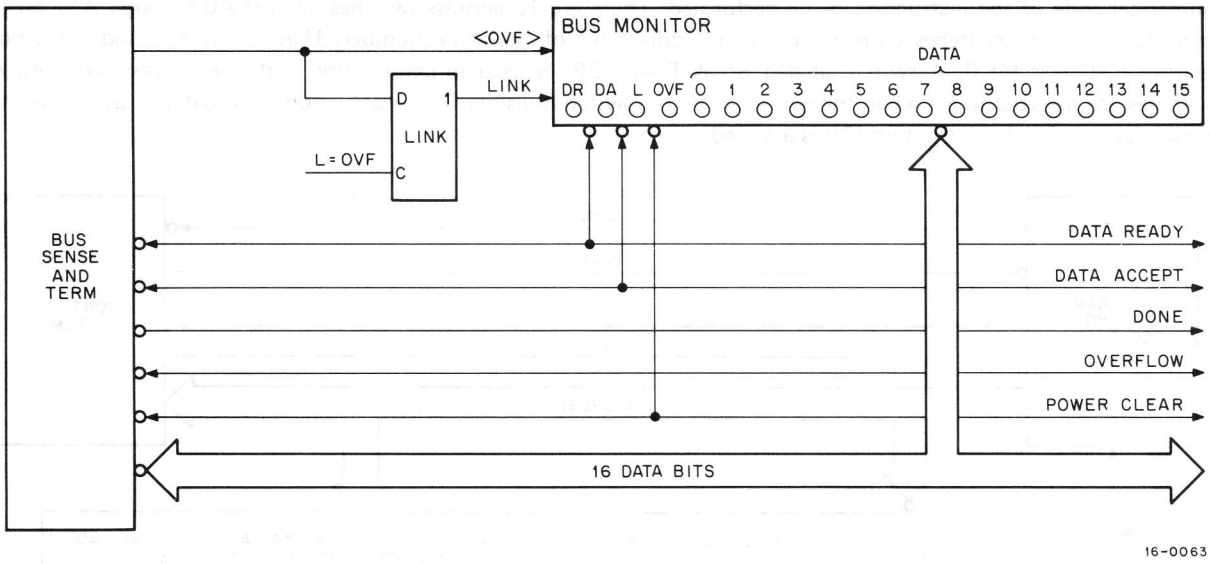


Figure 5-1 Bus Monitor Module M7322, Application Diagram

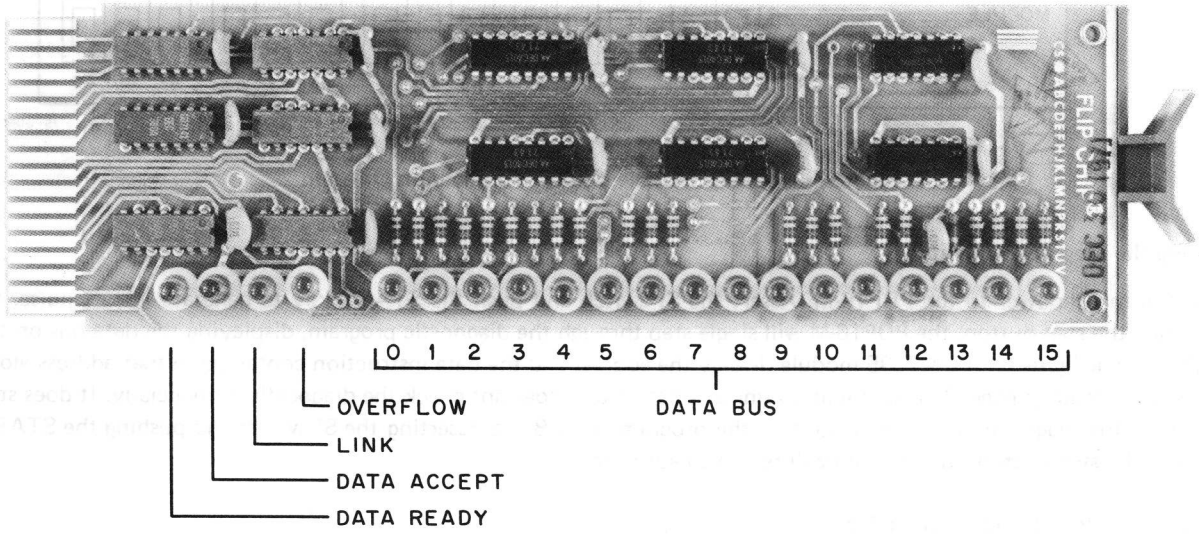


Figure 5-2 Bus Monitor Module M7322

5.1.2.2 Service Module M7335 – The service module plugs into slot B01 via extender cable 7007222. The M7335 module (Figures 5-3 and 5-4) contains an 8-bit Data Register and a 12-bit Address Register. Bits 10 and 11 of the Address Register are not used; bit 9 of the Address Register is the page bit. When lit, PAGE1 is selected and the opposite is true for PAGE0. Bits 0 through 8 contain the address; bits 0 through 7 of the Data Register contain the numerical code of the instruction being performed. There are 12 address switches labeled A0 through A11 on the module, and these switches correspond to the address bit of the same number. Hence switch 0 and bit 0 both represent address bit 0. A switch labeled Break Point (BP) is used in conjunction with the address switches. All switches are asserted to a 1 when the white dot on the switch is visible. The pushbutton step switch is used when the switch labeled Single Instruction (SI) is asserted.

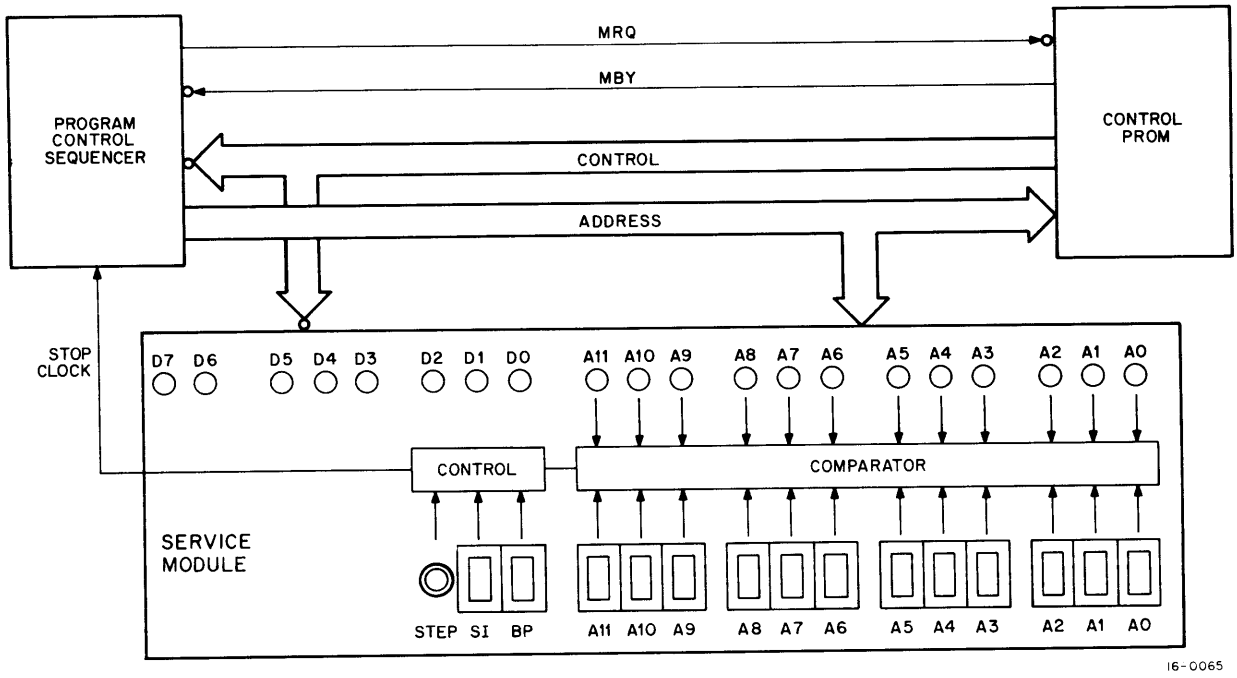


Figure 5-3 Service Module M7335, Application Diagram

Using the Step and SI Switches

First turn on power to the PDP16-M. Assert the SI switch and push the START key to generate a start pulse. By pushing the step button, the PDP16-M will single step through the diagnostic program, displaying the data bus on the M7322. The lights on the M7335 module display the address and the data instruction contained in that address along with the memory page. This is not an examine function and does not check the diagnostic sequencially. It does step through the diagnostic in the manner that the program runs. By de-asserting the SI switch and pushing the START key or the step button, the program will return to auto run.

Using the BP and Address Switches

The BP and address switches are used to halt the diagnostic at a particular address without having to single step through the program to that point. By asserting the BP switch, placing the desired stop address in the switches, setting page switch to the page desired, turning power on, and pushing the START key the PDP16-M will auto run until reaching the break point; it then halts. For example, assume the diagnostic failed at PAGE1 address 221 (1221). Using the break point feature, the program could be stopped at address 214 of PAGE1 (1214) and the single step feature could then be employed. This avoids having to single step through the entire diagnostic. To use the break point function, the address selected has to contain an instruction being performed by the program. Locations that contain jump addresses or HALT commands should not be used as break points. The break point halt will occur before the instruction is executed. Refer to the diagnostics listing to select an appropriate break point address.

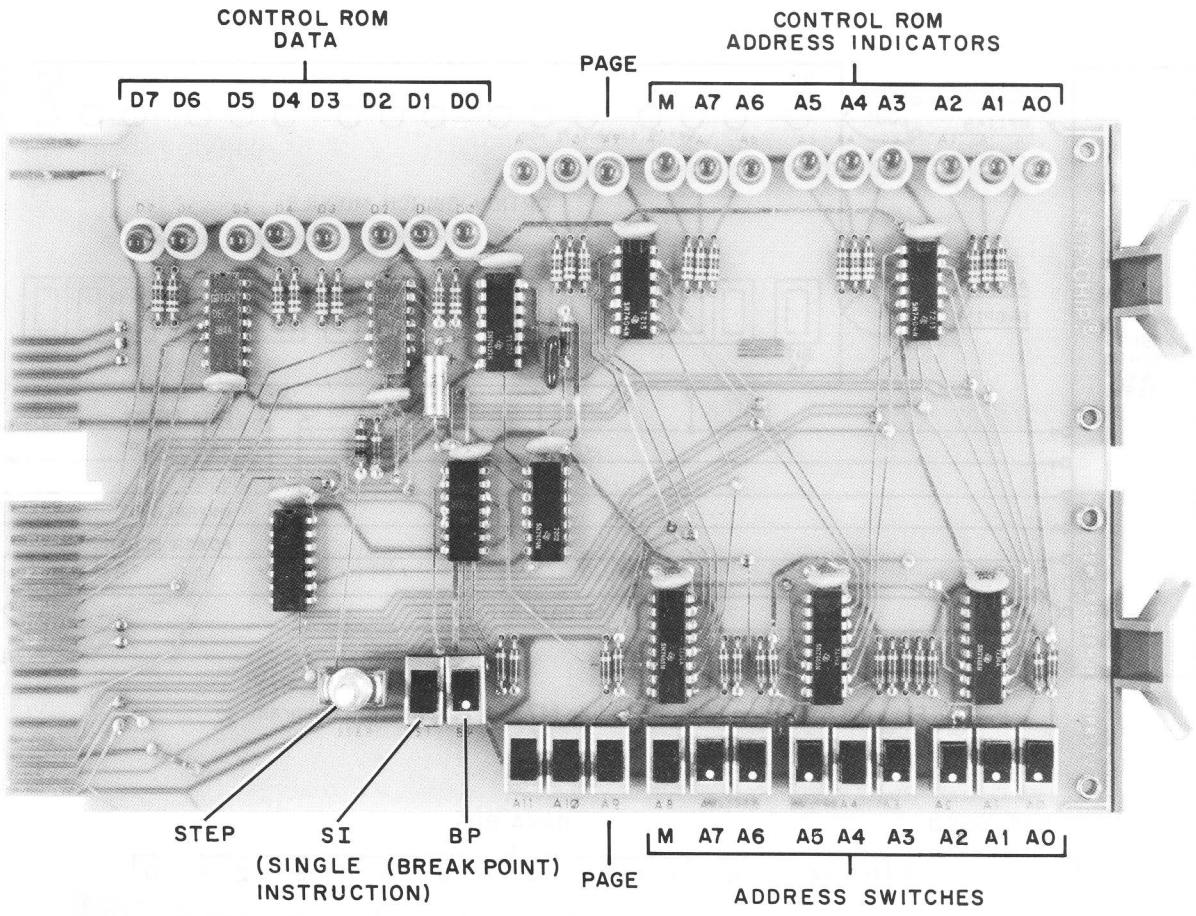


Figure 5-4 Service Module M7335

5.1.2.3 Option Switch Module M7334 – To run the option diagnostic, steps 5 through 7 of Paragraph 5.1.4 must be completed and the basic diagnostic must have run without error. The M7334 module (Figures 5-5 and 5-6) has a 16-bit Data Register and 16 switches. Each switch identifies a particular option to the diagnostic program. In only one application is more than one switch used at a time. To test an option, find the desired switch setting in Table 5-2 and assert the switch to a 1 (white dot showing). In situations where data is to be examined, the Data Register will contain the data read.

The diagnostics have been written to test for correct data and to identify and isolate inoperative register bits. For instance, a register is loaded with a particular bit pattern, read back, and tested to determine if the data is the same. If it is not, the program will illuminate the Data Register lights that are not correct and halt. This feature of the diagnostics is helpful in troubleshooting modules.

Set the desired switch setting, turn power on, and run the diagnostic single step or auto, using the instructions in Table 5-2.

5.1.3 Maintenance Programs

The MAINDEC diagnostics required for this procedure have been preloaded into the M7327 PROMs and are designated M7327 YA to YD. These modules are included in the repair kit listed in Table 5-1. The M7327 YA and M7327 YB modules, which plug into slots C16 and D16, respectively, are PAGE0 or the option diagnostic. Slots C17 and D17 house the M7327 YC and YD modules, respectively. These modules contain the basic diagnostic or PAGE1. The diagnostic listings are also included in the repair kit listed in Table 5-1.

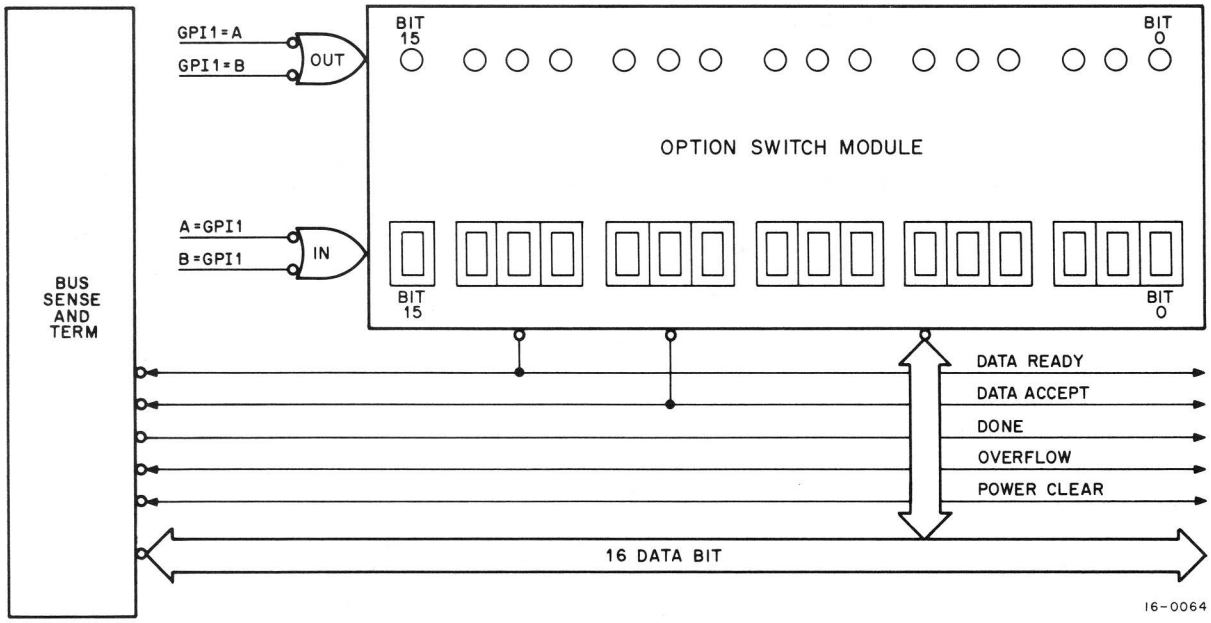


Figure 5-5 Option Switch Module M7334, Application Diagram

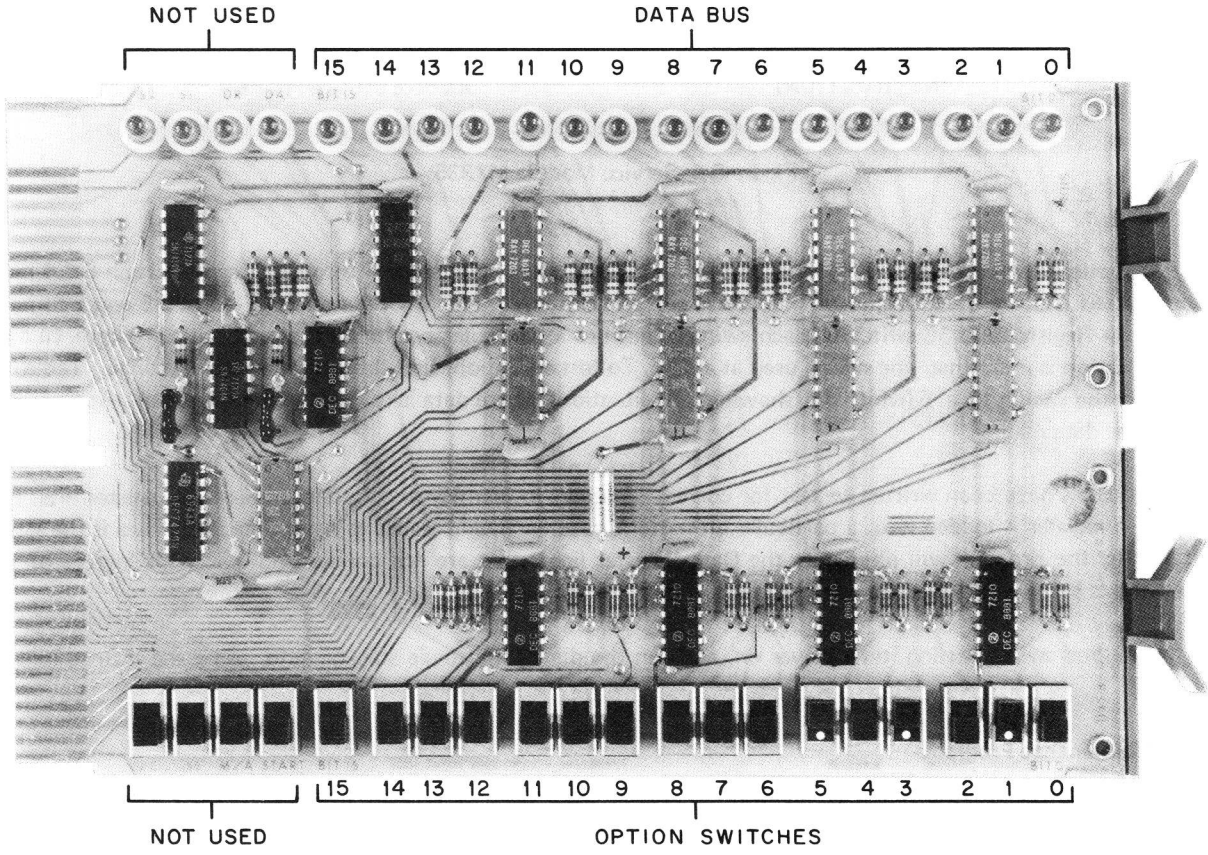


Figure 5-6 Option Switch Module M7334

Table 5-2
Option Diagnostic Key

Switch	Option	Slot No.	Module Tested	Run Mode	Symptoms of Correct Operations	Option Test Times
0	DB16-A	AB13	M7311	Single Step & Auto	Using single step, watch the bus monitor up count the data bus to a count of 10_8. Put into auto run and watch up count. Runs until error or power down.	10 min.
1	DB16-A	AB14	GPI3 M7311	Single Step & Auto	Same as switch 0. Up count starts at 2_8.	10 min.
2 & 15	DB16-A	AB15 C/D15	DATA PROM M7311 M7327	Single Step	RUN light OFF. Proper data displayed in the light Switch Register on M7334 Control Module. 134701 152303 161375 011707 007301 133762 005377 007746 147420 005750 134420 152352 161020 000457 054346 000021 055671 002456	If customer PROM, check all locations.
3	MR16-D	AB8	CONSTANT GEN M7325	Single Step	RUN light OFF and 177773 displayed in the light Switch Register (M7334).	15 min.

Table 5-2 (Cont)
Option Diagnostic Key

Switch	Option	Slot No.	Module Tested	Run Mode	Symptoms of Correct Operations	Option Test Times
4	MS16-D	A6	MEM1 M7319	Auto	RUN light ON. Bus monitor lights all on and flickering.	30 min.
5	MS16-E	A7	MEM2 M7324	Auto	RUN light ON. Same as switch 4.	30 min.
6	MS16-C	A4	SP1–16 M7318	Auto	RUN light ON. Shows an up count in the bus monitor.	20 min.
7	MS16-C	A3	SP17–32	Auto	Same as switch 6.	20 min.
8	DC16-A	A16	SI1 M7313	Auto	RUN light OFF and OCTAL 400 is displayed in the light Switch Register (M7334), after the program HLTS in LOC 0313. Test shows an up count to 400_8 in the bus monitor lights.	25 times
9	DC16-A	A17	SI2 M7313	Auto	Same as switch 8.	25 times
10	KFL16	D2	FF4–6 M7306	Auto	RUN light ON and bits 4 and 5 are ON in the bus monitor. 177777 displayed in Switch Register and lights on M7334.	10 min.
11					Not used.	
12	DA16-F	D14	PDP-11 INT M623	Single Step & Auto	RUN light is ON and data lights in the bus monitor are ON. Single step until the data bus seems to complement.	10 min.
13 – 14					Not used.	
15					Used with switch 2.	

5.1.4 Maintenance Setup

1. Remove the customers PCS16-B, M7327 memory PROM or PROMs and replace with the four diagnostic M7327 YA – YD memory PROMs. Place M7327 YA in slot C16, M7327 YB in slot D16, M7327 YC in slot C17, and M7327 YD in slot D17 (Figure 5-7). Slots D16 and D17 contain the basic diagnostic and slots C16 and C17 contain the option diagnostic.

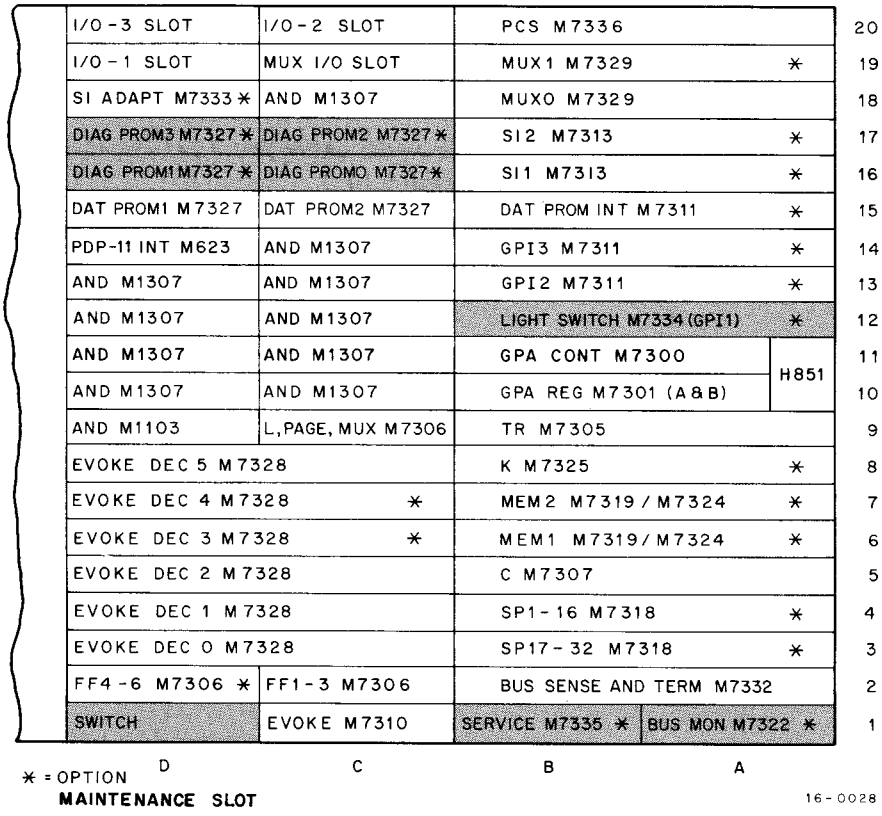


Figure 5-7 Logic Assembly Maintenance Configuration Diagram

2. Insert input/output jumper modules No. 1 and No. 2 (W971) in slots CD19 and CD20, respectively, and connect Mate-N-Lok serial I/O jumper plugs on module M7333 located in slot D18.

NOTE

The user must install jumper wires on these modules and Mate-N-Lok plugs before they can be installed. Refer to Appendix B for details.

3. Insert two 7007222 cables, one in slot A01 and one in B01.

4. Insert M7322 Bus Monitor into the cable from slot A01. Insert M7335 Service Module into the cable from slot B01. The M7335 is a double-width module and the cable is inserted over the A section of the output/input "Gold Fingers."

NOTE

The basic diagnostic is now ready to run. Press the START switch and allow the basic diagnostic to run for 10 minutes.

5. To run the option portion of the diagnostic, remove the M7311 from slot AB12 and insert the M7334 Option Switch Module on a double extender module (W984).

NOTE
The basic and option diagnostics will not run at the same time.

6. Remove the M7327 YC and YD modules from slots C17 and D17 and place in slots C15 and D15.

7. Run the appropriate option test following the switch setting and times specified in Table 5-2 and the maintenance procedure on the M7334 in Paragraph 5.1.2.3.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of procedures performed prior to the initial operation of the computer and periodically during its operating life. These procedures include visual inspections, cleaning, mechanical checks, and operational testing. A log should be kept for recording specific data that indicates the performance history and rate of deterioration; such a record can be used to determine the need and time for performing corrective maintenance on the system.

Scheduling of computer usage should always include specific time intervals set aside for scheduled maintenance purposes. Careful diagnostic testing programs can then reveal problems which may only occur intermittently during on-line operation (Paragraph 5.1).

Digital Equipment Corporation suggests the schedule defined in Table 5-3.

5.3 CORRECTIVE MAINTENANCE

5.3.1 Repair Procedure

Always follow the Repair Procedure Flow Diagram in Figure 5-8. Strict adherence to this flow will ensure the most efficient use of your time (Paragraph 5.1). For this procedure, the basic diagnostic errors have been divided into two sections: control and data.

a. Data error: A data error occurs when the diagnostic halts at a legal location having a data code of 271 (HLT). The RUN light will be off. By checking the 8-bit data lights on the M7335 (for a 271) and the address location in the diagnostic listing, a data error can be suspected. For these type failures, swap the modules as described in Paragraph 5.3.2.1.

b. Control error: A control error is to be assumed if the PDP16-M halts or the program hangs up at any location except a legal halt. If this is the case, swap the modules as described in Paragraph 5.3.2.2.

The M7307 4-word Constant Generator (C) is tested for proper timing circuitry only when the basic diagnostic is in auto run. To examine the 4 words, check the jumpers to see what they are cut for. Using the break point function, halt the program at location 1242. Single step the program and visually check the data on the M7322 Bus Monitor data bus.

Table 5-3
Preventive Maintenance Schedule
(3 months or 500 hours)

Type		Action
Cleaning	a.	Clean the exterior and interior of the computer cabinet, using a vacuum cleaner and/or clean cloths moistened in nonflammable solvent.
	b.	Clean the air filter. Use a vacuum cleaner to remove accumulated dirt and dust, or wash with clean hot water and thoroughly dry before using.
Lubricate		Lubricate slide mechanisms and casters with a light machine oil or powdered graphite. Wipe off excess oil.
Inspect	a.	Visually inspect equipment for general condition. Repaint any scratched areas.
	b.	Inspect all wiring and cables for cuts, breaks, fraying, wear, deterioration, kinks, strains, and mechanical security. Tape, solder, or replace any defective wiring or cable covering.
	c.	Inspect the following for mechanical security: key switch, lamps, connectors, transformers, fans, capacitors, etc. Tighten or replace as required.
	d.	Inspect all module mounting panels; be sure that each module is securely seated in its connector. Remove and clean any module that may have collected excess dirt or dust.
	e.	Inspect power supply components for leaky capacitors, over-heated resistors, etc. Replace any defective components.
	f.	Check the output of the H740 Power Supply as specified in Paragraph 5.3.1. Use a multimeter to make these measurements without disconnecting the load. If any output voltage is not within tolerance, the supply is considered defective, and corrective maintenance should be performed.
Perform	a.	Run all relevent diagnostic programs to verify proper computer operation. Each program should run for the time specified in Paragraph 5.1.4.
	b.	Enter preventive maintenance results in the log book.

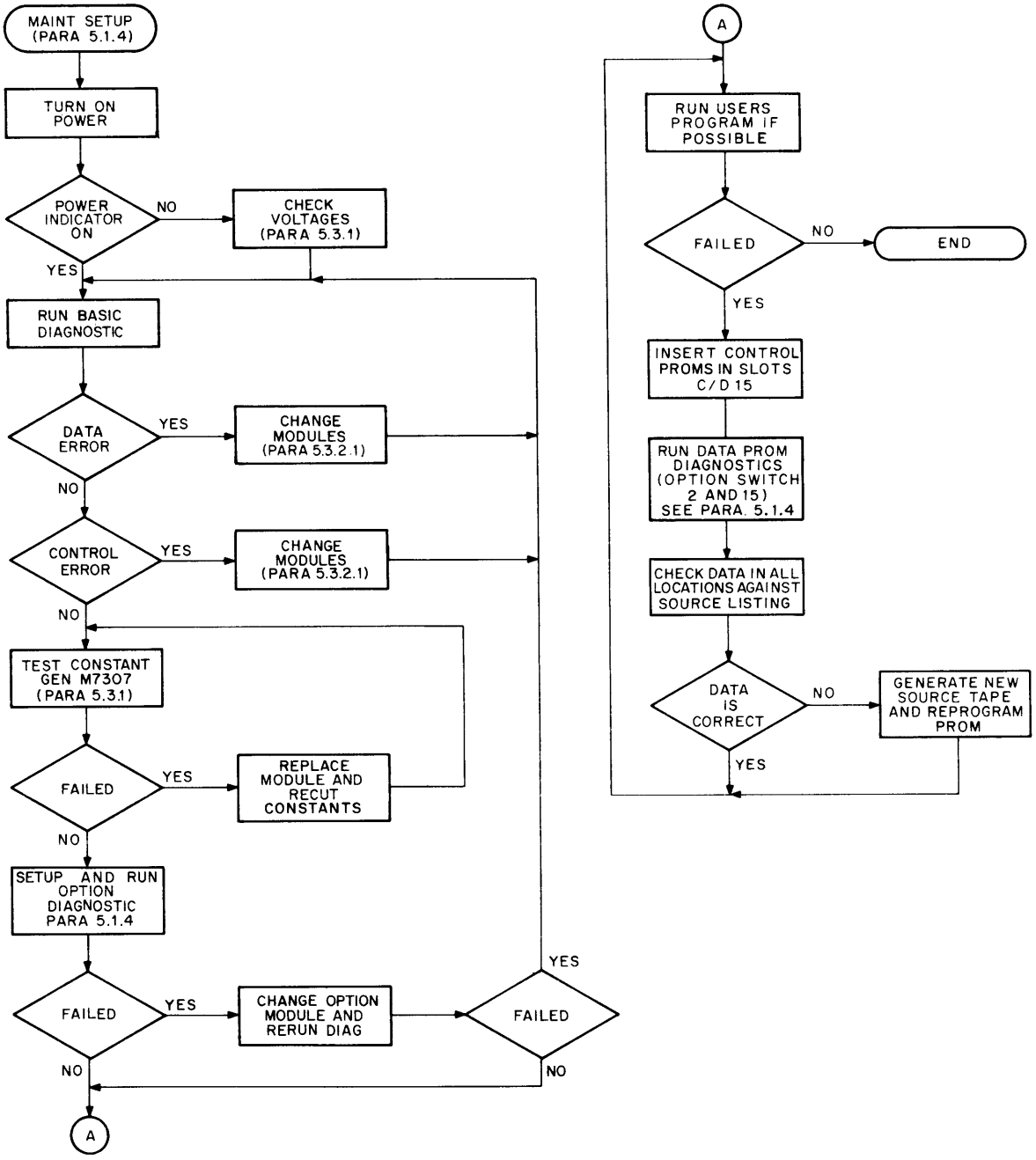


Figure 5-8 Repair Procedure Flow Diagram

When power supply problems are suspected, the H740 Power Supply can be checked by referring to Table 5-4. Controls and fuses are identified in Figure 5-9.

Table 5-4
DC Voltages

Wire Color	Voltages (dc)
Red	+4.8 to +5.2 Vdc
Blue	-14.5 to -15.5 Vdc
Black	GND
Orange	+1.0V to +2.0V
Gray	+2.8V to +5.5V

Maintenance of the data control bus may be required if the basic philosophy of the module swapping does not fix the problem. The bus must then be checked for broken, nicked, or burnt wires, broken or bad pins, loose wirewraps, and for any obstructions in the bus slots or pins. If the bus is to be checked, first turn off power and unplug the ac cord. Remove the four screws under the chassis that hold the bus in place. Lift the bus out, being careful not to bend any logic pins. The power harness is long enough to enable the bus to remain hooked up for dc power.

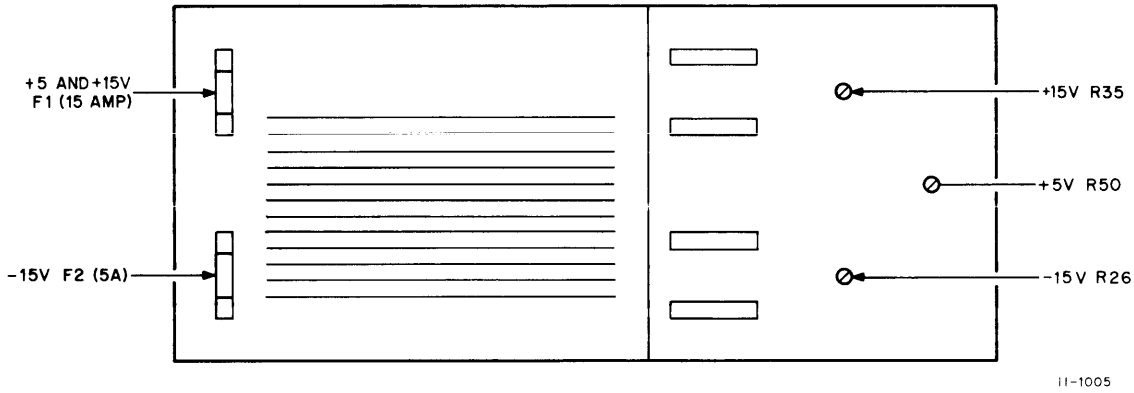


Figure 5-9 H740 Power Supply Fuses and Adjustment Controls

5.3.2 Module Swapping Priorities

5.3.2.1 Data Error – For a suspected data error, swap the modules listed in the exact order written. Strict adherence to this list will ensure the most efficient use of your time.

Module	Slot No.
M7336	AB20
M7332	AB02
M7300	AB11
M7301	AB10
M7311	AB12
M7305	AB09
M7307	AB05
M7306	C09
M7306	C02

Swap modules listed in Paragraph 5.3.2.2 before swapping the modules below.

M1307	C10 to C14, C18, D10, D13
M1103	D9

5.3.2.2 Control Error – For a suspected control error, swap the modules listed in the exact order written. Strict adherence to this list will ensure the most efficient use of your time.

Module	Slot No.
M7336	AB20
M7332	AB02
M7328	CD03
M7328	CD04
M7328	CD05
M7328	CD08
M7306	C09
M7310	C01
M7329	AB18
M1307	D13
M1307	C18
M1307	C14

APPENDIX A
HARDWARE OPTION DESCRIPTIONS

All memory (control and data) and I/O options that are offered for the PDP16-M are discussed in this appendix. Each option is covered in a separate description. The descriptions include details on operation, installation, and programming. The options covered are:

DA16-F	PDP-11 Peripheral Interface (M623)
DB16-A	Parallel I/O (M7311)
DC16-A	Serial I/O (M7313)
KFL16	Boolean Outputs/Flags (M7306)
MR16-D	Constant Generator (M7325)
MR16-E/F	Data PROM (M7327)
MS16-C	Scratch Pad Register (M7318)
MS16-D	Data R/W MOS Memory (M7319)
MS16-E	Data R/W MOS Memory (M7324)
PCS16-B	Control PROM (M7327)
PCS16-D	Boolean Input Multiplexer (M7329)

Maintenance procedures including details on diagnostic tests for the options are presented in Chapter 5.

DA16-F
PERIPHERAL INTERFACE OPTION (M623)

The PDP16-M has been prewired to interface with PDP-11 peripheral devices that do not need to become master devices. Only accumulator-type transfers can transpire between the PDP16-M and PDP-11 peripherals. One prewired module slot, slot D14, is reserved on the logic assembly for installing the DA16-F option (module M623). This module contains AND gate bus drivers that interface with the data transfer interlock control signals of the PDP16-M and the PDP-11 device (Figure 1). In addition to the M623 module, the following items are also required when connecting a PDP-11 device to a PDP16-M:

1. One H803 Connector Block
2. Three BC02X-05 or three BC03H-05 cables
3. One KTM16 Bus terminator option (M962)

NOTE

A BC11A cable (preferably BC11A-02) is also required. This cable is supplied with the PDP-11 peripheral device.

The control signals, the address, and the data required for operating a PDP-11 peripheral are distributed between three slots on the PDP16-M logic assembly. Therefore, three cables are necessary. Since the pin assignments for the various signals on the PDP16-M I/O slots do not match those of the PDP-11 device input slot, an H803 Connector Block is employed to match the signals through wire wrapping. In addition, the H803 Connector Block is used to provide ground and +3V to certain PDP-11 device input lines. Figure 2 and Table 1 detail the pins on the connector block to be wire wrapped.

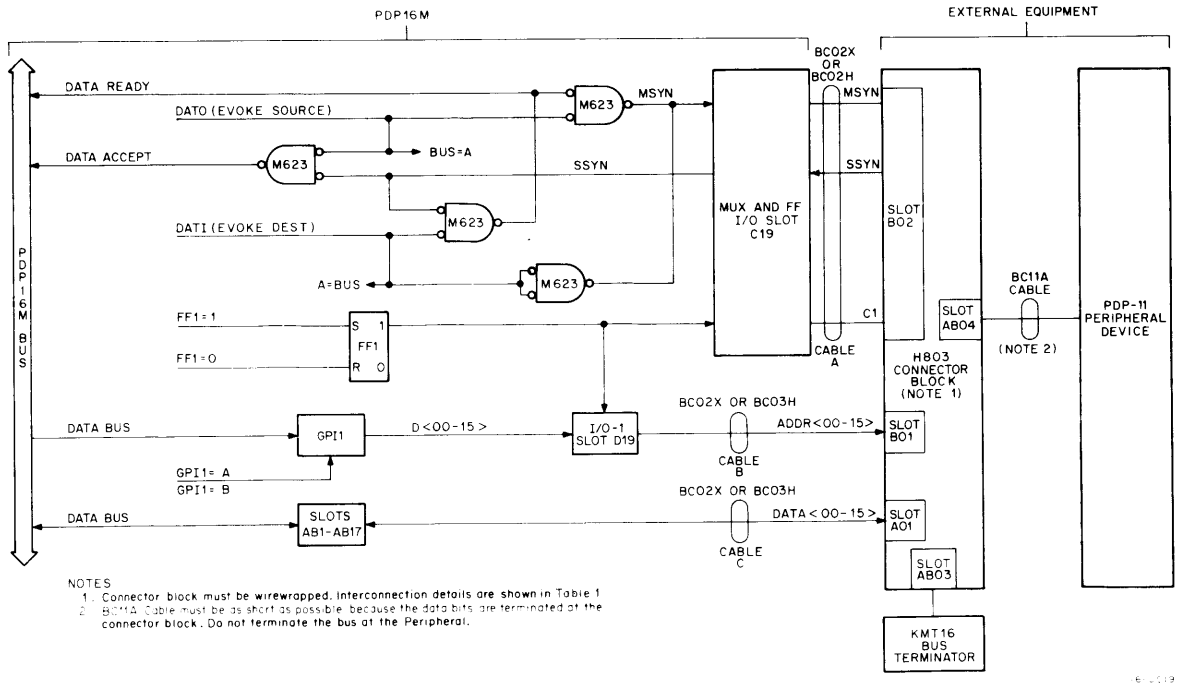


Figure 1 PDP-11 Peripheral Interface Option DA16-F, Block Diagram

After the H803 Connector Block is wire wrapped, the cables can be installed as shown in Figure 1. The KTM16 option must be installed in slot A03 of H803 to terminate the data bus.

The instructions that evoke data transfers between the PDP16-M and the PDP-11 peripheral devices are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). No additional evoke decoders are required. Besides the instructions expressly implemented for transferring data to or from the peripheral, some standard instructions are also used in programming the data transfers because of the manner in which the device is interfaced with the PDP16-M. That is, FF1 is used as a flag to denote the direction (input or output) of the data transfer, and GPI1 is used to transfer the device address.

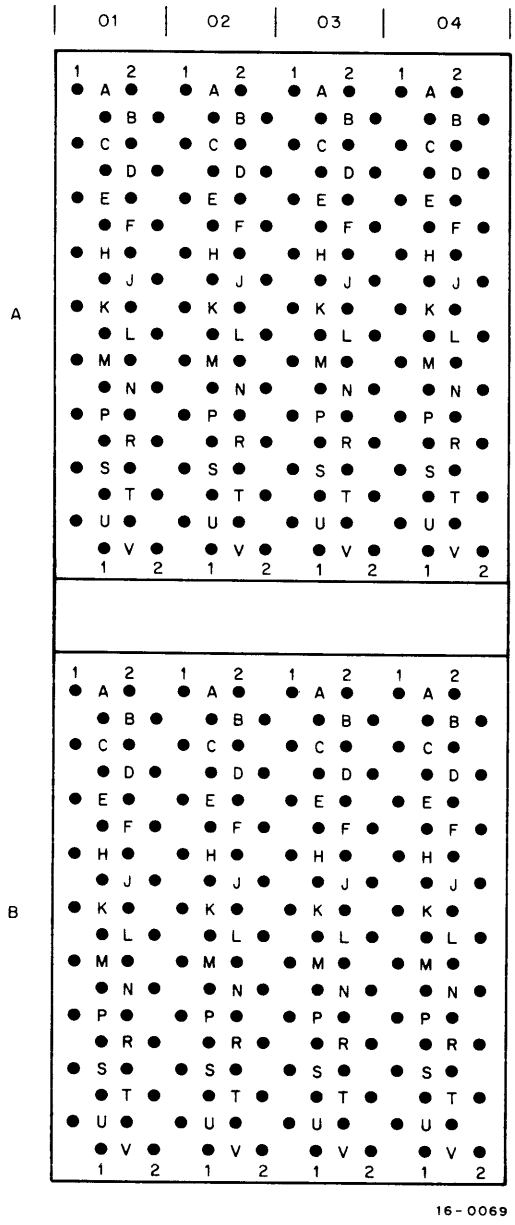


Figure 2 H803 Connector Block, Pin Assignments

The machine code (octal), execution time, and description of all instructions relevant to programming data transfers between the PDP16-M and the PDP-11 peripheral device follow:

SEND DATA TO DEVICE

Evoke (Octal Code)	Time (μsec)	Instruction	Description
057	1.8	FF1 = 1	Prepare input section of device.
040	2.2	GPI1 = A	Send address to device from A Register.
255	2.2	GPI1 = B	Send address to device from B Register.
275	–	DATO	Send data from A Register to device.

READ DATA FROM DEVICE

Evoke (Octal Code)	Time (μsec)	Instruction	Description
056	1.8	FF1 = 0	Prepare output section of device.
040	2.2	GPI1 = A	Send address from A Register to device.
255	2.2	GPI1 = B	Send address from B Register to device.
274	–	DATI	Read device data into A Register.

A summary of PDP-11 low-speed peripheral device addresses, status registers, and control registers is given in Appendix A of the *PDP16-M User's Guide.* When addressing a PDP-11 device, the complement of the given address must be used because the address lines are driven with TTL levels from GPI1 rather than open-collector drivers.

NOTE

A new PDP-11 Peripheral Interface option, Unibus converter/I/O Interface Module, will be available in the future. This option will simplify the interfacing procedure.

Table 1
H803 Connector Block Wire-Wrap Connections

PDP16-M Signal Name	From	To	From	To	PDP-11 Signal Name
+5V	*A01A2	A04A2	A04A2	B04A2	+5V
GND	*A01C2	A04C2	A04C2	A04T1	GND
GND	*A01T1	A04T1	A04T1	B04C2	GND
			B04C2	B04T1	GND
+5V	*B01A2			B04A2	+5V
GND	*B01C2			B04C2	GND
GND	*B01T1			B04T1	GND
+5V	A01A2	A03A2	A03A2	B03A2	+5V
+5V	B01A2			B03A2	+5V
GND	A01C2	A03C2	A03C2	B03C2	GND
GND	B01C2			B03C2	GND
GND	A01T1	A03T1	A03T1	B03T1	GND
GND	B01T1			B03T1	GND

Table 1 (Cont)
H803 Connector Block Wire-Wrap Connections

PDP16-M Signal Name	From	To	From	To	PDP-11 Signal Name
DATA BIT 00	A01A1	A03A1	A03A1	A04C1	D00
DATA BIT 01	A01B1	A03B1	A03B1	A04D2	D01
DATA BIT 02	A01C1	A03C1	A03C1	A04D1	D02
DATA BIT 03	A01D1	A03D1	A03D1	A04E2	D03
DATA BIT 04	A01E1	A03E1	A03E1	A04E1	D04
DATA BIT 05	A01F1	A03F1	A03F1	A04F2	D05
DATA BIT 06	A01H1	A03H1	A03H1	A04F1	D06
DATA BIT 07	A01J1	A03J1	A03J1	A04H2	D07
DATA BIT 08	A01K1	A03K1	A03K1	A04H1	D08
DATA BIT 09	A01L1	A03L1	A03L1	A04J2	D09
DATA BIT 10	A01M1	A03M1	A03M1	A04J1	D10
DATA BIT 11	A01N1	A03N1	A03N1	A04K2	D11
DATA BIT 12	A01P1	A03P1	A03P1	A04K1	D12
DATA BIT 13	A01R1	A03R1	A03R1	A04L2	D13
DATA BIT 14	A01S1	A03S1	A03S1	A04L1	D14
DATA BIT 15	A01U1	A03U1	A03U1	A04M2	D15
+3V			B03A1	B04F1	ACLO
+3V			B03B1	B04F2	DCLO
D00	B01B2			B04H2	A00
D01	B01D2			B04H1	A01
D02	B01E2			B04J2	A02
D03	B01F2			B04J1	A03
D04	B01H2			B04K2	A04
D05	B01J2			B04K1	A05
D06	B01K2			B04L2	A06
D07	B01L2			B04L1	A07
D08	B01M2			B04M2	A08
D09	B01N2			B04M1	A09
D10	B01P2			B04N2	A10
D11	B01R2			B04N1	A11
D12	B01S2			B04P2	A12
D13	B01T2			B04P1	A13
D14	B01U2			B04R2	A14
D15	B01V2			B04R1	A15
GND			B04T1	B04S2	A16
GND			B04S1	B04S1	A17
+3V			B03C1	B04U2	C0
MSYN	B02K2	B03D1	B03D1	B04V1	MSYN
SSYN	B02V2	B03E1	B03E1	B04U1	SSYN
FF1	B02N2			B04T2	C1
GND	B02T1			B04T1	GND

* Use 933 Bus Strips for these connections (power and ground). For all other connections, use 24 AWG bus wire.

DB16-A
PARALLEL I/O OPTION (M7311)

One parallel I/O channel (GPI1) is included in the basic PDP16-M. Two additional channels can be added by implementing one DB16-A option (module M7311) for each channel. Two prewired module slots are reserved on the PDP16-M logic assembly for installing the M7311 I/O modules. Both slots are wired directly to the PDP16-M register transfer bus. The module slots are also wired to I/O slots on the logic assembly to facilitate convenient interfacing to external equipment. To implement either I/O channel, it is necessary only to install the option module in one of the assigned slots. No other wiring or set-up procedure is required except to connect the external equipment to the interfacing I/O slot. Refer to Chapter 2 of the *PDP16-M User's Guide* for interfacing details.

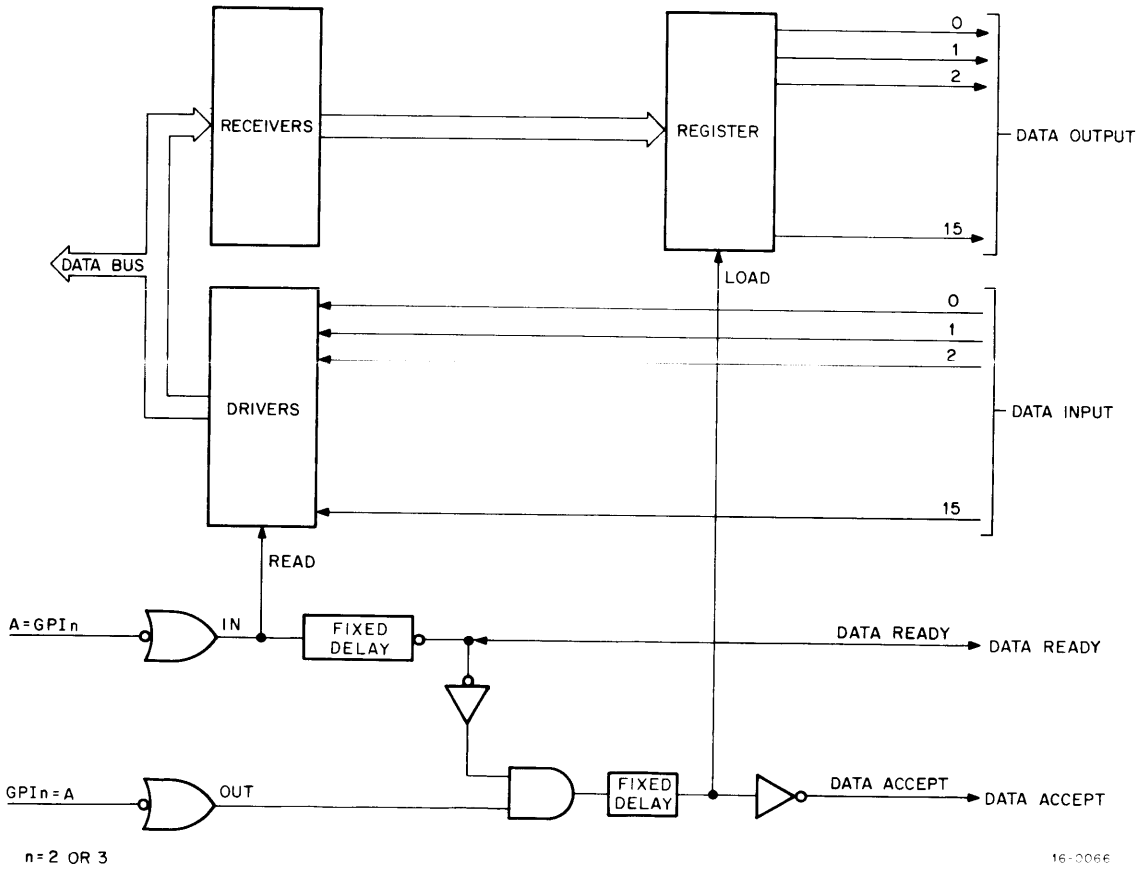


Figure 1 Parallel I/O Option DB16-A, Block Diagram

The M7311 I/O module contains 16 bus receivers and drivers, a 16-bit data output register, and evoke logic (Figure 1). The module is identical to the one used for the standard I/O channel in the basic PDP16-M. The register outputs and receiver inputs (bus drivers) are TTL levels. Each output bit of the register can drive up to 10 unit loads (16 mA) and each receiver input must be driven with at least 1 unit load (1.6 mA). The two prewired I/O module slots are each assigned a different mnemonic for programming reasons. The mnemonics are: GPI2 for slot AB13 and GPI3

for slot AB14. The instructions that evoke data transfers between the PDP16-M and the external equipment via the parallel I/O channels are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). No additional evoke decoders are required. The machine code (octal), execution time, and description of each instruction follows:

CHANNEL NO. 2 (GPI2)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
042	2.2	GPI2 = A	GPI2 gets A (Data Out)
043	2.0	A = GPI2	A gets GPI2 (Data In)

CHANNEL NO. 3 (GPI3)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
044	2.2	GPI3 = A	GPI3 gets A (Data Out)
045	2.0	A = GPI3	A gets GPI3 (Data In)

Notice that the B Register cannot be used in programming data transfers via the optional parallel I/O channels. However, both A and B Registers can be used in programming data transfers via the standard parallel I/O channel (GPI1) (Paragraph 4.3.4).

Output data is preserved (buffered) in the output data register until another output data transfer is executed. Input data, however, is not buffered and can therefore change at any time.

Input and output data may or may not be structured, depending on the application. If data is to be transferred sequentially to or from the external equipment, it may be necessary to synchronize the transfers to accommodate the operating speed of the external equipment. The FF_n output, the EXT_n input, or one or more I/O data bits can be employed as flags for synchronizing the data transfers.

It is for this reason that the FF1–3 outputs are wired to the respective parallel I/O interface slots. The state of the FF_n outputs, the EXT_n inputs, and the odd data bits (A Register contents) can be tested using the IF instruction to facilitate their use in synchronizing data transfers.

For example:

```
IF FF2, LABEL1
IF FF3, LABEL2
IF EXT1, LABEL3
IF A<1>, LABEL 4
IF A<3>, LABEL 5
```

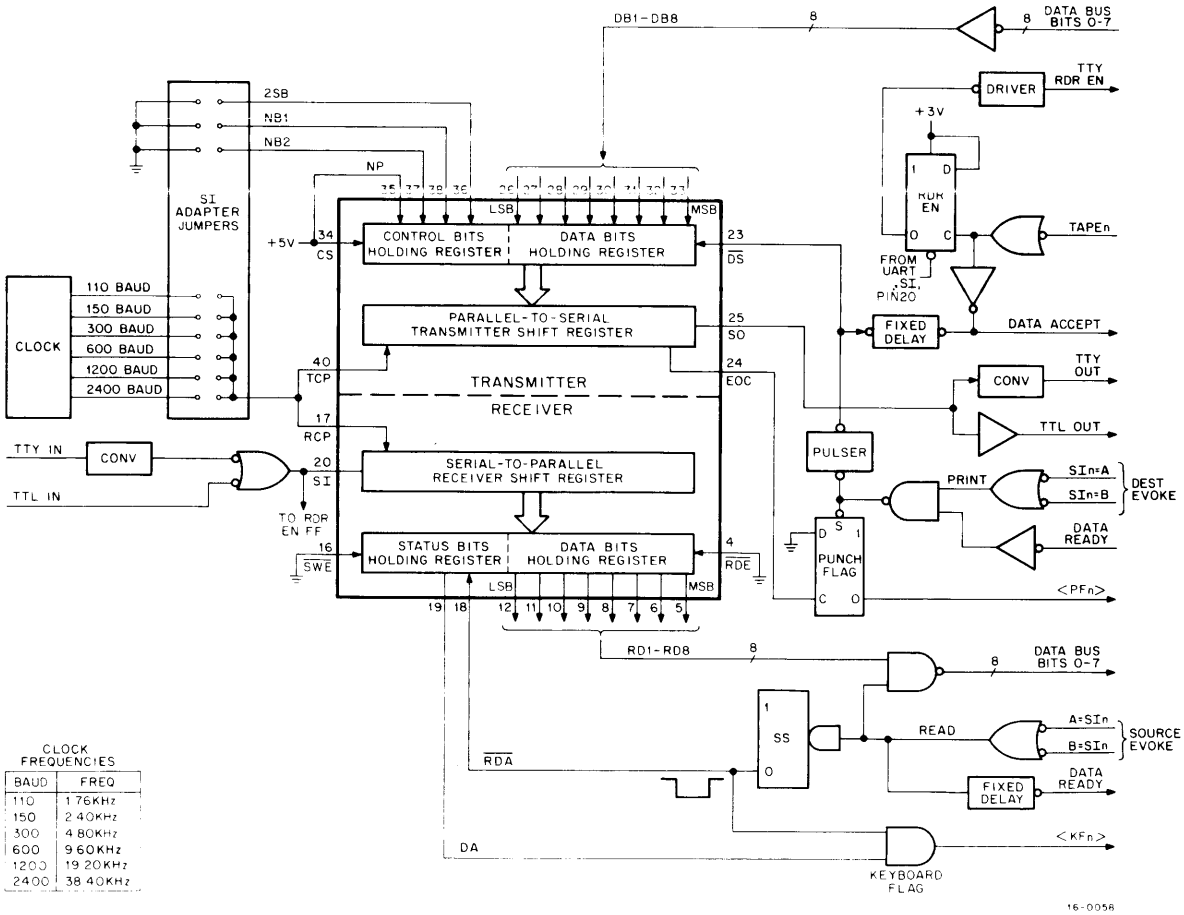
The PCS16-D multiplexer option must be implemented if it becomes necessary to test the even bits of the A Register.

DC16-A
SERIAL I/O OPTION (M7313)

Two serial I/O channels can be implemented in a PDP16-M. Both channels require interface adapter DC16-B (M7333 module) to provide character format selection and TTY current loop connections. Three prewired module slots are reserved on the PDP16-M logic assembly for implementing the serial I/O channels: two are reserved for the M7313 I/O Modules and one is reserved for the M7333 Interface Adapter Module. The two slots for the M7313 modules are wired directly to the PDP16-M register transfer bus.

FUNCTIONAL DESCRIPTION

The M7313 I/O module (Figure 1) contains one LSI chip, designated the UART, and some control logic to interface with the PDP16-M Register Transfer bus (and ASR 33 paper tape reader if used). The module also contains signal converters for handling TTL and TTY compatible serial data signals of the terminal device. Therefore, TTY and TTL compatible terminal devices can be connected directly to the I/O channels. EIA converters, on standard K-series modules, can be purchased from DEC to interface with long communications lines via modems. These modules are not offered as PDP16-M options.



CLOCK FREQUENCIES

BAUD	FREQ
110	1.76KHz
150	2.40KHz
300	4.80KHz
600	9.60KHz
1200	19.20KHz
2400	38.40KHz

Figure 1 Serial I/O Option DC16-M, Block Diagram

The UART (Universal Asynchronous Receiver/Transmitter) is a full duplex receiver-transmitter. The chip accepts asynchronous serial binary characters from the terminal and converts them to a parallel format for the PDP16-M. It also accepts parallel binary characters from the PDP16-M and converts them to a serial asynchronous stream (including start and stop bits) for the terminal. When transferred to and from the register transfer bus, the data bits are right justified to the LSB (bit 0) of the data bus.

The UART is universal in that the number of desired data bits (5, 6, 7, or 8), the number of stop bits (1 or 2) and the required baud rate (110, 150, 300, 600, 1200, 2400) are externally selectable. The characteristics are selected by installing a specific combination of jumpers on the interface adapter module. Other I/O connections on the UART are for controlling and synchronizing data transfers between the terminal and the PDP16-M register transfer bus. Table 1 lists and describes the UART input and output signals that are used in the PDP16-M serial I/O channels.

Table 1
UART I/O Connections

Pin No.	I/O	Name	Symbol	Function
1	I	V_{CC} Power Supply	V_{CC}	+5V supply
2	I	V_{GG} Power Supply	V_{GG}	-12V supply
3	I	Ground	G	Ground
4	I	Received Data Enable	$\overline{RDE}$	A low on the receiver enable line places the received data onto the output lines.
5–12	O	Received Data Bits	RD8–RD1	These are the eight data output lines. These lines may be wire-ORed. When 5-, 6-, or 7-level code is selected, the most significant unused bits are low. Character will be right justified into the least significant bits. RD1 (pin 12) is the least significant bit, RD8 (pin 5) is the most significant bit. A high indicates a mark.
13	O	Receive Parity Error	PER	Not used
14	O	Framing Error	FER	Not used
15	O	Overrun	OR	Not used
16	I	Status Word Enable	$\overline{SWE}$	A low on this line places the status word bits (PE, DA, TBMT, FE, OR) onto the output lines.
17	I	Receiver Clock Line	RCP	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud rate.
18	I	Reset Data Available	$\overline{RDA}$	A low on this line will reset the DA line.

Table 1 (Cont)
UART I/O Connections

Pin No.	I/O	Name	Symbol	Function
19	O	Received Data Available	$\overline{DA}$	This line goes to high when an entire character has been received and transferred to the receiver holding register.
20	I	Serial Input	SI	This line accepts the serial bit input stream. A high must be present when data is not being received. High is a mark; low is a space.
21	I	External Reset	XR	Should be pulsed after power turn on (Power Clear) to a high. Resets all registers. Sets serial output line to a high. Sets TBMT to a high. Sets EOC to a high.
22	O	Transmitter Buffer Empty	TBMT	Not used
23	I	Data Strobe	$\overline{DS}$	A low to high transition on this line will enter the data bits into the data bits holding register. Data loading is controlled by the rising edge of $\overline{DS}$.
24	O	End of Character	EOC	This line goes to a high each time a full character including stop bits is transmitted. It remains at this level until the start of transmission of the next character. Start of transmission is defined as the mark to space transition of the start bit. It will remain at a high when data is not being transmitted.
25	O	Serial Output	SO	This line will serially, by bit, provide the entire transmitted character. It will remain at a high when no data is being transmitted. High is a mark; low is a space.
26–33	I	Data Bit Inputs	DB1–DB8	These are the eight parallel data input lines. If 5, 6, or 7 bits are transmitted, the least most significant bit is used. DB1 is the least most significant bit (pin 26). DB8 is the most significant bit (pin 33). A high input will cause a mark (high) to be transmitted.
34	I	Control Strobe	CS	A high on this lead will enter the control bits (POE NB1, NB2, SB, NP) into the control bits holding register. This line can be strobed or hard wired to a high level.

Table 1 (Cont)
UART I/O Connections

Pin No.	I/O	Name	Symbol	Function
35	I	No Parity	NP	A high on this lead will eliminate the parity bit from the transmitted and received character. The stop bits will immediately follow the last data bit on transmission. The receiver will not check parity or reception. It will, when asserted, also clamp the PE to a low.
36	I	Two Stop Bits	2SB	This lead will select the number of stop bits. One or two to be appended immediately after the parity bit. A low will insert one stop bit and a high will insert two stop bits.
37–38	I	Number of Bits/ Character	NB2, NB1	These two leads will be internally coded to select either 5, 6, 7, or 8 data bits/character.
			NB2 (37)	**NB1 (38)** **Bits/Character**
			0 (L)	0 (L) 5
			0 (L)	1 (H) 6
			1 (H)	0 (L) 7
			1 (H)	1 (H) 8
39	I	Even Parity Select	POE	Not Used
40	I	Transmitter	TCP	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud rate.

The serial asynchronous bit stream for each character produced and received by the UART contains one start bit, five to eight data bits and one or two stop bits (Figure 2). A parity bit, which may be odd, even, or turned off, is also acceptable to the UART, but is not implemented for the PDP16-M. If implemented, the parity bit will follow the last data bit.

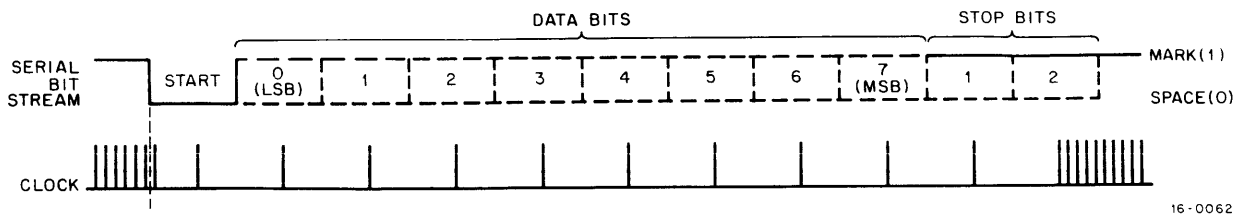


Figure 2 Character Bit Stream Format Options

Both the receiver and the transmitter are double buffered. The UART will internally synchronize the start bit with the clock to ensure uniform encoding and decoding of the serial bit stream. Each bit of the serial stream is maintained at 16 clock periods.

Receiver

When the receiver is idle and the first mark to space transition occurs on the serial input (SI, pin 20) line, the receiver will sample the serial input line at the 8th clock pulse and thereafter at multiples of 16 clock pulses until each selected data and stop bit is sensed. The serial input line is sampled first at the 8th clock pulse to validate the start bit and then at multiples of 16 clock pulses to decode the data and stop bits. The start bit is validated to guard against false triggering due to noise spikes. The receiver will revert to the idle condition if the start bit is not validated.

If the start bit is validated, the receiver will enter the data entry state and store the state of the serial input line for each data sampling point in the receiver shift register. One clock pulse after the stop bit(s) is sampled, a parallel data transfer between the receiver shift register and the holding register is executed. At the same time, the Data Available (DA) flag in the status bits holding register is set.

Transmitter

When the transmitter is idle, the serial output (SO, pin 25) line will be marking (logic high). A low to high transition of the data strobe (DS, pin 23) causes a mark to space transition on the serial output line. The delay between the data strobe and mark to space transition is one clock period. The transmitter produces one start bit, 5, 6, 7, or 8 data bits and 1 or 2 stop bits. The number of data and stop bits are determined by the control bits holding register. The serial output line is presented with the least significant data bit (DB1, pin 26) first and the most significant data bit (DB8, pin 33) last. The stop bit(s) follows the last data bit. All bits of the serial output stream are maintained at a constant width of 16 clock periods. The End Of Character flag (EOC, pin 24) will be low any time a character is in the process of being converted and transmitted; the flag will go high each time a full character including the stop bit(s) is transmitted.

Interface Control

The UART is interfaced with the terminal device via input receivers/converters and output drivers/converters. Both TTY and TTL compatible signals are available. Combinational and sequential logic are used for interfacing the PDP16-M register transfer bus with the UART. Logic is included for printing (or displaying) a character on the terminal and for reading a character from the terminal keyboard or paper tape reader.

The following instructions evoke data transfers between the PDP16-M A and B Registers and the terminal.

PRINT/DISPLAY		READ	
Destination	**Source**	**Destination**	**Source**
SI_n	A	A	SI_n
SI_n	B	B	SI_n
			$TAPE_n$

n = 1 or 2

The $TAPE_n$ command must precede the A and B = SI_n instructions when reading from an ASR 33 paper tape reader. This command advances the paper tape one character and transfers the serial bit stream to the UART. Whenever the $TAPE_n$ command is executed, the RDR EN flip-flop is set and a DATA ACCEPT signal is issued. The RDR EN flip-flop is reset by the first transition of the serial input bit stream. The $TAPE_n$ command is not required for reading characters from other terminals. When the serial input bit stream is fully assembled and transferred to the data bits holding register, the keyboard flag (KF_n) goes high. This flag can be tested by the following instruction:

IF KF_n, LABEL

After the flag goes high, the A = SI_n or B = SI_n instruction can be used to transfer the data to the PDP16-M A or B Registers. A DATA READY signal is issued by the serial I/O module (Source Register) and a DATA ACCEPT signal is issued by the Destination Register (A or B) to interlock the data transfer.

In printing or displaying a character on a terminal, the A or B Register must first be loaded with the character (justified to the LSB, bit 0) and the SI_n = A or SI_n = B instructions must be executed. After the DATA READY signal is issued by the Source Register (A or B), the PUNCH FLAG flip-flop is set, causing the Punch flag (PF_n) to go low. At the same time, the data strobe (DS, pin 23) is pulsed. On the low to high transition of the pulse, the data is loaded into the data bits holding register and the conversion and transmission operation is started. After a full character including the stop bit(s) is transmitted to the terminal, the END OF CHARACTER (EOC, pin 24) signal goes high, causing the PUNCH FLAG flip-flop to be reset and the Punch flag (PF_n) to go high. The flag can be tested by the following instructions:

IF PF_n, LABEL

After the flag goes high, the next instruction can be executed.

Clock

The clock for encoding and decoding the serial asynchronous data stream is derived from a frequency divider chain that is driven by an 844.8 kHz crystal oscillator (Figure 3). One of seven operating frequencies can be selected from the divider chain simply by installing a jumper on the interface adapter module. The operating speed and quality of the communication line are the determining factors for selecting the operating frequencies. The following frequencies are produced by the frequency divider chain.

Operating Frequency	Terminal Speed
1.76 kHz	110 baud
2.4 kHz	150 baud
4.8 kHz	300 baud
9.6 kHz	600 baud
19.2 kHz	1200 baud
38.4 kHz	2400 baud

NOTE
The operating frequency is 16 times the terminal baud rate.

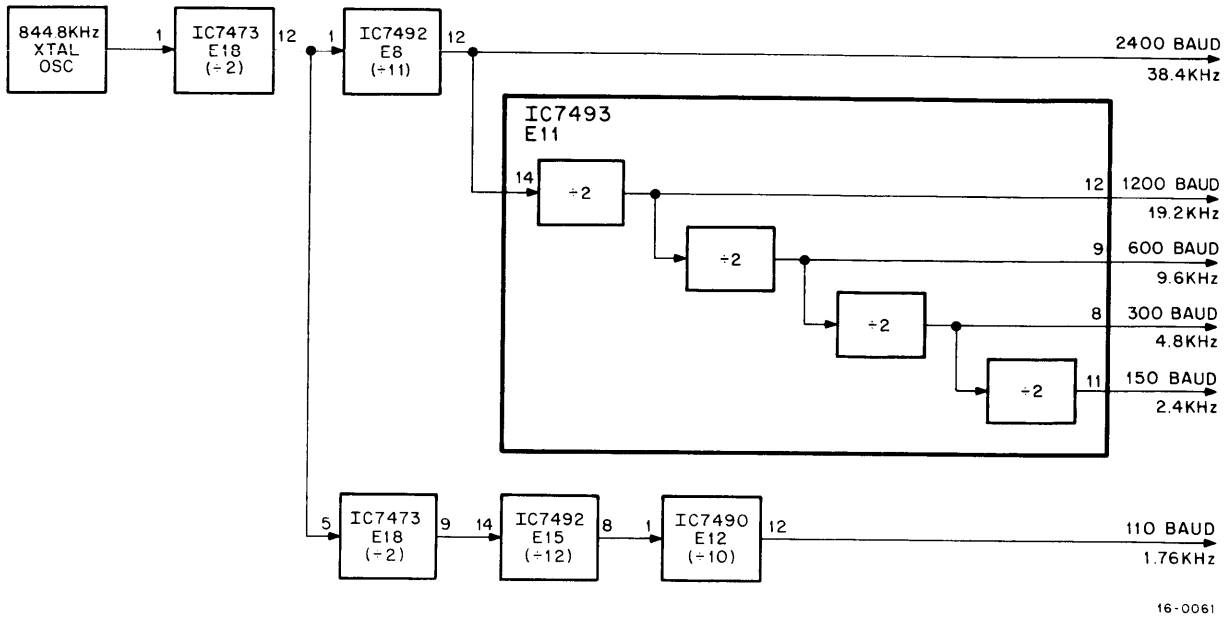


Figure 3 Clock Frequency Divider Chain, Block Diagram

INSTALLATION

Three prewired module slots are reserved on the PDP16-M logic assembly for implementing the serial I/O channels. They are:

Slot	Module	Name
AB16	M7313	SI1
AB17	M7313	SI2
D18	M7333	SI Adapter

The SI adapter, module M7333, contains a set of split lugs and a Mate-N-Lok connector for each channel (Figure 4). The split lugs facilitate jumper installation for selecting the desired bit stream format. The number of data bits, stop bits and channel baud rate can be selected to complement the terminal device. Use the following chart for installing the required jumpers.

Stop Bits	1	2				
SB	Yes	No				
Data Bits	5	6	7	8		
NB1	Yes	No	Yes	No		
NB2	Yes	Yes	No	No		
Baud Rate	110	150	300	600	1200	2400
110	Yes					
150		Yes				
300			Yes			
600				Yes		
1200					Yes	
2400						Yes

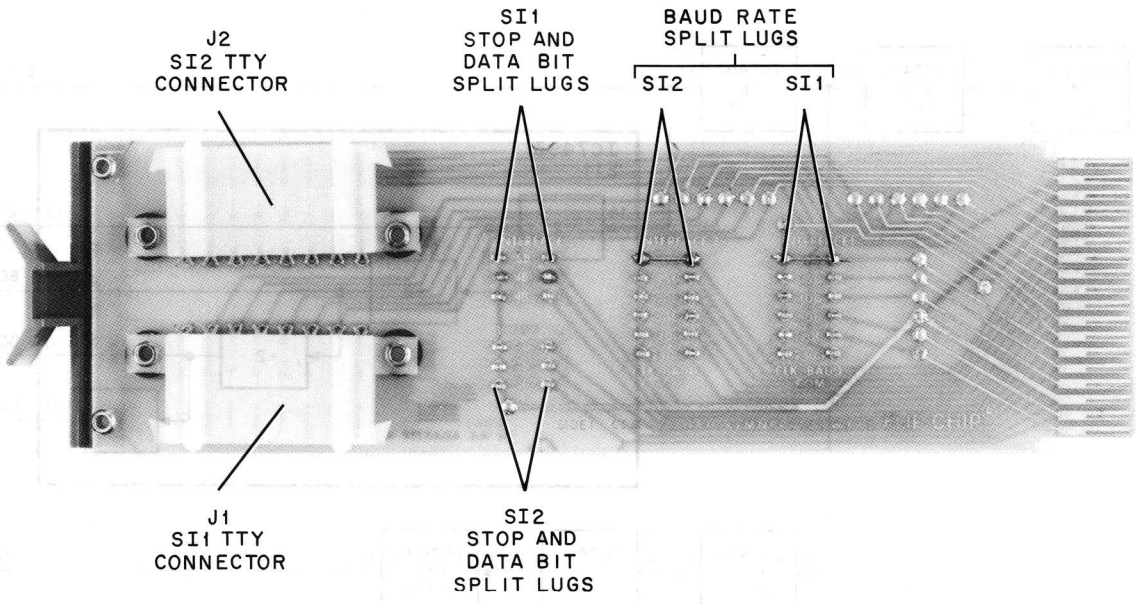


Figure 4 SI Adapter Module M7333, TTY Connectors and Split Lug Identification

The Mate-N-Lok connector is the TTY 20-mil current loop interface connector for interfacing with the terminal device. TTL compatible serial I/O connections are made available on the MUX I/O slot (C19).

PROGRAMMING

The instructions that evoke data transfers between the PDP16-M and a terminal via the two serial I/O channels (LET instruction) are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). No additional evoke decoders are required. The machine code (octal), execution time, and description of each instruction follows:

CHANNEL NO. 1 (SI1)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
050	3.5	SI1 = A	ST1 gets A (Data Out)
051	2.1	A = SI1	A gets SI1 (Data In)
052	1.7	TAPE1	Move paper tape and assemble one character
251	2.1	B = SI1	B gets SI1 (Data In)
252	3.5	SI1 = B	SI1 gets B (Data Out)

CHANNEL NO. 2 (SI2)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
053	3.5	SI2 = A	SI2 gets A (Data Out)
054	2.1	A = SI2	A gets SI2 (Data In)
055	1.7	TAPE2	Move paper tape and assemble one character
253	2.1	B = SI2	B gets SI2 (Data In)
254	3.5	SI2 = B	SI2 gets B (Data Out)

The TAPE1 and TAPE2 commands are required in a program only when reading data from a paper tape. They need not be programmed when reading data from other types of devices, that is, keyboards or modems.

Random data transfers between the terminal device and the PDP16-M are not possible since the serial I/O receiver/transmitter (UART) must convert the data from serial to parallel and vice versa. The conversion time is determined by the selected baud rate. For example, at a baud rate of 110 with a character format of one start bit, eight data bits, and two stop bits, the maximum transfer rate possible is 10 characters per second (100 milliseconds per character). Since the PDP16-M operates at a much faster speed, the data transfers must be synchronized to the conversion speed of the UART. For this reason, each channel has two flags: one flag (PF_n) is set when a character is punched or displayed; the other flag (KF_n) is set when a character is assembled and ready to be read into the computer. The flag outputs are received and multiplexed by multiplexer 0 so that the IF instruction can be used to test the flags for synchronizing the data transfers.

The flags are received by the following channels if multiplexer 0.

MUX0 Channel	Input
31	KF1
32	PF1
33	KF2
34	PF2

KFL16
BOOLEAN OUTPUT/FLAG OPTION (M7306)

Three Boolean outputs/flags are included in the basic PDP16-M (Paragraphs 1.2 and 2.6). Three additional Boolean outputs/flags (FF4 through FF6) can be added by implementing the KFL16 option (M7306 module) (Figure 1). The option module contains three flip-flops that can be set, reset, and tested under program control. One prewired module slot, slot D2, is reserved on the PDP16-M logic assembly for installing the M7306 Option Module. The logic 1 sides (TRUE) of the flip-flops are wired to the MUX and FF I/O slot on the logic assembly to facilitate convenient interfacing when the flip-flops are used as Boolean outputs. To implement this option, it is only necessary to install the option module in the assigned slot. No other wiring or set-up procedure is required, except if used as Boolean outputs, to connect the external devices to be driven to the MUX and FF I/O slot. Refer to Chapter 2 of the *PDP16-M User's Guide* for interfacing details.

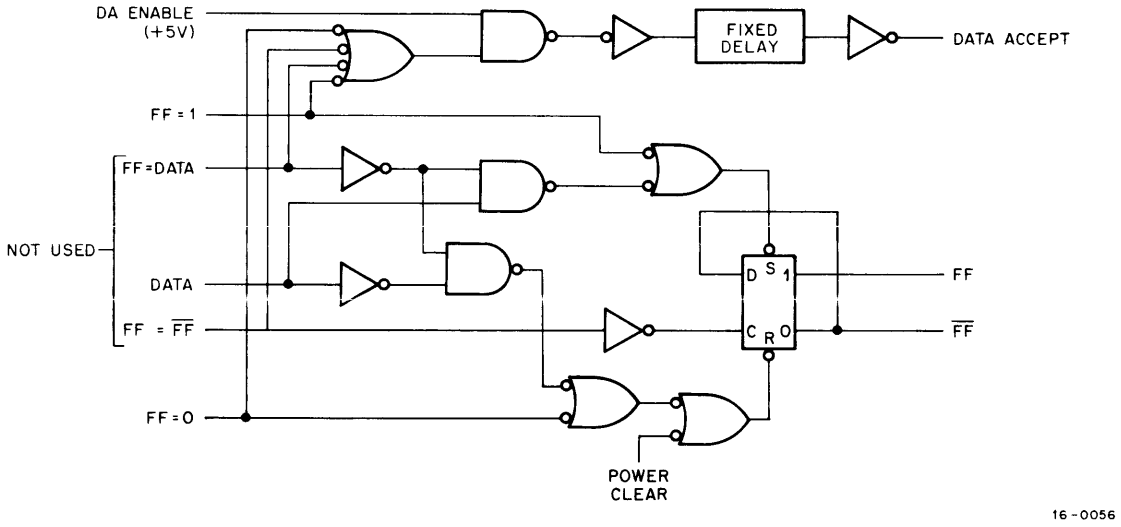


Figure 1 Boolean Output/Flag Option KFL16, Block Diagram (1 of 3 Circuits)

The instructions that cause the flip-flops to be set and reset are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). No additional evoke decoders are required. The machine code (octal), execution time, and description of each instruction follows:

SET FF_n

Evoke (Octal Code)	Time (μsec)	Instruction	Description
065	1.8	FF4 = 1	Set FF4
067	1.8	FF5 = 1	Set FF5
071	1.8	FF6 = 1	Set FF6

RESET FF_n

Evoke (Octal Code)	Time (μsec)	Instruction	Description
064	1.8	FF4 = 0	Reset FF4
066	1.8	FF5 = 0	Reset FF5
070	1.8	FF6 = 0	Reset FF6

The state of the flip-flop can also be tested using the IF instruction to facilitate the use of the flip-flops as program flags. The machine code (octal), execution time, and description of the instructions follows:

Machine Code (Octal)		Time (μsec)		Instruction	Description
MEM0	MEM1	False	True		
354	355	2.0	3.2	IF FF4, LABEL	Test FF4
356	357	2.0	3.2	IF FF5, LABEL	Test FF5
360	361	2.0	3.2	IF FF6, LABEL	Test FF6

MR16-D
CONSTANT GENERATOR OPTION (M7325)

A 4-word diode ROM for storing constants is included in the basic PDP16-M. Transformer ROM storage for 24 additional constants can be added by implementing the MR16-D option (M7325 module). The module contains 16 toroidal cores and data gating logic (Figure 1). Each 16-bit constant is installed by stringing a wire from a split lug through or around (adjacent hole) each core to the companion split lug. Twenty-five split lugs are provided at each end of one core bank for this purpose (Figure 2). One split lug pair is a test (T) pair to which a test wire is connected. The test wire is strung through all cores to show the direction in which the wires for the constants must be threaded. When installed, each wire establishes a current path for enabling and reading out a specific constant. A logic 1 is produced where the wire is threaded through the core and a logic 0 is produced where the wire is threaded around the core (through the adjacent hole). When installing constants, the wires should be connected to companion lug pairs so that a given constant wire can be easily identified. The lugs are numbered so that companion pairs can be identified. The numbers assigned to the lugs correspond to the constant number (K1 through K24).

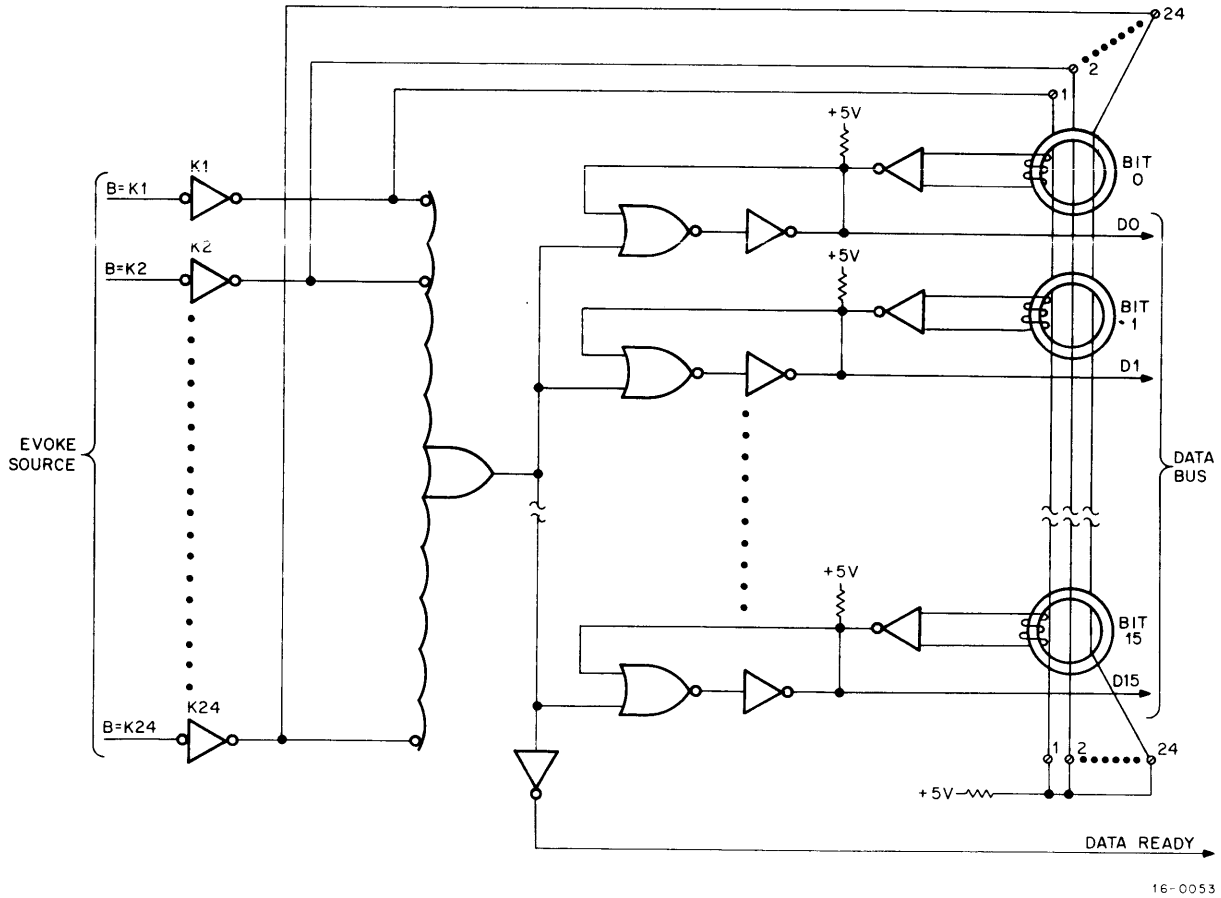


Figure 1 Constant Generator Option MR16-D, Block Diagram

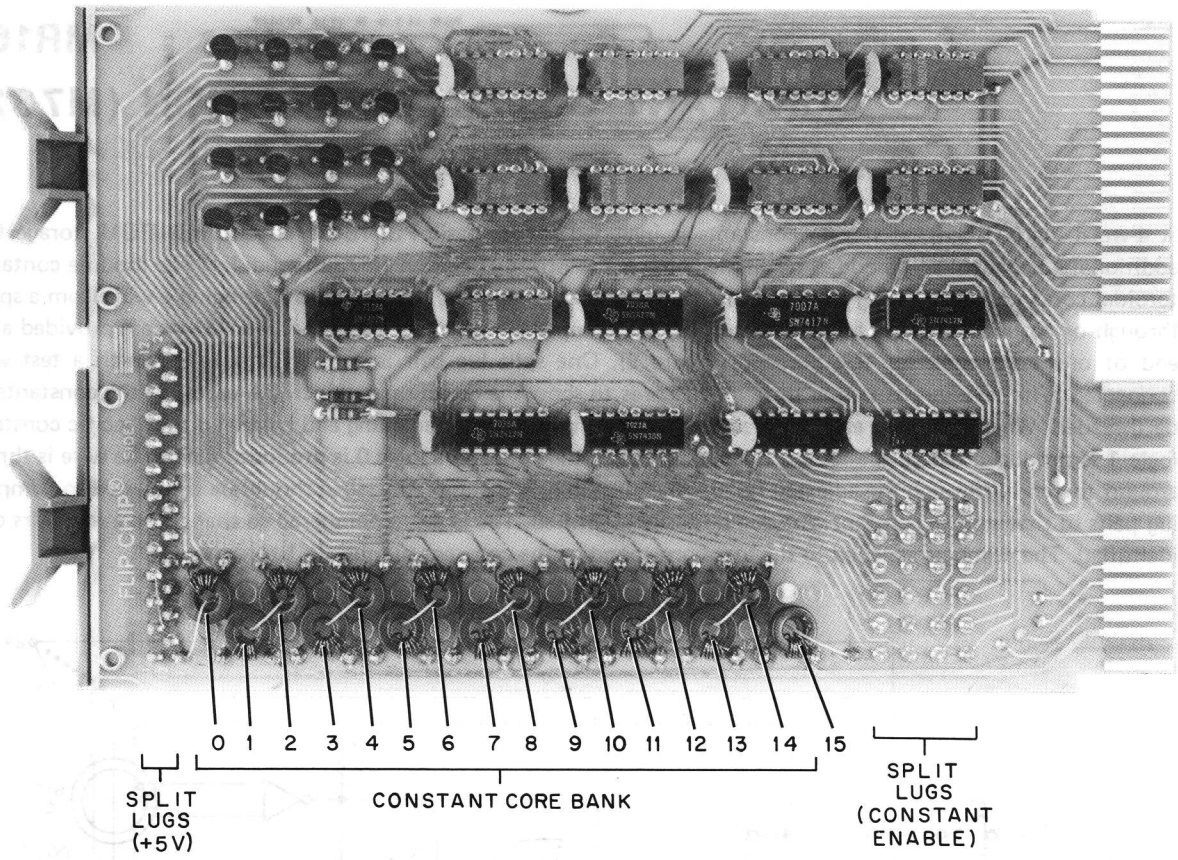


Figure 2 Constant Generator Module M7325, Core Bank and Split Lug Location

Prewired module slot ~~AB18~~ AB8 on the PDP16-M logic assembly is reserved for the M7325 Constant Generator Module. To implement this option, it is only necessary to install the module in the assigned slot. Except for threading and connecting the constant wires, no wiring or set-up procedure is required. The module slot is prewired directly to the register transfer bus. If it becomes necessary to change the constants from time to time, it can be done simply by rethreading the wires or by installing an alternate constant generator module.

The instructions that evoke data transfers from the constant generator to the Destination Register are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). No additional evoke decoders are required. The machine code (octal), execution time, and description of each instruction follows:

Evoke (Octal Code)	Time (μsec)	Instruction	Description
100	2.4	B = K1	B gets K1
101	2.4	B = K2	B gets K2
102	2.4	B = K3	B gets K3
103	2.4	B = K4	B gets K4
104	2.4	B = K5	B gets K5
105	2.4	B = K6	B gets K6
106	2.4	B = K7	B gets K7
107	2.4	B = K8	B gets K8
110	2.4	B = K9	B gets K9

Evoke (Octal Code)	Time (μsec)	Instruction	Description
111	2.4	B = K10	B gets K10
112	2.4	B = K11	B gets K11
113	2.4	B = K12	B gets K12
114	2.4	B = K13	B gets K13
115	2.4	B = K14	B gets K14
116	2.4	B = K15	B gets K15
117	2.4	B = K16	B gets K16
120	2.4	B = K17	B gets K17
121	2.4	B = K18	B gets K18
122	2.4	B = K19	B gets K19
123	2.4	B = K20	B gets K20
124	2.4	B = K21	B gets K21
125	2.4	B = K22	B gets K22
126	2.4	B = K23	B gets K23
127	2.4	B = K24	B gets K24

MR16-E/F
DATA PROM OPTION (M7327)

The data PROM (programmable read-only memory) option extends the read-only data memory of the PDP16-M (Figure 1). One or two data PROM options (M7327 modules) can be implemented. Each option (MR16-E) provides 256 8-bit bytes of storage. Both options (MR16-F) must be implemented to obtain 256 16-bit words of storage. In addition, a DB16-A general purpose interface option (M7311 module) is required when implementing the PROM(s) to interface the PROM(s) with the register transfer bus. This option is also used in establishing the parallel I/O channels of the PDP16-M. However, in implementing the PROM option, the M7311 module serves as the Memory Address Register (MAR) and provides the necessary address/data gating logic and the bus drivers and receivers. The data PROM(s), which is identical to the control PROM, can be used not only to store additional constants but also to store canned messages (ASCII or EBCDIC characters), tables, or data arrays. Three prewired module slots are reserved on the PDP16-M logic assembly for implementing the data PROM option: two are reserved for the M7327 PROM modules and one is reserved for the M7311 General Purpose Interface Module. The slot for the general purpose interface module, slot AB15, is wired directly to the register transfer bus. Each M7327 PROM module provides storage for 256 8-bit bytes. Slot C15 is wired to the general purpose interface module to transfer the eight data bits from the PROM to the eight low order bits of the register transfer bus, and slot D15 is wired to transfer the data to the eight high order bits of the bus. If only eight data bits are implemented (one MR16), the other eight bits will always contain 1s when the data is transferred.

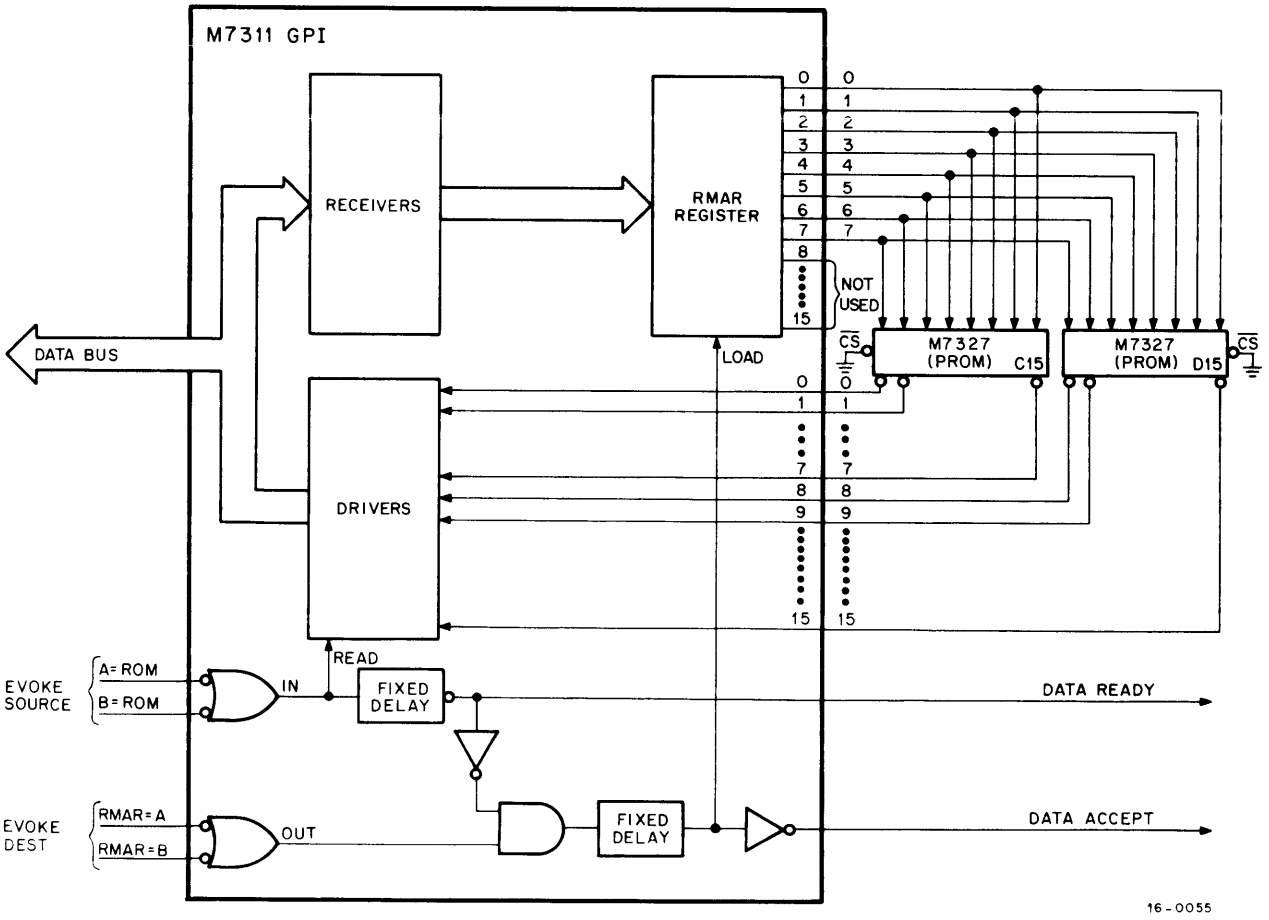


Figure 1 Data PROM Option MR16-E/F, Block Diagram

The loading procedure for the data PROM is identical to that described for the control PROM. Refer to Chapter 5 of the *PDP16-M User's Guide.* The procedure for preparing the object tape, however, is different. Since a PDP16-M program does not contain data, no provision for handling data is included in the PAL16 Assembler. Therefore, object code must be used to define the required data constants, messages, and arrays to be loaded into the PROM. The object tape can be prepared under the control of the Symbolic Editor.

If both data PROMs are to be implemented, one tape must be prepared for each PROM. After the tape is punched, the PROM can be loaded using the utility software/hardware package as described in Chapter 5 of the *PDP16-M User's Guide.* Only the following characters can be used in preparing the object code for the PROM.

Character	Function
Three consecutive octal digits followed by CR and LF.	To specify an 8-bit constant.
Octal Character Code	To specify ASCII or EBCDIC characters for canned messages.
% followed by three octal numbers.	Select random PROM load address (preset PC with new address).
$	To indicate end of object code.

To form a 16-bit constant (for data tables or arrays), the coder must break up the desired 16-bit number into two 8-bit octal numbers, one for each data PROM. Two tapes, each containing one half of the constant, must then be prepared. Care must be taken to ensure that both 8-bit parts of the constant fall in the same absolute location of the PROMs. Then, when the constant of that location is read, the correct 16-bit constant is transferred to the specified Destination Register. Because the complement of the constant is stored in the PROM, the data must be complemented to obtain the correct constant. Two instructions are available for complementing the data. They are: A = ANOT and B = BNOT.

It is important to remember that the object code is loaded under control of the utility load program in sequential locations starting with location 000 unless the address is changed using the % sign followed by an octal number. The address and/or base addresses of the constants, messages, and arrays must be recorded for the application programmer's use. Before a data transfer from the PROM to a Destination Register can be programmed, the desired PROM location must be addressed. Once addressed, the general purpose interface retains the address in a Buffer Register until another address is transferred. The instructions that evoke address and data transfers are decoded by the standard evoke decoders of the PDP16-M. No additional evoke decoders are required. The machine code (octal), execution time, and description of each instruction follows:

ADDRESS PROM

Evoke (Octal Code)	Time (μsec)	Instruction	Description
134	2.2	RMAR = A	RMAR gets A (send address to PROM Memory Address Register)
146	2.2	RMAR = B	RMAR gets B (send address to PROM Memory Address Register)

READ DATA

Evoke (Octal Code)	Time (μsec)	Instruction	Description
135	2.3	A = ROM	A gets ROM (transfer data to A Register)
011	2.4	*A = ANOT	Complement data
147	2.3	B = ROM	B gets ROM (transfer data to B Register)
031	2.4	*B = BNOT	Complement data

*After the constant is read, it must be complemented to obtain the correct constant because the constants are stored in complement form. This step can be avoided if the object code for the data PROM is prepared in complement form.

MS16-C
SCRATCH PAD REGISTER OPTION (M7318)

One temporary storage register (the byte and word addressable Transfer Register, TR) is included in the basic PDP16-M. Thirty-two additional word addressable temporary storage registers (Scratch Pad Registers) can be added by implementing two MS16-C options (M7318 modules) and two PCS16-C options (M7328 modules). The M7318 module contains 16 high-speed word addressable registers (Figure 1), and the M7328 module contains the evoke decoders for these registers. The evoke decoders decode scratch pad instruction codes to evoke data transfers between the specified Source and Destination Registers (Paragraph 4.2.4). All 32 Scratch Pad Registers need not be implemented. Installing one MS16-C option and one PCS16-C option provides 16 Scratch Pad Registers. Four prewired module slots are reserved on the PDP16-M logic assembly for installing the option modules. The two slots for the M7318 Scratch Pad Register Modules are wired directly to the PDP16-M register transfer bus. The two slots are assigned their own respective sets of mnemonics for programming reasons. To implement either 16 or 32 Scratch Pad Registers, it is necessary only to install the option modules in the assigned slots. No other wiring or set-up procedure is required. Slot assignments for the scratch pad option are as follows:

Slot	Module	Assigned Function
AB4	M7318	SP1–SP16 Registers (Group 1)
AB3	M7318	SP17–SP32 Register (Group 2)
CD6	M7328	Evoke Decoder 3 (SP1–SP16)
CD7	M7328	Evoke Decoder 4 (SP17–SP32)

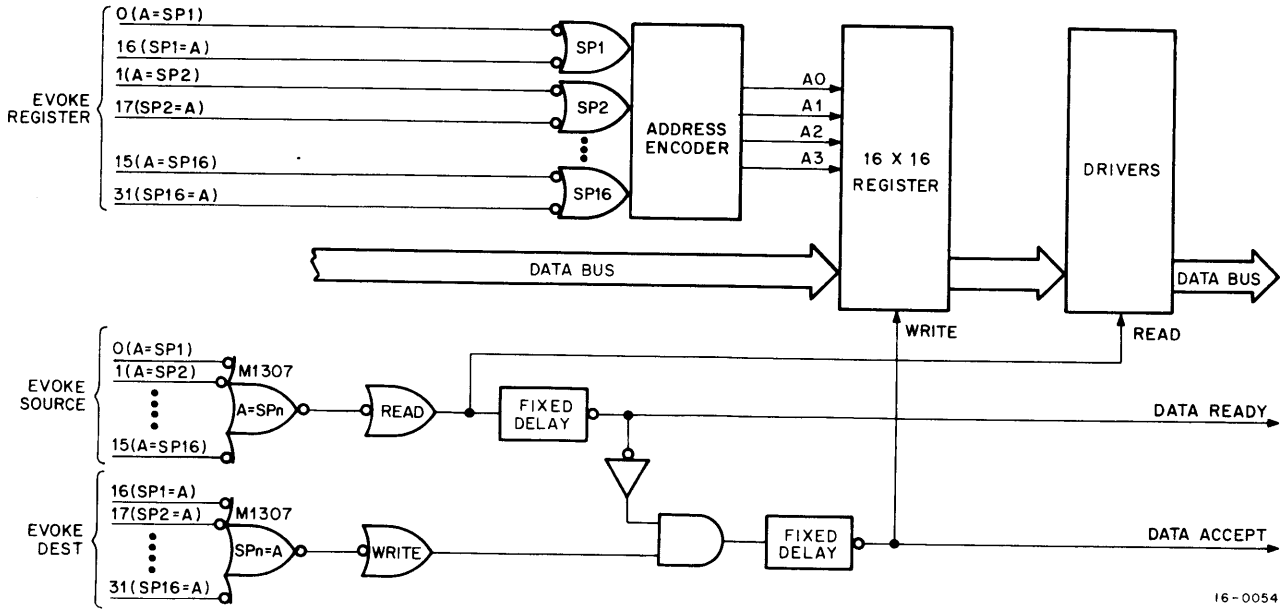


Figure 1 Scratch Pad Register Option MS16-C, Block Diagram

The above slot assignments must be adhered to in installing the options and/or programming the data transfers because the Source and Destination Register evoke signals are hard wired. The instructions that evoke data transfers to and from the Scratch Pad Registers are decoded by the evoke decoders. The machine code (octal), execution time, and description of each instruction follows:

SCRATCH PAD REGISTER GROUP 1 (SP1–SP16)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
140	2.2	A = SP1	A gets SP1
141	2.2	A = SP2	A gets SP2
142	2.2	A = SP3	A gets SP3
143	2.2	A = SP4	A gets SP4
144	2.2	A = SP5	A gets SP5
145	2.2	A = SP6	A gets SP6
146	2.2	A = SP7	A gets SP7
147	2.2	A = SP8	A gets SP8
150	2.2	A = SP9	A gets SP9
151	2.2	A = SP10	A gets SP10
152	2.2	A = SP11	A gets SP11
153	2.2	A = SP12	A gets SP12
154	2.2	A = SP13	A gets SP13
155	2.2	A = SP14	A gets SP14
156	2.2	A = SP15	A gets SP15
157	2.2	A = SP16	A gets SP16
160	2.6	SP1 = A	SP1 gets A
161	2.6	SP2 = A	SP2 gets A
162	2.6	SP3 = A	SP3 gets A
163	2.6	SP4 = A	SP4 gets A
164	2.6	SP5 = A	SP5 gets A
165	2.6	SP6 = A	SP6 gets A
166	2.6	SP7 = A	SP7 gets A
167	2.6	SP8 = A	SP8 gets A
170	2.6	SP9 = A	SP9 gets A
171	2.6	SP10 = A	SP10 gets A
172	2.6	SP11 = A	SP11 gets A
173	2.6	SP12 = A	SP12 gets A
174	2.6	SP13 = A	SP13 gets A
175	2.6	SP14 = A	SP14 gets A
176	2.6	SP15 = A	SP15 gets A
177	2.6	SP16 = A	SP16 gets A

SCRATCH PAD REGISTER GROUP 2 (SP17–SP32)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
200	2.2	A = SP17	A gets SP17
201	2.2	A = SP18	A gets SP18
202	2.2	A = SP19	A gets SP19

SCRATCH PAD REGISTER GROUP 2 (SP17–SP32) (Cont)

Evoke (Octal Code)	Time (μsec)	Instruction	Description
203	2.2	A = SP20	A gets SP20
204	2.2	A = SP21	A gets SP21
205	2.2	A = SP22	A gets SP22
206	2.2	A = SP23	A gets SP23
207	2.2	A = SP24	A gets SP24
210	2.2	A = SP25	A gets SP25
211	2.2	A = SP26	A gets SP26
212	2.2	A = SP27	A gets SP27
213	2.2	A = SP28	A gets SP28
214	2.2	A = SP29	A gets SP29
215	2.2	A = SP30	A gets SP30
216	2.2	A = SP31	A gets SP31
217	2.2	A = SP32	A gets SP32
220	2.6	SP17 = A	SP17 gets A
221	2.6	SP18 = A	SP18 gets A
222	2.6	SP19 = A	SP19 gets A
223	2.6	SP20 = A	SP20 gets A
224	2.6	SP21 = A	SP21 gets A
225	2.6	SP22 = A	SP22 gets A
226	2.6	SP23 = A	SP23 gets A
227	2.6	SP24 = A	SP24 gets A
230	2.6	SP25 = A	SP25 gets A
231	2.6	SP26 = A	SP26 gets A
232	2.6	SP27 = A	SP27 gets A
233	2.6	SP28 = A	SP28 gets A
234	2.6	SP29 = A	SP29 gets A
235	2.6	SP30 = A	SP30 gets A
236	2.6	SP31 = A	SP31 gets A
237	2.6	SP32 = A	SP32 gets A

The B Register cannot be used in programming data transfers to and from the Scratch Pad Registers.

MS16-D
DATA R/W MOS MEMORY OPTION (M7319)

The MS16-D data R/W MOS memory option extends the read/write data memory of the PDP16-M (Figure 1). One or two data memory options (M7319 modules) can be implemented. Each data memory option provides 256 words of storage. Two prewired module slots are reserved on the PDP16-M logic assembly for installing the M7319 modules. To implement a data memory option, it is necessary only to install the option module in one of the assigned slots. No other wiring or set-up procedure is required.

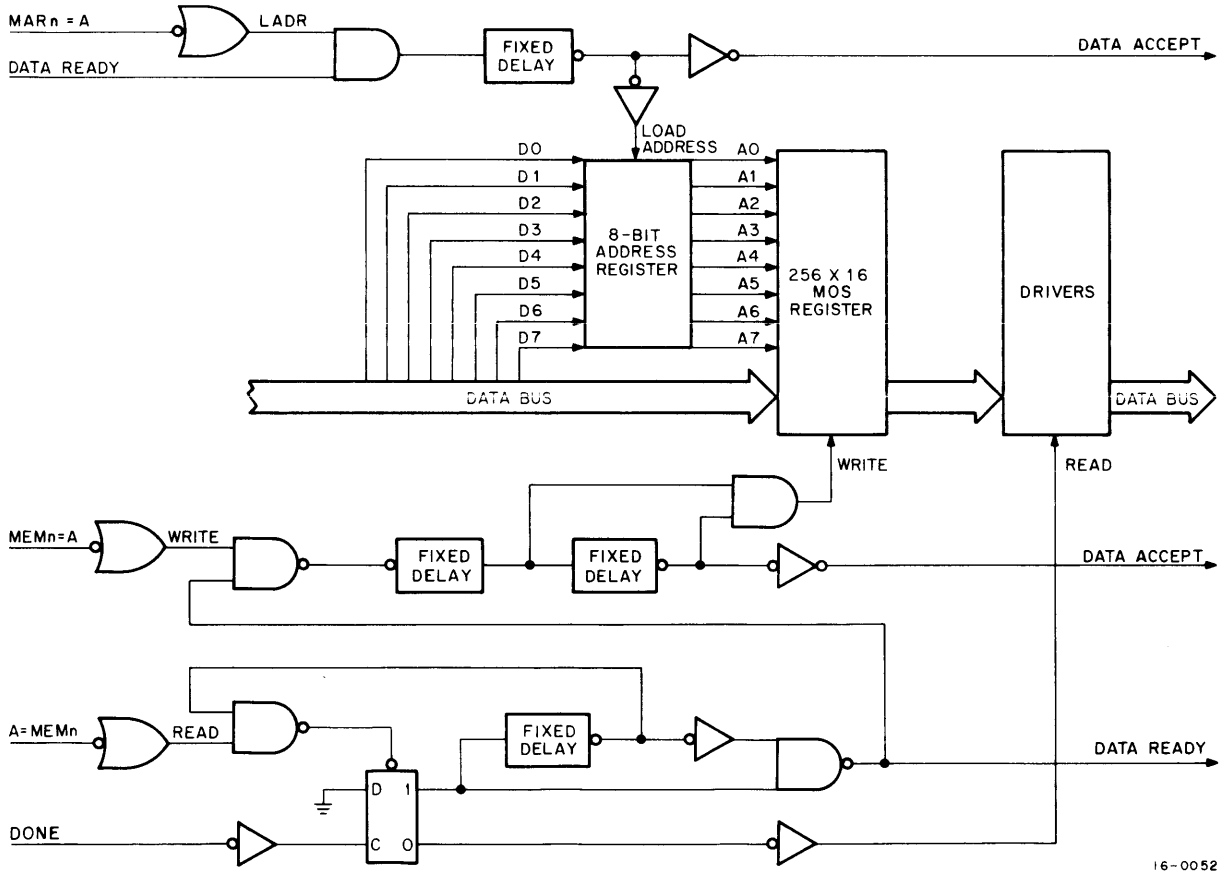


Figure 1 Data R/W MOS Memory Option MS16-D, Block Diagram

The M7319 module contains an 8-bit Memory Address Register (MAR), a 256 X 16 Data Register (MEM), 16 bus drivers, and evoke logic for loading the address, reading data, and writing data. The instructions that evoke address and data transfers between the PDP16-M working registers and the memory options are decoded by the standard evoke decoders of the PDP16-M (Paragraph 4.2.4). The two prewired module slots are each assigned different mnemonics for accessing the Memory Address and Data Registers. The mnemonics are:

Slot	Memory Address Register	Data Register
AB6	MAR1	MEM1
AB7	MAR2	MEM2

The above slot assignments must be adhered to in installing the options and/or programming address and data transfers because the Source and Destination Register evoke signals are hard wired.

The machine code (octal), execution time, and description of each instruction follows:

TRANSFER ADDRESS

Evoke (Octal Code)	Time (μsec)	Instruction	Description
240	2.3	MAR1 = A	MAR1 gets A (send address to MEM1 Memory Address Register)
243	2.3	MAR2 = A	MAR2 gets A (send address to MEM2 Memory Address Register)

TRANSFER DATA

Evoke (Octal Code)	Time (μsec)	Instruction	Description
241	3.6	MEM1 = A	MEM1 gets A (write data)
242	3.9	A = MEM1	A gets MEM1 (read data)
244	3.6	MEM2 = A	MEM2 gets A (write data)
245	3.9	A = MEM2	A gets MEM2 (read data)

The B Register cannot be used in programming address and data transfers involving the R/W MOS memory option.

MS16-E
DATA R/W MOS MEMORY OPTION (M7324)

The MS16-E R/W MOS data memory extends the read/write data memory of the PDP16-M. One or two data memory options (M7324 modules) can be implemented. Each data memory option provides 1024 words of storage. With the exception of the memory size, which requires a 10-bit address, the MS16-E option is identical to the MS16-D option. Only two data R/W MOS memory options (MS16-D and/or MS16-E) can be implemented. Refer to MS16-D option description for installation and programming details.

PCS16-B
CONTROL PROM OPTION (M7327)

The control PROM (programmable read-only memory) extends the control program memory of the PDP16-M. One control PROM is included in the basic PDP16-M, while three are optional. Each PROM provides program storage for 256 8-bit words. Four prewired module slots are reserved on the PDP16-M logic assembly for the control PROMs. They are:

Slot		Name	Remarks
PROM0	C16	MEM0, PAGE0	Standard locations ($0000 - 0377_8$)
PROM1	D16	MEM1, PAGE0	Optional locations ($0400 - 0777_8$)
PROM2	C17	MEM0, PAGE1	Optional locations ($1000 - 1377_8$)
PROM3	D17	MEM1, PAGE1	Optional locations ($1400 - 1777_8$)

Refer to Paragraph 4.2.2 for the description of the memory and page select logic and refer to Chapter 5 of the *PDP16-M User's Guide* for details on loading, simulating, and checking the application program.

PCS16-D
BOOLEAN INPUT MULTIPLEXER OPTION (M7329)

One Boolean input multiplexer (MUX0) for multiplexing 30 external and internal inputs is included in the basic PDP16-M (Paragraph 4.2.3). One additional Boolean input multiplexer (MUX1) can be added by implementing the PCS16-D option (M7329 module). The option module multiplexes 30 additional external and internal Boolean inputs which can be selected for test under program control using the IF instruction. The MUX1 command must be declared in the program to select the optional multiplexer. If the test is found to be true, a branch to another instruction is executed; if the test is found to be not true, then the next instruction is executed. One prewired module slot, slot AB19, is reserved on the PDP16-M logic assembly for installing the M7329 Multiplexer Module. The slot is wired directly to the control memory bus. The module slot is also wired to the MUX and FF I/O slot on the logic assembly to facilitate convenient interfacing for external Boolean inputs. To implement the multiplexer option, it is only necessary to install the option module in its assigned slot. No other wiring or set-up procedure is required except to connect the external Boolean inputs, if used, to the MUX and FF I/O slot. Refer to Chapter 2 of the *PDP16-M User's Guide* for interfacing details.

The M7329 Multiplexer Module contains two data selector chips and output signal combining logic (Figure 1). Each chip can handle 16 inputs. Only one input is selected at any one time. The selection is made by the IF instruction machine code bits 1 through 5. The machine code serves as the address for the data selectors. The machine code (octal), execution time, and description of the MUX1 IF instruction set follows:

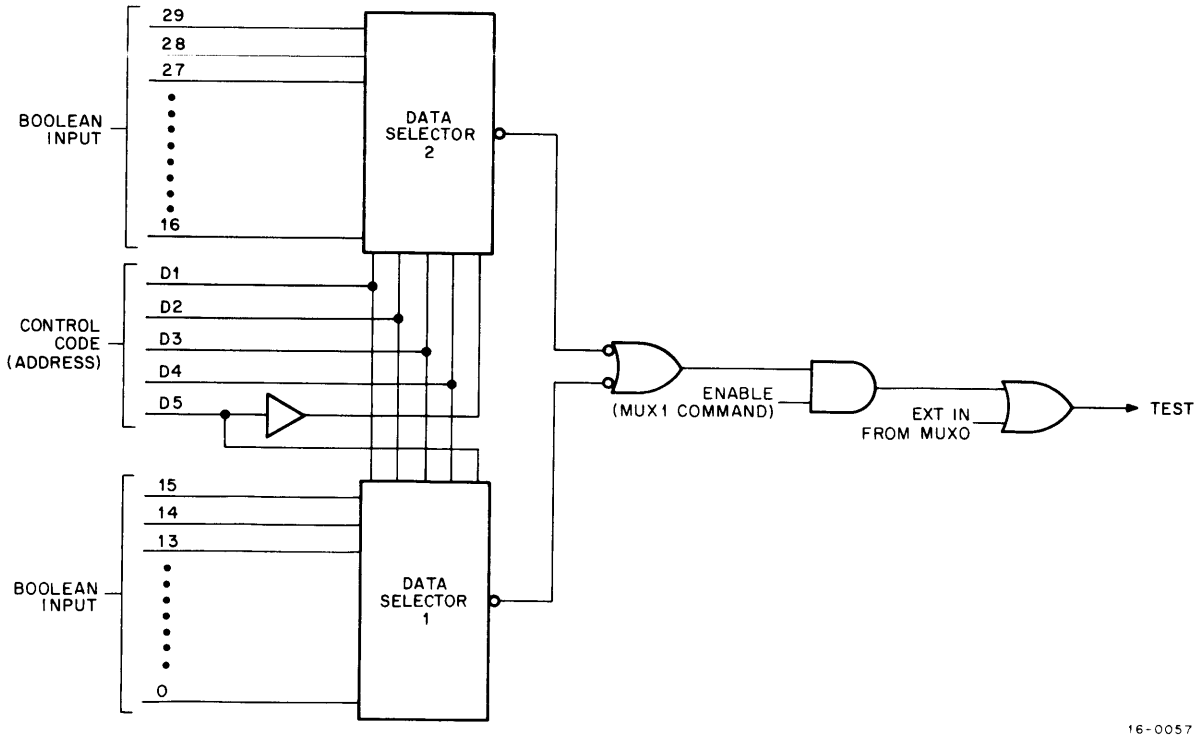


Figure 1 Boolean Input Multiplexer Option PCS16-D, Block Diagram

Machine Code (Octal)		Time (μsec)		Instruction	Description
MEM0	**MEM1**	**False**	**True**		
300	301	2.0	3.2	GOTO	Test channel 0 input (+3V)
302	303	2.0	3.2	IF A<0>, LABEL	Test channel 1 input (A<0>)
304	305	2.0	3.2	IF A<2>, LABEL	Test channel 2 input (A<2>)
306	307	2.0	3.2	IF A<4>, LABEL	Test channel 3 input (A<4>)
310	311	2.0	3.2	IF A<6>, LABEL	Test channel 4 input (A<6>)
312	313	2.0	3.2	IF A<8>, LABEL	Test channel 5 input (A<8>)
314	315	2.0	3.2	IF A<10>, LABEL	Test channel 6 input (A<10>)
316	317	2.0	3.2	IF A<12>, LABEL	Test channel 7 input (A<12>)
320	321	2.0	3.2	IF A<14>, LABEL	Test channel 8 input (A<14>)
322	323	2.0	3.2	IF B<0>, LABEL	Test channel 9 input (B<0>)
324	325	2.0	3.2	IF B<15>, LABEL	Test channel 10 input (B<15>)
326	327	2.0	3.2	IF EXT7, LABEL	Test channel 11 input (EXT7)
330	331	2.0	3.2	IF EXT8, LABEL	Test channel 12 input (EXT8)
332	333	2.0	3.2	IF EXT9, LABEL	Test channel 13 input (EXT9)
334	335	2.0	3.2	IF EXT10, LABEL	Test channel 14 input (EXT10)
336	337	2.0	3.2	IF EXT11, LABEL	Test channel 15 input (EXT11)
340	341	2.0	3.2	IF EXT12, LABEL	Test channel 16 input (EXT12)
342	343	2.0	3.2	IF EXT13, LABEL	Test channel 17 input (EXT13)
344	345	2.0	3.2	IF EXT14, LABEL	Test channel 18 input (EXT14)
346	347	2.0	3.2	IF EXT15, LABEL	Test channel 19 input (EXT15)
350	351	2.0	3.2	IF EXT16, LABEL	Test channel 20 input (EXT16)
352	353	2.0	3.2	IF EXT17, LABEL	Test channel 21 input (EXT17)
354	355	2.0	3.2	IF EXT18, LABEL	Test channel 22 input (EXT18)
356	357	2.0	3.2	IF EXT19, LABEL	Test channel 23 input (EXT19)
360	361	2.0	3.2	IF EXT20, LABEL	Test channel 24 input (EXT20)
362	363	2.0	3.2	IF EXT21, LABEL	Test channel 25 input (EXT21)
364	365	2.0	3.2	IF EXT22, LABEL	Test channel 26 input (EXT22)
366	367	2.0	3.2	IF L, LABEL	Test channel 27 input (LINK)
370	371	2.0	3.2	IF PWOK, LABEL	Test channel 28 input (POWER OK)
372	373	2.0	3.2	Not used	Ground return for external inputs

APPENDIX B
MAINTENANCE HARDWARE CONSTRUCTION PROCEDURE

To facilitate diagnostic testing without having to connect the parallel and serial I/O channels to external equipment, the following jumper modules and plugs must be prepared by the user.

Interface Jumper Module 1

Interface Jumper Module 2

Two Serial I/O Jumper Plugs

Two W971 double-height modules and two Mate-N-Lok plugs are included with the equipment shipped. The user should install jumpers on the modules and plugs as detailed in the following paragraphs.

Interface Jumper Module 1

a. Secure the following items:

1. W971 Module
2. 22 AWG Bus Wire
3. Teflon Tubing

b. Using the Teflon tubing as insulation, connect the following pins together.

From	To
BA1	BB2
BB1	BD2
BC1	BE2
BD1	BF2
BE1	BH2
BF1	BJ2
BH1	BK2
BJ1	BL2
BK1	BM2
BL1	BN2
BM1	BP2
BN1	BR2

From	To
BP1	BS2
BR1	BT2
BS1	BU2
BU1	BV2
AK2	AV2
AA1	AB1
AB1	AC1
AC1	AD1
AD1	AE1
AE1	AF1
AF1	BA1

Interface Jumper Module 2

a. Secure the following items:

1. W971 Module
2. 22 AWG Bus Wire
3. Teflon Tubing

b. Using the Teflon tubing as insulation, connect the following pins together.

From	To	From	To
BA1	BB2	AA1	AB2
BB1	BD2	AB1	AD2
BC1	BE2	AC1	AE2
BD1	BF2	AD1	AF2
BE1	BH2	AE1	AH2
BF1	BJ2	AF1	AJ2
BH1	BK2	AH1	AK2
BJ1	BL2	AJ1	AL2
BK1	BM2	AL1	AN2
BL1	BN2	AM1	AP2
BM1	BP2	AN1	AR2
BN1	BR2	AP1	AS2
BP1	BS2	AR1	AT2
BR1	BT2	AS1	AU2
BS1	BU2	AU1	AV2
BU1	BV2	AK1	AM2

Serial I/O Jumper Plugs

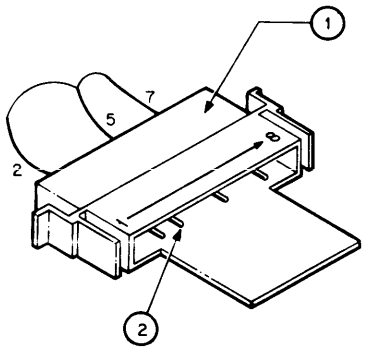
a. Secure the following items:

1. Two Mate-N-Lok plugs
2. Six male pins
3. 24 AWG Teflon stranded wire

b. On each plug connect pins 2, 5, and 7 together (Figure B-1).

CAUTION

The serial I/O interface module (M7313) will be damaged if the wrong pins are connected together. A total of eight pins can be installed in the connector; the pin insertion slots are not numbered — but are designated 1–8 as shown.



1-Mate-N-Housing (male) DEC No.12-9340-01
2-Connector Pins (male) DEC No.12-9378
4 required per cable

16-0068

Figure B-1 Serial I/O Jumper Plug

APPENDIX C
SIGNAL LISTING

Alphabetic signal listings with associated pin assignments of PDP16-M I/O and BUS signals and PDP-11 I/O signals are contained in this appendix (Tables C-1, C-2, and C-3).

Table C-1
PDP16-M I/O Slot Pin Assignments (By Signal Name)

Signal	Slot	Pin
AUTO RUN	D01	S1/U1
CONTINUE	C19	M2
EXT 1	C19	A1
EXT 2	C19	B1
EXT 3	C19	C1
EXT 4	C19	D1
EXT 5	C19	E1
EXT 6	C19	F1
EXT 7	C19	H1
EXT 8	C19	J1
EXT 9	C19	K1
EXT 10	C19	L1
EXT 11	C19	M1
EXT 12	C19	N1
EXT 13	C19	P1
EXT 14	C19	R1
EXT 15	C19	S1
EXT 16	C19	U1
EXT 17	C19	V1
EXT 18	C19	B2
EXT 19	C19	D2
EXT 20	C19	L2
EXT 21	C19	A2
EXT 22	C19	C2
FF1	C19	N2
FF1	D19	V1
FF2	C19	P2
FF2	C20	V1
FF3	C19	R2
FF3	D20	V1

Table C-1 (Cont)
PDP16-M I/O Slot Pin Assignments (By Signal Name)

Signal	Slot	Pin
FF4	C19	S2
FF5	C19	T2
FF6	C19	U2
GPI1 D00	D19	B2
GPI1 D01	D19	D2
GPI1 D02	D19	E2
GPI1 D03	D19	F2
GPI1 D04	D19	H2
GPI1 D05	D19	J2
GPI1 D06	D19	K2
GPI1 D07	D19	L2
GPI1 D08	D19	M2
GPI1 D09	D19	N2
GPI1 D10	D19	P2
GPI1 D11	D19	R2
GPI1 D12	D19	S2
GPI1 D13	D19	T2
GPI1 D14	D19	U2
GPI1 D15	D19	V2
GPI1 FF1	D19	V1
GPI1 I00	D19	A1
GPI1 I01	D19	B1
GPI1 I02	D19	C1
GPI1 I03	D19	D1
GPI1 I04	D19	E1
GPI1 I05	D19	F1
GPI1 I06	D19	H1
GPI1 I07	D19	J1
GPI1 I08	D19	K1
GPI1 I09	D19	L1
GPI1 I10	D19	M1
GPI1 I11	D19	N1
GPI1 I12	D19	P1
GPI1 I13	D19	R1
GPI1 I14	D19	S1
GPI1 I15	D19	U1
GPI2 D00	C20	B2
GPI2 D01	C20	D2
GPI2 D02	C20	E2
GPI2 D03	C20	F2
GPI2 D04	C20	H2
GPI2 D05	C20	J2
GPI2 D06	C20	K2
GPI2 D07	C20	L2
GPI2 D08	C20	M2
GPI2 D09	C20	N2
GPI2 D10	C20	P2

Table C-1 (Cont)
PDP16-M I/O Slot Pin Assignments (By Signal Name)

Signal	Slot	Pin
GPI2 D11	C20	R2
GPI2 D12	C20	S2
GPI2 D13	C20	T2
GPI2 D14	C20	U2
GPI2 D15	C20	V2
GPI2 FF2	C20	V1
GPI2 I00	C20	A1
GPI2 I01	C20	B1
GPI2 I02	C20	C1
GPI2 I03	C20	D1
GPI2 I04	C20	E1
GPI2 I05	C20	F1
GPI2 I06	C20	H1
GPI2 I07	C20	J1
GPI2 I08	C20	K1
GPI2 I09	C20	L1
GPI2 I10	C20	M1
GPI2 I11	C20	N1
GPI2 I12	C20	P1
GPI2 I13	C20	R1
GPI2 I14	C20	S1
GPI2 I15	C20	U1
GPI3 D00	D20	B2
GPI3 D01	D20	D2
GPI3 D02	D20	E2
GPI3 D03	D20	F2
GPI3 D04	D20	H2
GPI3 D05	D20	J2
GPI3 D06	D20	K2
GPI3 D07	D20	L2
GPI3 D08	D20	M2
GPI3 D09	D20	N2
GPI3 D10	D20	P2
GPI3 D11	D20	R2
GPI3 D12	D20	S2
GPI3 D13	D20	T2
GPI3 D14	D20	U2
GPI3 D15	D20	V2
GPI3 FF3	D20	V1
GPI3 I00	D20	A1
GPI3 I01	D20	B1
GPI3 I02	D20	C1
GPI3 I03	D20	D1
GPI3 I04	D20	E1
GPI3 I05	D20	F1
GPI3 I06	D20	H1
GPI3 I07	D20	J1

Table C-1 (Cont)
PDP16-M I/O Slot Pin Assignments (By Signal Name)

Signal	Slot	Pin
GPI3 I08	D20	K1
GPI3 I09	D20	L1
GPI3 I10	D20	M1
GPI3 I11	D20	N1
GPI3 I12	D20	P1
GPI3 I13	D20	R1
GPI3 I14	D20	S1
GPI3 I15	D20	U1
GROUND	C19	T1
MSYN	C19	K2
SI1 SI	C19	F2
SI1 SO	C19	E2
SI2 SI	C19	J2
SI2 SO	C19	H2
SSYN	C19	V2

Table C-2
PDP16-M Data Bus Pin Assignments (By Signal Name)

Signal	Pin (Slots AB01 – AB17)
Data Bit 00	AA1
Data Bit 01	AB1
Data Bit 02	AC1
Data Bit 03	AD1
Data Bit 04	AE1
Data Bit 05	AF1
Data Bit 06	AH1
Data Bit 07	AJ1
Data Bit 08	AK1
Data Bit 09	AL1
Data Bit 10	AM1
Data Bit 11	AN1
Data Bit 12	AP1
Data Bit 13	AR1
Data Bit 14	AS1
Data Bit 15	AU1
DATA ACCEPT	BA1
DATA READY	BB1
DONE	BC1
OVERFLOW	BD1
POWER CLEAR	BE1

Table C-3
PDP-11 Unibus Pin Assignments (By Signal Name)

Signal	Pin	Signal	Pin
A00L	BH2	D06L	AF1
A01L	BH1	D07L	AH2
A02L	BJ2	D08L	AH1
A03L	BJ1	D09L	AJ2
A04L	BK2	D10L	AJ1
A05L	BK1	D11L	AK2
A06L	BL2	D12L	AK1
A07L	BL1	D13L	AL2
A08L	BM2	D14L	AL1
A09L	BM1	D15L	AM2
A10L	BN2	GROUND	AB2
A11L	BN1	GROUND	AC2
A12L	BP2	GROUND	AN1
A13L	BP1	GROUND	AP1
A14L	BR2	GROUND	AR1
A15L	BR1	GROUND	AS1
A16L	BS2	GROUND	AT1
A17L	BS1	GROUND	AV2
ACLOL	BF1	GROUND	BB2
BBSYL	AP2	GROUND	BC2
BG4H	BE2	GROUND	BD1
BG5H	BB1	GROUND	BE1
BG6H	BA1	GROUND	BT1
BG7H	AV1	GROUND	BV2
BR4L	BD2	INITL	AA1
BR5L	BC1	INTRL	AB1
BR6L	AU2	MSYNL	BV1
BR7L	AT2	NPGH	AU1
C0L	BU2	NPRL	AS2
C1L	BT2	PAL	AM1
D00L	AC1	PBL	AN2
D01L	AD2	+5V*	AA2
D02L	AD1	+5V*	BA2
D03L	AE2	SACKL	AR2
D04L	AE1	DCLOL	BF2
D05L	AF2	SSYNL	BU1

*+5V is wired to these pins to supply power to the bus terminator only.

+5V should never be connected via the Unibus between system units.

APPENDIX D
PDP16-M MACHINE CODES

This is a list of all PDP16-M machine instructions. The basic PDP16-M hardware consists of:

Quantity	Model No.	Name	Module No.	Slot
1	KBS16-A	Bus Control	M7332	AB2
1	KAC16	GPA Control Unit	M7300	AB11
1	KAR16	GPA Register Unit	M7301	AB10
1	MR16-A	4-Word Constants Generator	M7307	AB5
1	MS16-A	Transfer Register	M7305	AB9
1	DB16-A	General Purpose Interface 1	M7311	AB12
1	PCS16-A	PCS Control	M7336	AB20
1	PCS16-B	PCS Control PROM	M7327	C16
4	PCS16-C	Evoke Decoders (0, 1, 2, 5)	M7328	CD3,4,5,8
1	PCS16-D	MUX0	M7329	AB18
2	KFL16	Flags (1,2,3)	M7306	C2

REGISTER TRANSFER INSTRUCTIONS (EVOKE)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
000	2.4	A=0	0	0		
001	2.4	A=B	0	1		
002	2.4	A=A+1	0	2		
003	2.4	A=A-1	0	3		
004	2.4	A=A+B	0	4		
005	2.4	A=A-B	0	5		
006	2.4	A=XORB	0	6		
007	2.4	A=AORB	0	7		
010	2.4	A=AB	0	10		
011	2.4	A=ANOT	0	11		

REGISTER TRANSFER INSTRUCTIONS (EVOKE) (Cont)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
012	2.4	A=A/2	0	12		
013	2.4	A=AX2	0	13		
014	2.4	A=A+1(S)	0	14		
015	2.4	A=A-1(S)	0	15		
016	2.4	A=A+B(S)	0	16		
017	2.4	A=A-B(S)	0	17		
020	2.4	A=A/2(S)	0	20		
021	2.4	A=AX2(S)	0	21		
022	2.4	B=0	0	22		
023	2.4	B=A	0	23		
024	2.4	B=A+B	0	24		
025	2.4	B=A-B	0	25		
026	2.4	B=AXORB	0	26		
027	2.4	B=AORB	0	27		
030	2.4	B=AB	0	30		
031	2.4	B=BNOT	0	31		
032	2.4	B=B/2	0	32		
033	2.4	B=A+B(S)	0	33		
034	2.4	B=A-B(S)	0	34		
035	2.4	B=B/2(S)	0	35		
036	2.4	EXA	0	36		
037	2.4	EXB	0	37		
040	2.2	GPI1=A	1	0		
041	2.0	A=GPI1	1	1		
042	2.2	GPI2=A	1	2	DB16-A	AB13
043	2.0	A=GPI2	1	3	DB16-A	AB13
044	2.2	GPI3=A	1	4	DB16-A	AB14
045	2.0	A=GPI3	1	5	DB16-A	AB14
046	2.4	B=C1	1	6		
047	2.4	B=C2	1	7		
050	3.5	SI1=A	1	10	DC16-A	AB16
051	2.1	A=SI1	1	11	DC16-A	AB16
052	1.7	TAPE1	1	12	DC16-A	AB16
053	3.5	SI2=A	1	13	DC16-A	AB17
054	2.1	A=SI2	1	14	DC16-A	AB17
055	1.7	TAPE2	1	15	DC16-A	AB17
056	1.8	FF1=0	1	16		
057	1.8	FF1=1	1	17		
060	1.8	FF2=0	1	20		
061	1.8	FF2=1	1	21		
062	1.8	FF3=0	1	22		
063	1.8	FF3=1	1	23		
064	1.8	FF4=0	1	24	KLF16	D2
065	1.8	FF4=1	1	25	KLF16	D2
066	1.8	FF5=0	1	26	KLF16	D2
067	1.8	FF5=1	1	27	KLF16	D2

REGISTER TRANSFER INSTRUCTIONS (EVOKE) (Cont)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
070	1.8	FF6=0	1	30	KLF16	D2
071	1.8	FF6=1	1	31	KLF16	D2
072	1.8	PAGE0	1	32	MORE THAN 2 PCS16-B	CD16 CD17
073	1.8	PAGE1	1	33	MORE THAN 2 PCS16-B	CD16 CD17
074	1.8	L=0	1	34		
075	1.8	L=1	1	35		
076	1.8	MUX0	1	36		
077	1.8	MUX1	1	37	PCS16-D	AB19
100	2.4	B=K1	2	0	MR16-D	AB8
101	2.4	B=K2	2	1	MR16-D	AB8
102	2.4	B=K3	2	2	MR16-D	AB8
103	2.4	B=K4	2	3	MR16-D	AB8
104	2.4	B=K5	2	4	MR16-D	AB8
105	2.4	B=K6	2	5	MR16-D	AB8
106	2.4	B=K7	2	6	MR16-D	AB8
107	2.4	B=K8	2	7	MR16-D	AB8
110	2.4	B=K9	2	10	MR16-D	AB8
111	2.4	B=K10	2	11	MR16-D	AB8
112	2.4	B=K11	2	12	MR16-D	AB8
113	2.4	B=K12	2	13	MR16-D	AB8
114	2.4	B=K13	2	14	MR16-D	AB8
115	2.4	B=K14	2	15	MR16-D	AB8
116	2.4	B=K15	2	16	MR16-D	AB8
117	2.4	B=K16	2	17	MR16-D	AB8
120	2.4	B=K17	2	20	MR16-D	AB8
121	2.4	B=K18	2	21	MR16-D	AB8
122	2.4	B=K19	2	22	MR16-D	AB8
123	2.4	B=K20	2	23	MR16-D	AB8
124	2.4	B=K21	2	24	MR16-D	AB8
125	2.4	B=K22	2	25	MR16-D	AB8
126	2.4	B=K23	2	26	MR16-D	AB8
127	2.4	B=K24	2	27	MR16-D	AB8
130	2.3	TR=A	2	30		
131	2.1	A=TRU	2	31		
132	2.1	A=TRL	2	32		
133	2.1	A=TR	2	33		
134	2.2	RMAR=A	2	34	PCS16-B and DB16-A	ABCD15
135	2.3	A=ROM	2	35	PCS16-B and DB16-A	ABCD15
136	2.4	B=C3	2	36		
137	2.4	B=C4	2	37		
140	2.2	A=SP1	3	0	MS16-C	AB4
141	2.2	A=SP2	3	1	MS16-C	AB4

REGISTER TRANSFER INSTRUCTIONS (EVOKE) (Cont)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
142	2.2	A=SP3	3	2	MS16-C	AB4
143	2.2	A=SP4	3	3	MS16-C	AB4
144	2.2	A=SP5	3	4	MS16-C	AB4
145	2.2	A=SP6	3	5	MS16-C	AB4
146	2.2	A=SP7	3	6	MS16-C	AB4
147	2.2	A=SP8	3	7	MS16-C	AB4
150	2.2	A=SP9	3	10	MS16-C	AB4
151	2.2	A=SP10	3	11	MS16-C	AB4
152	2.2	A=SP11	3	12	MS16-C	AB4
153	2.2	A=SP12	3	13	MS16-C	AB4
154	2.2	A=SP13	3	14	MS16-C	AB4
155	2.2	A=SP14	3	15	MS16-C	AB4
156	2.2	A=SP15	3	16	MS16-C	AB4
157	2.2	A=SP16	3	17	MS16-C	AB4
160	2.6	SP1=A	3	20	MS16-C	AB4
161	2.6	SP2=A	3	21	MS16-C	AB4
162	2.6	SP3=A	3	22	MS16-C	AB4
163	2.6	SP4=A	3	23	MS16-C	AB4
164	2.6	SP5=A	3	24	MS16-C	AB4
165	2.6	SP6=A	3	25	MS16-C	AB4
166	2.6	SP7=A	3	26	MS16-C	AB4
167	2.6	SP8=A	3	27	MS16-C	AB4
170	2.6	SP9=A	3	30	MS16-C	AB4
171	2.6	SP10=A	3	31	MS16-C	AB4
172	2.6	SP11=A	3	32	MS16-C	AB4
173	2.6	SP12=A	3	33	MS16-C	AB4
174	2.6	SP13=A	3	34	MS16-C	AB4
175	2.6	SP14=A	3	35	MS16-C	AB4
176	2.6	SP15=A	3	36	MS16-C	AB4
177	2.6	SP16=A	3	37	MS16-C	AB4
200	2.2	A=SP17	4	0	MS16-C	AB3
201	2.2	A=SP18	4	1	MS16-C	AB3
202	2.2	A=SP19	4	2	MS16-C	AB3
203	2.2	A=SP20	4	3	MS16-C	AB3
204	2.2	A=SP21	4	4	MS16-C	AB3
205	2.2	A=SP22	4	5	MS16-C	AB3
206	2.2	A=SP23	4	6	MS16-C	AB3
207	2.2	A=SP24	4	7	MS16-C	AB3
210	2.2	A=SP25	4	10	MS16-C	AB3
211	2.2	A=SP26	4	11	MS16-C	AB3
212	2.2	A=SP27	4	12	MS16-C	AB3
213	2.2	A=SP28	4	13	MS16-C	AB3
214	2.2	A=SP29	4	14	MS16-C	AB3
215	2.2	A=SP30	4	15	MS16-C	AB3
216	2.2	A=SP31	4	16	MS16-C	AB3
217	2.2	A=SP32	4	17	MS16-C	AB3

REGISTER TRANSFER INSTRUCTIONS (EVOKE) (Cont)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
220	2.6	SP17=A	4	20	MS16-C	AB3
221	2.6	SP18=A	4	21	MS16-C	AB3
222	2.6	SP19=A	4	22	MS16-C	AB3
223	2.6	SP20=A	4	23	MS16-C	AB3
224	2.6	SP21=A	4	24	MS16-C	AB3
225	2.6	SP22=A	4	25	MS16-C	AB3
226	2.6	SP23=A	4	26	MS16-C	AB3
227	2.6	SP24=A	4	27	MS16-C	AB3
230	2.6	SP25=A	4	30	MS16-C	AB3
231	2.6	SP26=A	4	31	MS16-C	AB3
232	2.6	SP27=A	4	32	MS16-C	AB3
233	2.6	SP28=A	4	33	MS16-C	AB3
234	2.6	SP29=A	4	34	MS16-C	AB3
235	2.6	SP30=A	4	35	MS16-C	AB3
236	2.6	SP31=A	4	36	MS16-C	AB3
237	2.6	SP32=A	4	37	MS16-C	AB3
240	2.3	MAR1=A	5	0	MS16-D or E	AB6
241	3.6	MEM1=A	5	1	MS16-D or E	AB6
242	3.9	A=MEM1	5	2	MS16-D or E	AB6
243	2.3	MAR2=A	5	3	MS16-D or E	AB7
244	3.6	MEM2=A	5	4	MS16-D or E	AB7
245	3.9	A=MEM2	5	5	MS16-D or E	AB7
246	2.2	RMAR=B	5	6	PCS16-B and DB16-A	ABCD15
247	2.3	B=ROM	5	7	PCS16-B and DB16-A	ABCD15
250	2.0	TR=0	5	10		
251	2.1	B=SI1	5	11	DC16-A	AB16
252	3.5	SI1=B	5	12	DC16-A	AB16
253	2.1	B=SI2	5	13	DC16-A	AB17
254	3.5	SI2=B	5	14	DC16-A	AB17
255	2.2	GPI1=B	5	15		
256	2.0	B=GPI1	5	16		
257	2.4	B=A+1	5	17		
260	2.4	B=A+1(S)	5	20		
261	2.4	B=A-1	5	21		
262	2.4	B=A-1(S)	5	22		
263	2.4	B=AX2	5	23		
264	2.4	B=AX2(S)	5	24		
265	2.4	B=A/2	5	25		
266	2.4	B=A/2(S)	5	26		
267	1.8	L=OVF	5	27		
270	1.8	L=LNOT	5	30		
271	–	HALT	5	31		
272	2.4	A=B/2	5	32		
273	2.4	A=B/2(S)	5	33		

REGISTER TRANSFER INSTRUCTIONS (EVOKE) (Cont)

Machine Code (Octal)	Time (μsec)	Instruction	Evoke Decoder No.	Evoke Decoder Channel	Option	Slot
274	–	DATI	5	34		
275	–	DATO	5	35		
276	2.3	TRU=A	5	36		
277	2.3	TRL=A	5	37		

CONDITIONAL JUMP INSTRUCTIONS (INPUT MULTIPLEXER)

Machine Code (Octal)*		Time (μsec)		Instruction	Multiplexer No. **	Multiplexer Channel
MEM0	MEM1	False	True			
300	301	2.0	3.2	GOTO	0	00
302	303	2.0	3.2	IF EXT1,	0	01
304	305	2.0	3.2	IF EXT2,	0	02
306	307	2.0	3.2	IF EXT3,	0	03
310	311	2.0	3.2	IF EXT4,	0	04
312	313	2.0	3.2	IF EXT5,	0	05
314	315	2.0	3.2	IF EXT6,	0	06
316	317	2.0	3.2	IF DZ,	0	07
320	321	2.0	3.2	IF DP,	0	10
322	323	2.0	3.2	IF DN,	0	11
324	325	2.0	3.2	IF OVF,	0	12
326	327	2.0	3.2	IF A<1>,	0	13
330	331	2.0	3.2	IF A<3>,	0	14
332	333	2.0	3.2	IF A<5>,	0	15
334	335	2.0	3.2	IF A<7>,	0	16
336	337	2.0	3.2	IF A<9>,	0	17
340	341	2.0	3.2	IF A<11>,	0	20
342	343	2.0	3.2	IF A<13>,	0	21
344	345	2.0	3.2	IF A<15>,	0	22
346	347	2.0	3.2	IF FF1,	0	23
350	351	2.0	3.2	IF FF2,	0	24
352	353	2.0	3.2	IF FF3,	0	25
354	355	2.0	3.2	IF FF4,	0	26
356	357	2.0	3.2	IF FF5,	0	27
360	361	2.0	3.2	IF FF6,	0	30
362	363	2.0	3.2	IF KF1,	0	31
364	365	2.0	3.2	IF PF1,	0	32
366	367	2.0	3.2	IF KF2,	0	33
370	371	2.0	3.2	IF PF2,	0	34
372	373	2.0	3.2	IF CLK,	0	35
300	301	2.0	3.2	GOTO	1	00
302	303	2.0	3.2	IF A<0>,	1	01
304	305	2.0	3.2	IF A<2>,	1	02

CONDITIONAL JUMP INSTRUCTIONS (INPUT MULTIPLEXER) (Cont)

Machine Code (Octal)*		Time (μsec)		Instruction	Multiplexer No. **	Multiplexer Channel
MEM0	MEM1	False	True			
306	307	2.0	3.2	IF A<4>,	1	03
310	311	2.0	3.2	IF A<6>,	1	04
312	313	2.0	3.2	IF A<8>,	1	05
314	315	2.0	3.2	IF A<10>,	1	06
316	317	2.0	3.2	IF A<12>,	1	07
320	321	2.0	3.2	IF A<14>,	1	10
322	323	2.0	3.2	IF B<0>,	1	11
324	325	2.0	3.2	IF B<15>,	1	12
326	327	2.0	3.2	IF EXT7,	1	13
330	331	2.0	3.2	IF EXT8,	1	14
332	333	2.0	3.2	IF EXT9,	1	15
334	335	2.0	3.2	IF EXT10,	1	16
336	337	2.0	3.2	IF EXT11,	1	17
340	341	2.0	3.2	IF EXT12,	1	20
342	343	2.0	3.2	IF EXT13,	1	21
344	345	2.0	3.2	IF EXT14,	1	22
346	347	2.0	3.2	IF EXT15,	1	23
350	351	2.0	3.2	IF EXT16,	1	24
352	353	2.0	3.2	IF EXT17,	1	25
354	355	2.0	3.2	IF EXT18,	1	26
356	357	2.0	3.2	IF EXT19,	1	27
360	361	2.0	3.2	IF EXT20,	1	30
362	363	2.0	3.2	IF EXT21,	1	31
364	365	2.0	3.2	IF EXT22,	1	32
366	367	2.0	3.2	IF L,	1	33
370	371	2.0	3.2	IF PWOK,	1	34
372	373	2.0	3.2	Not used		

SUBROUTINE INSTRUCTIONS

Machine Code (Octal)	Time (μsec)	Instruction
374	3.2	CALL – Jump to a Subroutine in Memory 0
375	3.2	CALL – Jump to a Subroutine in Memory 1
376	3.2	EXIT – Return from a Subroutine

*Codes are given for jumps into or within memory 1 and into or within memory 2. The least significant bit of the machine code is the M (memory) bit.

**Multiplexer 1 (PCS16-D) is optional and resides in slot AB19 of the logic assembly. The MUX0 and MUX1 commands are used to select one or the other multiplexer.

READER'S COMMENTS

PDP16-M MAINTENANCE MANUAL
DEC-16-HMMMA-A-D

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

_____

What faults do you find with the manual? _____

_____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

_____

_____

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Would you please indicate any factual errors you have found. _____

_____

_____

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Please describe your position. _____

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