digital INTEROFFICE MEMORANDUM

DATE: October 23, 1969

SUBJECT: KA11 Design Critique or "How I Might Do It Now"

TO: Bruce Delagi

FROM: Jim O'Loughlin

cc: KA11 Design Review Committee
KA11 Log
Status Report

COMPANY CONFIDENTIAL

Summary

The KA11 is designed, breadboarded, and in the prototype stage; release to production and high volume production is imminent. Design changes are limited to fixes (necessary fixes).

This critique attempts to catalog those areas that might be improved in the design of a new processor or in the redesign of the present processor. (High volume might make this desirable). All questioned areas are noted independent of meritorious solutions; the Design Review may reveal more.

Data Paths

1. The multiple input latch might be replaced with edge-triggered storage. The original use of latches facilitated: multiple inputs; speed of data transfer; and inexpensive data storage. The first is still true. The use of H series D-type flip-flops compromises the second, as does the present additional clocking level required on data path control signals. The use of the shift register (Signetics 8271B) or some multiple, edge-triggered, flip-flops eases the cost.

In general, the savings in the data path storage was expended in control.

2. The use of a quad adder (Signetics 8260) which is fast (54 nanoseconds for 16 bits) and provides the AND function without resorting to DeMorgans Theorem and multiple cycles.

3. The allowance of an internal memory Read and Write within the same cycle would speed (and perhaps simplify) machine operation.

4. The location of shift/rotate gating at the inputs to the data path might be investigated for the next processor. The cost is great for multiple inputs; the time savings moderate.

5. A direct path from the data path output to input is necessary for faster operation in multiply or divide.

Memory

1. The memory appears satisfactory, but both polarities of the output might be desired with direct bus access. No memory inhibit exists to allow expansion beyond 16 words.

Bus Interface

1. The bus has evolved and so has the processor interface with the result containing a great deal of history. The processor, as a bus master, is also responsible for bus operation and overall timing. this adds to cost and complexity.

2. A great number of pulse circuits are used within the asynchronous bus interface to provide delay and pulses. The pulse is occassionally used twice with the low pulse level providing an immediate set or clear and the delayed rising edge used as a clock input. Such use reduces the number of pulse circuits but no apparent method appears for elimination.

3. The need for some delay elements is questionable when the average gate delay is considered. Worst case (fast gates) require such discrete circuit delays. The inclusion of such delays slows the bus transactions. Is our present pragmatic worst-case design philosophy too liberal or conservative?

4. The use of the cheap, discrete circuit, one-shots results in large tolerances with correspondingly larger delays in ansynchronous operation; the use of the Fairchild 9601 I.C. would provide tighter tolerances at some cost.

5. The previous mentioned ability to Read and Write within the same machine cycle would reduce the bus operations. The elimination of a single bus cycle would free a state specifically for rest (BSRØ is now used and must be also used in the DATO operation as a data Read). The DATO operation would most benefit from the reduction.

The use of byte-shifting input hardware would free two bus cycles but require the shift/rotate gating below the adder.

6. The addition of bus access from Memory would provide some speed on some address and data operations. It would cost in control logic.

7. The NPR servicing (as well as the BR) has perhaps suffered most in the evolution of bus and processor. The determination of next bus master does occur simultaneously with processor operation, but the granting is similar to the previous PTR sequence. BR servicing has a low priority and does not occur on trap instructions.

The processor asserts BBSY when it is in control, independent of bus operation. Since this involves considerable basic design, the more desirable method of asserting BBSY on a bus operation cannot be implemented.

General Timing

1. The use of H Series to speed and control skew should allow high speed operation at a system clock period of 280 nanoseconds. Because machine instructions are complicated, little can be done to ease this requirement. Parallel paths in the new processor might allow fewer cycles of greater period.

2. Clock skew on flip-flop inputs was accentuated by the gating of flip-flop clock inputs by data change. This gating is provided by the shift register (Signetics 8271B) and has been used to replace the above in most instances. The delay within the combinational logic and the inertia delay in the state flip-flops limits the effect of skew on the gated inputs.

3. The use of shift registers and the asynchronous clock has worked well. With a machine of many states it appears to be the way to go. The use of an additional flip-flop, CLK OFF, is necessitated by the clock rest state and need for console input. A cleaner method would involve a different clock rest state; the continued use of separate console timing; and the elimination of a gating level in a critical skew path.

4. The use of separate timing for console operation appears proper with the main clock turned off. This might be re-evaluated as the clock must be turned on for a EXAM (DATI) and DEP (DATO). The use of system clock with a full shift register might reduce the number of gating inputs on combinational logic or, at least, provide a full dedicated console rest state.

5. The use of the DATA WAIT flip-flop provides simplification in bus operation, latch operation, and combinational logic gating. It specifically indicates that the machine is waiting for a bus response; it also requires considerable control logic. Can a savings be made?

Logic Gating

1. The combinational logic was somewhat minimum, and has been compromised slightly by module assignment. These modules are straightforward and easily tested by CMT programs. The new processor might minimize more by using more machine states but this would add to machine time.

2. Fixes have been made to make existing logic work; the overall logic, therefore, is not as minimum as it might be.

Printed Circuits

1. The present constraints upon the use of 80 mil tape in layout (if enforced) prohibits some KA11 boards. The original (and proper design) estimate of 60 IC per quad board is not correct if 120 mil tape must be used. In addition to prohibiting boards, extensive time is required in all layout.

In time, the use of 60 IC on a control logic layout will be standard. The layout should include the layout suggestions in "Large Module Layout, Revision 2". If the constraints still exist, then a 50 IC's maximum should be considered.

2. The committment to layout and etch of untested logic on large boards should be avoided. Schedules don't allow it; but the book-keeping on module corrections is extensive.