G. Saviers

2-0035-9

digital INTEROFFICE MEMORANDUM

DATE: 18 February 1969

SUBJECT: PDP-11 Electrical Design Review Minutes

TO: PDP-11 Design Review Committee
Engineering Committee
R. Cady
N. Mazzarese

FROM: Jerry Butler

The first session of the PDP-11 Design Review was held on Monday, 17 February 1969. The following people were present:

R. Pyle	I. Morris	G. Fligg
R. Best	D. Dubay	R. Cady
G. Saviers	G. Butler	

Roger Cady outlined the project goals as follows:

The PDP-11 is being designed to meet the low-cost market. It will sell in configurations which cost less than the PDP-8/L and will expand into configurations as large as some PDP-9's. The principal PDP-11 customer will be the Original Equipment Manufacturer. The PDP-11 will meet the requirements of a customer who is sold on 16 bits. The PDP-11 will have 8-bit byte handling capability. Manufacturing cost targets are as follows:

8-bit Processor - $700-$800
8-bit, 4K, 3 usec Memory - $850
Power Supply & Cabinet - $250

Two PDP-11 machines are proposed:

Model A - 16-bit Processor with 16-bit, 1 usec Memory
Model B - 8-bit Processor with 8-bit, 3 usec Memory

The planned delivery schedule includes the following:

Date	Hardware	Peripherals	Software
Fall '69	Model B	Teletype only	PDP-10 Simulator, Basic Assem., Edit, Math Pkg., ODT

Date	Hardware	Peripherals	Software
Jan '70	Model B	Paper Tape Reader, Punch, & Other Small Peripherals	Complex Assembler FORTRAN
Summer '70	Model A	Larger Peripherals (Disk, Magtape)	Monitor System

The Design Review Committee cautioned Roger Cady that the largest machine should be designed at the same time as the small one to make sure that the largest system can really be built without a lot of compromises. It isn't necessary to deliver the large machine first, but its design should proceed concurrent with the small machine.

The PDP-11 is designed to be modular in nature. Each "macro module" will plug into the power supply and the I/O bus. Each macro module will consist of two or four quad height, extended depth modules. Typical "macro modules" are a processor, a memory, or a peripheral.

The Design Review Committee suggested that Roger find out what the manufacturing rejection rate of quad boards will be. Roger tentatively plans to use the depot repair facility for field maintenance. ECO's on quad board machines will be almost impossible and very costly. Roger should present to the Design Review Committee the details of a plan for field maintenance in respect to the quad board. Field Service spares investment should be estimated and a plan for keeping Field Service stocked should be presented. The choice to use quad (large) boards is based on expected reduction in manufacturing costs due to minimizing wiring.

Bit numbering and hexadecimal notation were discussed and the Committee agreed that hexadecimal notation should be used and that the numbering of bits should be the inverse of that used by early DEC machines.

The machine addressing schemes were discussed. It was pointed out that if a chain of 16-bit memory reference instructions began at an odd byte address, the 16-bit or 2-byte memory would end up making as many memory references as the 8-bit memory in spite of its larger word size. It will be the function of the complex assembler to optimize the code to minimize this problem. The Committee agreed that simulating a number of programs on the PDP-10 will show the effectiveness of this assembler and could also show what the optimum memory word sizes would be (i.e., 8, 16, 24, 32 bits, etc.).

It was also pointed out that with the basic assembler, the programmer would have to optimize his own programs. With the complex assembler, the assembler will do it, but it may take as much as 32K bytes of memory for this program to run satisfactorily.

In discussing the PDP-11 instruction set, the ADD BYTE, AND BYTE, COMPARE BYTE, and LOAD BYTE instructions were covered.

It was suggested that the LOAD BYTE instruction clear the upper byte to zeros instead of copying the sign into those bits. The ADD BYTE instruction is fine as is (sign with 7 bits magnitude).

It was suggested that an "OR" instruction be added to the instruction set in place of some other less useful instruction. Using the op codes now occupied by "AND" byte and "ADD" byte was suggested but not agreed to by the Committee.

The next Design Review meeting will be held at the same place (Conference Room A, building 12) and at the same time (1:00) on February 24. The instruction set will be discussed in further detail at this session. Roger Cady will make available the competitive analysis data on the instruction set for the Committee's analysis and general comment.

If I have omitted something or failed to comment correctly on the minutes, please contact me as soon as possible at X2215.

Members of PDP-11 Design Review Committee

R. Pyle	I. Morris	G. Fligg
R. Best	D. Dubay	R. Cady
G. Saviers	G. Butler	D. Zereski
A. Kotok	H. Godfrey	

Members of Engineering Committee

R. Doane	R. Cady	J. St. Amour
K. Olsen	W. Melesky	T. Stockebrand
R. Best	A. Kent	R. Clayton
G. Butler		

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