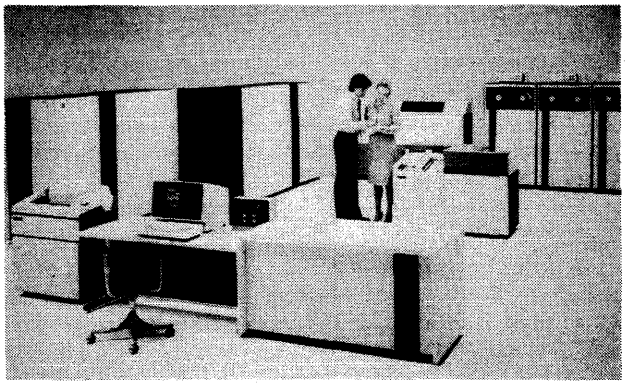
ICL Atlas 10



ICL has introduced two ultra-high powered computer systems - the Atlas 10 Models 15 and 25. Both are compatible with the largest IBM and other plug-compatible computers and have processing powers between three and five times greater than the IBM 3033 computer.

This picture shows the single processor ICL Atlas 10 Model 15 computer.

The ICL Atlas 10 series consists of two computers, one a dual version of the other. They are Fujitsu based systems in the super-computer class, offering a three to five times performance increase over the IBM 3033. Their chief target is the IBM 308X series but they are compatible with IBM's System 370, 303X and 308X series.

MODEL: Atlas 10 Model 15; Atlas 10 Model 25.

CONFIGURATIONS: One or two central processors, from 16 to 64MB of main memory in single processor version, from 32 to 128MB in dual processor system (Model 25). Up to four channel processors can be attached, each with up to 16 I/O channels, to either Model 15 or 25.

COMPETITION: IBM 308X series and other PCMs such as Olivetti and BASF using Hitachi based computers and NAS and Amdahl.

PRICING: Atlas 10 model 15, 16M bytes main memory, 16 channels, Service Processor, console, VDU, printer priced at £1.7 million; Atlas 10 model 25, basic model plus extensive disk capacity, magnetic tapes and two 2000 lpm printers priced at £2.99 million.

MANAGEMENT SUMMARY

The ICL Atlas 10 series comprises, at present, two models, the model 15 and model 25. Both were announced in May 1982 and scheduled for initial deliveries in summer 1983. They are very large scale systems based on the Fujitsu M380/382 and will compete strongly with machines like the IBM 308X series and other top-end mainframes. Their main attractions are their claimed three to five times power increase over the IBM 3033, their ability to run all relevant IBM software, and their compactness and relatively low power consumption. An additional appeal of these computers is that they are backed by ICL, which, after a very shaky 1981 and early 1982 are now well on the road to financial stability once again.

The Atlas 10 model 25 is essentially a dual model 15. The model 15 can be field upgraded to a model 25. The power increase of the model 25 over the model 15 is 1.7, with this being a real increase because of the duality, rather than theoretical increases in power which are often claimed due to purely processor upgrades. Since the difference between the two models is a duplication of processors and therefore a corresponding increase in power, everything which follows applies to both machines unless otherwise stated.

The power of a machine is a direct function of its processing and data handling capabilities. In virtually all applications today, including the scientific, there will usually be large amounts of information to handle especially as massive databases become commonplace. Thus, the number of processors in a multiprocessor configuration is significant, as is the way these processors are assigned.

When viewed from this perspective the Atlas 10 fares well. It is one processor in basic form but can have one of two ➢

CHARACTERISTICS

VENDOR: ICL, ICL House, Putney, London SW15. Telephone (01)-788-7272.

MANUFACTURER: Fujitsu Ltd., Communications and Electronics, Tokyo, Japan.

MODELS: ICL Atlas 10 Model 15 with two alternative processors: ICL Atlas 10 Model 25, based on Fujitsu Facom Models M380 and M382 respectively.

DATE ANNOUNCED: May 1982 for both models.

DATE OF FIRST DELIVERY: As a Fujitsu machine—summer 1982 in Japan. First deliveries Atlas models—spring 1983.

DATA FORMATS

BASIC UNIT: 8-bit byte. Each byte can represent one alphanumeric character, two BCD digits or 8 binary bits. Two consecutive bytes form a half-word of 16-bits, four consecutive bytes a word of 32-bits and eight consecutive bytes a double word of 64 bits. ➢

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central processors (one at ten million instructions per second (mips) and the other at 15 mips) from one to four channel processors and a service processor. These service up to 64M bytes of main memory split into two main storage units (MSUs).

The actual processing on the Atlas 10 is also aided by three functional units. They accelerate processing by dividing it between an instruction unit, an execution unit and a Local Buffer Storage. Details of the instruction unit and the execution unit are given in the Characteristics section of this report. The Local Buffer Storage, (LBS), is a high speed unit, and has a capacity of 64K bytes composed of a series of 4K-bit RAMs with a 5.5 nanosecond access time. The purpose of this LBS unit is the same as a cache memory-that is, to hold the most frequently used instructions and data. The total effect of these elements on the processing power of the Atlas 10 series is considerable.

The Atlas 10 matches its processing power with efficient data handling capability by the use of from one to four Channel Processors (CHPs) and, if network activities are contemplated, by the addition of ICL 2806G Communications Control Processors. A maximum nominal data transfer rate of 96M bytes per second can be achieved with the four channel processors.

The complement of from one to four CHPs is controlled by the (maximum one) Memory Control Unit (MCU). The model 15 has one MCU and the model 25 two MCUs. The MCU controls data transmission between the main memory unit or units (one standard, two maximum) called Main Storage Units (MSUs) and the central processor; it also controls data transmission between the CPU and the channel processors. In addition, the MCU handles the reporting of errors to a service processor, one of which is standard on the Atlas 10 series. This logs all errors and effects diagnostic tests. The remaining duty of the MCU is to look after the reconfiguration function, if a faulty CPU, MSU or CHP is found.

This error handling function of the MCU is enhanced by its 256K byte Global Buffer Storage (GBS) which has a 16 nanosecond access time. It ensures that all 4-bit errors, called "single block" by ICL, are corrected and that all 8-bit errors (double block) are detected and reported. Possible error on the Atlas 10 is minimized by (a) the use of multi-chip carriers to decrease the number of internal connections and signal path lengths (b) the use of Emitter Coupled Logic, which packs up to 1300 gates per chip, this minimizing connection lengths and (c) by using extensive error correction codes and alternative chip assignments with automatic fallback to parts of buffer storage.

The Channel Processors (minimum one, maximum 4 on both the model 15 and 25), can be envisaged as a giant multiplexer with 16 channels going to input/output and one going to the (MCU).

The maximum data rate of a Channel Control Processor (CHP) is 24M bytes per second. Configurations of the CHP can have any number of the maximum 16 channels allocat-

FIXED POINT OPERANDS: Range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING POINT OPERANDS: One word consisting of a 24-bit fractional part and a 7-bit hexadecimal exponent in "short" format: two words comprising a 56-bit fraction and a 7-bit exponent in "long" format or four words in extended precision format.

INSTRUCTIONS: 2, 4 or 6 bytes long specifying 0, 1 or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: MOS (Metal Oxide Semiconductor) 64K-bit dynamic RAM chips.

CAPACITY: model 15; 16, 24, 32, 48 or 64 megabytes. Model 25; 32, 48, 64, 96 or 128 megabytes. Main memory is made up of one or more Main Storage Units (MSUs), with each MSU having up to a maximum of 32 megabytes capacity. A maximum of four MSUs can be linked to the one Memory Control Unit (MCU) in a system. Each MSU consists of two segments and a Memory Access Controller (MAC) to control the segments. Two access modes are available. One is block fetch mode to transfer MSU data to the Global Buffer Store (GBS), a form of cache memory—and the other is block store mode to transfer (swap) data from the GBS to the MSU. Interleaving is used for optimum access/addressing efficiency.

CYCLE TIME: the normal 150 nanosecond cycle time of the 64K-bit RAMS used for main storage is aided by what amounts to two forms of cache memory. The first, called Local Buffer Store (LBS), fulfills the role of normal conventional cache memory, and the second, called Global Buffer Store, (GBS), is not only associated with and accessible from the central processor (as is conventional cache) but is also accessible from the Channel Processors (CHPs). The effect of these cache memory equivalents which both operate on a Least Recently Used (LRU) basis is considerable, especially since the LBS uses 4K bit chips with an access time of 5.5 nanoseconds and the GBS uses 16K bit chips with an access time of 16 nanoseconds.

The capacity of the LBS is 64K bytes and it works in the same way as conventional cache memory. The best way to regard LBS is to consider it as an array of 64 rows with each row comprising 16 boxes of 64 bytes per box. The initial contents of the LBS are selected by a hashing algorithm which puts a selected part of the main memory into those 64K bytes. If this hashing algorithm is successful, a very large portion of addresses used in instructions will, in fact, access LBS. If a miss occurs, in other words, the address is not in the LBS, then the contents of main memory in that address are placed into LBS. Hence the term "Least Recently Used" (LRU) applied to this type of establishment of cache memory contents.

LBS contains three types of memory array, LBS, TAG, TBS DATA and the REPLACE ARRAY. LBS TAG contains the real addresses which correspond to the maximum 64 entries x 16 ways, where each entry contains up to 64 bytes. LBS DATA contains 64 bytes of data and 8 parity bits. REPLACE ARRAY handles the utilization frequency of the data in the LBS. AS stated above, the entry with the lowest utilization frequency is the first to be replaced in the LBS.

ed at block multiplexer channels, but the maximum number of these channels which can be byte multiplexer channels is four. The data transfer rate on byte multiplexer channels is up to 110K bytes/second, dependent on mode and each Block Multiplexer Channel, 3M bytes per second. Each CHP can have up to 1024 or 2048 sub-channels. Controllers are connected to channels and peripheral are addressed and accessed directly via sub-channels.

The main peripheral units on the Atlas 10 systems are disks and workstations in the form of VDU terminals. The disks, called "disc enclosures" by ICL, can provide very high capacities. Typical of these would be the ICL 6421 which provides two "disc enclosures" that have a maximum capacity of 0.9K million bytes (1.8 gigabytes) in native mode and 0.635 gigabytes in IBM 3350 competitive mode. These can be backed up for record keeping purposes by a variety of high speed, high density magnetic tape drives.

Workstations for the Atlas 10 series are offered only in the form of local 1920 character VDUs. Remote workstations are not provided directly, but sub-systems, such as ICL's DRS 20 series or ICL's System 25, will meet most needs.

The main printer offered for the Atlas series is one with a speed of 2000 lines per minute, although, if very high speed is required, ICL's laser printer at over ten times that speed could be attached.

Unlike many previous ICL machines stemming from the mid-seventies, the Atlas 10 series, along with many recent ICL systems, has excellent communications and networking capabilities. These are handled by one or more ICL 2806 Communications Control Processors (CCPs), each of which contains an independent processor, storage, channel adapters and line control units. These CCPs can be used to interface Atlas 10 computers to networks and communications entities of many types, including packet-switched and other X-level protocol-using systems. They can also be used with ICL's Information Processing Architecture.

Software for the Atlas 10 series is considerable and of major significance. ICL provides the facility of running under either Atlas OS or IBM's MVS/SP operating system. VM 370, using the AVM Assist feature, will also run on these machines. The software, in more general terms, has been specifically designed to allow packages written by software houses and others primarily to run on IBM machines, to run, without modification, on Atlas 10.

As may be expected on this class of machine, the maximum 64M bytes of actual main memory is augmented by the availability of 16M bytes of virtual memory per address space. This allows up to 1536 (MVS limit) active tasks to be resident, using the currently available MVS. Future software releases will permit the use of up to 2 gigabytes of virtual memory per address space. Optimization of resources is carried out in Atlas OS by software called System Decision Management (SDM). SDM keeps a check on the resources used by programs and transactions and automatically adjusts the frequency of serving the units used, stops

The maximum capacity of the Global Buffer Storage (GBS) is 256K bytes. It can be shared by a maximum of two CPUs and four Channel Processors (CHPs).

The way the GBS works can best be understood by considering GBS to be just one location. If an instruction addresses main memory and the main memory location addressed happens to be the one location in GBS, then GBS will report to the addressing mechanism that it contains the information and the GBS location will then be read or written to as required. If, however, GBS does not contain the address, then the slower main memory location addressed will have its contents swapped with the existing contents of the GBS location so that from that point on, every time that location is addressed, there will be automatically routing to the GBS. This entire procedure is known as "store swapping."

CHECKING: the two main features present in the extensive checking carried out on the Atlas 10 series computers are automatic error checking and correction (ECC) and automatic reconfiguration.

The entire storage area is read at fixed intervals and the ECC corrects one-bit errors if present, rewriting the bit to main memory. ECC also detects two or more one-bit errors in the same storage element.

Automatic switching to an alternative memory device happens if a further one-bit error is found at another address in the same device. Each segment of the MSU has an alternative spare memory device, which is assigned an arbitrary address and to which switching takes place as required.

STORAGE PROTECTION:

The whole of main memory is divided up into 2K or 4K pages. Each page has its own flag bits which inform the system whether that particular page is read or write accessible. If an invalid read or write attempt is made, then an interrupt occurs. In addition to this form of protection, the absolute locations, 0–511, used by the system, are totally prohibited and protected from use.

RESERVED STORAGE: the absolute locations 0–511 are reserved for interrupt routines, program status words and other system requirements. Control storage, which contains microprograms for pipelining operations among other things, consists of 2048 words, each of 104 bits in the Executon Unit and 768 words of 190 bits in the Instruction Unit. These two microprogrammed units operate in parallel independently of the CPU to enhance that unit's overall throughput.

CENTRAL PROCESSORS

The Atlas 10 model 15 can be considered as the single central processor version of the Atlas 10 model 25, in the same way as the Fujitsu M380 can be thought of as having half the CPU power of the M382, the Fujitsu models being the base for the Atlas 10 system models. The other processors in an Atlas 10 system are the Channel Processors (CHPs) and the Service Processors (SVPs). Both CHPs and SVPs are units which are independent of their CPUs.

The maximum configuration of an Atlas 10 model 15 comprises one central processor, four channel processors, one Memory Control Unit (MCU), one Service Processor and two Main Storage Units (MSUs) each of 32 megabytes.

The maximum configuration of the Atlas 10 model 25 is two central processors (each identical to that on the model 15), four channel processors, two Service Processors each con-

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queues becoming too long for the system to handle in a reasonable response time, and prevents the system running out of resources altogether. When there is more than one central processor, as on the Atlas 10 model 25 or when loosely coupled, SDM is replaced by its expanded version, called Global System Decision Management (GSDM).

What SDM and GSDM do not do is handle input/output streams. This side of resource management is carried out by Job Management (JES), this looks after the scheduling and spooling of I/O streams under conditions varying from loosely coupled systems to networks.

For program development and interactive execution of programs, ICL provides under Atlas OS, a timesharing system called TSS. Among other things, TSS enables commands to be given for the use of high-level languages (Cobol, Fortran and PL/1, for example) and also offers debugging and tuning facilities for those same languages.

Compilers available include those for APL, Algol, Cobol, RPG, Basic, Fortran 77, Fortran HE and Lisp. Macro-level compilers, such as Hyper Cobol aid rapid program developement.

Database and related areas are catered for under Atlas OS by the Advanced Informaton Manager (AIM). This comprises a number of relatively independent software components, such as: Dictionary and Directory Management Subsystem, (DDMS), Data Base Management Subsystem (DBMS) and Application Control Program (ACP). Most importantly in this context is that a relational database facility with query language is available under AIM.

In the "user friendly area," that is, helping the user by reducing console operations and systems controls, Atlas OS is not wanting either. The aids in this field come under the title of Advanced Operation Facility (AOF), under which there are a number of separate subsystems, such as the Operation Procedure Facility, which allows users to generate their own operating procedures. For example, the Save-halt command stops a job in such a way that execution can be resumed later without any difficulty. Multiple jobs are also synchronized under AOF. These and other aids indicate that this important area of Operating System usage has been given considerable thought.

A vital and increasingly important part of software is that which is offered for communications. Under Atlas OS, there is the IBM compatible Virtual Telecommunications Access Method (VTAM) and Basic Telecommunications Access Method (BTAM) as the major facility for communication between host and terminals. To back these up in the network area, Flexible Network Architecture (FNA) is offered. This can be used with X.25 and SNA systems.

Fuller informaton on these facilities and the software in general is given under the "Software" heading in the Characteristics section of this report.

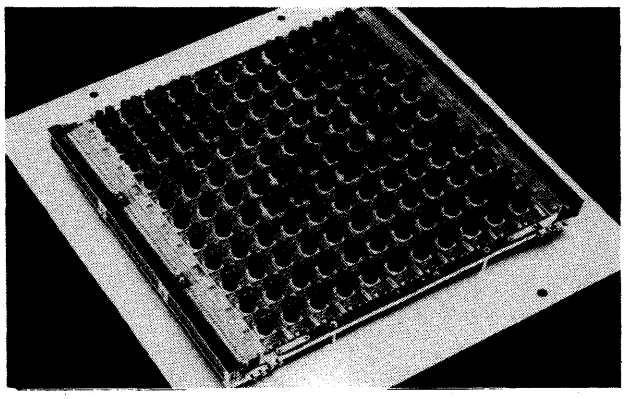
nected to an MCU, two Memory Control Units and four MSUs, each of 32M bytes.

The technology consists of high-speed logic LSI (Large Scale Integration), high density mounting and air cooling. The LSI used is based on a delay time of 350 picoseconds (10-12 seconds) per gate with 400 or 1300 gates per chips used, dependent on the function. Up to 400 circuit gates are mounted on a 4.5mm square chips with a maximum power consumption of 3.0 watts. For main memory 64K-bit chips are used. For other storage, such as the cache memories, 4K-bit RAMs (5.5 ns access time) or 16K-bit RAMs (16 ns access time) are used.

The central processor consists of three individual units called Instruction (I), Execution (E) and Storage (S). The I-unit controls fetching and decoding instructions processing interrupt requests together with its unit's pipeline functions. There are four 8-byte instruction buffer registers in the I-unit, from which instructions can be selected and taken to the local pipeline. One of these registers is used for branch control, through which pipelining itself is very much accelerated when compared to the conventional approach, even if this also involves pipelining techniques. The pipeline itself is a multiphase unit and is one of two pipelines used in the central processor complex, the other being used in the E-unit is controlled by a microprogram kept in control storage.

The E-unit executes instructions from the I-unit. It contains its own pipeline and has 13 arithmetic functional elements and several work registers for intermediate results. The start of the pipeline in the E-unit is called LUCK—Logical Unit and Checker. It carries out preprocessing and is fed directly by the I-unit before passing its data on to the rest of the E-unit. LUCK's function is to effect logical operations (AND, OR, exclusive OR), to predict condition codes, to compare operands and exponents and to keep operand information for both the I- and S-units. The output of LUCK is stored in an intermediate register and sent to the functional block. Apart from LUCK, the remaining elements in the E-unit comprise adder, shifters, a 64-bit high speed multiplier, a 64-bit decimal adder and a high speed divider among other elements, which also include an ALIGN function, whose purpose is to align two 64-bit fractions. Control of arithmetic instructions is effected by microinstructions in the Control Storage.

The S-unit reads instructions and reads/writes operands at the request of the I-unit. Instructions are read in 8-byte units. Operands are read/written in varying length units up to 8-bytes maximum. Dynamic Address Translation (DAT) is also included in the S-unit. The major functional blocks of the S-unit are the:



Pictured is a Multilayer printed circuit board used in the Atlas 10 computer which can accomodate up to 121 LSI logic and RAM chips.

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COMPETITIVE POSITION

The Atlas 10 model 15 is a uniprocessor rated at 10 or 15 mips, dependent on the processor selected. In its 15 mips form, it compares favorably with the performance of the dyadic IBM 3081K, the uniprocessor Amdahl 580, NAS 9070 DPC and has a similar performance to the Siemens 7890–F. Price advantages of 15-20 percent are claimed by ICL over corresponding IBM models.

In performance terms, the dual processor Atlas 10 model 25 is comparable to IBM's 3084 and the Siemens 7890–S and somewhat more powerful than the Amdahl and NAS offerings. In price terms the Atlas is again considerably below IBM's US prices for a comparable configuration of the IBM 3084, but Atlas is not greatly below Amdahl's US quotes.

ADVANTAGES AND RESTRICTIONS

The main advantage ICL has in strategic terms, is that it seems to have a closer entente with Fujitsu than anyone else, apart perhaps from Amdahl, in which Fujitsu has around 35% of the equity. Fujitsu also seems to be pulling ahead of IBM in the super-computer class with its systems using 64K–bit chips and VLSI, producing more compact (and more reliable?) machines. In hardware terms, as a result there appear to be very definite advantages for ICL, especially when price comparisons with IBM are made.

But this is far from being the whole story. Anyone offering compatible products is, in extreme circumstances, at the mercy of the base matrix supplier—and this really means software. Siemens, for example, is actively marketing its BS 3000 operating system, although a large proportion of their customers employ MVS and VM operating systems.

The potential users of the Atlas systems in Europe are provided for, at least at this level, so that software compatibility in the short term is not going to be a problem. However, with the drift towards MVS/XA, more question marks appear. NAS has committed themselves towards supplying a compatible system within a year of IBM's announcement and Amdahl has made a similar statement. ICL has adopted a more conservative view and has said 18 months from first customer shipment.□

- **TLB (Translation Lookaside Buffer)**
- **LBS (local Buffer Storage)**
- **STO stack**
- **BI stack**
- **Store buffer**

The TLB converts virtual to real addresses at high speed. It can be thought of as a two element array with each element comprising 256 bits, which represent validity bits, real address, logical address, storage protection key and space identifier ID. The two elements in the array are accessed simultaneously.

The LBS is dealt with under the STORAGE section of this report.

The STO stack retains 128 segment table origin addresses for virtual storage purposes. The 128 spaces associated with thes origins may be used simultaneously. A 7–bit space identifier ID is assigned to each segment table's leading address and registered in the TLB.

The BI (Buffer Invalidation) stack is used to contain up to 16 so-called buffer invalidation addresses which are checked by the S-unit to see if any of them correspond to addresses used in the LBS. If any such addresses are found in the LBS, these are invalidated. The reason for this is that a store operation is performed for both the LBS and the MCU (Memory Control Unit) when a store request is received from the I-unit. No problem arises when only one CPU is used, but when two CPUs are used, difficulties occur. A store operation is carried out for the MCU only when a store request is received from the channels AND the second CPU. In this case the data in the LBS of the second CPU and that in the MCU will not correspond, unless steps are taken to make them correspond. This is done by making the MCU send the address of the store request from the channels and the first CPU to the other CPU. This address is termed the BI or buffer invalidation address.

The Store buffer is a mechanism for buffering store requests to the MCU. Four 8–byte buffers are available for this purpose.

Apart from the central processor, there are channel processors and at least one service processor. Both the Atlas 10 model 15 and the model 25 can have from one to four channel processors (CHPs).

CHANNEL PROCESSORS

A single CHP can handle up to 16 channels, of which up to four can be Byte Multiplexer Channels (MXCs) and any number can be Block Multiplexer Channels (BMCs). The maximum data transfer rate on each BMC is up to 110 kilobytes per second and on each MXC (each capable of data streaming) the rate is 3 megabytes per second nominally. Device addressing is so organized to provide either 1024 or 2048 channels to each CHP.

An important facet of the way the systems is set up is that Dynamic Address Translation (DAT) can also be carried out with respect to storage references by channels. Real memory addresses are calculated through a virtual Channel Command Word address (CCW) which is part of a special command which locks a channel into virtual mode operation. Translation Lookaside Buffers (TLBs) are then used to find the real address in the same way as they are used in the CPU. The advantage of this is that there is significant saving in Operating System overhead, since the Operating System does not then have to check page boundaries for chains and data areas. In addition, free space arising from main store usage fragmentation can be used for more CCWs.

Another I/O command can be used to lock the channel program into Real Address mode. In this or the virtual mode, the IBM Indirect Data Address method can be applied.

On the Atlas 10 model 25 only, another useful feature is the Channel Cross Call facility. This enables any channel in the system to be accessed by either of the two CPUs.

SERVICE PROCESSORS: one Service Processor (SVP) is used in an Atlas 10 model 15 configuration and two in an

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Atlas 10 model 25 system. An SVP comprises a CPU, memory, floppy disk units, display and keyboard. It is used to monitor and change CPU states, effect initial program loading, reset the system as required and control CPU start/stop.

The SVP also carries preventive diagnosis and automatic error logging. It operates independently of the Atlas 10 CPU. Its performance monitor on the console display indicates CPU and channel busy conditions. It also monitors conditions such as power supply status and air inlet temperature with visible and aural alarms for malfunction.

CONTROL ELEMENTS AND LINKAGES: the main element of control, apart from the control storage itself, is the Memory Control unit (MCU). One of these is provided on an Atlas 10 model 15 and two on the model 25. The purpose of the MCU is controlling main storage access from up to two CPUs and up to four CHPs. The MCU contains the Global Buffer Storage (GBS), a Key Buffer, Extended ECC and a facility for checking main memory and providing fall back and other facilities.

The GBS has already been discussed in this report under the CYCLE TIME heading. It is a high speed form of cache memory, which significantly reduces access time to the main storage.

The Key Buffer contains enough keys to handle any memory up to the maximum 128M bytes of the Atlas 10 model 25. The assemblage of keys, one for every 2K page in memory, is on a unit called the System Console Interface. Each key consists of an access control bit section, a reference bit section and a change bit section. The object of the Key Buffer is to store the reference and change bits of the page which has recently been referenced so that security checks will be speeded up—that is, instead of having to refer to the keys themselves to find out if a page can be read or written, it is normally sufficient to refer to the Key Buffer.

The Extended ECC (Error Check and Control) is used for ensuring, as far as is possible, that no errors occur in GBS. The unit of data in the GBS is 8 bytes (64-bits). 16 check bits are added to these 64 bits, giving a total of 80 bits, which are divided into 4-bit groups which are called blocks. All single block errors are automatically corrected and all double block mistakes are flagged.

INSTRUCTION REPERTOIRE: the set of instructions on the Atlas 10 series machines comprises 195 instructions. These include the IBM System/370 Universal Instruction Set consisting of 156 instructions.

INTERRUPTS: Two types of interrupts can be generated; normal and error. Normal interrupts include channel end, device end, attention status, and busy status. Error interrupts include those caused by data parity error, address parity error, invalid buffer address, keyboard, parity error, keyboard invalid address, command byte parity, and invalid command.

Additional key features standard on the Atlas 10 include:

- Channel indirect addressing, which permits contiguous areas of virtual storage to be mapped into noncontiguous areas of real storage.
- Data streaming, which permits data transfer rates up to 3 megabytes/second on block multiplexer channels.
- Extended addressing, which permits the addressing of real storage in excess of 16M bytes. User programs and portions of the control program can be located at real addresses up to 6M bytes for MVS and up to 64M bytes for AOS.
- A soon to be released 31-bit addressing capability, which expands both real and virtual storage addressing to 2 billion bytes. Both 24-bit and 31-bit programs can execute concurrently.
- System/370 extended facility, which speeds up certain supervisor functions, improves the efficiency of dynamic address translation, and improves CPU availability by protecting certain low-address central storage locations, all while operating under MVS/SP or Atlas OS.
- Byte-oriented operand feature, which allows byte boundary alignment of the operands of most unprivileged instructions.
- Virtual machine assist (VMA), which improves virtual system performance under VM/370 or AUM, as offered by ICL, by reducing the time in the real supervisor state.
- Preferred Machine Assist, which is designed to improve the performance of an MVS or Atlas OS guest machine running under VM/SP or AUM. The feature provides the guest operating system with complete control of the processor, dedicated channels, and I/O devices.
- 3033 Extension, a microcode assist that improves MVS/SP or Atlas OS performance via controlled, cross-address-space access.

INPUT/OUTPUT CONTROL

Input/output on the Atlas 10 series is handled by from one to a maximum of four Channel Processors (CHPs). Each CHP controls up to 16 channels, all of which may be Block Multiplexer Channels (BMCs) and a maximum of four of which may be Byte Multiplexer Channels (MXCs). The transfer rate of each BMC is 3M bytes per second and that of each MXC is 80K bytes per second. The maximum data transfer rate per CHP is 24M bytes per second.

Operating System overhead is reduced considerably by the channel Dynamic Address Translation (DAT). Real memory addresses are obtained via a virtual address called a Channel Command Word (CCW) address which is issued by a special order which locks a channel to operate in virtual mode. The OS overheads are saved, because OS no longer has to check page boundaries for chains and data areas. In addition, free space arising from store usage fragmentation may be used for more CCWs.

Another command peculiar to the Atlas 10 is that used to lock the channel into Real Address mode. In either this or the virtual mode, the IBM Indirect Data Address method can still be used.

MASS STORAGE

ICL or IBM disk drives or those from other PCMs may be connected to the Atlas 10 models. The ICL models are of very large capacity and comprise the ICL Model 6421/2, a fixed disk using the ICL 1774A controller. The capacity is 2 x 446 megabytes in native mode or 6 in 3175 or 3750 compatible mode. Average access time is approximately 26 milliseconds and the transfer rate is 1198 kilobytes per second.

As far as the IBM mass storage devices are concerned, nearly all those which can be connected to the 303X series can also be linked to the Atlas 10 series.

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Many models of IBM mass storage can be connected to Atlas systems. These include IBM 3370, 3375, and 3380 units.

INPUT/OUTPUT UNITS

I/O units can be divided into terminals, magnetic tape units, printers and other units. ICL offers a wide variety of these products, but among those which are especially suitable for the Atlas 10 series are the following.

ICL Model 6292 Display Controller: this interfaces directly to a channel on the Atlas 10 and can be used in either burst or byte mode. It can control up to a maximum of 12 displays with three adapters (each adapter controls up to 4 displays). For cable lengths, see below.

ICL Model 6262 Visual Display Unit: is available in two forms—6262R (monochrome) or 6262K (tricolour, red/green/white). Both these have 1920 characters (24 lines x 80) and can have either of 2 keyboard layouts, each having 87 character keys and 24 program function keys.

ICL 6286CI Display Printer: desk-top, bidirectional dot-matrix with a speed of 180 chs./sec.

Standard cable length for either displays or display printer is 600 meters. Options are available to permit connections up to 1500 meters.

Magnetic tape units in the ICL range for the Atlas 10 series include the following 9-track units, all requiring the 1748A controller.

ICL Model 613A: recording density 6250/1600, with a transfer rate of 1250/320 kilobytes per second.

ICL Model 613M: recording density 6250/1600 bpi, transfer rate 781/200 KB/sec.

ICL Model 613E: recording density 1600/800 bpi, transfer rate 320/160 KB/sec.

Of the printers which are most suited to the Atlas 10 models, the one which ICL quotes in particular, is the ICL Model 650D, which is a train printer with an interchangeable cartridge. This printer has a speed of 200 lines per minute with 132, 136 or 150 print positions and a character set of 48 or 60 characters. This printer has its controller built in. Another printer which may be attached is the ICL laser printer which operates at well over 20,000 lines per minute and 12 lines per inch.

As a front-end system ICL offers ICL 2806 Communications Control Processors (CCPs) for the Atlas 10 series. Each CCP contains an independent processor, memory, channel adapters and line control units. The Flexible Network Architecture (FNA) software is used for running the CCPs. This supports packet switching protocols, including the X-level, together with having the ability to interface to ICL's Information Processing Architecture (IPA).

Peripheral devices from other manufacturers (PCMs) may also be used on the Atlas 10 series products.

SOFTWARE

Software for the Atlas 10 series, is very wide-ranging including a great amount of IBM software which will run unaltered on these ICL-Fujitsu machines.

Specifically, the user has the option of using either the ICL Atals Operating System (OS) or IBM's MVS/SP. IBM's VM/370 will also function with the aid of the AVM Assist feature of the Atlas 10. Programs from third parties, designed for the IBM range, can also be run on Atlas 10.

ATLAS OPERATING SYSTEM (OS)

The Atlas 10 operating system, OS, is split into several interconnected parts. These are:

- Superivsor
- I/O Control
- System Decision Management (SDM)
- Resource Access Control Facility (RACF)
- Recovery Management System (RMS)
- Advanced Operations Facility (AOF)
- Time Sharing System (TSS)
- Job Entry System (JES)
- Virtual and Basic Telecommunications Access Method (VTAM:BTAM)
- Network Control Program (NCP)

These perform the following functions:

Supervisor: the job of the superivsor is to handle virtual storage assignment for all the active tasks in the system. This virtual storage is up to 16M bytes in length and is supported by Dual Address Space and, in a later release, by 31-bit addressing. The supervisor also manages the Dynamic Address Translation (DAT) feature used for main memory and channels, together with separate segment tables, the translation look-aside buffer, used for translating virtual addresses to real addresses, and the extended real store assignment of maximum 64M bytes capacity.

I/O Control: the most important tasks handled by OS are the chaining of jobs into virtual storage and the parallel access to sequential data sets—thus minimizing time needed. Atlas OS supports varied buffering and access modes, including VSAM (Virtual Storage Access Method) data sets and Virtual Input/Output (VIO) for permanent or temporary datasets. Atlas OS also offers full cataloging facilities and utilities for centralized management of volumes and datasets. For data security and efficient space usage purposes automated migration of data sets is provided. OS also gathers statistics for user accounting.

System Decision Management (SDM): SDM monitors system resources used by transactions and domains and adjusts this usage by automatic changes of service ratios to individual units thus minimizing ENQ (Enqueue) delays. It also prevents resource depletion. SDM covers batch, remote batch, time sharing, real time processing and multi-processor use of resources.

Resource Access Control Facility (RACF): this is a security facility. RACF monitors all attempted access to system resources through multiple level passwords.

Recovery Management System (RMS): probably one of the most important facets of OS, RMS works in conjunction

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with the hardware reliability features (RAS) to ensure high levels of availability of all functional elements through, among other things, quick recovery procedures. The recovery features include: hardware machine check handlers to isolate errors and to collect diagnostic information; alternate facility handlers which automatically retry alternative channel paths or, when possible, alternative CPUs, and error recovery procedures for failed I/O operations. Atlas OS's recovery features include functional recovery routines (FRR) to localize, collect failure data and to recover/terminate processing in a controlled manner for quicker diagnosis and return to normal function.

Advanced Operation Facility (AOF): AOF is designed to make the Atlas 10 as user friendly as possible. Its main function is to reduce to a minimum console operations and control functions in the hands of the operator. Ther is also a user-own-operation-procedure facility (OPF) which allows the user to generate his own operating procedures. Among individual elements in AOF are TASS, DSF, MRF and PDL. TASS (Tool for Automatic Scheduling of System operation) automatically synchronises multiple jobs. DSF (Demand Sysout Facility) enables users to get their own output, again relieving operator load, as does the Message Routing Facility (MRF) by means of which users can respond directly to their own job's queries. Automatic Volume Recognition (AVR) permits operators to premount volumes on any available disk or magnetic tape drive. For logging purposes, there are two main aids, PDL (Performance Data Logger) and PDA (Performance Data Analyser). PDA Multiple Console Support (MCS) smooths the communications between operator and OS.

TSS (Time Sharing System): the facilities which TSS offers include; conversational entry of batch jobs, compatibility with batch mode, improved timesharing through dynamic swap and interval control, a full range of security functions, debugging aids, such as syntax checkers for Cobol, Fortran and PL/1 and dump trace and display routines. There is a full set of commands within TSS.

Job Entry System (JES): includes spooling and scheduling of I/O streams under a wide variety of conditions, such as loosely coupled and networked systems. JES/E, Job Entry Extension provides dependent job control functions for loosely coupled systems with flexible commands for switching global and local (software) processors. JES/MAS, Job Entry System/Multi-Access Spool allows multiple system sharing of job queues with spooling on shared disks for load balancing and effective resource utilization. The Job Entry Subsystem/Network Job Entry (JES/NJE) offers processing sharing among multiple host computers.

Basic and Virtual Telecommunications Access Methods (BTAM and VTAM): compatible with the IBM facilities of the same name and are used for communications between host computer and terminals. VTAM supports the distributed communications processing environment which is shared between host and communications control processor (CCP) operating under the Network Control Program (NCP).

Network Control Program: NCP manages line and terminal control functions. Protocols for asynchronous, binary synchronous and SDLC are also offered through the NCP. The packet switching protocol, X.25 and SNA are available through Flexible Network Architecture (FNA) and can be interfaced to ICL's Information Processing Architecture (IPA). In the VTAM–G environment, the MultiSystem Networking Facility (MSNF) enables a terminal to access multiple host computers. Using the DataStream Compatibility (DSC) function sub-host computers and cluster controllers can utilize data from or the facilities of the host computer's operating system.

LANGUAGES: there is a wide range of language compilers for the Atlas 10 systems: these include Assembler, APL, Basic, Cobol, Fortran, Lisp, P1/1, RPG and Algol. Some other compilers, such as HyperCobol are designed to improve programmer productivity by means of special facilities, which provide syntax schecking, prompting and interactive debugging. Several compilers, ANS Cobol, Fortran IV, Fortran 77 and PL/1, provide optimizing options which improve resource utilization and execution speed together with an option for generating reentrant object programs.

PRICES

In common with most European manufacturers, ICL release typical configuration prices only.

Atlas 10 Model 15 (10 mips)—central processor, service processor (SVP) including controller, color CRT, keyboard and serial printer, 16M bytes of main memory, 16 channels: £1.7 million

Atlas 1 model 15 (15 mips)—central processor, SVP including controller, colour CRT, keyboard and serial printer, 16M bytes of main memory, 16 channels: £2.2 million

Atlas 10 model 15 (15 mips)—central processor, SVP including controller, color CRT, keyboard, serial printer, 2x1774A disk controllers (4 x storage directors), 4 x 2 channel switches, 4x6421 A2 disks, 4x6421 C2 disks, 24x6421 B2 disks (the A2, C2 and B2 designators refer to connecting methods: the capacity of each 6421 disk is 446.5M bytes in native mode and 317.5M bytes in 3350 mode; thus, total capacity is either 14 gigabytes or 10 gigabytes dependent on use), crosscall adapters, 1x650D 2000 lpm printers: £2.99 million.■