IBM 3081

MANAGEMENT SUMMARY

The long-awaited initial model of IBM's H-Series was announced on November 12, 1980, as the 3081 Processor Complex. The new system, featuring a tightly-coupled dual-processor design, is claimed by IBM to have about twice the performance of its 3033 Model U system. This puts the new 3081 in the 10 to 12 MIPS (million instructions per second) range. The 3081 is compatible with both the IBM System/370 and 303X systems, and offers improved price/performance over both.

IBM's announcement of the 3081 was tied in with sweeping price cuts on its 303X and 304X family of large processors, as well as the announcement of a new entry-level 3033, the Model Group S. While there had been much speculation on the ultimate design of the 3081, its appearance has left no doubts about IBM's intention to compete vigorously in the high-peformance arena.

PROCESSORS AND PERIPHERALS

The 3081 is what IBM calls a "dyadic" processor complex, consisting of two integrated CPUs operating under a single operating system. Each processor has access to 16, 24, or 32 megabytes of shared storage and its own set of channels. IBM states that although the 3081's dyadic structure is similar to the MP and AP complexes found in its 303X series, the new architecture is unique in that channel affinity and channel sets may be assigned to either CPU. Each processor has a 32K-byte high-speed buffer as well as a 26-nanosecond cycle time. The two-way integrated structure of the 3081 processors is said to offer greater system availability, since processing can continue in a reduced state even with one of the processors down. Channels can be automatically switched under program control to the functioning processor until the problem can

IBM has taken a decisive step forward in the high-performance computer arena with the first of its much-heralded H-Series processors, the 3081 Processor Complex. The new system is a dual-processor configuration that IBM says has about twice the performance of a single-processor 3033. The 3081 is supported by both the MVS/SP and VM/SP operating systems. The first systems are scheduled for delivery in the fourth quarter of 1981.

CHARACTERISTICS

MANUFACTURER: International Business Machines Corporation, Data Processing Division, 1133 Westchester Avenue, White Plains, New York 10604. Telephone (914) 696-0100.

MODELS: 3081 Processor Complex.

DATE ANNOUNCED: November 12, 1980.

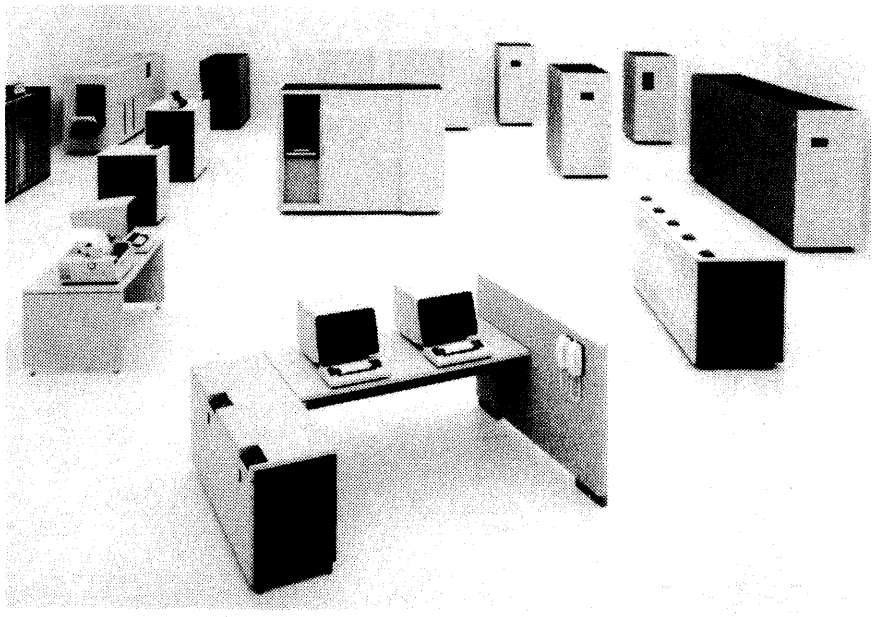
DATE OF FIRST DELIVERY: Fourth quarter 1981.

DATA FORMATS

BASIC UNIT: 8-bit byte. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short"



IBM's 3081 Processor Complex is a high-performance system in the range of 10 to 12 MIPS (million instructions per second). It features a dyadic processor design, up to 32 megabytes of memory, and up to 24 integrated channels.

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be corrected. The 3081 cannot, however, be split into two uniprocessors executing simultaneously.

A highlight of the 3081 is the packaging of its logic components. The 3081 uses the Schottky TTL logic chip, similar to that used in IBM's 4300 Series. While the chip technology is not new, the packaging is significant. Up to 118 chips are sealed in a helium-filled unit called the Thermal Conduction Module (TCM). The TCM is a field-replaceable unit (FRU) for ease of maintenance, and is designed to tie into the 3081's water-cooled environment. Each CPU is made up of eight TCMs, all mounted on a ceramic multi-layered board that contains all necessary connections.

IBM claims the new TCM affords increased computing power while reducing space requirements by about 21 percent, cooling by 70 percent, and power consumption by about 66 percent when compared to the company's 3033U processor with eight megabytes of memory.

Central storage in the 3081 is based on 16K-bit RAM modules, and comes in three sizes: 16, 24, and 32 megabytes. It is described as "two-level" storage, consisting of main memory modules plus a high-speed 32K-byte buffer (cache) unit for each processor. Main memory has error checking and correction (ECC) code bits. All single-bit errors are corrected, and most double- and multiple-bit errors are detected. Main memory is shared between the two CPUs. The memory access time is 312 nanoseconds using an eight-byte data path between processor and memory. Memory is added in eight-megabyte increments and costs $25,000 per megabyte.

The new system includes as standard the 3033 Extension feature, which improves processor execution times for functions such as I/O processing, paging, and real storage management. Extended Addressing, also standard, permits real storage capacity up to 32 megabytes.

The 3081 Processor Complex is built around the 3081 Processor Unit; a unique service and support component called the 3082 Processor Controller; the 3087 Coolant Distribution Unit (CDU), which regulates the flow of chilled water within the CPUs; a 3089 Power Unit (or any other suitable 415-Hz source); and a minimum of three display consoles. An IBM 3278 Model 2A is required as the system console. A 327X or any appropriate IBM display can be designated the operator console, and, optionally, a service support console. In addition, a 3081 complex should include a card reader, printer, tape drives, and disk drives.

The 3082 Processor Controller, which extends the service processor concept of other IBM systems, provides the following functions: 1) monitors and controls the 3081 complex, 2) houses the interface logic for each channel, 3) controls system reconfigurations, 4) performs automatic central storage validation testing and address assignment, and 5) provides system diagnostics and maintenance.

format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; or 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4 or 6 bytes in length, specifying 0, 1, or 2 memory addresses, respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: MOS (metal oxide semiconductor); 16K-bit RAM chips.

CAPACITY: 16, 24, or 32 megabytes.

CYCLE TIME: 312 nanoseconds.

CHECKING: All data paths between the central processor and main storage are parity-checked by byte. When the data is retrieved, single-bit errors are detected and corrected automatically, and most multiple-bit errors are detected and signalled so that appropriate program action can be taken.

STORAGE PROTECTION: The Store and Fetch Protection features, which guard against inadvertent overwriting and/or unauthorized reading of data in specified 2048-byte blocks of storage, are standard in all models. The storage protection array is maintained by the system controller.

RESERVED STORAGE: Similar to the System/370, main memory is reserved for interrupt routines, program status words, CPU timer logout area, machine-check interrupt code, and register save area.

CENTRAL PROCESSORS

The 3081 Processor Complex uses two central processors in a dyadic, or tightly coupled, arrangement. The basic processor unit includes the two integrated CPUs, shared central storage (up to 32 megabytes), an external data controller (EXDC) for channel control, and a system controller.

Each of the 3081 central processors is microcode-controlled and includes an instruction element (IE), variable field element (VFE), execution element (EE), control storage element (CSE), and buffer control element (BCE). The central processor cycle time is 26 nanoseconds.

Instruction sequencing, address generation for storage requests, and initiation of storage requests are handled by the instruction element (IE). The IE contains its own buffers, registers, and hardware to process instructions other than those executed in the VFE.

All storage-to-storage (SS and SSE) instructions are executed in the variable field element (VFE). The VFE has a decimal adder, two input (source) registers, and two output (sink) registers. While the IE is using data contained in one VFE input register, it can also be filling the other input register. Likewise, the IE moves data from the VFE output registers to the storage data register in the IE.

The execution element (EE) performs the following arithmetic operations: fixed point multiply/divide, convert to binary, convert to decimal, floating point, and extended precision floating point.

The control storage element (CSE), a logical component in the central processor that contains control storages and registers, controls microcode execution in the central processor. Microcode is paged in from the system area in main memory by the pageable part of control storage.

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COMPARISON TO THE 303X SERIES

	3033U	3033MP	3081
SYSTEM CHARACTERISTICS			
Date of introduction	March 1977	April 1978	November 1980
Date of first delivery	March 1978	3rd qtr. 1979	4th qtr. 1981
Number of central processors	1	2	2
Principal operating systems	OS/VS1, SVS, VM/370,	OS/VS1, SVS, VM/370,	MVS/SP, VM/SP
Monthly rental, basic system (4-year lease)	$80,320	$162,631	$93,000
Production status	New production	New production	New production
MAIN STORAGE			
Storage type	MOS	MOS	MOS
Read cycle time, nanoseconds	348	348	312
Write cycle time, nanoseconds	696	696	312
Bytes fetched per cycle	8	8	8
Storage interleaving	8-way	8-way	2-way
Minimum capacity, bytes	4,194,304	8,388,608	16,777,216
Maximum capacity, bytes	25,165,824	33,554,432	33,554,432
Increment size, bytes	4,194,304	4,194,304	8,388,608
Error correcting memory	Yes	Yes	Yes
BUFFER STORAGE			
Cycle time, nanoseconds	57	57	26
Bytes fetches per cycle	4, 8	4, 8	128
Capacity, bytes	65,536	131,072	32,768 (each buffer)
Time to fetch 8 bytes, nanoseconds	115	115	52
RELOADABLE CONTROL STORAGE			
Capacity	3072 108-bit words plus 1,024 126-bit words	6,144 108-bit words plus 1,024 126-bit words	NA
PROCESSING UNIT			
Machine cycle time, nanoseconds	57	57	26
Relative performance level to 3033	1.0	1.6 to 1.8	1.9 to 2.1
Processing unit features:			
Clock Comparator and CPU Timer	Standard	Standard	Standard
Dynamic Address Translation	Standard	Standard	Standard
Floating-Point	Standard	Standard	Standard
Extended-Precision Floating-Point	Standard	Standard	Standard
Direct Control	Standard	Standard	No
Virtual Machine Assist	No	No	Standard
OS/VS1 Extended Control Program Support	No	No	No
Instruction Retry Hardware	Standard	Standard	Standard
System/370 Extended Facility	Standard	Standard	Standard
3033 Extension	Optional	Optional	Standard
Extended Addressing	Optional	Optional	Standard
Multiprocessor systems			
Tightly coupled	Yes	Yes	Yes
Loosely coupled	Yes	Yes	Yes
Attached Processor System	3042	None	None
Integrated Storage Control	None	None	None
I/O CONTROL			
Integrated channels, standard	2 groups of 6	4 groups of 6	2 groups of 8
Integrated channels, optional	1 group of 4	2 groups of 4	1 group of 8
Selector channels	None	None	None
Data rates, bytes per second:			
Byte multiplexer	40,000 to 75,000	40,000 to 75,000	40,000 to 75,000
Block multiplexer	1.5 or 3.0 million	1.5 or 3.0 million	1.5 or 3.0 million
Maximum I/O data rate, bytes/sec.	26 million	52 million	72 million

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Input/output operations are controlled via the external data controller (EXDC), an integrated I/O processor that contains the system's channels. Sixteen integrated channels are standard in the 3081. Eight additional channels are optional. The channels can be grouped into two sets, one for each processor. Up to 16 channels can be assigned to a set. Should one processor fail, the channel set switching feature permits the other processor to assume all channel activity. Up to four channels can be byte multiplexer channels. Block multiplexer channels have the Data Streaming feature as standard, and can have both data streaming and non-data streaming devices intermixed on the same channel. Each block multiplexer channel, when operating in the data streaming mode, provides a maximum data transfer rate of 3 megabytes per second. Aggregate data rates across 24 channels of 72 megabytes per second are possible, according to IBM. Each channel can address up to 256 I/O devices or subchannels. Up to two Channel-to-Channel Adapters (feature #1850 for the first, 1851 for the second) are available to connect two processors (System/360, System/370, or 4300), via their channels, into "loosely-coupled" configurations.

This high-performance I/O capability permits a wide range of configurability in the 3081, particularly in the area of high-speed direct access storage devices. For example, IBM's new 3380 DASD operates at the maximum 3-megabytes per second transfer rate, making it an ideal choice for the 3081 user, particularly since all the 3081's block multiplexer channels support the data streaming feature. I/O devices available to the 3081 user are summarized in the Characteristics section of this report and detailed in Report 70C-491-06.

System reliability, availability, and serviceability (RAS) is assured through specific system features: 1) use of LSI circuitry packaged on thermal conduction modules (TCMs), 2) a checkpoint retry facility to detect processor errors, 3) automatic error data analysis with processor in continuous operation, and 4) several testing and monitoring facilities within the complex to keep a close eye on major system functions.

Data integrity and security in the 3081 are maintained via key-controlled and low address storage protection, storage error checking, parity checking, Pageable Link Pack Area (PLPA) checking, and channel command and processor checkpoint retry facilities.

Additional standard features on the 3081 include dynamic address translation (DAT), System/370 extended facility, the System/370 universal instruction set, virtual machine assist (VMA), and the byte-oriented operand feature.

SOFTWARE AND SUPPORT

The 3081 is supported by the MVS/SP (Multiple Virtual Storage/System Product) and VM/SP (Virtual Machine/System Product) operating systems. MVS support for the 3081 will be via MVS/SP Release 1, to be available with enhancements as of March 1981. Two additional upgrades of MVS/SP, Releases 2 and 3, will also support the 3081, and will be available in June 1981 and October 1981,

Immediate execution of in-place microinstructions is handled by a lookaside directory within control storage. Newly paged microinstructions overlay the least recently used (LRU) microcode.

Data movements between the central processors and memory are handled by the buffer control element (BCE). The BCE performs virtual-to-real address translation, controls the 32K-byte buffer (cache), and includes a 32K-byte cache, directory, directory lookaside table (DLAT), dynamic address translation (DAT) hardware, and a store-back array.

Each central processor has a 32K-byte cache storage unit for high-speed access to instructions and data. The cache has a two-cycle access time for eight bytes of data. Address translation is performed in parallel. Lines of data in the cache are replaced using a least recently used (LRU) algorithm. The absolute addresses for lines of data contained in the cache are located in the directory.

Virtual-to-real address translation is performed by dynamic address translation (DAT) hardware. Once a virtual address is translated, the real address of the referenced page is stored in the directory lookaside table (DLAT), which contains up to 128 virtual/real address pairs. Virtual addressing is limited to 16 megabytes. Using the standard extended addressing feature, addressing in excess of 16 megabytes of real storage can be achieved.

The 3081 uses improved packaging techniques for its logic circuitry. Based on Schottky TTL in the form of gate arrays, the circuitry is contained in an enclosure called the thermal conduction module (TCM). The TCM is a helium-filled, encapsulated unit that has up to 118 silicon logic chips mounted on a multilayered ceramic substrate. Each central processor is made up of eight TCMs mounted on a multilayered board, which contains all chip and module interconnections. No external wiring or cabling is needed as a result of this design. The module is covered by a cold plate through which chilled water is circulated for heat dissipation. The TCM, according to IBM, provides increased computing power while reducing space requirements by 21 percent, cooling facilities by about 70 percent, and power requirements by about 66 percent when compared to the IBM 3033 Model U8. The TCM is a field-replaceable unit (FRU).

Memory in the 3081 is implemented in monolithic and LSI technologies. A two-level design is used in each processor: central, or main, storage and the 32K-byte buffer (cache). Main Storage is available in 16-, 24-, or 32-megabyte capacities, and is shared by both processors. The system area, typically an area of memory of at least 262K bytes, is designated at initial microcode load (IML) for system usage and is not available for user programs. Main memory is configured in two or more direct-access basic storage elements (BSEs) which have the logic for fetching or storing doublewords from or into the data arrays. Memory has two-way interleaving of contiguous 2K-byte blocks of storage. Error checking and correction (ECC) bits are stored with data in the data arrays.

The system controller is the switching point in the 3081, and interrconnects the logical units of the complex: the two central processors, central storage, and the external data controller (EXDC). It performs the following activities:

- **Controls data transfers.**
- **Resolves conflicts between the two CPUs.**
- **Switches data flow between various processor components; CPUs, memory, and EXDC.**

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respectively. VM/SP Release 1, for VM/370 support, will be available in the first quarter of 1981. The 3081 is not supported natively by either DOS/VSE with or without Advanced Functions or VS1 Basic Programming Extensions (BPE). IBM indicated it will provide local programming support to the following situations: 1) DOS/VSE Systems Control Programs executing in conjunction with Release 3 of VSE Advanced Functions program, and 2) VS1 BPE programs, both of which are running under VM/SP on a 3081. IBM said that any program written for the System/370 or 303X can be run on a 3081 using MVS/SP or VM/SP provided the program 1) is not time-dependent, 2) is not dependent on the mix of system facilities and peripherals in the 3081, and 3) does not depend on results or functions as defined in the System/370 Principles of Operation. Details on these operating systems, as well as communications software and database management and applications programs, can be found in Report 70C-491-06.

COMPETITIVE POSITION

The chief competitors to IBM's 3081 currently are the plug-compatible Amdahl 580 Series and National Advanced Systems' AS/9000 family. The Amdahl 580 consists of two models, the uniprocessor 5860 and dual-processor 5880. The AS/9000 comes in three versions: the entry level AS/9000N, the standard AS/9000, and the dual-processor AS/9000 DPC. The 5860 is rated at about 13 MIPS (million instructions per second) and the AS/9000 is rated at about 10 MIPS, both in a uniprocessor configuration. The dual-processor Amdahl 5880 and NAS AS/9000 DPC are substantially more powerful than the 3081. On the horizon are two other U.S.-based companies. Storage Technology Corporation (STC) and Acsys, Inc. (recently founded by Dr. Gene Amdahl), which have announced their intentions to develop and market systems in the H-Series range. The established mainframe community has acknowledged the 3081's introduction calmly, and no doubt has its own responses well under way.

The 3081 Processor Complex with 16 megabytes of storage (model D16) costs $3,720,000 in its basic configuration, and can be leased over four years for $93,000 per month. Maintenance costs $7,050 per month. The 3082 Processor Controller with 16-channel support costs $220,000, leases over four years for $5,500 per month, and has a monthly maintenance charge of $1,080. The first customer shipments will be in the fourth quarter of 1981, and will be 16-megabyte systems. Larger systems with 24 and 32 megabytes will be available in the first quarter of 1982.

Over the past few years, IBM has permitted bits and pieces of its H-Series to reach the public. Now that the door has opened somewhat wider with the 3081, and reflecting on past IBM announcements, some pointed questions must be asked. The most important of these is, "Is the 3081 the *real* H-Series?" Is it the first of a series? (Most likely.) Will it prove to be an evolutionary dead end as did the System 370/155 and 165? (Hopefully not.) And is it a bridge to the real "H?" (Good Question.) Judging from IBM's large-systems activities over the past

- Maintains the storage protection array and the time-of-day clock.
- Blocks access to central storage from a requesting processor until the processor in use has successfully completed a data transfer.
- Assigns priorities to and keeps track of storage module accesses.

Error handling in the 3081 is provided on several levels for maximum efficiency. All recovery procedures are handled through the 3082 Processor Controller. Error correction and recovery are tried as the first step. Processor checkpoint retry in the CPUs, channel error detection and recovery for the channels, and error checking and correction in central storage represent the specific methods used in the individual system elements. If an error cannot be pinpointed through normal routines, the 3082 initiates a probability calculation as to the most likely place an error could occur.

Processor checkpoint retry uses a series of error detection latches and backup facilities which are periodically tested by each processor for errors. If there are no errors, a checkpoint is taken by the CPU. A checkpoint is a reference marker, stored within the backup facilities, that retains information about the state of the CPU at the time the checkpoint was taken. If an error is detected by a CPU, instruction execution stops, the CPU generates an error logout, and returns to the last checkpoint. The processor can be restored to its operational state as of the checkpoint, and processing can be restarted from this point.

Retry is performed up to seven times by the CPU. If the error has not been corrected by the seventh retry, the processor either enters the check-stop state or takes a machine-check interruption. An interruption is also generated in the check-stop state. If the error is corrected by the seventh try, normal processing resumes. According to IBM, processor checkpoint retry is an improved recovery method over older systems because it involves a retry of a series of instructions, rather than of a single instruction.

Detecting channel errors can involve either the 3082 Controller or an I/O control unit, depending on the error. If the 3082 is involved, error recovery can be performed via the control program, or the 3082 can temporarily stop channel operation to investigate channel status information before reinitializing the I/O devices in use. If the error is detected by a control unit, the 3082 may not have to be used, since the control unit can issue a command retry to the channel without an I/O interruption occurring.

Within central storage, all single-bit errors are detected and corrected. Error checking and correction (ECC) also detects all double-bit and most multiple-bit errors but does not correct them.

The IBM 3081 has a high level of reliability, availability, and serviceability (RAS) assured through several important system features:

- A central processor, made up of eight TCMs and associated board, that needs no external wiring or TCM-to-TCM cabling.
- An integrated two-way processor design that permits a failed CPU to be removed from the configuration, while processing can continue on the other CPU. This allows continued processing and deferred servicing.
- The ability to switch channels associated with a failed CPU to the functioning CPU.
- The 3082 Processor Controller, which provides a wide range of maintenance and diagnostic routines for on-site

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year, we will probably have answers to these questions within the coming twelve months.□

servicing, and has a data communication link for contacting IBM field support personnel.

- Remote diagnostics conducted by IBM support personnel using the field engineering RETAIN program.

3082 PROCESSOR CONTROLLER: This is a unique, free-standing processor that concurrently supervises and monitors all ongoing activities in the 3081 complex. Two models are available, depending on the number of channels present: Model 16, for 16 channels, and Model 24, for 24-channel systems. The 3082 acts as the controller for the system console (typically on IBM 3278 Model 2A), the service support console, and an optional programming support console. The system console interacts directly with the 3081, displays system status, and performs all standard console functions. The service support console interacts with the diagnostic routines built into the 3081 and can also function as a backup console. The programming support console is a 3278 Model 2 equipped with a switch to change from a programming support device to a diagnostic console.

The 3082 Processor Controller also functions as the system monitor and supervisor, providing the following services:

- Controls system power-on sequencing and initial microcode load (IML).
- Monitors voltage levels and coolant flow in the processors.
- Controls dynamic reconfiguration of processor elements such as CPUs, central storage arrays, channel groups, and interface adapter elements.
- Performs a system sampling operation that can extract specific system performance data.
- Initiates processor unit error recovery measures such as checkpoint retry and error analysis and isolation.
- Provides a data communications link to IBM field support.
- Contains an integrated processor control file with system information libraries for microcode, I/O configuration, channel parameters, and diagnostics.

The 3081 Processor Complex also includes a 3087 Coolant Distribution Unit (CDU) and a 3089 Power Unit (or other appropriate 415-Hz power supply). The 3087 CDU controls the temperature and flow of chilled water through the thermal conduction modules (TCMs). The CDU has two pumps, one of which is on stand-by for activation if the operating pump fails.

OPERATIONAL MODE: The 3081 operates in the Extended Control (EC) mode. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, the virtual-storage-oriented operating systems must be used.

INSTRUCTION REPERTOIRE: The 3081 uses the System/370 Universal Instruction Set, which includes 156 instructions that provide binary, decimal, and floating-point arithmetic operations. The System/370 instruction set includes complete arithmetic facilities for processing variable-length decimal and fixed-point binary operands, as well as instructions which handle loading, storing, comparing, branching, shifting, editing, radix conversion, code translation, logical operations, packing, and unpacking. In addition, a group of "privileged instructions," usable only by the operating system, handle input/output and various hardware control functions.

INTERRUPTS: Two types of interrupts can be generated; normal and error. Normal interrupts include channel end, device end, attention status, and busy status. Error interrupts include those caused by data parity error, address parity error, invalid buffer address, keyboard, parity error, keyboard invalid address, command byte parity, and invalid command.

Additional key features standard on the 3081 Processor Complex include:

- Channel indirect addressing, which permits contiguous areas of virtual storage to be mapped into noncontiguous areas of real storage.
- Channel set switching, which dynamically switches channel sets between processors under program control.
- Data streaming, which permits data transfer rates up to 3 megabytes/second on block multiplexer channels.
- Extended addressing, which permits the addressing of real storage in excess of 16 megabytes. With MVS/SP, user programs and portions of the control program can be located at real addresses up to 32 megabytes.
- System/370 extended facility, which speeds up certain supervisor functions, improves the efficiency of dynamic address translation, and improves CPU availability by protecting certain low-address central storage locations, all while operating under MVS/SP.
- Byte-oriented operand feature, which allows byte boundary alignment of the operands of most unprivileged instructions.
- Virtual machine assist (VMA), which improves virtual system performance under VM/370 by reducing the time VM/370 spends in the real supervisor state.
- 3033 Extension, a microcode assist that improves MVS/SP performance via controlled, cross-address-space access.

Up to two channel-to-channel adapters are optional on the 3081 to interconnect the 3081 and another system via a channel from each unit. An additional eight-channel group, which increases the number of channels from 16 to 24, is also optional.

INPUT/OUTPUT CONTROL

The 3081 uses an external data controller (EXDC) to handle all I/O operations. A fully integrated I/O processor, the EXDC contains 16 channels as standard, with an option for 8 more. Channels are organized logically into two sets (one for each CPU), with a maximum of 16 channels permitted in one set. Physically, the channels are configured into two (standard) or three groups of 8 channels each.

Channels can be configured as either byte or block multiplexer channels. A maximum of four byte multiplexer channels per system is possible. Block multiplexer channels are generally used when byte multiplexer channels are not needed. Any channel in the system can be given a valid channel address, but the addresses must be contiguous within the channel set. Block multiplexer channels can operate in either the standard DC interlock or 3-megabytes-per-second data streaming mode. Up to eight I/O control units can be attached to either a byte or block multiplexer channel, and each channel can address up to 256 I/O devices (each on its own subchannel).

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The EXDC has a microcode-controlled Channel Processing Element (CPE) that fetches channel command words (CCWs), starts and ends data server element (DSE) operations, analyzes status, posts interruptions, and assists DSEs in command chaining and indirect addressing. The CPE has up to three DSEs (each associated with a channel set) that control data transfers between the I/O devices and central storage. Each DSE operates with eight interface adapter elements (IAEs) that are connected to the channels in the DSE. An IAE performs service-in and service-out tagging, identifies incoming data transfers and signals the proper DSE, and provides data during data transfers.

MASS STORAGE

The 3081 can use nearly all of the mass storage devices available in the 303X Series (Report 70C-491-06), plus the following high-performance models in particular:

IBM 3370 DIRECT-ACCESS STORAGE: Provides up to 285.6 megabytes of storage per actuator and 571.3 megabytes per drive. The 3370 can be connected to a 3880 Storage Control unit. The 3370 was introduced in 1979 with the introduction of the IBM 4300 Series. The 3370 employs thin-film technology heads and high-density LSI circuitry. Each 3370 has a single 571.3 megabyte spindle of disks which are accessed by two independent, movable actuators. The 3370 makes use of fixed block architecture, which provides for recording data in permanent pre-formatted 512-byte blocks on the disk surface. Each block of data is separately addressable and separately accessible, either singly or in contiguous strings of a variable number of blocks (maximum, approximately 65,000). The 3370 has 558,000 blocks per actuator, 285,696,000 bytes per actuator, and 571,392,000 bytes per drive. Minimum, average, and maximum head movement times are 5, 20, and 40 milliseconds, respectively. Average rotational delay is 10.1 milliseconds, and the data transfer rate is 1,859 megabytes per second.

The 3370 is available in two models. The 3370 Model A1 contains the control adapter functions required for attachment to the 3880. The 3370 Model B1 attaches through an A1 unit. Up to three 3370 Model B1s can be attached to a 3370 Model A1 for a maximum of four units per string.

IBM 3375 DIRECT-ACCESS STORAGE: The 3375 is a newer count-key-data formatted disk drive that provides 819 million bytes of storage capacity. It was announced by IBM on June 11, 1980, and is designed primarily for use with IBM 303X, 4300, and 3081 processors. The 3375 is similar in most respects to the 3370 Direct-Access Storage that was introduced with the 4300 Series computers in January 1979. The principal differences between the two devices are in storage capacity and data format. The 3375's 819-megabyte capacity is 43 percent larger than the 3370's 571 megabytes, and the 3375 uses the count-key-data format employed in the 3380, the 3350, and other large-capacity IBM disk drives in contrast to the fixed 512-byte blocks used in the 3370 and 3310.

Each 3375 drive contains one nonremovable head and disk assembly (HDA). The HDA has two actuators, each providing independent access to approximately 409 million bytes of data. Average seek time is 19 milliseconds, average rotational delay is 10.1 milliseconds, and data is transferred at the rate of 1.859 million bytes per second. There are two models of the 3375. Model A1 contains a storage control interface and connects to a 3880 Model 1 or 2 Storage Control. Up to three 3375 Model B1 drives can be attached to a 3375 Model A1 for a maximum string capacity of 3.27 billion bytes.

The 3375 provides significant savings in floor space, power, heat output, and cost per byte when installed in place of existing IBM 3340 or 3350 disk storage. The 3375 subsystem also offers numerous improvements in reliability, availability, and serviceability. No scheduled preventive maintenance is required. Data error bursts of up to 16 bits are detected and corrected automatically if the bursts do not span more than two contiguous bytes. First customer shipments of the 3375 are planned for the third quarter of 1981.

IBM 3380 DIRECT-ACCESS STORAGE: Announced on June 11, 1980, the 3380 offes a significantly larger storage capacity, faster data transfer rate, and lower cost per byte than any previous IBM disk drive. Each 3380 drive unit has a data storage capacity of 2.52 billion bytes, an average seek time of 16 milliseconds, an average rotational delay of 8.3 milliseconds, and a data transfer rate of 3.0 megabytes per second. Each 3380 unit contains two 1.26-billion-byte head and disk assemblies (HDAs), which are permanently mounted and house the heads, disks, and access mechanisms in a sealed enclosure. Each HDA, in turn, has two actuators, and each actuator accesses 630 megabytes of data. A 3380 string can consist of up to 4 drive units and 16 actuators, with each actuator operating independently and overlapping its seeking and rotational position sensing operations with those of other actuators. There are six models of 3380 Direct Access Storage, all with the same 2.52-gigabyte storage capacity.

The 3380 can be used with the 3081 Processor Complex. One of two new models of the 3880 Storage Control, Model 2 or Model 3, is a prerequisite. Up to two 4-unit strings of 3380 drives can be connected to one of the two storage directors on the 3880 Model 2, and to both storage directors on the 3880 Model 3. A 3081 processor, equipped with the Data Streaming feature, can handle the full 3.0-megabytes/second data transfer rate of the 3380.

As compared to a 3350 disk subsystem of equivalent storage capacity, a 4-unit 3380 string offers savings of approximately 65 percent in floor space, 70 percent in power consumption, and 75 percent in heat load. IBM says the 3380 also incorporates major advances in reliability, availability, and serviceability. First customer shipments of both the 3380 and the new models of the 3880 Storage Control are scheduled for the first quarter of 1981.

3880 STORAGE CONTROL: This control unit provides two completely independent paths for the transfer of file positioning commands and data between an IBM central processor channel and direct-access storage devices. Each path, called a Storage Director, attaches to a block multiplexer channel on a 3081 system. Both Storage Directors can be attached to the same channel, to different channels on the same processor, or to channels on two separate processors.

There are three models of the 3880. Model 1 can accommodate various combinations of 3330/3340/3350/3370/3375 storage units. Model 2 functions similarly to Model 1 except that one of the two storage directors can also attach 3380 disk drives. Model 3 is designed to attach 3380 drives only to a 3081 system. The speed matching buffer option (#6550) must be attached to a Model 2 or 3 when the 3380 device is used. A two-channel switch (#8170/8171) and eight-channel switch (#8172) can be selected to increase the number of channels connected to a storage director from two to eight.

Up to 14 3340/3344 disk drives can be configured on a storage director. As many as 16 3330/3333/3350 drives can be configured in various combinations on a director. At the high-performance end, a storage director can attach a maximum of 16 3370/3375 drives or 8 3380 drives.

INPUT/OUTPUT UNITS

The 3081 can support a wide range of peripheral devices, several of which are listed below. Please refer to the I/O

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Units section of Report 70C-491-06 for specifications of the individual units.

- 3420 Magnetic Tape unit (through 3803 Tape Control)
- 1442 Card Read/Punch
- 1442 Card Punch
- 2501 Card Reader
- 2520 Card Read/Punch
- 2520 Card Punch
- 2540 Card Read/Punch (through 2821 control)
- 3505 Card Reader
- 3525 Card Punch (through 3525 Punch Adapter)
- 3203 Model 5 Printer
- 3211 Printer (through 3811 control)
- 3800 Printing Subsystem
- 1255 Magnetic Character Reader
- 1419 Magnetic Character Reader
- 1287 Optical Reader
- 1288 Optical Page Reader
- 3881 Optical Mark Reader
- 3886 Optical Character Reader
- 3890 Document Processor
- 3814 Switching Management System
- 3705 Communications Control

TERMINALS: Numerous IBM display terminals, batch terminals, and typewriter terminals can be connected to a 3081 system in remote and/or local configurations. For details, please refer to Reports 70D1-491-45, 70D2-491-11, 70D2-491-12, 70D3-491-46, 70D4-491-41, and 70D4-491-43 in the Peripherals section of DATAPRO 70 (Volume 2).

COMMUNICATIONS CONTROL

Remote communications in the 3081 Processor Complex are handled via the IBM 3705-II Communications Controller and related SCPs. Please refer to Report 70C-491-06 for details on these facilities.

SOFTWARE

The 3081 Processor Complex is supported natively by the MVS/SP and VM/SP operating systems. Any program written for the System/370 or 303X can be run on a 3081 using MVS/SP or VM/SP provided the program 1) is not time-dependent, 2) is not dependent on the mix of system facilities and peripherals in the 3081, and 3) does not depend on results or functions as defined in the System/370 Principles of Operation. The 3081 is not supported natively by either DOS/VSE with or without Advanced Functions or VS1/Basic Programming Extensions (BPE). IBM indicated it will provide local programming support to the following situations: 1) DOS/VSE Systems Control Programs executing in conjunction with Release 3 of VSE/Advanced Functions programs, and 2) VS1/BPE programs, both of which are running under VM/SP on a 3081.

MVS (MULTIPLE VIRTUAL STORAGE): MVS (OS/VS2) is IBM's large-scale operating system, designed to handle multiprocessor configurations. Its latest version is Release 3.8, onto which several major enhancements have been added. A detailed summary of MVS can be found in Report 70C-491-06. The current program product targeted for use in the 3081 is the MVS/System Product (MVS/SP). Utilizing two versions of the Job Entry Subsystem, JES 2 and JES 3, MVS/SP has three announced levels, Releases 1, 2, and 3, the highlights of which follow.

MVS/SYSTEM PRODUCT—JES 2/3 RELEASE 1: The next stage of MVS enhancements came in the form of MVS/SP-JES 2/3 Release 1. MVS/SP is a generic term referring to the various announced releases of MVS/SP-JES 2 (5740-XYS) and MVS/SP-JES 3 (5740-XYN). MVS/SP Release 1 includes all the functions of MVS/SE Releases 1 and 2 plus the following:

- Support for the IBM 3380 DASD operating through the 3880 Controller Models 2 or 3 using either the Data Streaming or the 3880 Speed Matching Buffer features.
- Support for the IBM 3375 DASD operating through the 3880 Controller Models 2 or 3 using the Data Streaming feature.
- Support for the Data Facility/Device Support Release 1 program product (5740-AM7), which provides data management control for the 3380 DASD and 3880 controllers.
- Support for 3278 and 3279 displays as multiple console support (MCS) consoles.
- Performance equivalent to a system running MVS Release 3.8 with MVS/SE Release 2.

MVS/SP-JES 2/3 Release 1 was announced on June 11, 1980, and was scheduled for initial deliveries in November 1980. It was updated on November 12, 1980 to provide support for the IBM 3081 Processor complex.

MVS/SP-JES 2/3 Release 2: This product, announced on June 11, 1980, and scheduled for delivery in June 1981, will provide the following enhancements over MVS/SP Release 1:

- Cross memory services, which offers the potential to reduce system virtual storage requirements and improve data isolation. It utilizes the microcode-assisted 3033 Extension feature on the 3081.
- Global resource serialization, which improves the Enqueue/Dequeue (ENQ/DEQ) structure, extends the function to the multiprocessor environment, and can serialize access to system resources across processor boundaries.
- Improved reliability, accessibility, and serviceability (RAS) functions.
- Improved installation management of the paging subsystem by directing VIO pages to specific page data sets.
- Enhanced NJE job networking facilities in MVS/SP-JES 2.
- Support of the 3375 and 3380 DASD as spool and checkpoint devices.

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MVS/SP-JES 2/3 Release 3: The third update for MVS/SP was announced on November 12, 1980, is scheduled for release in October 1981, and will feature the following enhancements over Release 2:

- Support for up to 32 megabytes of addressable storage, in conjunction with the Extended Addressing feature.
- Support for the IBM 3081 Processor Complex.
- Performance increases of about 10 percent on uniprocessors and 12 percent on attached/multiprocessors in TSO/batch environments.
- Performance increases of about 6 percent on UP systems, or slightly more on AP/MP systems, in heavy batch and on-line IMS/batch environments.
- Improved memory management techniques; cross memory, paging, and swapping in particular.
- Enhanced JES 3 global resources to provide greater processor potential.
- Improved RAS, particularly to reduce the number of unscheduled IPLs.

VM/SP: The 3081 is also supported by VM/SP, which extends the capabilities of the VM/370 Release 6 product. A detailed summary of VM/370 and VM/SP can be found in Report 70C-491-06. Highlights of the most recent enhancements to VM/SP, as of June 11, 1980, include the following:

- Support for multiprocessor configurations.
- Support for the 3042 Model 2 Attached Processor.
- Support for the 3380 DASD using the 3880 Model 2 or 3 Storage Controller as a paging, spooling, SYSRES, or mini-disk device.
- Support for the 3375 DASD.
- Support for the 3800 Printing Subsystem as a virtual spooling device.
- 3270 Display System enhancements.
- Improved RAS functions such as missing I/O interrupt detection, dynamic space allocation for a dump after IPL, and checkpoint limit expansion for spool files.
- Enhanced security functions.
- CMS/DOS upgrade to the VSE/Advanced Functions product, and support for VSE/VSAM Release 2 and VM/Interactive File Sharing.
- Support MVS/SP-JES 2/3 as guest operating systems. Cross memory services of Release 2 of MVS/SP are supported, and the 3033 Extensions feature is not required in this situation.
- Support for the 3081 Processor Complex, as of November 12, 1980.

Additional details on the compilers, assemblers, data base management systems, communications software, and applications software products available to 3081 users are covered in Report 70C-491-06.

PRICING

MAINTENANCE: IBM offers both contract and on-call maintenance support. The basic monthly maintenance charge includes any period of 9 consecutive hours between 7:00 a.m. and 6:00 p.m. Monday through Friday. Customers may also purchase extended maintenance coverage that includes 12, 16, 20, or 24-hour coverage on weekdays, Saturdays, Sundays, and holidays. A premium is also charged for 9-hour, 5-day maintenance in which the 9-consecutive-hours period falls outside the 7:00 a.m. to 6:00 p.m. limits.

On-call maintenance service is charged at hourly rates that are shown in the following table. The majority of equipment is in Maintenance Class 3.

	Normal Working Hours	Outside Normal Working Hours
Class 1	$74.00	$86.00
Class 2	92.00	107.00
Class 3	100.00	115.00

LEASE TERMS: The IBM Agreement for Lease or Rental of IBM Machines, instituted in April 1977, defines three usage plans by which monthly charges are determined, IBM assigns each machine to one of these three plans.

Plan A provides the customer with up to 176 hours of billable time per month. Time used in excess of that amount is charged at an hourly rate that is 1/176th of the Monthly Rental Charge (MRC) multiplied by the Additional Use Charge Percent (usually 10 percent).

Plan B includes umlimited usage of the unit in the Monthly Rental Charge or Monthly Lease Charge.

Plan C monthly charges are determined by multiplying the amount of processing performed by the machine (not the time in use) by the Monthly Use Charge specified for the particular unit. The processing is measured by a meter attached to the unit. The monthly charges include all equipment maintenance, insurance charges, and property taxes.

The most significant change brought about by the new agreement was the ability to include equipment with differing lease terms on a single lease contract and the special long-term lease plans that had been offered under several amendments to the previous lease agreement. Specifically, the Extended Term Plan (ETP), Fixed Term Plan (FTP), Term Lease Plan (TLP), and Alternate Term Plan (ATP) were discontinued. However, the new agreement permits lease terms similar to those of the discontinued plans to be routinely implemented. Customers with existing term plan agreements can continue with those contracts and extend them in accordance with their provisions. IBM has stipulated final termination dates beyond which none of these discontinued plans may be extended. These dates are listed below.

Extended Term Plan	April 3, 1980
Fixed Term Plan	April 3, 1981
Term Lease Plan	April 3, 1982
Alternate Term Plan	April 3, 1983

Customers having no new agreement after these dates will revert to the Monthly Availability Charge under the previous lease agreement.

PURCHASE OPTIONS: In August 1974, IBM extended its Purchase Option Plan to allow users renting under the Monthly Availability Charge (MAC), Extended Term Plan (ETP), and Fixed Term Plan (FTP) to accumulate up to 36 months of purchase option credits toward the purchase of the equipment. The total amount accrued cannot exceed 50 percent of the purchase price of the equipment at the date of purchase. The 48-month Term Lease Plan also permits the

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accumulation of purchase credits through 48 months to a maximum of 50 percent of the purchase price. Previously, the Monthly Availability Charge contract permitted accumulation of up to 12 months of purchase option credits, and the Fixed Term Plan and Extended Term Plan included provision for accumulation of up to 24 months of purchase option credits. Under terms of the new lease agreement, users purchasing their rented or leased systems may apply between 50 and 60 percent of the accumulated monthly charges to the purchase price. The specific percentage allowed is dependent upon the equipment.

SOFTWARE: IBM has five designations for its software products: System Control Programs (SCP), Program Products (PP), Application Programs (PPA), Field-Developed Programs (FDP), and Installed User Programs (IUP).

System Control Programs provide those functions which are fundamental to the operation and maintenance of a system (e.g., loader, scheduler, supervisor, and data management) and include the DOS/VS and OS/VS operating systems and the VM/370 Virtual Machine Facility. SCPs are provided to IBM customers at no charge and to non-IBM customers for nominal distribution costs (namely, the cost of the media and a duplication charge). IBM customers also receive full IBM software support, which includes all updates, temporary fixes, and generally all enhancements to the software packages. All other IBM software is separately priced.

SCPs are modified by Selectable Units (SUs), which are microcode packages that implement the same types of enhancements that were formerly provided by subsequent releases of software packages. At present, SUs are also provided at no charge, but only to IBM customers with the appropriate equipment.

In addition, basic monthly charges have been established for maintenance of the IBM system control programs and other licensed program products. The minimum term of agreement is one year. A customer with multiple systems will have a choice as to how he can have local programming support handled at his locations. Should the user have IBM perform local program support at all computer sites, he pays the Basic Monthly License fee for all locations. If the user decides, however, to control the installation and support of designated license programs from a central site, he pays the Basic License Fee at the central site and a Distributed Systems License Option (DSLO) monthly fee for all other locations. The DSLO rates are lower than the basic monthly support charges.

Support charges for the systems software products described in this report are listed at the end of the equipment price list. Local programming support for 3081 systems is provided in two categories: Category A, which includes support for DOS/VSE, OS/VS1 Release 7, and VM/370 Release 6, and Category B, which includes all SCPs in Category A, MVS Release 3.8, and all supporting SCPs for MVS/SP. Refer to the following chart for monthly rates.

LOCAL PROGRAMMING SUPPORT CHARGES

Processor	Monthly Program Support Charge	Monthly Additional Program Support Charge
3081 (A)	$1,085	$651
(B)	1,550	930

All other programming service and assistance is charged at $107 per hour during regular hours and $123 per hour during non-regular hours.

Program Products include all language processors, communications support programs, and utility programs, and are licensed separately. Monthly license charges are listed under "Software Prices" in report 70C-491-06 and include full IBM software support. Application Programs (PPAs) are problem- and industry-oriented software packages that are also licensed separately, including full support. Also available on an individual-charge basis, but without centralized IBM programming support, are numerous Field-Developed Programs and Installed User Programs for the 3081.

SUPPORT CENTER: The centralized IBM Support Center provides 24-hour, 7-day customer access by telephone (an 800 number is provided). It utilizes the Software Support Facility data base, which incorporates every problem encountered and resolved (or unresolved) by the central support group. The customer is assisted in making out any APAR (program problem report), and he gets advice on temporary fixes or bypasses.

The Support Center is the first level of support. If it cannot resolve a problem, the customer is put in touch with the Change Team Support Specialist, who is directly familiar with the section of coding relating to the problem being reported. If, after working with this individual, the problem still cannot be resolved, the PSR (Program Support Representative) from the customer's local office will be dispatched to assist. Under the new support plan, many of the facilities that were previously provided by IBM support personnel at no charge have become billable activities.

SUPPORT: IBM Systems Engineering assistance is available to 3081 users at a basic rate of $79.00 per hour.

EDUCATION: IBM "Professional Courses" are individually priced. System Features Instruction is offered to users of IBM data processing equipment at no charge. Customer Executive Seminars, Industry Seminars, and promotional sessions are still offered at no charge by IBM invitation.

EQUIPMENT: The following system illustrates a possible 3081 Processor Complex configuration. It includes all the necessary control units and adapters, and does not include any specialized software. Pricing for individual devices can be found in Report 70C-491-06. The system includes the 3081 Model D16, with 16 megabytes of main memory and 16 channels, the 3082 Processor Controller, the 3087 Power Coolant and Distribution Unit, the 3089 Power Supply, three 3278-2A consoles with associated keyboards, four 3375 DASD (3,280 megabytes of storage) and four 3380 DASD (10,000 megabytes) with associated 3880 Model 2 Controller, a tape subsystem consisting of two 3803 controllers and eight 3420 Model 6 tape drives with dual density, an 800-cpm card reader, a 200-cpm card punch, two 3286-2 printers, a 3800 Printing Subsystem, and a 2000-lpm 3211 printer. The purchase price is $5,386,070, monthly maintenance is $14,413, and the system leases over two years (except the 3081, 3082, 3087, and 3089, which lease over four years) for $134,425 per month.■