Harris H500

MANAGEMENT SUMMARY

Harris Corporation's acquisition of Datacraft Corporation in 1794 lead to the formation of Harris' Computer System Division which has continued to market Datacraft's Slash Series and has introduced the Series 100, 500, and 800 virtual memory systems.

The H500 was initially introduced as the packaged S500 system but in September 1979 prices were reduced and the system was restructured. The new memory prices reflect Harris use of 16K memory chips and the planned early use of 64K chips on the same memory boards. The basic system now includes only a processor, memory, and console. Its price is $99,600.

The H500 is a virtual memory system capable of performing concurrent time-sharing, batch, remote job entry, and real-time processing. Harris states that the H500 is suited for distributed processing, transaction processing, and communications applications as well as scientific applications. The major hardware components of the basic system are the CPU, main memory, cache memory, shared memory, priority interrupt system, I/O channels, Scientific Arithmetic Unit (SAU), and console. An operating system, five language processors, and support utilities are also included.

Memory can be addressed by word, double word, byte, or bit by the standard instruction set. Full word as well as byte manipulation and Boolean operations with bits can be performed. Two's complement arithmetic is performed on parallel, binary, fixed-point operands.

The H500 operating system, Vulcan, is a multi-programming, multi-lingual virtual memory operating system. It supports concurrent operation of interactive time-sharing, multi-level batch, and real-time processing

The Harris 500 is essentially an enhanced version of the Slash 6 virtual memory system with unbundled hardware components and additional software. The basic 24-bit virtual-memory systems consist of a CPU, 64K words of memory, an operating system, and five language compilers. The basic system costs $99,600, with a typical user configuration selling for about $175,000.

CHARACTERISTICS

MANUFACTURER: Harris Corporation, Computer Systems Division, 1200 Gateway Drive, Fort Lauderdale, Florida 33309. Telephone (305) 974-1700.

Founded in 1895 as a manufacturer of automatic printing presses, Harris Corporation is now a high-technology company supplying a broad range of equipment and services for communications and information handling. The Computer Systems Division came into being in 1974 after Harris acquired Datacraft Corporation, a minicomputer manufacturer.

MODEL: H500.

DATE ANNOUNCED: NA.

DATE OF FIRST DELIVERY: NA.

NUMBER INSTALLED TO DATE: NA.

DATA FORMATS

BASIC UNIT: 24-bit word.

FIXED-POINT OPERANDS: 24-bit words and 48-bit double words. Data is represented in two's-complement binary notation.

A typical Harris H500 virtual memory system includes 704K words of MOS memory with error correction, 300 megabytes of mass storage, a 9-track 800/1600 bpi tape unit, DMA communications processor, console CRT and six terminals. Large data basis can be supported and up to 64 interactive terminals can be driven by the H500. Main memory of the 24-bit word system can be expanded to 1,024K words.

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as well as the Total Data Base Management System, remote job entry, and remote job hosting. Harris claims that a full H500 system can support up to 32 terminals.

Options available for the H500 include memory expansion to one million words, up to 1,200 megabytes of disk storage, 800/1600 or 6250/1600 bpi magnetic tape units, up to 32 terminals, card and paper tape equipment, and data communications facilities.

While no applications packages are available from Harris, the systems software support provided with each system is sufficient so that users can readily develop their own applications software.

The applications which have been implemented by Harris users for real-time multiprogramming and time-sharing environments include simulation, nuclear experiments, supervisory control, telemetry, avionics checkout, geophysical research, astronomy, medical analysis, chemical analysis, and engineering problem-solving. A broad range of peripheral equipment is available, and the input/output structure of these systems assures effective usage of the peripheral devices.

Harris systems are directed at the OEM market, system houses for turnkey operations, and direct end-user supply.

Harris services its equipment on a maintenance contract basis, with field service personnel operating out of 10 sales offices in the United States. Offices are located in major metropolitan areas near large installation sites.

Services offered by the vendor include consultation for design and testing of applications software, interface software, and system software, as well as in-house or in-field training on the processor, peripherals, and software for user system programmers and maintenance personnel.

USER REACTION

Datapro was able to contact three H500 users with a total of ten systems installed. All three of the users purchased their systems and all did their own applications programming. Two of the users were using their systems in a business environment, and were using the full operating system and COBOL. One user was operating in a scientific environment using the Vulcan operating system, FORTRAN, and some assembly language.

The ten systems had one CPU apiece with from 192K to 780K bytes of memory and from 380 to 2,400 megabytes of storage. One or two magnetic tape drives and six to nine terminals were included in each system.

The table below summarizes the ratings assigned by the se H500 users.

FLOATING-POINT OPERANDS: A double-precision floating-point hardware option (Scientific Arithmetic Unit—SAU) is available for the H500. The SAU option contains hardware for operating on double-precision numbers which have a signed 39-bit mantissa and an 8-bit exponent. Sign, zero, or overflow status is determined after each operation.

INSTRUCTIONS: Most instructions of the H500 computers are one word in length. Direct addressing to 32K words of memory is provided in the majority of memory reference instructions, with additional instructions, such as branches, that directly address up to 65,536 words.

Operation codes are usually either 6 or 12 bits in length, and instruction formats vary widely. There are 11 distinct field arrangements within the 24-bit instruction word. However, within these 11 arrangements there are multiple field uses that expand the number of format descriptions greatly. Three representative format descriptions are presented here, but they by no means exhaust the possibilities.

Memory reference instructions are of two basic types. The standard memory reference uses the high-order six bits for the operation code, the next bit for an indirect addressing indicator, the next two bits for indexing, and 15 bits for the address field. The second format is the long branch; the high-order six bits are the operation code, the next bit is an indicator for indirect addressing, the bit after that is an operation code extension, and the last 16 bits form an address field. Another significant format is for register-to-register instructions; the operation code occupies the 12 high-order bits, with the last 12 bits divided equally to designate two registers. Memory beyond 65K words is reachable through the virtual memory addressing system or through indirect referencing at a timing penalty of one memory cycle per level.

INTERNAL CODE: ASCII.

MAIN STORAGE

TYPE: NMOS with single-bit error correction.

CYCLE TIME: 300 nanoseconds, or as fast as 70 nanoseconds if the desired instruction or operand is already in cache memory. The 6K byte cache memory is divided into two partitions, one for instructions and the other for operands, each of which is searched in parallel. Harris claims an average "hit" rate of 90%.

CAPACITY: The standard H500 includes 192K bytes (64K words) of main memory which can be expanded in 192K-byte increments to 3,072K bytes.

CHECKING: Single-bit error correction is employed using a 5-bit Hamming code for each 24-bit word. All single-bit main memory errors are detected and corrected, and most multiple-bit errors are detected. The 5-bit check character is generated for each word as it is written into memory and recomputed when the word is read.

STORAGE PROTECTION: Hardware storage protection is optional on the H500. The program-restrict/instruction-trap option defines and protects specific areas under program control through the use of upper and lower limit registers.

RESERVED STORAGE: The H500 reserves from 16 to 48 memory addresses for external interrupt handling. Sixteen priority interrupt levels are standard and up to 48 are optionally available. Internal interrupts, called executive traps, reserve words for each of the eight internal interrupts.

Two thousand words of cache memory and a shared memory system are also included in the H500. The shared memory can be configured with either MOS or core memory. A single

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION AND SPEED	MANUFACTURER
MAGNETIC TAPE		
6630, 6631	Seven-track, 556/800 bpi, 45 ips, tension arm	Wangco
6700	Nine-track 6250/1600 bpi, 75 ips	Wangco
6840-1,2	Nine-track, 800 bpi, 45 ips, tension arm	Wangco
6850-1,2	Nine-track, 800/1600 bpi, 45 ips, tension arm	Wangco
6890-1,2	Nine-track, 800/1600 bpi, 75 ips, vacuum column	Wangco
LINE PRINTERS		
4410	180 cps serial printer	Dataproducts
4110	300 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4115	240 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4120	600 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4125	436 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4130	900 lpm, drum type, 64-char. set, 136 positions	Dataproducts
4135	660 lpm, drum type, 96-char. set, 136 positions	Dataproducts
4710	500 lpm, 1.2 ips plot, 11-inch plot/123-col. print, 1024 nibs, 96-char. set	Versatec
4720	1000 lpm, 2.3 ips plot, 11-inch plot/123-col. print, 1024 nibs, 96-char. set.	Versatec
4730	300 lpm, 75 ips plot, 20-inch plot/232-col. print, 96-char. set	Versatec
4740	1200 lpm, 3 ips plot, 20-inch plot/232-col. print, 96-char. set	Versatec
4750	1000 lpm, 1 ips plot, 11-inch plot/132-col. print, 96-char. set	Versatec
CARD EQUIPMENT		
3010	300 cpm reader, 550 card I/O stackers, 80-column	Documation MXXXL
3020	600 cpm reader, 1000 card I/O stackers, 80-column	Documation MXXXL
3030	1000 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
3110	300 cpm reader, 500 card I/O stackers, 80-column	Documation MXXXL
3120	600 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
3130	1000 cpm reader, 1000 card I/O stacker, 80-column	Documation MXXXL
PAPER TAPE EQUIPMENT		
2030/2035	300 cps reader/75 cps punch (2035 is for fanfold tape)	Remex
2040	300 cps reader/spooler	Remex
2050	2040 with 7.25-inch reel	Remex
2060	75 cps punch/spooler	Remex
2095	Paper tape spooler	Remex
TERMINALS		
2110, 2130	Modified ASR-33; 8530 is remote terminal; 10 cps	Teletype
2140	Modified KSR-33; 8540 is remote terminal; 10 cps	Teletype
2150	Modified ASR-35; 8550 is remote terminal; 10 cps	Teletype
2160	Modified ASR-35; 8560 is remote terminal; 10 cps	Teletype
2210	ASR-733 TTY; 8710 is remote terminal	TI
2220	KSR-733 TTY; 8720 is remote terminal	TI
2310	Interactive CRT 24 lines x 80 char. 9600 bps; 2315 has hard-copy device; 8610 is a remote terminal; 8615 is a remote terminal with hard-copy device; 8630 has RS-232 interface; 8635 has RS-232 interface and hard-copy device	Tec
2320	733 replacement CRT, 24 lines x 80 char., 9600 bps; 2325 has hard-copy device; 8620 is a remote terminal; 8625 is a remote terminal with hard-copy device; 8640 with RS-232 interface; 8645 with RS-232 interface and hard-copy device	Tec
2350	Teletype replacement CRT; 24 lines x 80 chars., with keyboard	Infoton

	Excellent	Good	Fair	Poor	WA*
Ease of operation	2	1	0	0	3.7
Reliability of mainframe	2	1	0	0	3.7
Reliability of peripherals	1	2	0	0	3.3
Maintenance service:					
Responsiveness	2	1	0	0	3.7
Effectiveness	1	1	1	0	3.0

CPU can interface with up to four shared memory systems, with a maximum of one million words available to each CPU.

CENTRAL PROCESSORS

GENERAL: The H500 central processing units are shared-program, fixed-word-length asynchronous processors. Standard features include a maintenance aid processor, priority

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	Excellent	Good	Fair	Poor	WA*
Technical support	1	1	1	0	3.0
Manufacturer's software:					
Operating system	2	1	0	0	3.7
Compilers & assemblers	0	3	0	0	3.0
Ease of programming	1	2	0	0	3.3
Ease of conversion	3	0	0	0	4.0
Overall satisfaction	2	1	0	0	3.7

*Weighted Average on a scale of 4.0 for Excellent.

The average system had been installed for less than nine months, so that some of the ratings were rather tentative. The strongest positive statement came from the scientific user who stated that he was getting higher throughput than had been obtained from a large mainframe. The user who gave the lowest ratings stated that he had been through a rather difficult previous installation of H120 systems but the system's performance had eventually improved and he assumed that the same thing would happen with his H500.□

interrupt control system including 16 external priority interrupts, I/O channels, paging hardware, cache memory, a scientific arithmetic unit (SAU), hardware multiply/divide/square root, bit processor, internal traps, and five general-purpose registers.

Two's compliment arithmetic is performed in parallel, binary, fixed-point operands, floating point arithmetic is performed concurrently by the SAU.

The 24-bit arithmetic logic unit (ALU) includes several busses for transferring data between registers and the ALU. Arithmetic functions performed include addition, subtraction, multiplication, division, and square root computation. The ALU also computes addresses during memory reference operations. In user mode, the paging control logic implements address translation and demand paging techniques.

CPU memory interface circuits consist of address and data-handling busses and registers, and either parity generation and checking or error checking and correction code logic. Memory interface circuits include a 48-bit data register for retaining both the read and write data, a 20-bit address register for the physical memory location, and multiplexing logic for data handling and address control.

Single- and double-precision transfers are performed between the CPU and SAU, with double transfers taking two cycles. Some SAU instructions can be prefetched when the SAU is busy.

Options for the H500 include memory expansion to 3,072K bytes (1,024 words), an interprocessor communications facility, priority interrupt expanders, a 100K-Hz real-time clock and additional chassis slots.

The H500 CPU consists of a single multi-layer printed circuit board that contains the ALU, registers, bootstraps, the first eight external priority interrupts, and the timing/control logic necessary to execute the instruction set. The ALU is composed of six high-speed microprocessor chips, each representing a 4-bit logic slice. Auxiliary PROM's are utilized for instruction decoding and subsequent microcode execution, resulting in program and feature compatibility with the Slash series computers. Of the 16 CPU working registers, 5 are accessible to the programmer, and 3 of these are indexable.

Standard features of the H500 CPU include eight external priority interrupts, eight bootstraps, power fail shutdown/restart, clock, and hardware multiply, divide, and square root. CPU options include a bit processor, stall alarm, program restrict/instruction trap, interval timer, 8 executive traps, 16 additional external priority interrupts, and program halt and address trap.

CONTROL STORAGE: None.

REGISTERS: There are 8 registers and 2 pseudo-registers in the H500 computers, plus registers required for virtual memory operation. Five of the registers are accessible to the programmer: the A and E registers, which are 24-bit general-purpose registers, with the A register used primarily as an accumulator and the E register used primarily as an extension to the A register; and the I, J and K registers, which are 24-bit general-purpose registers that can also be used for indexing. The D register is a 47-bit double pseudo-register comprising the A and E registers. The B register is an 8-bit pseudo-register which is bits 0-7 of the A register.

The other registers and their use follow. The 4-bit C register indicates the status of arithmetic, compare, I/O, logical, shift, and transfer operations. The P register holds the current instruction address and is 20 bits in length. The Instruction register holds the instruction being executed and is 24 bits in length.

Either 1,024 or 4,096 12-bit Virtual Address Registers (VAR) can be supplied with the H500, depending upon memory and page sizes. Ten bits store the memory address of the page and two bits control access to the page. Upper and lower page limit registers are provided for each user program, with two sets of 1,024 one-bit page registers to record reading and writing activity in the pages. Four additional registers are used to store the register addresses required in the virtual memory system.

ADDRESSING MODES: H500 addressing is accomplished in either standard or compatible mode. Direct and indirect addressing and indexing are affected by the operating mode. Within the standard (called address extension mode) and compatibility modes, software runs in either user or monitor mode. In monitor mode addresses need not be translated since the monitor system is confined to the lowest 64K words of memory. In user mode the virtual memory system performs the address translation.

In the standard operating mode, up to one megaword of memory can be addressed directly. Memory is divided into up to 32 32K maps. Direct addressing in standard mode is accomplished by appending the 15-bit address from the instruction to the 5-bit map indicator to form an effective instruction address. Addresses from standard long branch instructions (16-bit address without provision for indexing) and all extended instructions are not modified. The second word of extended instructions contains a 20-bit address.

When the indirect addressing bit of an instruction is set the contents of the addressed 20-bit word are used for the effective instruction address, unless bit 23 of the address word is set indicating another level of indirect addressing Each of the indirect levels can be indexed to provide further address modification.

A two-bit field can be used to specify one of the three index registers to modify either direct or indirect addresses.

Compatibility mode allows the H500 to run all programs written for the Harris Slash 6 processor without recompilation. However only 16 bits of the program counter are utilized, which limits direct addressing to 64K words. The 15-bit instruction address used in compatibility mode limits direct addressing to either the upper or lower half of the

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64K word area. Modification of the 15-bit instruction address by means of indirect address words containing 18-bit addresses permits a standard instruction to address up to 256K words. Compatibility mode addresses can also be indexed.

INSTRUCTION REPERTOIRE: Two hundred forty-one instructions are available with the H500. The standard instruction set is grouped into instruction types, and the number of instructions of each type is tabulated below.

Instruction Type	
Arithmetic	42
Branch	14
Compare	11
Input/Output	7
Logical	9
Priority Interrupt	22
Shift	12
Transfers	36
Miscellaneous	11
Bit processor	17
Scientific Arithmetic Unit	47
Virtual Memory	13

INSTRUCTION TIMINGS: The following are minimum times for full-word fixed-point operands in register-to-register operations, given in microseconds.

Add/Subtract:	0.36
Multiply/Divide:	6.06/12.66
Compare:	0.96

INTERRUPTS: Eight internal traps are included in the H500 to facilitate the operation of the VULCAN operating system. Sixteen external priority interrupt levels are standard, with up to 48 levels optionally available.

PHYSICAL SPECIFICATIONS: The H500 is 71 inches high, 48.75 inches wide, and 34.5 inches deep. It can operate from between 50°F to 113°F, and from 20% to 80% non-condensing relative humidity. Power requirements are 120/240 + 10% or 120/208 ± 10% at either 60 or 50 Hz ± 3 Hz. Maximum current drawn on 24 amperes and the heat dissipation is 18.750 BTU per hour. The weight of the system is 1200 pounds.

INPUT/OUTPUT CONTROL

I/O CHANNELS: Three types of Direct Memory Access channels are available, including the Direct Memory Access Communications Processor (DMAC), Integral Block Channel (IBC), External Block Channel (XBC), and Universal Block Channel (UBC). A Programmed Input Output Channel (PIOC) is also available.

The IBC is a DMA channel dedicated to handle the block-mode card reader and floppy disc controller concurrently. The PIOC can accept up to four integral device controllers, two integral device controllers and a 100K-Hz real-time clock, or up to 12 external device controllers.

The XBC is used for custom-designed external controllers where control is desired over word count and memory address information. The XBC has the facility to communicate with up to eight external devices on a user-assigned priority basis.

The UBC supports command and data chaining and is primarily for high-speed devices such as disc and tape units. The UBC is actually two logical, concurrent 24-bit channels with a data transfer rate of 4.9 megabytes per second for input and 3.9 megabytes per second for output. (The speed of the IBC and XBC can best be characterized as the speed of the external devices.) Up to 16 device controllers can be attached to the UBC.

SIMULTANEOUS OPERATIONS: DMA channels, after control circuitry initialization, can perform block transfer operations of 24-bit words without affecting processor memory fetches. All PIOC transfers are fully buffered and tie up the CPU or memory for one cycle per transfer.

CONFIGURATION RULES

The number of peripherals is limited only by the number of I/O channels and the quantity of peripherals that each type of channel can handle. The 24-bit DMACP, IBC, and UBC can each handle 16 peripherals, while the XBC handles 8 as a maximum.

MASS STORAGE

5200 CARTRIDGE DISC SYSTEM: Provides storage for 10.8 million bytes on double platters. The controller supplied can handle up to four disc units total. The data transfer rate is 300,000 bytes per second. Average head positioning time is 35 milliseconds, and average rotational delay is 12.5 milliseconds. The 5200 is manufactured by Control Data Corp.

5500 DISC STORAGE MODULE: Provides 40, 80, 150, or 300 million bytes of storage with a single drive and controller. The 40/80-megabyte controller can support three additional drives, providing another 120 or 240 million bytes of storage. The 150/300-megabyte controller can support one additional drive. Transfer rates are up to 1.2 million bytes per second. Average head positioning time is 30 milliseconds, with an average rotational delay of 8.3 milliseconds. The 5500 Series units are manufactured by Control Data Corporation.

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

COMMUNICATIONS CONTROL

The 8100 Series Asynchronous/Synchronous Controllers operate at up to 9600 bps, and most operating parameters are set by program.

The 8310 Communications Multiplexer provides a common logic chassis for up to eight channel boards. Each board can handle a synchronous line interface or a dual asynchronous line interface of the 83XX type.

The 8430 Direct Memory Access Communications Processor (DMACP) is dedicated to serial data communications with up to eight asynchronous devices, or one synchronous and four asynchronous devices. Available interfaces include RS-232C, 20 ma current loop, and Harris differential. Single 24-bit control words or data blocks are passed between the DMACP and the CPU. A microprocessor included in the DMACP board controls the transfers independent of the CPU.

COMMUNICATIONS SOFTWARE: A Remote Job Entry subsystem supported by DMS provides the capability for communication with certain host computers concurrently with other processing. All standard terminal features are supported for communication with the following systems: as a Univac 1004 with the Univac 1100 Series computers; as a Control Data 200 User Terminal with the CDC 6000/7000 Series; as an IBM 2780 with the IBM 360/370 series. Any DMS interactive terminal, either CRT or teletypewriter, may serve the RJE subsystem. Message transmission and reception use the host system's protocol. I/O spooling is an integral part of the system.

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INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

SOFTWARE

The basic software package supplied as standard with each system depends on the particular system configuration chosen. The operating system is VULCAN.

Also supplied are APL interpreter, a FORTRAN IV Compiler, COBOL compiler, Interactive BASIC Compiler, SNOBOL 4, RPG II, Harris MACRO Assembler, Diagnostic FORTRAN Compiler (FORGO), Sort/Merge, Indexed Sequential File Handler, post-mortum dump, Utility Package, Cross Reference, Symbolic Debugger, Link Loader, and a complete set of diagnostics for the mainframe, memory and peripherals.

OPERATING SYSTEM: The *Virtual Core Manager (VULCAN)* occupies 10,000 to 32,000 words. System size depends on several factors, including the number of concurrently active user programs, system table sizes, and the number of nonresident handlers loaded at a given time. According to Harris, the system will generally occupy less than 20,000 words of core. Absolute minimum VULCAN configurations require 32K words of core for real-time applications, and if interactive or batch environments are required, minimum memory sizes of 49K to 65K words will be needed.

VULCAN's features include disc file security on a multi-level basis, re-entrant processors and libraries which minimize the additional memory required by multiple users, re-entrant code generation (which implies separation of program space into code and data sections), spooling of input and output of either the data or jobstream type for local or remote terminals, interprogram communications either by message or parameter, integral systems accounting, and a Remote Job Entry (RJE) subsystem for emulation of several different terminal types.

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Any interactive terminal, either CRT or teletypewriter, may serve the RJE subsystem. Message transmission and reception use the host system's protocol.

LANGUAGES: Eight languages are currently being offered for use on the H500.

APL is a conversational language that is particularly well suited for operating on numeric and character array-structured data. Using APL, variables can be shared and also examined and changed, and program action can be readily traced. Features of APL include dynamically variable user's workspace size, chaining of APL programs to previously prepared run-time programs, multiple statement lines, standard H500 file naming formats, and extended single operators which allow the user to fully evaluate character strings and write user-defined functions to perform output formatting and function editing. The language is built around a set of unique symbols, each of which represents a desired operation. The nature of the language is such that complex expressions are easily constructed by the programmer. According to Harris, APL produces concise code.

FORTRAN IV is based on but exceeds ANSI X3.9-1966. Harris-supported extensions include random-access I/O; indexed sequential file operations; memory-to-memory data conversion through encode/decode statements; double-buffered and overlapped I/O capabilities through asynchronous I/O statements, which include processing of variable-length and arbitrary-format records in both input and output; free-format I/O, allowing for basic I/O without using FORMAT statements; control functions for end-of-file and I/O or FORMAT errors in all I/O statements; a DATA statement extension for arrays; octal and literal constants; recursive subprograms; in-line assembly code for statements and variables or constants; implied DO loops in DATA statements; program-controlled loading of program overlay segments which have been separately compiled; pseudo-random number generations; services in real-time digital and analog I/O functions; and bit manipulation functions. A diagnostic FORTRAN compiler (FORGO) serves as a companion to Harris extended FORTRAN IV.

Interactive BASIC contains 54 statements and language enhancements for string manipulation, extended Boolean operators and IF statements, logical I/O and picture format facilities, and editing for input. Built-in real-time capabilities allow for use of external interrupts, initiation of programs, parameter passing from other programs regardless of language, and operator communications. A compiler mode that produces linkable code is included in Harris' BASIC, as well as a conventional interpreter mode.

RPG II as implemented by Harris allows for interchange of files between itself and FORTRAN IV or assembly-language programs, as well as creation of these files by programs coded in any of the three languages. Harris RPG II language extensions include array and table equivalencing, main program execution initiation, array element manipulation, source library use, and one- to six-byte binary numeric fields. Sequential, indexed sequential, and direct access files are also supported.

The *MACRO Assembler* is a two-pass system that supports over 700 mnemonic operation codes and a range of pseudo-operations which can, among other things, create 11 different constant types. The assembler features nested and recursive macro capabilities.

COBOL conforms to ANSI X3.23-1974. As with FORTRAN, the COBOL compiler generates re-entrant code. It features 44 verbs and modifications, 49 levels of qualification, arbitrary deeply nested conditional statements, 32-digit accuracy in intermediate calculations, facilities for using CORRESPONDING, and standard debugging tools.

TOTAL is a host-language data base management system implemented much along the same lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL provides an effective means for organizing and managing diverse data to make it both efficient and convenient for application programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc. and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL allows the user to relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particular single-

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entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL data base is composed of multiple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL, they also reduce the amount of disc storage required to hold information by eliminating duplicate fields or records.

A randomizing algorithm is used by TOTAL to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disc space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL files is propvided through the Call statement for application programs written in COBOL, FORTRAN, or assembly language. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

The interactive language allows nonprogrammers to extract information that is stored in the TOTAL data base by means of a simple, English-like, nonprocedural information retrieval language.

UTILITIES: Other software includes an indexed sequential disc access method callable by FORTRAN IV or assembly-language programs; a sort/merge package callable by FORTRAN IV, RPG II, or assembly language; and a macro cross-assembler written in FORTRAN IV.

APPLICATIONS: Harris does not supply application packages.

PRICING

POLICY: Harris offers its systems primarily for purchase, although third-party leasing (one-year term) is available on a negotiated basis. Some software costs are bundled in the system prices, except for items such as the operating system; the remote batch terminal emulation software, which is priced at $5,000; TOTAL Basic, priced at $10,000; TOTAL Central, priced at $12,800; and T-ask priced at $10,000; and some utilities.

Special considerations apply for volume purchases of virtual-memory systems. When the first purchase of a H500 system is made by an OEM or volume-purchase end-user, no OEM, CPU, peripheral, or business volume discounts apply. Any additions or upgrades to a system, however, will be eligible for appropriate CPU/peripheral discounts. Down-grade substitutions are permitted with a penalty of 20 percent of the deleted item's list price; the items to be substituted will be charged at full list price. CPU's purchased in H500 systems will count toward CPU and peripheral totals for other OEM purchases, and the final "dollar total" on the systems will apply to total business volume for other purchases.

SUPPORT: Maintenance is performed by service personnel working out of Harris CSD service offices in the U.S. Maintenance contracts are developed on the basis of local or remote service areas. A local service area is defined as the area within a 50-mile radius of a Harris CSD service office. All other areas are considered remote. For non-contract maintenance, prime-time hourly rates are $45 and $50 per man-hour; minimum billing for these customers is four hours for local service and eight hours for remote service. Remote service area customers, whether on contract or not, are billable at actual cost for tourist-class air travel or at $0.20 mile for automobile usage, and for meals and lodging.

Under contract, maintenance is available for 9 prime-shift hours from 7 am to 6 pm Monday through Friday. Additional maintenance hours are available by negotiation with Harris at prime monthly rates plus an extra charge.

Installation charges are made, but are negotiable depending on the size and quantity of systems sold. Programming and maintenance training are separately priced and are available either at the installation site or at Harris' Fort Lauderdale facility. Training courses are offered in maintenance for the processors, Scientific Arithmetic Unit, and peripherals. A software course on VULCAN is currently being offered.

EQUIPMENT: The following typical H500 system includes the Vulcan operating system, five language processors, system utilities, and all required control units, adapters, and cables.

An H500 with 192K words of memory, 600 lpm printer, 80-megabyte disk drive and controller, 45 ips 800 bpi tape drive and controller, DMA communications processor and channels is priced at $176,200.■

Harris H500

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PROCESSOR			
The H500 computer; includes system console, 18-slot chassis, 16 priority interrupts, 2K word cache memory, paging hardware, hardware multiply/divide/square root, bit processor, programmer's control panel, maintenance and processor, virtual memory system			
PROCESSOR			
H500	With 192K bytes (64K words) of MOS memory, operating system, 5 compilers, and support utilities	$99,600	$605
PROCESSOR OPTIONS			
022	100K-Hz real-time clock	1,500	10
024	Runtime meter	150	10
050	Priority interrupt with 8 priority interrupts	750	10
051	Priority interrupt expander with 32 priority interrupts	3,500	40
052	Priority interrupt expander with 24 priority interrupts	3,000	30
060	Interprocessor Communications Facility option; includes two link universal block channels and priority interrupt generator connections	8,100	55
045	Programmed I/O channel (PIOC)	1,200	10
047	Universal block channel (UBC)	3,300	20
048	External block channel (XBC)	2,000	15
049	Internal block channel (IBC)	2,000	10
650	Priority interrupt group; consists of 8 priority interrupts	750	10
072	Expansion pack; including 22-slot I/O chassis and power supplies	6,800	20
073	Memory expansion chassis for up to 9 memory modules	7,500	20
074	Extended Memory kit; interface module for 073	2,000	—
076	Slot Enable kit; includes 4 slots for shared memory ports and 3 slots for additional memory modules	1,000	—
077	Additional Slot Enable kit; includes 4 slots for additional memory modules	1,000	—
MASS STORAGE			
5260	10.8-megabyte double platter cartridge disc drive and controller	16,400	140
5261	10.8-megabyte add-on double-platter cartridge disc drive	11,000	110
5265	Cartridge disc platter	500	—
5510	40-megabyte storage module drive and controller	23,300	255
5511	40-megabyte storage module drive	15,900	175
5530	80-megabyte storage module drive and controller	26,900	300
5531	80-megabyte add-on storage module drive	19,500	225
5550	300-megabyte storage module drive and controller	43,650	450
5551	300-megabyte storage module drive	34,250	400
MAGNETIC TAPE			
6630	Seven-track, 556/800 bpi, 45 ips tension arm drive and controller; 4 drives maximum	12,750	115
6631	Seven-track, 556/800 bpi, 45 ips add-on drive	9,500	95
6840	Nine-track, 800 bpi, 45 ips tension arm drive and controller; 4 drives maximum	12,900	115
6841	Nine-track, 800 bpi, 45 ips add-on drive	9,900	99
6850	Nine-track, 800/1600 bpi, 45 ips, tension arm drive and controller; 4 drives maximum	17,000	155
6851	Nine-track, 800/1600 bpi, 45 ips add-on drive	10,500	105
6660	Nine-track, 800/1600 bpi, 45 ips vacuum column drive and controller; 4 drives maximum	18,000	160
6661	Nine-track, 800/1600 bpi, 45 ips add-on drive	11,000	110
6710	Nine-track 6250/1600 bpi, 75 ips vacuum column drives and controller; 4 drives maximum	51,500	NA
6711	Nine-track 6250/1600 bpi, 75 ips add-on drive	20,000	NA
6720	Nine-track auto load 6250/1600 bpi, 75 ips vacuum column drive and controller, 4 drives maximum	52,500	NA
6721	Nine-track auto load 6250/1600 bpi, 75 ips add-on drive	21,000	NA
6890	Nine-track, 800/1600 bpi, 75 ips vacuum column drive and controller; 4 drives maximum	21,500	180
6891	Nine-track, 800/1600 bpi, 75 ips add-on drive	13,000	130
6710	Nine-track, 1600/6250 bpi, 75 ips vacuum column drive and controller	37,000	440
6711	Nine-track, 1600/6250 bpi, 75 ips add-on drive	24,300	200
6720	Nine-track 1600/6250 bpi, 75 ips vacuum column drive and controller (for drives 3 and 4, feature 6295 is needed)	38,000	450
6721	Nine-track, 1600/6250 bpi, 75 ips add-on drive	25,300	210
LINE PRINTERS/PLOTTERS			
4110	300 lpm printer, 64 character, with controller	13,500	135
4115	240 lpm printer, 96 character, with controller	15,000	145
4120	600 lpm printer, 64 character, with controller	18,900	175
4125	436 lpm printer, 96 character, with controller	20,900	195

Harris H500

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
LINE PRINTERS/PLOTTERS (Continued)			
4130	900 lpm printer, 64 character, with controller	24,900	250
4135	660 lpm printer, 96 character, with controller	27,400	270
4410	180 cps serial printer	3,950	50
4720	1000 lpm printer, 2.3 ips simultaneous plotter and controller	19,500	195
4730	300 lpm printer, 0.75 ips simultaneous plotter and controller	17,500	175
4740	1200 lpm printer, 3 ips simultaneous plotter and controller	20,000	200
4750	1000 lpm printer, 1.0 ips simultaneous plotter and controller	24,500	200
CARD EQUIPMENT			
3010	300 cpm card reader and controller	10,000	55
3020	600 cpm card reader and controller	12,000	80
3030	1000 cpm reader and controller	13,500	100
3110	300 cpm card reader with DMA controller	5,150	55
3120	600 cpm card reader with DMA controller	6,980	70
3130	1000 cpm card reader with DMA controller	10,000	100
PAPER TAPE EQUIPMENT			
2030	300 cps reader/75 cps punch and controller	6,250	50
2035	2030 for fanfold tape	6,750	60
2040	300 cps reader/spooler and controller	3,900	35
2050	2040 with 7¼-inch reel	4,400	40
2060	75 cps punch/spooler and controller	5,000	45
2095	Paper tape spooler for 2010 and 2015	3,000	30
TELETYPEWRITERS			
2105	Teletype modification kit	350	—
2110	ASR-33 teletypewriter with controller	2,750	55
2115	Serial teletypewriter controller	750	10
2130	Modified ASR-33 teletypewriter	2,300	50
2140	Modified KSR-33 teletypewriter	2,100	40
2150	Modified ASR-35 teletypewriter	6,850	85
2160	Modified KSR-35 teletypewriter	4,400	55
CONSOLE DEVICES			
2210	30 cps ASR 733	5,500	70
2220	KSR 733	4,400	55
2310	Interactive CRT; 24 x 80 with keyboard and interface	5,500	80
2320	Teletype replacement CRT; 24 x 80 with keyboard and interface	3,350	45
2350	Teletype replacement CRT; 24 x 80 with keyboard and interface	2,450	25
COMMUNICATIONS			
8110	Synchronous controller; operates on 8-bit IOC; up to 9600 bps	2,750	30
8120	Asynchronous controller	1,250	15
8121	Additional asynchronous controller	1,250	15
8130	Asynchronous controller for RS-232 terminal on 8-bit IOC; up to 9600 bps	2,500	25
8310	Communications multiplexer for up to 16 asynchronous or 8 synchronous lines	3,000	30
8330	Synchronous line interface unit for RS-232C modem connection to multiplexer	1,200	15
8340-1	Dual Asynchronous line interface unit	750	10
8340-2	Dual Asynchronous line interface unit for RS-232C modem	850	10
8350	Dual Asynchronous line interface unit for 33 or 35 TTY	750	10
8360	Dual Asynchronous line interface unit for 8600 Series CRT	750	10
8370-1	Dual Asynchronous line interface unit for 8700 series terminal	750	10
8370-2	Dual Asynchronous line interface unit for 8700 series modem	850	10
8410	DMA communications MUX channel with two twin asynchronous ports; expandable to four twin asynchronous ports	4,600	40
8411	Additional DMA communications MUX channel	3,300	20
8422/5	Twin asynchronous ports	650	10
8430	DMA Communications Processor for up to four twin asynchronous ports, or one synchronous and two twin asynchronous ports	3,300	30
8435	ISODMACP; includes two ports for graphics terminals or plotters	5,900	70
8447	Synchronous port; up to 19,200 bps	1,200	15

Harris H500

SOFTWARE PRICES

	Purchase Price	Yearly Maint.
VULCAN Operating System: includes COBOL, FORTRAN, FORGO, SNOBOL, Sort/Merge, Index Sequential package, MACRO Assembler, Disk Copy, Cross Reference Program, DEBUG, and Symbolic Debugger	$3,000	NA
TOTAL Central	12,800	600
T-ask	10,000	500
Extended BASIC	5,000	420
APL	14,000	1200
RPG II	2,500	240
FORTRAN	3,000	240
RJE 2780/HASP II/UNIVAC 1100—1004/CDC 200 UT—6600 (Plus $5,000 installation charge)	1,000	NA
Diagnostics: for CPU, storage, peripherals, each	100	NA