Data General microNova

The microNova family is available in three basic configurations: chip sets, board computers, and fully packaged microNova minicomputers. All the packaged variations are built around the 40-pin mN601 NMOS microNova processor (foreground), which features a full 16-bit Nova architecture and main memory addressing capacity of up to 32K words.

Data General's microNova is fully compatible with the popular Nova Series minicomputers in architecture and utilizes the complete range of Nova software. The microNova is a 16-bit microprocessor in a 40-pin chip package, and is available by the chip, by the board, or by the box. Chip prices start at $225, board prices at $800, and minicomputer prices at $1,995.

MANAGEMENT SUMMARY

With the introduction of the 16-bit microNova in March 1976, Data General became the first major minicomputer manufacturer to introduce a full microprocessor-based computer line—from chips, through boards, to boxes. Using a DG-built microprocessor, the microNova is compatible with the older Nova line, enabling the full range of developed and tested Nova software to be used with the new processor.

By manufacturing its own chips, Data General has reinforced and slightly redefined its OEM position. It is apparent that integrated-circuit manufacturers are fast becoming a significant factor in the manufacture of minicomputers, and moves such as this one by DG are designed to put the company in a better position in case the IC manufacturers begin to encroach on its territory.

Moreover, effective competition in the low end minicomputer business means cost-cutting procedures—procedures that would eliminate repackaging IC's and placing heavy reliance on original source manufacturers for those IC's. This has led Data General into production of its own chips, and ultimately to the microNova. A strong plus for Data General and similar companies is in the area of software and system support, where the minicomputer makers have a major advantage over the semiconductor manufacturers.

CHARACTERISTICS

MANUFACTURER: Data General Corporation, Southboro, Massachusetts 01772. Telephone (617) 485-9100.

Data General is a leading manufacturer of minicomputers, peripherals, and associated equipment. The company maintains sales offices in most major North American cities and in South America, Europe, and Australia. Manufacturing operations are located at the company's Southboro, Massachusetts headquarters; in Westbrook, Maine; and in Sunnyvale, California. Assembly operations are also performed in Hong Kong and in Thailand.

MODELS: microNova Chip Set (model number unspecified); Microcomputer, Models 8562 and 8563; Minicomputer, Models 8560 and 8561; Development Systems, Models 9040, 9042, and 9043.

DATE ANNOUNCED: March 2, 1976.

DATE OF FIRST DELIVERY: December 1976.

DATA FORMATS

BASIC UNIT: 16-bit word or 8-bit byte.

FIXED-POINT OPERANDS: 16-bit words can be interpreted as signed or unsigned binary numbers, logical words, memory addresses, or portions of decimal character strings.

Decimal numbers can be either character decimal or packed decimal. In character decimal format, each digit is an 8-bit ASCII character, and the sign is either carried separately as an extra character at the beginning or end of the decimal string or by modifying either the first or last digit in the string. The packed decimal format places each digit in 4-bit hexadecimal code, with a separate sign character at one end of the string.

FLOATING-POINT OPERANDS: 32-bit single-precision operands with a 7-bit exponent and signed 24-bit fraction; and 64-bit double-precision operands with a 7-bit exponent and signed 56-bit fraction. Single and double-precision floating-point arithmetic is implemented through software subroutines. No hardware floating-point arithmetic is available.

INSTRUCTIONS: One-word instructions. There are four basic instruction types, each with different formats: Jump and Modify Memory, Move Data, I/O, and Arithmetic and Logic. In all instructions, bits 0 through 2 specify the instruction type.

In Jump and Modify instructions, bits 3 and 4 identify the specific function (op code), and the rest of the word con-

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Data General, however, is not alone in this field. Computer Automation, General Automation, IBM, Microdata, and Texas Instruments have all employed microprocessor chips, in one form or another, as early as 1971. But Data General was the first to manufacture and offer its product as a chip set, on a board as a microcomputer, and in a box as a minicomputer.

For OEM accounts, the microNova offers some interesting possibilities. They can start with a minicomputer development system, and integrate downward to microNovas on boards or to chip sets with a minimum of difficulties. Such a move permits production economies as volume increases, but does not require the heavy front-end investment associated with IC development or software conversion. At this writing, few vendors can make this type of offer.

All the package variations are built around the 40-pin mN601 NMOS microNova processor. The chip has the Nova 3 16-bit architecture and instruction set, hardware stack and frame pointer with stack overflow protection, 16-bit hardware multiply and divide real-time clock, all memory control and timing, integral hidden refresh logic for dynamic RAM's, four general-purpose accumulators (two of which can be used for indexing), programmed priority interrupt to 16 levels, CPU and memory control for DMA, and separate memory and input/output buses.

Besides the mN601, the chip set consists of two 20-pin bipolar mN634 Octal Memory Bus Transceivers, sixteen 20-pin NMOS mN606 chips to make a 4K-word RAM (Random Access Memory), two 20-pin bipolar mN633 Octal Memory Address Drivers, four 14-pin bipolar mN506 Quad Sense Amplifiers, a 20-pin mN629 CPU I/O Transceiver, a 20-pin bipolar mN636 I/O transceiver, a PC board, some TTL logic, and passive components. The chip set makes up a 4K-word RAM CPU system, and in a quantity of one, sells for $950.

All components of the chip set are produced by Data General. The mN606 4K-word RAM was introduced with the Nova 3 for first delivery in February 1976. The mN603 I/O Controller (IOC) provides the functions of the 47-line Nova I/O bus by decoding data from a two-line serial I/O bus up to 100 feet in length. The IOC also performs integral device identification, interrupt logic, and per-device interrupt masking.

The microNova microcomputer on a board combines an mN601 processor with 2K (Model 8562) or 4K (Model 8563) words of RAM, power fail/auto restart, and a real-time clock on a 7.5 by 9.5-inch board. The front edge of the board optionally provides operator panel functions, including lights and switch controls for lock, reset, start program load, and continue. Additional 7.5 by 9.5-inch boards are utilized for 4K or 8K words of RAM; 512, 1K, 2K, or 4K words of PROM; a PROM programmer; and various interfaces. The 2K-word microNova on a board is priced at $800 in a quantity of one.

The microNova as a minicomputer is available in a 9-slot chassis (Model 8561) and in an 18-slot chassis (Model

tains information used to calculate the effective address, including an 8-bit displacement, 2-bit index register specification, and 1-bit indicator to specify direct or indirect addressing.

In Move Data instructions, bits 3 and 4 address an accumulator, and the rest of the word is identical in structure to the Jump and Modify type above.

In I/O instructions, bits 5 through 9 specify the function (indication of transfer direction, selection of an I/O device register, and/or specification of an operation). Bits 3 and 4 select an accumulator for transfer, and bits 10 through 15 indicate a specific device.

Arithmetic and Logic instructions use bits 1 and 2 to identify an accumulator containing a second operand (if present), bits 5 through 7 to specify primary function, and the rest of the word to specify secondary functions, if any.

For all memory reference instructions, bits 5 through 15 are used for addressing, using bits 8 through 15 as the displacement or direct address. Each instruction and address 256 words directly, or can use either relative or base register addressing.

INTERNAL CODE: ASCII and binary.

MAIN STORAGE

TYPE: Dynamic MOS RAM, requiring 64 refresh cycles every 1.8 milliseconds. Refresh is overlapped with CPU execution.

CYCLE TIME: 960 nanoseconds.

CAPACITY: 32K words in 4K- and 8K-word increments.

CHECKING: None.

STORAGE PROTECTION: None.

RESERVED STORAGE: The microNova has 16 reserved words which function as auto-increment/auto-decrement registers.

CENTRAL PROCESSOR

The microNova is available as a chip set which includes the mN601 Microprocessor, mN606 4K RAM, and these System Buffer elements: mN634 Octal Memory Bus Transceiver, mN633 Octal Memory Address Driver, mN506 Quad Sense Amplifier, and two I/O Transceivers, mN629 and mN636.

Above this level, the microNova is available as a microcomputer on a 7.5 by 9.5-inch printed circuit board. Model 8562 comes with 2K words of dynamic RAM, while Model 8563 comes with 4K words.

In a minicomputer or development system configuration, the microNova features power fail/auto restart, real-time clock, rack-mountable 9- or 18-slot chassis with CPU and 4K RAM on a single board, operator's control panel, power supply, asynchronous interface boards, general-purpose I/O; interface boards, per-device data channel facility, up to 100 feet of external I/O bus, and PROM memory boards.

On the Models 8560 and 8561 microNova Minicomputers, automatic program load, battery backup, and a hand-held programmer's console are optional. These are standard on the Models 9040, 9042, and 9043 microNova Development Systems. Other options for both the minicomputer and development systems include PROM programmer, expansion chassis, card frames, and extender cards.

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION	MANUFACTURER
TERMINALS		
6040/6042	Dasher terminal printer; 30, 60 cps	Data General
6052/6053	CRT display; 1920-character, 64- and 96-character set, switch-selectable speeds from 110 to 19.6K bps	Data General
6012	CRT display; 1920-character, variable codes, local editing, EIA or 20-ma current loop interface, full or half-duplex; up to 4800 bps	Data General
4010A	ASR-33 teletypewriter; 10 cps	Teletype

8560). As a minicomputer development system, the microNova is available in an 18-slot chassis with an ASR-33 teletypewriter (Model 9040), a DG Dasher terminal (Model 9043), or a teletypewriter modification kit for the user's choice of terminal (Model 9042).

Both the minicomputer systems and the minicomputer development systems (MDS) are available with a diskette subsystem. On the minicomputer, the user may elect either 157K words (315K bytes) in a single diskette drive or 315K words (630K bytes) on a dual diskette drive. The MDS is available with a dual diskette drive as standard equipment. The diskette subsystem includes a DMA controller.

The minicomputer prices start at $1,995 for the Model 8561 in a single-unit quantity. MDS prices start at $10,565, not including the 72-inch cabinet. Power fail/auto restart and real-time clocks are standard on both the minicomputer and MDS, whereas automatic program load, battery pack, hand-held programmer's console, and rack cabinet are optional on the minicomputer but standard on the MDS. Other standard features of the minicomputer and MDS are additional RAM and/or PROM memory up to 32K words, asynchronous interface boards, addressability for up to 61 peripherals, and up to 100 feet of external I/O bus. Optional features include the PROM programmer, 9-slot expansion chassis, card frames, extender cards, and device connector cables.

Nova 3/4 and 3/12 development systems are available for users who need more power in system development.

Beside the aforementioned support by a wide range of Nova software, the microNova has its own development software. This is a special package consisting of the Disc Operating System, Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. The software developed under DOS will run under DOS or RTOS (Real Time Operating System). Both DOS and RTOS are subsets of RDOS. DOS is most logically used for development only. For run-time control, RTOS should be used because of its small memory space requirements. DOS requires 16K words of RAM, versus only 4K words for RTOS.

CONTROL STORAGE: 0.5K, 1K, 2K, or 4K words of PROM (programmable read-only memory) are available for the microNova. Each size of PROM module is separately mounted on a memory board. A PROM programmer on its own board permits PROM chip burning under program control. The programmer acts directly on the PROM board and is inserted in the chassis only when needed.

REGISTERS: The microNova has four 16-bit accumulators and a 15-bit program counter. Two accumulators can be used for address indexing.

The microNova, like the Nova 3, has a last-in/first-out (LIFO) push-down/pop-up stack implemented in any 256 consecutive memory locations and two additional hardware registers (the stack pointer and the frame pointer). The stack pointer identifies the first memory location designed as the stack, and the frame pointer marks intra-stack boundaries to permit several "register saves" to be accumulated in the stack. The frame pointer can be set randomly to access words stored in stack frames without popping an entire frame.

Also, like the Nova 3, the microNova has 16 reserved memory locations which function as auto-increment or auto-decrement registers when addressed directly.

ADDRESSING MODES: The microNova has six addressing modes: direct (256 words), indirect (multi-level), indexed, indexed-indirect (pre-indexing), program-relative, and program relative-indirect.

INSTRUCTION REPERTOIRE: The basic complement includes four Jump and Modify Memory instructions, two Move Data instructions, 16 I/O instructions, and eight Arithmetic and Logic instructions. There are 256 variations on each of the Arithmetic and Logic instructions. Hardware multiply/divide instructions are standard.

INSTRUCTION TIMINGS: The timings shown are for full-word, fixed point operands, in *microseconds.*

Load/Store	**2.88**
Add/Subtract	**2.4**
Multiply/Divide	**41.28/59.04**
Jump	**2.88**

INTERRUPTS: A 16-level programmed priority interrupt facility is used to recognize interrupts for I/O operations. Each device is wired to one of 16 bus positions, and is either authorized or denied authorization to interrupt particular service routines by an Interrupt Disable Mask Bit that corresponds to the bus positions of the device.

PHYSICAL SPECIFICATIONS: The microNova in a minicomputer configuration is housed in a chassis of either 9 or 18 slots. The 9-slot chassis is 5.25 inches high, 19 inches wide, and 14.5 or 23 inches deep; the greater depth is with battery backup. The 18-slot chassis has the same height and

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In March 1977, DG announced DOS BASIC for the microNOVA. Originally announced for the Nova series minicomputers, the DOS BASIC interpreter became available in May 1977. DOS BASIC is a subset of RDOS Extended BASIC and is upward-compatible with both RDOS and AOS extended BASIC.

Then, in November 1977, Data General increased the capabilities of the microNova in data communications, data acquisition, process control, and peripheral control applications. The new hardware and software enhancements include interfaces to implement asynchronous and synchronous protocols and to expand the range of process control, instrumentation, and related I/O applications. In addition to support software for the new interfaces, Data General announced RJE80 and HASP II capabilities, a paper-tape software package, and a PROM utility program.

Data General sees three prime areas of application for the microNova; medical and instrumentation, data communications, and process control. The implementation of serial I/O (with its potential for cabling up to 100 feet and high noise immunity), the IOC chip, and the significant quantity of tested software are indicative of DG's intention to make this portent of future applications a reality.

USER REACTION

Datapro interviewed four users of the microNova minicomputers. All of them were OEM's, and they had collectively programmed and installed a total of 37 microNova systems. One installation employed dual microNova processors communicating with two Eclipse computers to monitor emergency medical services. The rest of the microNova: medical and instrumentation, data communications included small business systems configured with the 6053 CRT display, the 6040 Dasher terminal printer, dual floppy disk drives, and 20K of memory; data acquisition for a paper mill configured with the 4332 A/D Interface, dual floppies, and 28K of memory; optical scanning; and photo color control. Most of the installed systems were less than a year old.

The table below summarizes the responses to Datapro's survey.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	1	3	0	0	3.3
Reliability of mainframe	3	1	0	0	3.8
Reliability of peripherals	0	3	1	0	2.8
Responsiveness of maintenance service	2	1	1	0	3.3
Effectiveness of maintenance service	1	1	2	0	2.8
Technical support maintenance service	1	1	2	0	2.8
Technical support	1	1	2	0	2.8
Operating systems	1	3	0	0	3.3
Compilers and assemblers	2	2	0	0	3.5
Ease of programming	3	1	0	0	3.8
Ease of conversion	1	1	0	0	3.5
Overall satisfaction	3	1	0	0	3.8

*Weighted Average on a scale of 4.0 for Excellent.

width; its depth, with or without the battery pack, is 27.5 inches. A microNova development system complete with dual diskette subsystem will fit into a 72-inch cabinet.

Power requirements for all chassis types are 100, 120, 220, or 240 VAC ±10 percent, 47 to 63 Hz. Operating temperatures are 32 to 132 degrees F. A relative humidity of up to 90 percent, noncondensing, can be tolerated. The processor outputs 1023 BTU/hour maximum. Air conditioning requirements are those of a normal office environment.

The 9-slot chassis weighs approximately 37 pounds without battery backup. The 18-slot chassis weighs approximately 52 pounds without battery backup. Add 5 pounds to the chassis weight for battery backup for either chassis.

INPUT/OUTPUT CONTROL

INPUT/OUTPUT CHANNELS: An I/O bus and a Direct Memory Access (DMA) channel are standard.

The I/O bus is serial in structure and can be up to 100 feet long. Bipolar transceivers differentially drive the microNova serial I/O signal on a parallel two-line basis. This technique offers high noise immunity and ease of cabling.

The basic I/O bus is etched in the backplane. It functions to provide communication between mainframe-based I/O boards and the CPU board. The basic I/O bus is offered with a standard extension of 15 feet to connect the dual diskette subsystem. Longer extensions as discussed above are optional. Mainframe-based I/O boards are connected to free-standing peripherals by a 50-line device cable. Speed of the I/O bus is 16.6 megahertz, which translates to a data transfer rate of up to 1 million words per second.

The Input/Output Controller (IOC), a 40-pin chip located at each device interface, decodes the serial I/O signal and routes it into a parallel 16-line bidirectional data bus for I/O operations. This is the logical equivalent of the 47-line Nova I/O system. The IOC has the ability to address up to 61 I/O devices. The program I/O facility has six commands for each device. Also incorporated are controller start, clear, and I/O pulses and the facility for programmed I/O, program interrupt, and DMA functions.

For the DMA channel, rates are quoted as 148,000 words per second for input and 173,000 words per second for output. The DMA channel can be used to increment the contents of storage locations by 1.

CONFIGURATION RULES

The microNova can have up to 61 peripheral devices attached to the I/O bus. The processor chassis is available with either 9 or 18 slots. Expansion chassis are available in the 9-slot size only. The actual number of peripherals that can be attached depends upon the available number of slots and the method of attachment.

Generally speaking, all peripherals require one slot for direct attachment. The processor is mounted on one board along with either 2K or 4K words of memory, and requires one slot. The PROM programmer requires one slot, the Asynchronous Interface Board requires one slot, each General-Purpose I/O Board requires one slot, the Terminal Interface Board requires one slot, and the Programmer's Console Board requires one slot. A maximum of two diskette controllers (up to eight drives) can be attached.

MASS STORAGE

6038 FLOPPY DISC SUBSYSTEM: Consists of a four-drive controller and either a 6038 single drive or a 6039 dual drive. Each floppy disc stores up to 315K bytes on 77

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GENERAL-PURPOSE INTERFACE BOARD: Provides a generalized programmed I/O, program interrupt, and DMA interface. An area on the board is pre-drilled and allocated for user-designed and built circuitry. Up to 35 IC's can be accommodated.

MODEL 4227 ASYNCHRONOUS LINE MULTIPLEXER: Controls up to four asynchronous communications lines. Each line can be configured for RS-232C or 20-ma current loop operation and individually programmed for number of bits per character (5 to 8), number of stop bits (1, 1.5, or 2), line speed (50 to 9600 bps), and parity (odd, even, or none). When enabled, parity is automatically checked/generated on each line. The multiplexer supports full- and half-duplex operation. The 4227 provides full character buffering on reception and transmission, program-controlled loopback testing, and modem control with automatic answer capabilities for Bell 103, 202, and 212 Series data sets.

MODEL 4426 SYNCHRONOUS LINE CONTROLLER: Interfaces to medium-speed (9600 bps) synchronous/bisynchronous communications lines, and provides a full- and half-duplex EIA RS-232C/CCITT V.24 interface and full character buffering on reception and transmission. When coupled with the optional Model 4228 hardware CRC generator, the synchronous line controller can select either of two standard check polynomials, CRC16 or CCITT16. Both idle and sync characters, as well as character size, parity, and loopback testing, are program-selectable. In receive mode, Model 4426 automatically synchronizes data and then strips out the sync character. Standard modem control is supplied for Bell 201, 203, 208, and 209 Series data sets. This synchronous controller also supports IBM Bisynch protocols with full transparency and is program code compatible with the SLM-2 Series synchronous multiplexer used on Data General Nova and Eclipse processors.

Up to four Model 4426 controllers can be configured with a single microNova minicomputer, allowing it to control a maximum of four synchronous lines. Only one CRC generator board is needed per system.

COMMUNICATIONS SOFTWARE

COMMUNICATIONS ACCESS MANAGER (CAM): A modular package that can be generated by the Communications System Generation Program (COMGEN) to include only those program segments required for each individual system. CAM operates under DOS and, since it uses the operating system's runtime-defined interrupt service, is brought into main memory from disc only as needed. This can free large segments of memory in a real-time communications system for other processing tasks.

CAM software can support both standard and special user-defined protocols, including Bisync (BSC) and an asynchronous terminal line procedure. Synchronous and asynchronous protocols can be intermixed. Multi-drop lines are supported through polling and selection sequences. Modem control support for auto answer/auto disconnect is a standard feature. CAM provides a queue for I/O completions that permits a single user task to control several asynchronous lines.

CAM also features a FORTRAN IV, FORTRAN V, or COBOL interface, permitting communications I/O in FORTRAN or COBOL programs.

REMOTE JOB ENTRY CONTROL PROGRAM (RJE80): Allows for remote job entry and communications between microNova processors and IBM 360/370 systems, or between microNova processors and other Data General computers. Support is provided for four types of RJE systems:

- Point-to-point communications between a Nova, Eclipse, or microNova emulating an IBM 2780/3780 and an IBM 360/370 host.
- Point-to-point communications between two Data General systems running RJE80.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with an IBM 360/370 host.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with a Nova or Eclipse or microNova master system also running RJE80.

RJE80 is supported by DOS as well as CAM. Features include horizontal and vertical printer format control; error detection on transmission and reception; and disc, tape, or card transmission to remote systems. Transmission between host systems may be to unattended RJE80 systems, and because of device-independent I/O capabilities, any combination of I/O devices can be utilized without additional software.

IBM HASP WORKSTATION EMULATOR: Lets a microNova emulate an IBM HASP remote job entry workstation. Its multileaving capability can include up to seven input and seven output data streams. Efficiency of data transmission is achieved through interleaving and data compression.

SOFTWARE

For all software specifications except DOS, DOS BASIC, and the special packages discussed below, see Report M11-304-101. Limitations on software use are predicated only on the memory size limitations of the microNova.

DISC OPERATING SYSTEM (DOS): A subset of RDOS, DOS is designed for use in development systems only. DOS requires a minimum of 16K words and includes a Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. Since DOS is a compatible subset of RDOS, any program developed under DOS can be run under RDOS or RTOS.

DOS BASIC: A subset of RDOS Extended BASIC, upward-compatible with both RDOS and AOS Extended BASIC. The interpreter takes advantage of operating system features by supporting device independence, and features extensions to the Dartmouth BASIC language. These extensions include string arithmetic, matrix operations, user-controlled output formatting, and sequential, random, and contiguous file management. DOS BASIC also offers several program development features and an assembly-language interface that allows subroutine calls. Both single- and multi-user versions of DOS BASIC have been released by Data General.

DOS BASIC implements string variables and literals, string concatenation, and string subsetting. Users can determine the location of a character within a string or the number of characters assigned to a string variable. They can also convert a numeric expression to a string that is its decimal representation, and return the decimal representation of a string variable or literal. In addition, READ and IF/THEN statements may employ strings. Matrix manipulation is achieved through a set of statements such as ADD, SUBTRACT, MULTIPLY, INVERT, and TRANSPOSE. Data General states that matrix dimensioning and redimensioning can easily be accomplished. Complete matrices can be read or written in a single I/O call.

The minimum hardware configuration for single-user DOS BASIC is any Nova computer, microNova computer, or

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Overall satisfaction with the microNova was high. This is not too surprising, since all of the users were OEM's who had expertise with the microNova and Nova computers and were familiar with Data General's service. They had chosen the microNova to configure and sell for very practical reasons, and they rated the reliability of mainframe, ease of programming, and ease of conversion highly.

All of the OEM's had service contracts with Data General, although one had just obtained it and based his "fair" rating of maintenance effectiveness on a single call to the manufacturer. This user rated Data General's responsiveness to the call as excellent. One of the OEM's we spoke with voiced what seemed to be the consensus of opinion about Data General's maintenance and technical support by commenting on the overall advantage of Data General's microNova to the OEM: "Data General offers substantial discounts to the OEM on some of the best hardware deliverable today. In short, you get a powerful system, acceptable service, and a great price." He cited documentation as an area that needs improvement, as he considered it difficult for the first-time user.

Two of the OEM's mentioned that their programmers found it necessary to make numerous changes in the operating system. Both were implementing new applications, however, and both gave the final version of the operating system a "good" rating. "There is not enough time," one of them commented, "for the manufacturer to test the operating system in every situation." Two users also reported having initial difficulties with the dual floppy disk drive, but said that once it was up and running, it was reliable.

All of the users were basically satisfied with the microNova, and they all mentioned the performance/price ratio as significant. "It is not generally known," said one of the OEM's, "that these small machines is a low price range can do such an incredible amount of work."□

tracks. Maximum storage capacity is 1.26 million bytes on a four-drive subsystem. Average head positioning time is 260 milliseconds, and average rotational delay is 83 milliseconds. Data transfer rate is 31K bytes/second. The 6038 drives feature IBM 3740 compatibility and are supported by Data General's RDOS operating system. The controller occupies one slot. The 6038 drives are manufactured by Data General.

INPUT/OUTPUT UNITS

The Model 4222 Digital I/O Interface, Model 4223 A/D Interface, and Model 4224 D/A Interface each occupy a single microNova board. They plug directly into the microNova chassis and provide it with stand-alone data acquisition and control capabilities.

MODEL 4222 DIGITAL I/O INTERFACE: Provides a digital device interface for 16 parallel input and 16 parallel output lines. It also furnishes two strobe output lines and one strobe input line. All lines are TTL-compatible. An internal/external data comparator compares real-time external data against an internal software-programmable condition, allowing the system to detect transient deviations from the condition via polling or interrupts and selectively mask bits for interrupt requests.

MODEL 4223 A/D INTERFACE: Incorporates two 8-channel multiplexers, a differential input instrumentation amplifier, a sample-and-hold unit, and a 12-bit successive approximation converter. Its 16 single-ended or 8 differential inputs are program-configurable. Auto-channel scan (with wraparound capability) and triggering modes are also program-selectable. The A/O subsystem offers jumper-selectable input voltage ranges of 0 to 5, 0 to 10, or ±10V. According to the vendor, a complete conversion requires only 33 microseconds.

MODEL 4224 D/A INTERFACE: This dual-channel, 12-bit subsystem provides a user-selectable, full-scale output of 0 to 5, 0 to 10, ±5, or ±10V, and, according to the vendor, settles to ±0.01 percent full-scale of the desired output value in seven microseconds. Each channel's output range is individually set.

DG/DAC INTERFACE BOARD: Interfaces the microNova to sensors, actuators, and associated electrical circuits. Each DG/DAC chassis can accommodate up to 16 chassis control cards with up to 16 lines per card for a total of 256 signal lines per chassis. Any mix of digital and analog cards is allowed in one DG/DAC chassis, which measures 8.75 by 19 by 22 inches, weighs 60 pounds, and comes with power supply, bus terminator, and bus cables.

MODEL 4229 DATA CHANNEL INTERFACE: Disables the microNova clocks and disconnects control and data signals from the memory bus when an I/O throughput device requests fast service. It then handles all data transfer control and memory refresh, and periodically restarts the CPU to avoid errors due to internal node leakage. Maximum throughput is 1 million words per second in a burst mode, with a typical throughput of 830K words per second.

MODEL 4220 PAPER-TAPE READER INTERFACE: Controls the Data General Model 6013, a 400-cps, 8-channel paper-tape reader. Sharing this interface board is the Model 4220-B Nova-compatible real-time clock. Model 4220-B does not affect the operation of the microNova integral real-time clock, and users can select either during system generation. Model 4220-B offers AC line or crystal control line; 10, 100, or 1000 Hz frequencies; and a program interrupt for a time-of-day clock or interval timing.

MODEL 4221 LINE PRINTER INTERFACE: Controls the Data General Model 4034C or 4034D 165-cps, 132-column matrix printers or equivalent printers. This full ASCII interface includes paper-tape advance character recognition.

SENSOR ACCESS MANAGER (SAM): Provides software support for the 4222, 4223, and 4224 data acquisition and control boards, and for the DG/DAC interface. SAM is a library of device handlers and subroutines that control I/O transfers between user programs and analog and digital sensor devices. It is callable by FORTRAN IV and assembly language programs.

See the Peripherals/Terminals table for specifications of the terminals that can be used with the microNova.

COMMUNICATIONS CONTROL

ASYNCHRONOUS INTERFACE BOARD: Provides single-line connection of teleprinters and 6012 Video Displays to the I/O bus. Device codes are jumper-selectable. Transmission speeds are 50 to 19.2K bps. Interface levels for RS-232C and 20-ma DC current loop are provided. Also provided are variable character lengths of 5, 6, 7, or 8 bits; either 1, 1.5 or 2 stop bits; and even, odd, or no parity. A firmware-based (256 words) Console Debug Option allows any ASCII console to supervise program execution, and also allows for modification of RAM locations and CPU registers. Included with this option is a multi-device loader routine.

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microNova computer on a board with 16K words of main memory, a dual diskette drive and controller, and one terminal with appropriate interface. The minimum hardware configuration for multi-user DOS BASIC is any microNova with 32K words of main memory, a dual diskette drive and controller, and two terminals with appropriate interfaces. Additionally, a wide variety of peripherals can be supported on a Nova-based DOS BASIC system, including diskette drives, magnetic tape drives, line printer, paper tape reader and punch, plotter, and multiple terminals. A maximum of 32K words of main memory can be supported.

OTHER SOFTWARE: Along with the RJE80, HASP II, CAM, and SAM software packages discussed elsewhere in this report, Data General provides paper-tape software consisting of an editor, assembler, and debugger, designed to operate in 4K words of memory. In addition, there is a PROM utility program that operates under DOS. The program prechecks the PROM card, then accepts an absolute binary file, programs the PROM chips inserted in the Data General Model 8574 PROM programmer board, and performs a postcheck validity test. It also allows users to specify optional start and stop addresses, program 2K and 4K PROM boards, and print an octal dump. Errors are reported and automatically retried 256 times.

PRICING

POLICY: Data General offers the microNova series on a purchase-only basis, with two types of separately priced maintenance agreements: the On-Call Service contract and the Depot Service contract, which involves return of faulty equipment to a designated repair location. In either case, all parts and labor are included at no additional cost.

Normal prime-time on-call contract service hours are 9 a.m. to 5 p.m. Charges quoted in the price list are applicable to customers within 100 miles of a service center. Additional but uniform monthly charges are in effect beyond 100 miles of a Data General service center. These charges are $150 for customers between 100 and 300 miles from the center and $225 for customers beyond 300 miles.

Under a Depot Service contract, any portion of a system may be covered, the minimum contract being $75. The customer assumes all transportation and insurance costs. For non-contract on-site service, the hourly maintenance rates are $40 for prime time and $48 for other times. A three-hour minimum applies. Depot service hourly labor charges are $30 for prime time and $48 for all other times.

Prices shown are for single-unit quantities, OEM quantity discounts apply, and are available from Data General upon request.

Data General software is licensed so as to be included without charge on a system with sufficient Data General hardware to operate it. The software is also available for purchase for use on configurations utilizing other than Data General equipment (e.g., peripherals, add-on memory, etc.).

Data General provides training courses for customers at its Southboro, Massachusetts headquarters, at its Western Training Center in El Segundo, California, and at its United Kingdom Training Center in Greenford, Middlesex, England. A special five-day course, "Designing with microNova," covering hardware components design and maintenance, memory systems, instruction set, interfacing, configuration, and program development, is offered. In addition to the centers listed above, this course can be taught at customer locations by special arrangement. Two training credits are given for each development system purchased by an end user, which entitle the customer to approximately one man-week of training. Schedules for training courses can be obtained at any Data General field office.

Software and Hardware Subscription Services are available. They provide automatic updates, additions, and documentation for a fixed yearly fee.

The Data General Users' Group provides a forum for interchange of programs. The programs are available for a fee to cover reproduction and distribution costs.

TYPICAL MICRONOVA DEVELOPMENT SYSTEM: Includes an 18-slot chassis containing CPU/4K-word RAM board with automatic program load, real-time clock and power fail/auto restart; 8K-word RAM board; 4K-word RAM board; terminal interface board; programmer's console board; and power supply with battery backup. Also included are a dual-diskette subsystem with integral data channel controller, hand-held programmer's console, and ASR-33 teletypewriter. All components except the ASR-33 are packaged in a 72-inch cabinet. Purchase price is $12,115.■

EQUIPMENT PRICES

		Purchase Price
PROCESSORS		
8562	microNova on a board with 2K words of RAM	$ 800
8563	microNova on a board with 4K words of RAM	950
8560	microNova Minicomputer in 18-slot chassis with 4K words of RAM	2,595
8561	microNova Minicomputer in 9-slot chassis with 4K words of RAM	1,995
PACKAGED SYSTEMS		
9040 & 9040A	microNova Development System with ASR-33 Teletypewriter	12,115
9042 & 9042A	microNova Development System with Teletypewriter Modification Kit	10,565
9043 & 9043A	microNova Development System with 60-cps Dasher terminal	13,015
PROCESSOR OPTIONS		
8565	Automatic Program Load	150
8575	Edge-Mounted Controls Indicator	200
8564	Hand-Held Programmer's Console	700
8566	Battery Backup	300
MEMORY		
8572	Board with 4K words of RAM	600
8573	Board with 8K words of RAM	950
8567	Board with 0.5K words of PROM	300

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EQUIPMENT PRICES

		Purchase Price
MEMORY (Continued)		
8568	Board with 1K words of PROM	375
8569	Board with 2K words of PROM	500
8570	Board with 4K words of PROM	750
8574	PROM Programmer	1,650
MASS STORAGE		
6038	Single Diskette Drive Subsystem with controller	2,900
6039	Dual Diskette Subsystem with controller	3,900
1098A	Carton of Diskettes	120
TERMINALS		
6042-1	Dasher 30-char./second KSR printer terminal; 132 columns	2,400
6043-1	Receive-only version of 6042-1	2,200
6040-1	Dasher 60-char./second KSR printer terminal; 132 columns	2,650
6041-1	Receive-only version of 6040-1	2,450
6012-H	Video Display Terminal; 24 lines by 80 characters	2,700
6052-1	CRT with 64-character set, switch-selectable speed from 110 to 19.6K bps; 24-line by 80-character screen	1,990
6053-1	Same as 6052-1 with 96-character set	2,290
HARDWARE AND INTERFACES		
4207	Asynchronous Interface Board	250
4208	Console Debug option	200
4210	General-Purpose Interface Board	250
4211	GPIO Wirewrap Pins/Sockets	200
1114	Predrilled Circuit Card	200
2303A	Extender Card	200
1115A	Card Puller Tool	50
8571	I/O Expansion Chassis	1,600
4212	Card Frame Assembly	250
4213	Power Supply	750
4214	Power Supply/Battery Backup	1,050
4220-A	Paper Tape Reader Interface	400
4220-B	Real-Time Clock	350
4220-A/4220-B	Combined Board	700
4221	Line Printer Interface	650
4222	Digital I/O Interface	400
4223	A/D Interface	1,150
4224	D/A Interface	800
4226	Synchronous Line Controller	400
4227	Asynchronous Line Multiplexer	500
4228	CRC Generator	250

CHIP PRICES (OEM only)

		PRICE RANGE			
		Quantity	Purchase Price	Quantity	Purchase Price
CHIPS					
mN601	CPU	1	$225	500	$95
mN603	IOC	1	100	500	60
mN606	4K words RAM	16	24	8,000	10
mN629	CPU 10X	1	60	500	25
mN636	IUC 10X	1	14	500	8
mN634	OCT MBX	2	20	1,000	8
mN633	OCT MAD	2	20	1,000	8
mN506	QUAD SA BD	4	24	2,000	10
1116A	Twelve 1K PROM chips	1	100	—	—
1117A	Twelve 2K PROM chips	1	250	—	—
CHIP SETS					
8563A	CPU with 4K words of RAM	1	900		
4210	General-Purpose Interface Chip Set	1	200		

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION	MANUFACTURER
TERMINALS		
6040/6042	Dasher terminal printer; 30, 60 cps	Data General
6052/6053	CRT display; 1920-character, 64- and 96-character set, switch-selectable speeds from 110 to 19.6K bps	Data General
6012	CRT display; 1920-character, variable codes, local editing, EIA or 20-ma current loop interface, full or half-duplex; up to 4800 bps	Data General
4010A	ASR-33 teletypewriter; 10 cps	Teletype

8560). As a minicomputer development system, the microNova is available in an 18-slot chassis with an ASR-33 teletypewriter (Model 9040), a DG Dasher terminal (Model 9043), or a teletypewriter modification kit for the user's choice of terminal (Model 9042).

Both the minicomputer systems and the minicomputer development systems (MDS) are available with a diskette subsystem. On the minicomputer, the user may elect either 157K words (315K bytes) in a single diskette drive or 315K words (630K bytes) on a dual diskette drive. The MDS is available with a dual diskette drive as standard equipment. The diskette subsystem includes a DMA controller.

The minicomputer prices start at $1,995 for the Model 8561 in a single-unit quantity. MDS prices start at $10,565, not including the 72-inch cabinet. Power fail/auto restart and real-time clocks are standard on both the minicomputer and MDS, whereas automatic program load, battery pack, hand-held programmer's console, and rack cabinet are optional on the minicomputer but standard on the MDS. Other standard features of the minicomputer and MDS are additional RAM and/or PROM memory up to 32K words, asynchronous interface boards, addressability for up to 61 peripherals, and up to 100 feet of external I/O bus. Optional features include the PROM programmer, 9-slot expansion chassis, card frames, extender cards, and device connector cables.

Nova 3/4 and 3/12 development systems are available for users who need more power in system development.

Beside the aforementioned support by a wide range of Nova software, the microNova has its own development software. This is a special package consisting of the Disc Operating System, Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. The software developed under DOS will run under DOS or RTOS (Real Time Operating System). Both DOS and RTOS are subsets of RDOS. DOS is most logically used for development only. For run-time control, RTOS should be used because of its small memory space requirements. DOS requires 16K words of RAM, versus only 4K words for RTOS.

CONTROL STORAGE: 0.5K, 1K, 2K, or 4K words of PROM (programmable read-only memory) are available for the microNova. Each size of PROM module is separately mounted on a memory board. A PROM programmer on its own board permits PROM chip burning under program control. The programmer acts directly on the PROM board and is inserted in the chassis only when needed.

REGISTERS: The microNova has four 16-bit accumulators and a 15-bit program counter. Two accumulators can be used for address indexing.

The microNova, like the Nova 3, has a last-in/first-out (LIFO) push-down/pop-up stack implemented in any 256 consecutive memory locations and two additional hardware registers (the stack pointer and the frame pointer). The stack pointer identifies the first memory location designed as the stack, and the frame pointer marks intra-stack boundaries to permit several "register saves" to be accumulated in the stack. The frame pointer can be set randomly to access words stored in stack frames without popping an entire frame.

Also, like the Nova 3, the microNova has 16 reserved memory locations which function as auto-increment or auto-decrement registers when addressed directly.

ADDRESSING MODES: The microNova has six addressing modes: direct (256 words), indirect (multi-level), indexed, indexed-indirect (pre-indexing), program-relative, and program relative-indirect.

INSTRUCTION REPERTOIRE: The basic complement includes four Jump and Modify Memory instructions, two Move Data instructions, 16 I/O instructions, and eight Arithmetic and Logic instructions. There are 256 variations on each of the Arithmetic and Logic instructions. Hardware multiply/divide instructions are standard.

INSTRUCTION TIMINGS: The timings shown are for full-word, fixed point operands, in *microseconds.*

Load/Store	**2.88**
Add/Subtract	**2.4**
Multiply/Divide	**41.28/59.04**
Jump	**2.88**

INTERRUPTS: A 16-level programmed priority interrupt facility is used to recognize interrupts for I/O operations. Each device is wired to one of 16 bus positions, and is either authorized or denied authorization to interrupt particular service routines by an Interrupt Disable Mask Bit that corresponds to the bus positions of the device.

PHYSICAL SPECIFICATIONS: The microNova in a minicomputer configuration is housed in a chassis of either 9 or 18 slots. The 9-slot chassis is 5.25 inches high, 19 inches wide, and 14.5 or 23 inches deep; the greater depth is with battery backup. The 18-slot chassis has the same height and

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In March 1977, DG announced DOS BASIC for the microNOVA. Originally announced for the Nova series minicomputers, the DOS BASIC interpreter became available in May 1977. DOS BASIC is a subset of RDOS Extended BASIC and is upward-compatible with both RDOS and AOS extended BASIC.

Then, in November 1977, Data General increased the capabilities of the microNova in data communications, data acquisition, process control, and peripheral control applications. The new hardware and software enhancements include interfaces to implement asynchronous and synchronous protocols and to expand the range of process control, instrumentation, and related I/O applications. In addition to support software for the new interfaces, Data General announced RJE80 and HASP II capabilities, a paper-tape software package, and a PROM utility program.

Data General sees three prime areas of application for the microNova; medical and instrumentation, data communications, and process control. The implementation of serial I/O (with its potential for cabling up to 100 feet and high noise immunity), the IOC chip, and the significant quantity of tested software are indicative of DG's intention to make this portent of future applications a reality.

USER REACTION

Datapro interviewed four users of the microNova minicomputers. All of them were OEM's, and they had collectively programmed and installed a total of 37 microNova systems. One installation employed dual microNova processors communicating with two Eclipse computers to monitor emergency medical services. The rest of the microNova: medical and instrumentation, data communications included small business systems configured with the 6053 CRT display, the 6040 Dasher terminal printer, dual floppy disk drives, and 20K of memory; data acquisition for a paper mill configured with the 4332 A/D Interface, dual floppies, and 28K of memory; optical scanning; and photo color control. Most of the installed systems were less than a year old.

The table below summarizes the responses to Datapro's survey.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	1	3	0	0	3.3
Reliability of mainframe	3	1	0	0	3.8
Reliability of peripherals	0	3	1	0	2.8
Responsiveness of maintenance service	2	1	1	0	3.3
Effectiveness of maintenance service	1	1	2	0	2.8
Technical support maintenance service	1	1	2	0	2.8
Technical support	1	1	2	0	2.8
Operating systems	1	3	0	0	3.3
Compilers and assemblers	2	2	0	0	3.5
Ease of programming	3	1	0	0	3.8
Ease of conversion	1	1	0	0	3.5
Overall satisfaction	3	1	0	0	3.8

*Weighted Average on a scale of 4.0 for Excellent.

width; its depth, with or without the battery pack, is 27.5 inches. A microNova development system complete with dual diskette subsystem will fit into a 72-inch cabinet.

Power requirements for all chassis types are 100, 120, 220, or 240 VAC ±10 percent, 47 to 63 Hz. Operating temperatures are 32 to 132 degrees F. A relative humidity of up to 90 percent, noncondensing, can be tolerated. The processor outputs 1023 BTU/hour maximum. Air conditioning requirements are those of a normal office environment.

The 9-slot chassis weighs approximately 37 pounds without battery backup. The 18-slot chassis weighs approximately 52 pounds without battery backup. Add 5 pounds to the chassis weight for battery backup for either chassis.

INPUT/OUTPUT CONTROL

INPUT/OUTPUT CHANNELS: An I/O bus and a Direct Memory Access (DMA) channel are standard.

The I/O bus is serial in structure and can be up to 100 feet long. Bipolar transceivers differentially drive the microNova serial I/O signal on a parallel two-line basis. This technique offers high noise immunity and ease of cabling.

The basic I/O bus is etched in the backplane. It functions to provide communication between mainframe-based I/O boards and the CPU board. The basic I/O bus is offered with a standard extension of 15 feet to connect the dual diskette subsystem. Longer extensions as discussed above are optional. Mainframe-based I/O boards are connected to free-standing peripherals by a 50-line device cable. Speed of the I/O bus is 16.6 megahertz, which translates to a data transfer rate of up to 1 million words per second.

The Input/Output Controller (IOC), a 40-pin chip located at each device interface, decodes the serial I/O signal and routes it into a parallel 16-line bidirectional data bus for I/O operations. This is the logical equivalent of the 47-line Nova I/O system. The IOC has the ability to address up to 61 I/O devices. The program I/O facility has six commands for each device. Also incorporated are controller start, clear, and I/O pulses and the facility for programmed I/O, program interrupt, and DMA functions.

For the DMA channel, rates are quoted as 148,000 words per second for input and 173,000 words per second for output. The DMA channel can be used to increment the contents of storage locations by 1.

CONFIGURATION RULES

The microNova can have up to 61 peripheral devices attached to the I/O bus. The processor chassis is available with either 9 or 18 slots. Expansion chassis are available in the 9-slot size only. The actual number of peripherals that can be attached depends upon the available number of slots and the method of attachment.

Generally speaking, all peripherals require one slot for direct attachment. The processor is mounted on one board along with either 2K or 4K words of memory, and requires one slot. The PROM programmer requires one slot, the Asynchronous Interface Board requires one slot, each General-Purpose I/O Board requires one slot, the Terminal Interface Board requires one slot, and the Programmer's Console Board requires one slot. A maximum of two diskette controllers (up to eight drives) can be attached.

MASS STORAGE

6038 FLOPPY DISC SUBSYSTEM: Consists of a four-drive controller and either a 6038 single drive or a 6039 dual drive. Each floppy disc stores up to 315K bytes on 77

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Overall satisfaction with the microNova was high. This is not too surprising, since all of the users were OEM's who had expertise with the microNova and Nova computers and were familiar with Data General's service. They had chosen the microNova to configure and sell for very practical reasons, and they rated the reliability of mainframe, ease of programming, and ease of conversion highly.

All of the OEM's had service contracts with Data General, although one had just obtained it and based his "fair" rating of maintenance effectiveness on a single call to the manufacturer. This user rated Data General's responsiveness to the call as excellent. One of the OEM's we spoke with voiced what seemed to be the consensus of opinion about Data General's maintenance and technical support by commenting on the overall advantage of Data General's microNova to the OEM: "Data General offers substantial discounts to the OEM on some of the best hardware deliverable today. In short, you get a powerful system, acceptable service, and a great price." He cited documentation as an area that needs improvement, as he considered it difficult for the first-time user.

Two of the OEM's mentioned that their programmers found it necessary to make numerous changes in the operating system. Both were implementing new applications, however, and both gave the final version of the operating system a "good" rating. "There is not enough time," one of them commented, "for the manufacturer to test the operating system in every situation." Two users also reported having initial difficulties with the dual floppy disk drive, but said that once it was up and running, it was reliable.

All of the users were basically satisfied with the microNova, and they all mentioned the performance/price ratio as significant. "It is not generally known," said one of the OEM's, "that these small machines is a low price range can do such an incredible amount of work."□

tracks. Maximum storage capacity is 1.26 million bytes on a four-drive subsystem. Average head positioning time is 260 milliseconds, and average rotational delay is 83 milliseconds. Data transfer rate is 31K bytes/second. The 6038 drives feature IBM 3740 compatibility and are supported by Data General's RDOS operating system. The controller occupies one slot. The 6038 drives are manufactured by Data General.

INPUT/OUTPUT UNITS

The Model 4222 Digital I/O Interface, Model 4223 A/D Interface, and Model 4224 D/A Interface each occupy a single microNova board. They plug directly into the microNova chassis and provide it with stand-alone data acquisition and control capabilities.

MODEL 4222 DIGITAL I/O INTERFACE: Provides a digital device interface for 16 parallel input and 16 parallel output lines. It also furnishes two strobe output lines and one strobe input line. All lines are TTL-compatible. An internal/external data comparator compares real-time external data against an internal software-programmable condition, allowing the system to detect transient deviations from the condition via polling or interrupts and selectively mask bits for interrupt requests.

MODEL 4223 A/D INTERFACE: Incorporates two 8-channel multiplexers, a differential input instrumentation amplifier, a sample-and-hold unit, and a 12-bit successive approximation converter. Its 16 single-ended or 8 differential inputs are program-configurable. Auto-channel scan (with wraparound capability) and triggering modes are also program-selectable. The A/O subsystem offers jumper-selectable input voltage ranges of 0 to 5, 0 to 10, or ±10V. According to the vendor, a complete conversion requires only 33 microseconds.

MODEL 4224 D/A INTERFACE: This dual-channel, 12-bit subsystem provides a user-selectable, full-scale output of 0 to 5, 0 to 10, ±5, or ±10V, and, according to the vendor, settles to ±0.01 percent full-scale of the desired output value in seven microseconds. Each channel's output range is individually set.

DG/DAC INTERFACE BOARD: Interfaces the microNova to sensors, actuators, and associated electrical circuits. Each DG/DAC chassis can accommodate up to 16 chassis control cards with up to 16 lines per card for a total of 256 signal lines per chassis. Any mix of digital and analog cards is allowed in one DG/DAC chassis, which measures 8.75 by 19 by 22 inches, weighs 60 pounds, and comes with power supply, bus terminator, and bus cables.

MODEL 4229 DATA CHANNEL INTERFACE: Disables the microNova clocks and disconnects control and data signals from the memory bus when an I/O throughput device requests fast service. It then handles all data transfer control and memory refresh, and periodically restarts the CPU to avoid errors due to internal node leakage. Maximum throughput is 1 million words per second in a burst mode, with a typical throughput of 830K words per second.

MODEL 4220 PAPER-TAPE READER INTERFACE: Controls the Data General Model 6013, a 400-cps, 8-channel paper-tape reader. Sharing this interface board is the Model 4220-B Nova-compatible real-time clock. Model 4220-B does not affect the operation of the microNova integral real-time clock, and users can select either during system generation. Model 4220-B offers AC line or crystal control line; 10, 100, or 1000 Hz frequencies; and a program interrupt for a time-of-day clock or interval timing.

MODEL 4221 LINE PRINTER INTERFACE: Controls the Data General Model 4034C or 4034D 165-cps, 132-column matrix printers or equivalent printers. This full ASCII interface includes paper-tape advance character recognition.

SENSOR ACCESS MANAGER (SAM): Provides software support for the 4222, 4223, and 4224 data acquisition and control boards, and for the DG/DAC interface. SAM is a library of device handlers and subroutines that control I/O transfers between user programs and analog and digital sensor devices. It is callable by FORTRAN IV and assembly language programs.

See the Peripherals/Terminals table for specifications of the terminals that can be used with the microNova.

COMMUNICATIONS CONTROL

ASYNCHRONOUS INTERFACE BOARD: Provides single-line connection of teleprinters and 6012 Video Displays to the I/O bus. Device codes are jumper-selectable. Transmission speeds are 50 to 19.2K bps. Interface levels for RS-232C and 20-ma DC current loop are provided. Also provided are variable character lengths of 5, 6, 7, or 8 bits; either 1, 1.5 or 2 stop bits; and even, odd, or no parity. A firmware-based (256 words) Console Debug Option allows any ASCII console to supervise program execution, and also allows for modification of RAM locations and CPU registers. Included with this option is a multi-device loader routine.

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GENERAL-PURPOSE INTERFACE BOARD: Provides a generalized programmed I/O, program interrupt, and DMA interface. An area on the board is pre-drilled and allocated for user-designed and built circuitry. Up to 35 IC's can be accommodated.

MODEL 4227 ASYNCHRONOUS LINE MULTIPLEXER: Controls up to four asynchronous communications lines. Each line can be configured for RS-232C or 20-ma current loop operation and individually programmed for number of bits per character (5 to 8), number of stop bits (1, 1.5, or 2), line speed (50 to 9600 bps), and parity (odd, even, or none). When enabled, parity is automatically checked/generated on each line. The multiplexer supports full- and half-duplex operation. The 4227 provides full character buffering on reception and transmission, program-controlled loopback testing, and modem control with automatic answer capabilities for Bell 103, 202, and 212 Series data sets.

MODEL 4426 SYNCHRONOUS LINE CONTROLLER: Interfaces to medium-speed (9600 bps) synchronous/bisynchronous communications lines, and provides a full- and half-duplex EIA RS-232C/CCITT V.24 interface and full character buffering on reception and transmission. When coupled with the optional Model 4228 hardware CRC generator, the synchronous line controller can select either of two standard check polynomials, CRC16 or CCITT16. Both idle and sync characters, as well as character size, parity, and loopback testing, are program-selectable. In receive mode, Model 4426 automatically synchronizes data and then strips out the sync character. Standard modem control is supplied for Bell 201, 203, 208, and 209 Series data sets. This synchronous controller also supports IBM Bisynch protocols with full transparency and is program code compatible with the SLM-2 Series synchronous multiplexer used on Data General Nova and Eclipse processors.

Up to four Model 4426 controllers can be configured with a single microNova minicomputer, allowing it to control a maximum of four synchronous lines. Only one CRC generator board is needed per system.

COMMUNICATIONS SOFTWARE

COMMUNICATIONS ACCESS MANAGER (CAM): A modular package that can be generated by the Communications System Generation Program (COMGEN) to include only those program segments required for each individual system. CAM operates under DOS and, since it uses the operating system's runtime-defined interrupt service, is brought into main memory from disc only as needed. This can free large segments of memory in a real-time communications system for other processing tasks.

CAM software can support both standard and special user-defined protocols, including Bisync (BSC) and an asynchronous terminal line procedure. Synchronous and asynchronous protocols can be intermixed. Multi-drop lines are supported through polling and selection sequences. Modem control support for auto answer/auto disconnect is a standard feature. CAM provides a queue for I/O completions that permits a single user task to control several asynchronous lines.

CAM also features a FORTRAN IV, FORTRAN V, or COBOL interface, permitting communications I/O in FORTRAN or COBOL programs.

REMOTE JOB ENTRY CONTROL PROGRAM (RJE80): Allows for remote job entry and communications between microNova processors and IBM 360/370 systems, or between microNova processors and other Data General computers. Support is provided for four types of RJE systems:

- Point-to-point communications between a Nova, Eclipse, or microNova emulating an IBM 2780/3780 and an IBM 360/370 host.
- Point-to-point communications between two Data General systems running RJE80.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with an IBM 360/370 host.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with a Nova or Eclipse or microNova master system also running RJE80.

RJE80 is supported by DOS as well as CAM. Features include horizontal and vertical printer format control; error detection on transmission and reception; and disc, tape, or card transmission to remote systems. Transmission between host systems may be to unattended RJE80 systems, and because of device-independent I/O capabilities, any combination of I/O devices can be utilized without additional software.

IBM HASP WORKSTATION EMULATOR: Lets a microNova emulate an IBM HASP remote job entry workstation. Its multileaving capability can include up to seven input and seven output data streams. Efficiency of data transmission is achieved through interleaving and data compression.

SOFTWARE

For all software specifications except DOS, DOS BASIC, and the special packages discussed below, see Report M11-304-101. Limitations on software use are predicated only on the memory size limitations of the microNova.

DISC OPERATING SYSTEM (DOS): A subset of RDOS, DOS is designed for use in development systems only. DOS requires a minimum of 16K words and includes a Command Line Interpreter, Text Editor, FORTRAN IV compiler, Macro Assembler, Library File Editor, and Relocatable Loader. Since DOS is a compatible subset of RDOS, any program developed under DOS can be run under RDOS or RTOS.

DOS BASIC: A subset of RDOS Extended BASIC, upward-compatible with both RDOS and AOS Extended BASIC. The interpreter takes advantage of operating system features by supporting device independence, and features extensions to the Dartmouth BASIC language. These extensions include string arithmetic, matrix operations, user-controlled output formatting, and sequential, random, and contiguous file management. DOS BASIC also offers several program development features and an assembly-language interface that allows subroutine calls. Both single- and multi-user versions of DOS BASIC have been released by Data General.

DOS BASIC implements string variables and literals, string concatenation, and string subsetting. Users can determine the location of a character within a string or the number of characters assigned to a string variable. They can also convert a numeric expression to a string that is its decimal representation, and return the decimal representation of a string variable or literal. In addition, READ and IF/THEN statements may employ strings. Matrix manipulation is achieved through a set of statements such as ADD, SUBTRACT, MULTIPLY, INVERT, and TRANSPOSE. Data General states that matrix dimensioning and redimensioning can easily be accomplished. Complete matrices can be read or written in a single I/O call.

The minimum hardware configuration for single-user DOS BASIC is any Nova computer, microNova computer, or

Data General microNova

microNova computer on a board with 16K words of main memory, a dual diskette drive and controller, and one terminal with appropriate interface. The minimum hardware configuration for multi-user DOS BASIC is any microNova with 32K words of main memory, a dual diskette drive and controller, and two terminals with appropriate interfaces. Additionally, a wide variety of peripherals can be supported on a Nova-based DOS BASIC system, including diskette drives, magnetic tape drives, line printer, paper tape reader and punch, plotter, and multiple terminals. A maximum of 32K words of main memory can be supported.

OTHER SOFTWARE: Along with the RJE80, HASP II, CAM, and SAM software packages discussed elsewhere in this report, Data General provides paper-tape software consisting of an editor, assembler, and debugger, designed to operate in 4K words of memory. In addition, there is a PROM utility program that operates under DOS. The program prechecks the PROM card, then accepts an absolute binary file, programs the PROM chips inserted in the Data General Model 8574 PROM programmer board, and performs a postcheck validity test. It also allows users to specify optional start and stop addresses, program 2K and 4K PROM boards, and print an octal dump. Errors are reported and automatically retried 256 times.

PRICING

POLICY: Data General offers the microNova series on a purchase-only basis, with two types of separately priced maintenance agreements: the On-Call Service contract and the Depot Service contract, which involves return of faulty equipment to a designated repair location. In either case, all parts and labor are included at no additional cost.

Normal prime-time on-call contract service hours are 9 a.m. to 5 p.m. Charges quoted in the price list are applicable to customers within 100 miles of a service center. Additional but uniform monthly charges are in effect beyond 100 miles of a Data General service center. These charges are $150 for customers between 100 and 300 miles from the center and $225 for customers beyond 300 miles.

Under a Depot Service contract, any portion of a system may be covered, the minimum contract being $75. The customer assumes all transportation and insurance costs. For non-contract on-site service, the hourly maintenance rates are $40 for prime time and $48 for other times. A three-hour minimum applies. Depot service hourly labor charges are $30 for prime time and $48 for all other times.

Prices shown are for single-unit quantities, OEM quantity discounts apply, and are available from Data General upon request.

Data General software is licensed so as to be included without charge on a system with sufficient Data General hardware to operate it. The software is also available for purchase for use on configurations utilizing other than Data General equipment (e.g., peripherals, add-on memory, etc.).

Data General provides training courses for customers at its Southboro, Massachusetts headquarters, at its Western Training Center in El Segundo, California, and at its United Kingdom Training Center in Greenford, Middlesex, England. A special five-day course, "Designing with microNova," covering hardware components design and maintenance, memory systems, instruction set, interfacing, configuration, and program development, is offered. In addition to the centers listed above, this course can be taught at customer locations by special arrangement. Two training credits are given for each development system purchased by an end user, which entitle the customer to approximately one man-week of training. Schedules for training courses can be obtained at any Data General field office.

Software and Hardware Subscription Services are available. They provide automatic updates, additions, and documentation for a fixed yearly fee.

The Data General Users' Group provides a forum for interchange of programs. The programs are available for a fee to cover reproduction and distribution costs.

TYPICAL MICRONOVA DEVELOPMENT SYSTEM: Includes an 18-slot chassis containing CPU/4K-word RAM board with automatic program load, real-time clock and power fail/auto restart; 8K-word RAM board; 4K-word RAM board; terminal interface board; programmer's console board; and power supply with battery backup. Also included are a dual-diskette subsystem with integral data channel controller, hand-held programmer's console, and ASR-33 teletypewriter. All components except the ASR-33 are packaged in a 72-inch cabinet. Purchase price is $12,115.■

EQUIPMENT PRICES

		Purchase Price
PROCESSORS		
8562	microNova on a board with 2K words of RAM	$ 800
8563	microNova on a board with 4K words of RAM	950
8560	microNova Minicomputer in 18-slot chassis with 4K words of RAM	2,595
8561	microNova Minicomputer in 9-slot chassis with 4K words of RAM	1,995
PACKAGED SYSTEMS		
9040 & 9040A	microNova Development System with ASR-33 Teletypewriter	12,115
9042 & 9042A	microNova Development System with Teletypewriter Modification Kit	10,565
9043 & 9043A	microNova Development System with 60-cps Dasher terminal	13,015
PROCESSOR OPTIONS		
8565	Automatic Program Load	150
8575	Edge-Mounted Controls Indicator	200
8564	Hand-Held Programmer's Console	700
8566	Battery Backup	300
MEMORY		
8572	Board with 4K words of RAM	600
8573	Board with 8K words of RAM	950
8567	Board with 0.5K words of PROM	300

Data General microNova

EQUIPMENT PRICES

		Purchase Price
MEMORY (Continued)		
8568	Board with 1K words of PROM	375
8569	Board with 2K words of PROM	500
8570	Board with 4K words of PROM	750
8574	PROM Programmer	1,650
MASS STORAGE		
6038	Single Diskette Drive Subsystem with controller	2,900
6039	Dual Diskette Subsystem with controller	3,900
1098A	Carton of Diskettes	120
TERMINALS		
6042-1	Dasher 30-char./second KSR printer terminal; 132 columns	2,400
6043-1	Receive-only version of 6042-1	2,200
6040-1	Dasher 60-char./second KSR printer terminal; 132 columns	2,650
6041-1	Receive-only version of 6040-1	2,450
6012-H	Video Display Terminal; 24 lines by 80 characters	2,700
6052-1	CRT with 64-character set, switch-selectable speed from 110 to 19.6K bps; 24-line by 80-character screen	1,990
6053-1	Same as 6052-1 with 96-character set	2,290
HARDWARE AND INTERFACES		
4207	Asynchronous Interface Board	250
4208	Console Debug option	200
4210	General-Purpose Interface Board	250
4211	GPIO Wirewrap Pins/Sockets	200
1114	Predrilled Circuit Card	200
2303A	Extender Card	200
1115A	Card Puller Tool	50
8571	I/O Expansion Chassis	1,600
4212	Card Frame Assembly	250
4213	Power Supply	750
4214	Power Supply/Battery Backup	1,050
4220-A	Paper Tape Reader Interface	400
4220-B	Real-Time Clock	350
4220-A/4220-B	Combined Board	700
4221	Line Printer Interface	650
4222	Digital I/O Interface	400
4223	A/D Interface	1,150
4224	D/A Interface	800
4226	Synchronous Line Controller	400
4227	Asynchronous Line Multiplexer	500
4228	CRC Generator	250

CHIP PRICES (OEM only)

		PRICE RANGE			
		Quantity	Purchase Price	Quantity	Purchase Price
CHIPS					
mN601	CPU	1	$225	500	$95
mN603	IOC	1	100	500	60
mN606	4K words RAM	16	24	8,000	10
mN629	CPU 10X	1	60	500	25
mN636	IUC 10X	1	14	500	8
mN634	OCT MBX	2	20	1,000	8
mN633	OCT MAD	2	20	1,000	8
mN506	QUAD SA BD	4	24	2,000	10
1116A	Twelve 1K PROM chips	1	100	—	—
1117A	Twelve 2K PROM chips	1	250	—	—
CHIP SETS					
8563A	CPU with 4K words of RAM	1	900		
4210	General-Purpose Interface Chip Set	1	200		