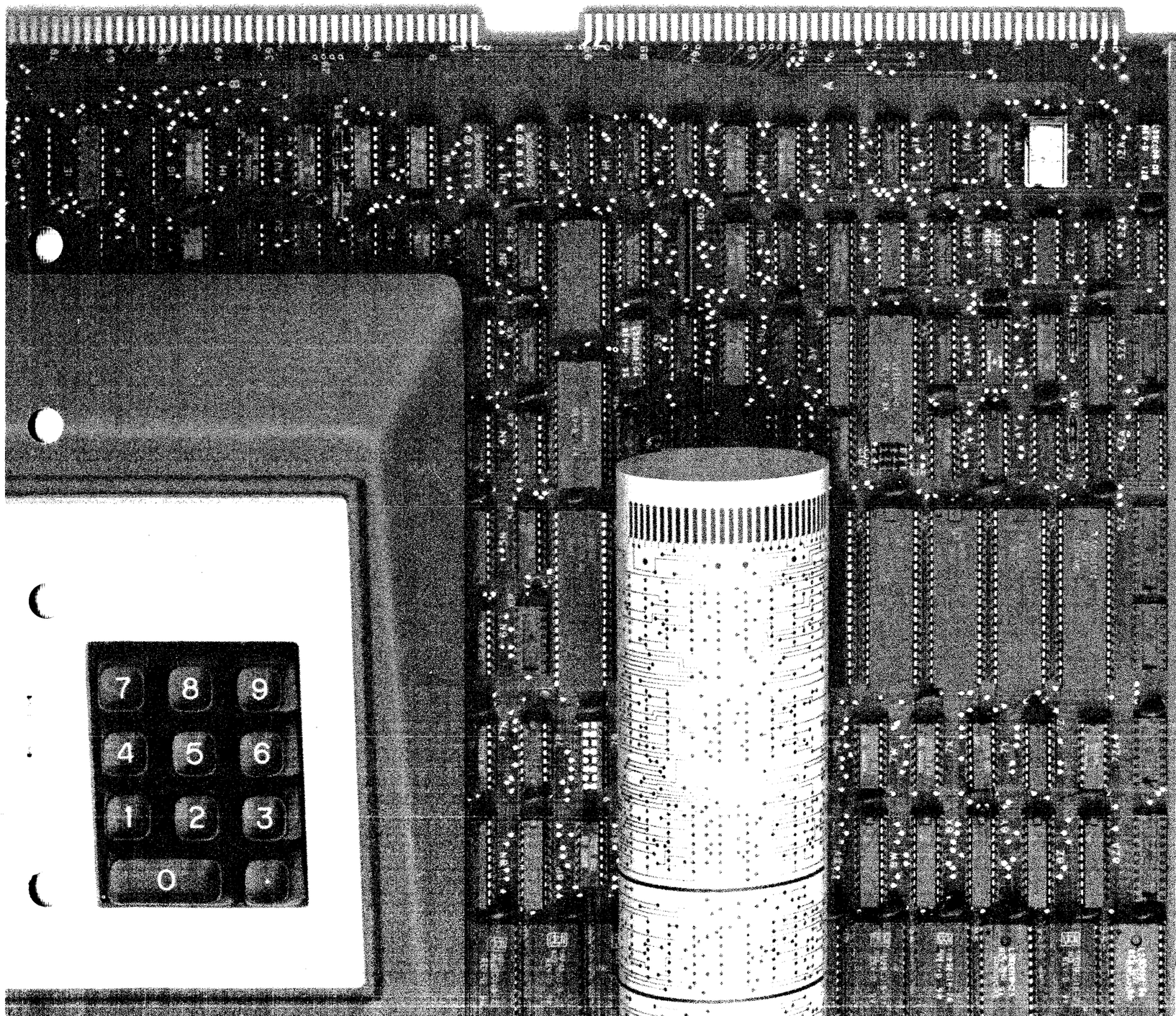
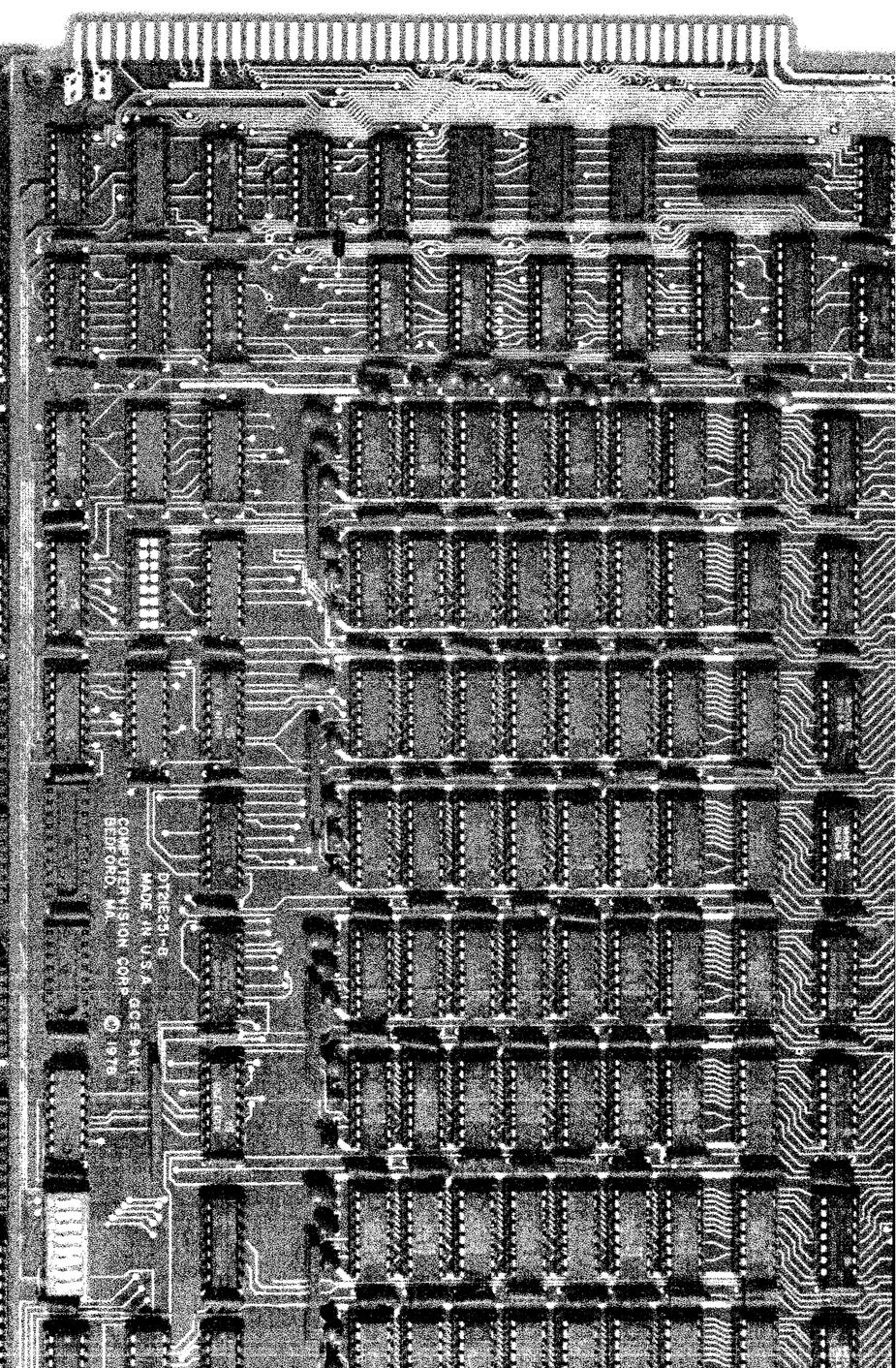
COMPUTERVISION

Technical

Programmable Communications Unit (PCU)

Logic Diagrams





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Programmable Communications Unit (PCU)

Logic Diagrams

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Order No. 001-00540-003

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SELD
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(BI DIRECTIONAL)
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IORQ
RD
WR
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ZRESET
MRESET
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A11B-A13B
ADDR DEC.
CS
BLK32
MEMRD
MEMORY DATA BUFFER
MCLK
CLKEN
SYSTEM CLOCK AND DIVIDER CKT. (7.3728 MHz)
3.686 MHz
1.843 MHz
SYSCLK
LEDIND
D0B-D7B
WRB
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LED'S
A
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WRPRTBTS
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SELB
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B
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EP10INT-20INT
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DSEL5
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IDATA7
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CLEAR
START
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CLRZBS
Z80 BUSY/ DONE
Z80INTR
RQENB/H
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SEL
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FIFO
SETPTS
CLRZBS
SETZBS
SETZDN
CLRRSTR
CLRERR
RSTDCH
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+5V
DS13
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RXDA,DCDA
SIO (Z80)
INT
RXDAEIAO
RCVCLKO
XMTCLKO
EXTXMTCLK0
CLRTOSENDO
RINGINDO
CARRIERDET
TXDAEIAO
REQTOSEND
WAIT/READY
PC (PORT0)
CONNECTOR
RXDAEIA1
RCVCLK1
XMTCLK1
CLRTOSEND1
RINGIND1
CARRIERDET
TXDAEIA1
EXTXMTCLK1
REQTOSEND
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DATATMNLRDYB
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CECTC
IORQB
RD
MIB
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A0B
A1B
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INT
CLKTRG0
CLKTRG1
CLKTRG2
CLKTRG3
FF
FF
D0-D7
ZRESET
RDB
MIB
IORQB
TXDB,RTSB
DS9
LED
+5V
DS10
LED
RXDB,DCDB
CTCCLK0
CTCCLK1
CTCCLK2
AOB
A1B
SYSCLK
D4B-D7B
SETPTS
SIO PORT LOOPBACK CONTROL LATCH
PORT0
DS14
+5V
DS11
PORT1

Programmable Communications Unit Simplified Block Diagram

Programmable Communications Unit
(New)
DS14E682

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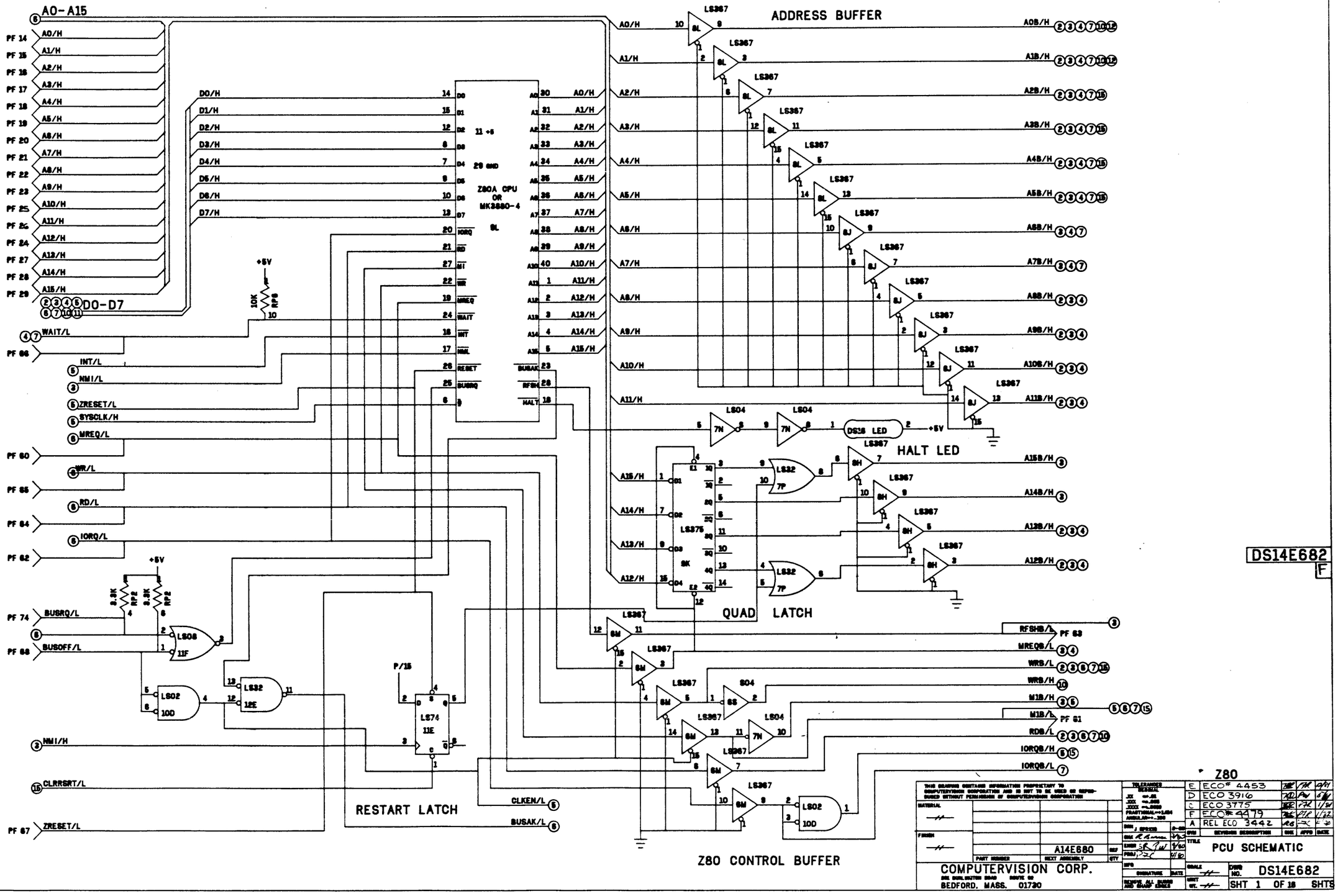

ADDRESS BUFFER
HALT LED
QUAD LATCH
RESTART LATCH
Z80 CONTROL BUFFER
Z80A CPU OR MK3880-4
A0-A15
D0-D7
DS14E682
F
Z80
E ECO# 4453
D ECO 3916
C ECO 3775
F ECO# 4479
A REL ECO 3442
PCU SCHEMATIC
DWG NO. DS14E682
SHT 1 OF 16 SHTS
A14E680
COMPUTERVISION CORP.
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A1B-A4B
RAMA0-RAMA3
D0B-D7B
Z80 ODD ADR
Z80 EVEN ADR
WRB/L
P/10
+5V
8.2K R10
OE-A/L
LS10 5P
CGP LATCH ENABLE
A9B/H
BLK32/L
A5B/H
A6B+A7B/H
A8B/H
A9B/H
A10B/H
A11B/H
A12B/H
A13B/H
RDB/L
LS27 6N
LS10 5P
ADR DECODER
LS04 7N
LS32 5N
LS04 4S
IORAMEN/H
IORAMEN/L
TTL IORAMEN/L PF 11
D0-D7
ODATA0-ODATA15
5K
5L
7K
7L
29706
+5V
GND
CGP LATCH ENABLE
TWO PORT RAM
DS14E682
F
SEE SHEET 1
PCU SCHEMATIC
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DWG NO. DS14E682
SHT 2 OF 18 SHTS

WRB/L
A3B/H
A10B/H
A2B/H
A9B/H
A1B/H
A8B/H
A0B/H
A7B/H
LS257A
6F
RAM MUX
LOGIC 0=A
INPUTS
4116
5E
5D
5C
6E
6D
MD0/H
MD7/H
MD6/H
MD5/H
MD4/H
MD3/H
MD2/H
MD1/H
S280
8F
PARITY CHECKER
MD0-MD7
A6B/H
A13B/H
A4B/H
A11B/H
A5B/H
A12B/H
P/5
7F
6C
7E
7D
7C
D0B/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
D6B/H
D7B/H
8E
PARITY GENERATOR
S32
8C
DELAY
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
D0-D7
RDB/L
A15B/H
A14B/H
LS138
8D
MEMORY BLOCK
DECODER
BLK0/L
BLK32/L
BLK16/L
LS08
9D
LS02
10D
PF 58
BLK0016/L
LS10
11C
IORAMEN/L
2.2K
RB1
+5V
MEMRD/L
NMI/L
NMI/H
LS74
9C
LS367
8G
DS15 LED
NMI LATCH
RP2
PF56
ENBLK16/L
PF 12
16K RAM
BLOCK 0
P/1
P/3
LS04
7N
MREQB/L
SYSCLK/H
RFSHB/L
M1B/H
10C
MEMORY
REFRESH
8.2K
RB0
RP1
CLRERR/L
ZRESET/L
LS132
12C
DS14E682
F
SEE SHEET 1
PCU SCHEMATIC
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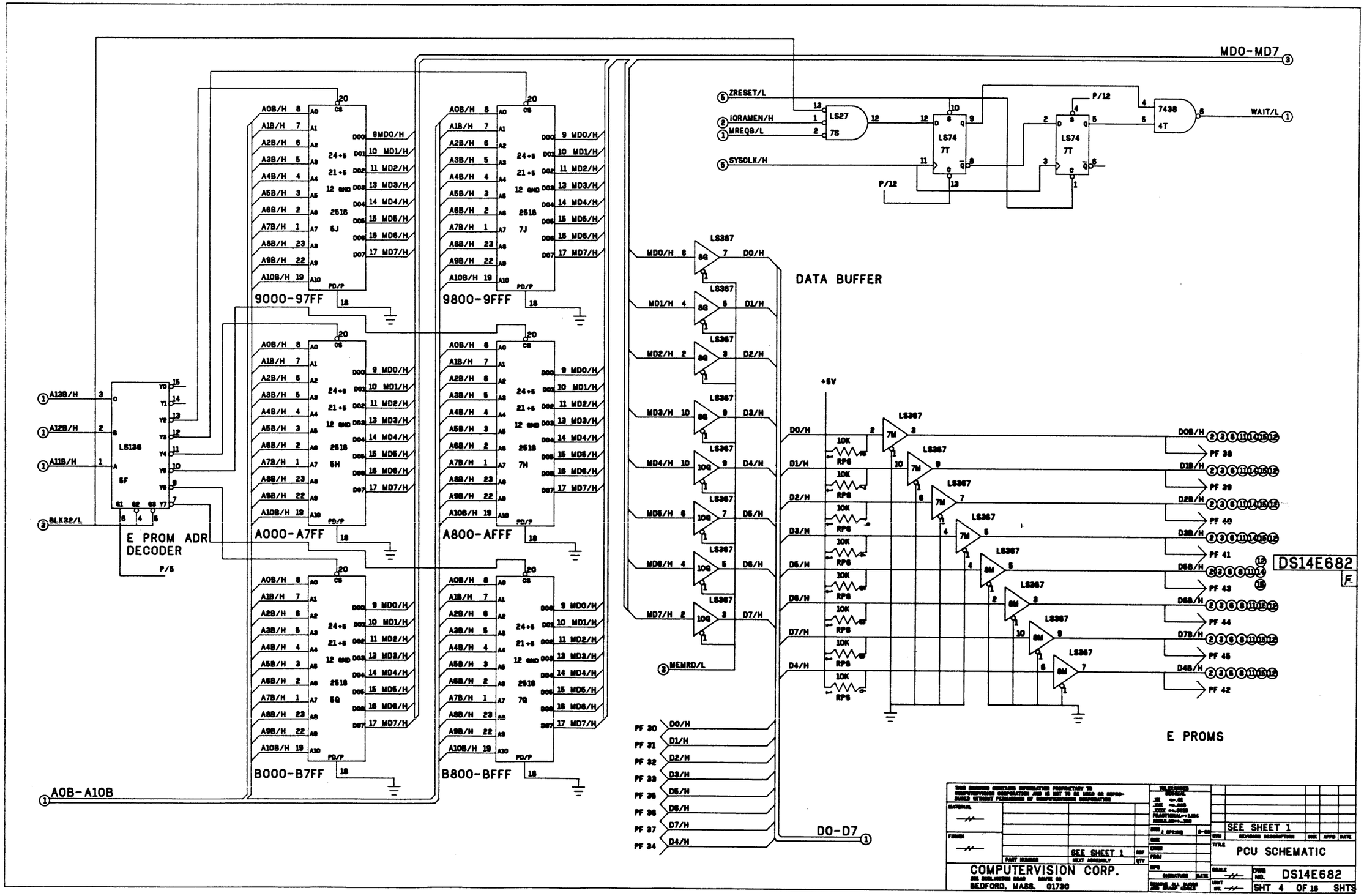
SHT 3 OF 18 SHTS


MD0-MD7
ZRESET/L
IORAMEN/H
MREQB/L
SYSCLK/H
LS27
7S
LS74
7T
7438
4T
WAIT/L
P/12
9000-97FF
9800-9FFF
A000-A7FF
A800-AFFF
B000-B7FF
B800-BFFF
LS138
5F
E PROM ADR DECODER
P/5
A13B/H
A12B/H
A11B/H
BLK32/L
A0B-A10B
LS367
DATA BUFFER
MEMRD/L
+5V
10K
RP6
DS14E682
E PROMS
D0-D7
SEE SHEET 1
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DWG NO. DS14E682
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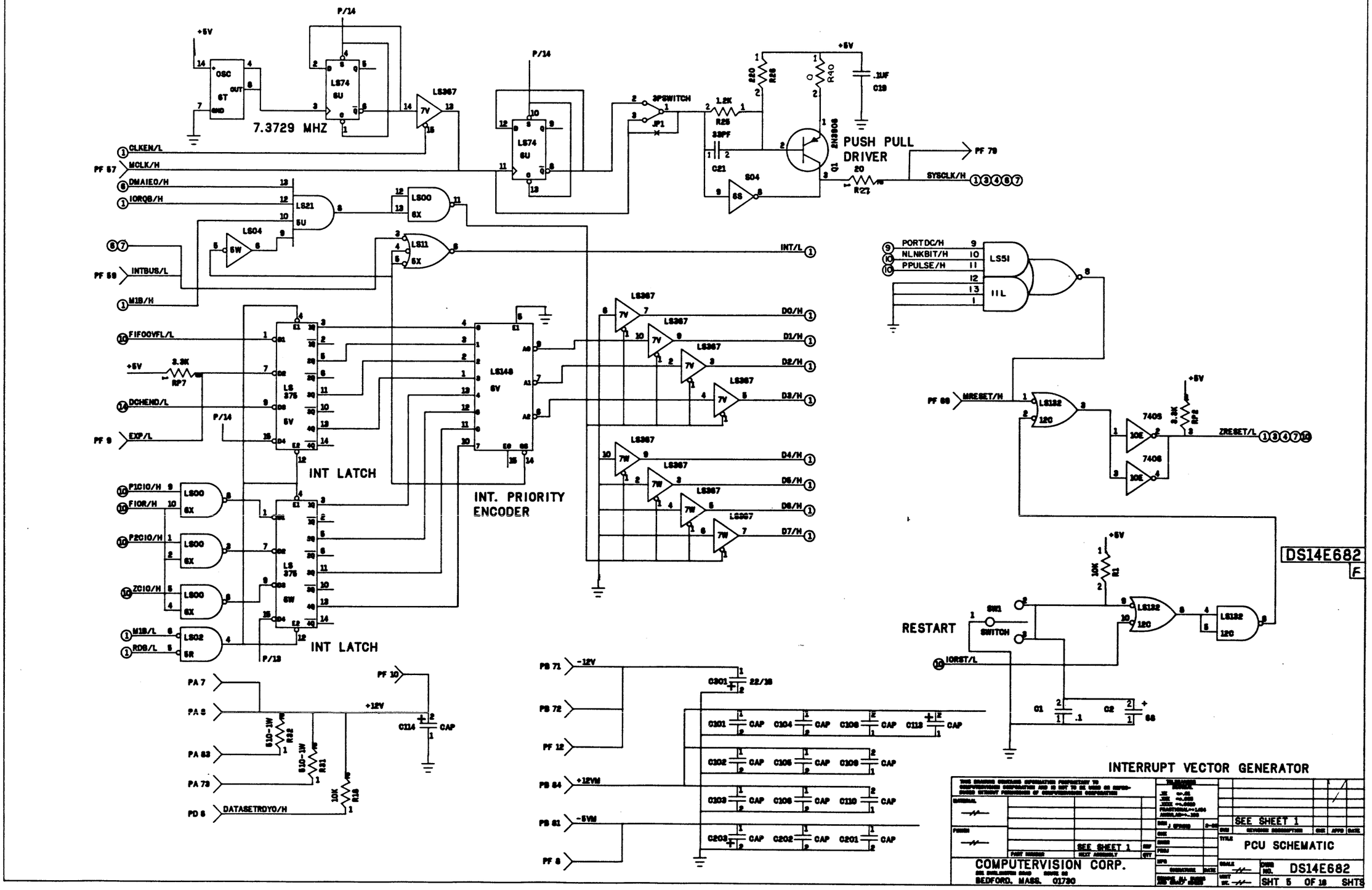
7.3729 MHZ
PUSH PULL DRIVER
INT LATCH
INT. PRIORITY ENCODER
INT LATCH
RESTART
INTERRUPT VECTOR GENERATOR
DS14E682
F
SEE SHEET 1
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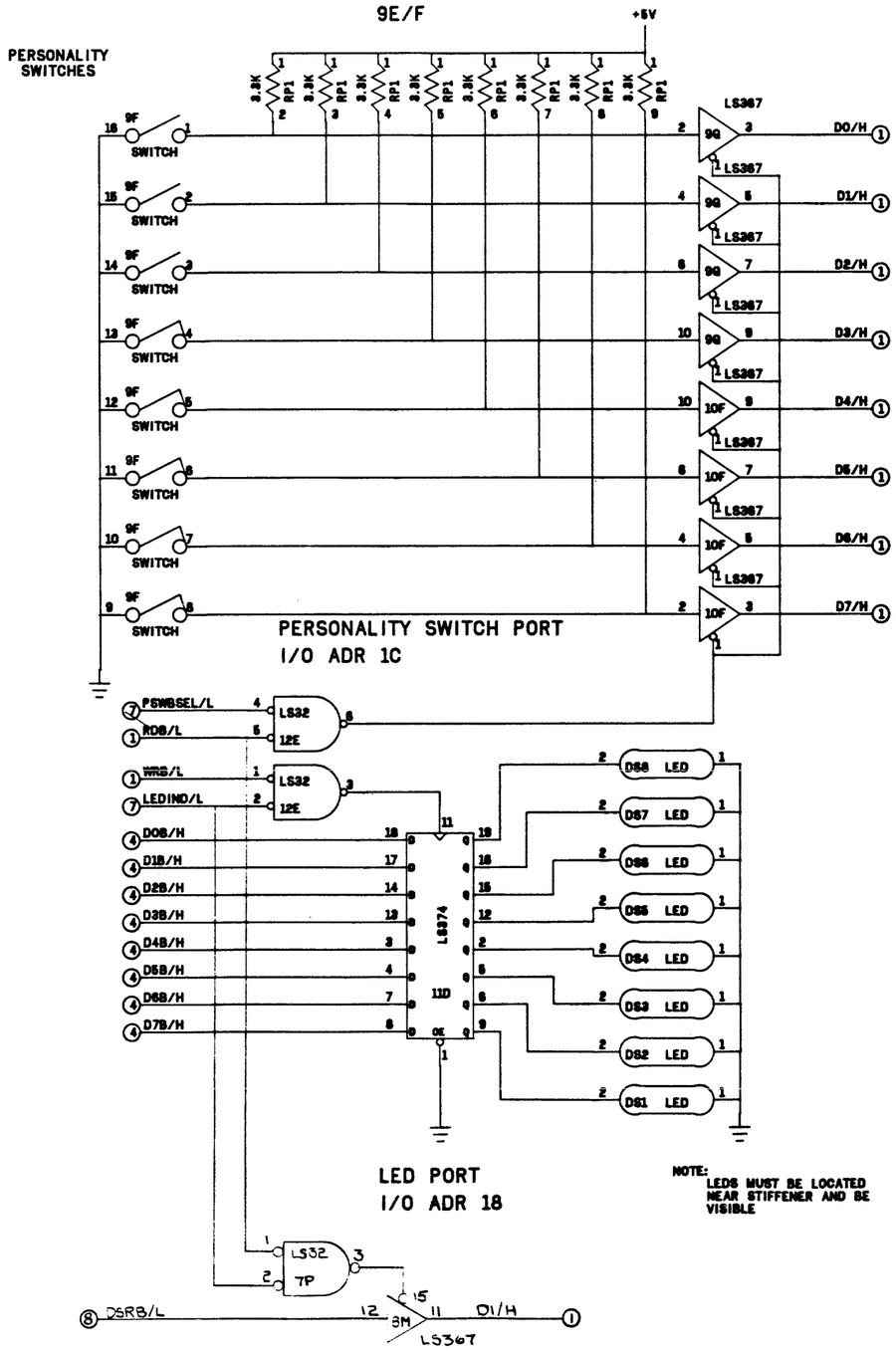
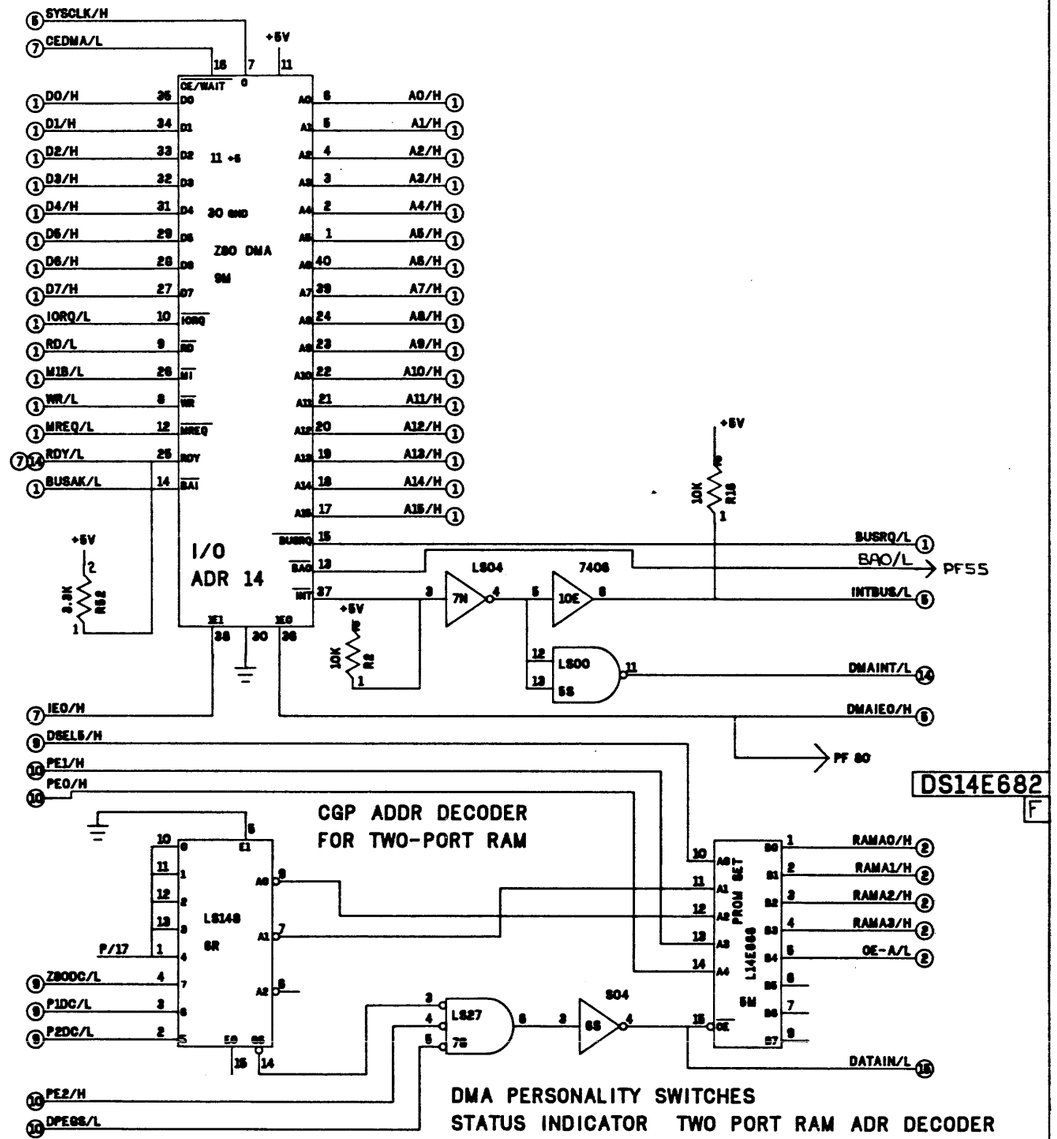
SHT 5 OF 18 SHTS





DS14E682

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PCU SCHEMATIC

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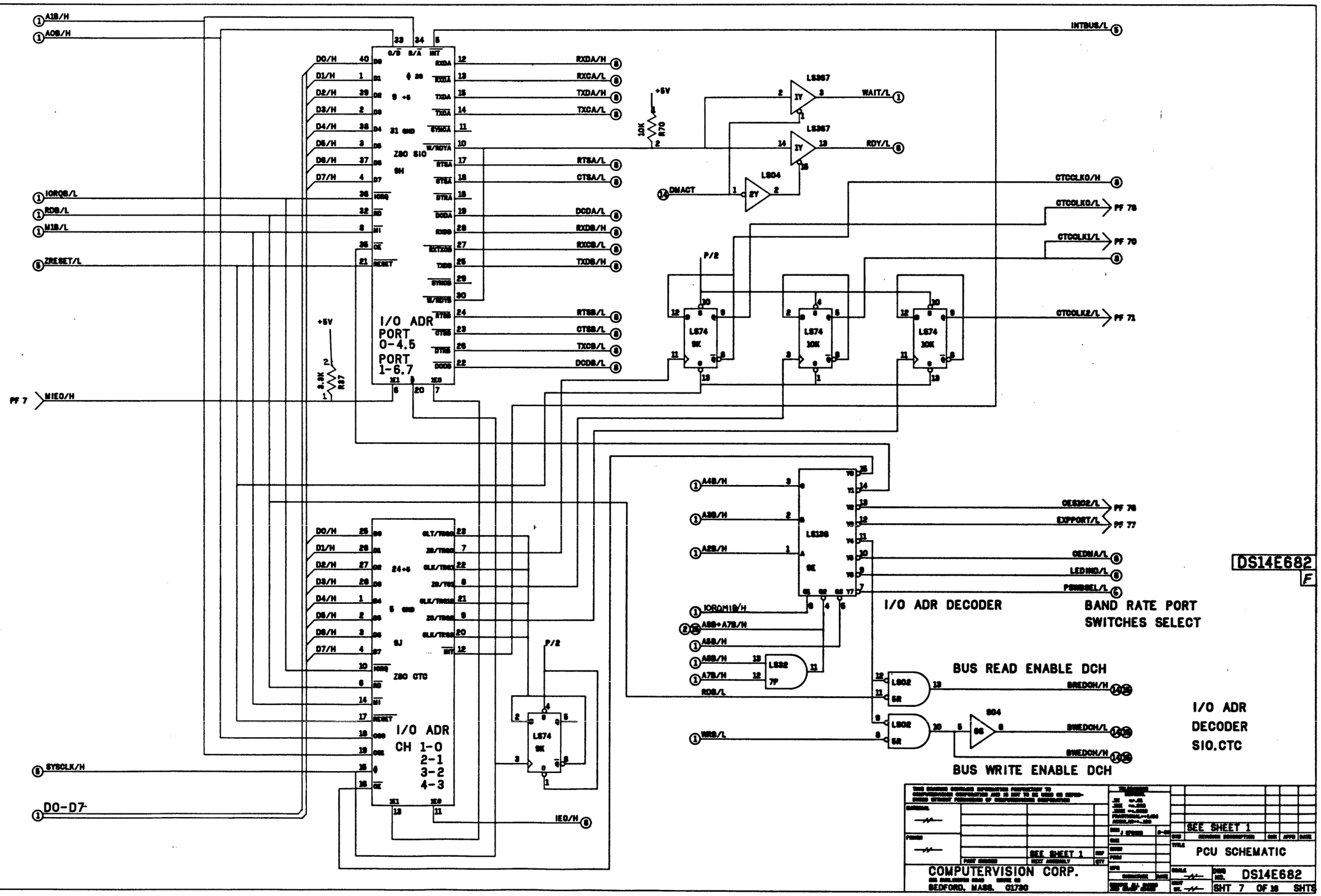
DWG NO. DS14E682

SHT 6 OF 16 SHTS



A1B/H
A0B/H
IORQB/L
RDB/L
M1B/L
ZRESET/L
PF 7
MIEO/H
SYSCLK/H
D0-D7
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80 SIO
9H
I/O ADR
PORT
0-4.5
PORT
1-6.7
RXDA/H
RXCA/L
TXDA/H
TXCA/L
RTSA/L
CTSA/L
DCDA/L
RXDB/H
RXCB/L
TXDB/H
RTSB/L
CTSB/L
TXCB/L
DCDB/L
+5V
10K
R70
LS367
WAIT/L
RDY/L
LS04
DMACT
INTBUS/L
CTCCLK0/H
CTCCLK0/L
PF 78
CTCCLK1/L
PF 70
CTCCLK2/L
PF 71
P/2
LS74
9K
10K
3.3K
R37
24+5
5 GND
9J
Z80 CTC
I/O ADR
CH 1-0
2-1
3-2
4-3
IEO/H
LS138
9E
A4B/H
A3B/H
A2B/H
IORQMIB/H
A8B+A7B/H
A5B/H
A6B/H
A7B/H
RDB/L
WRB/L
LS32
7P
LS02
5R
S04
8S
CES102/L
PF 76
EXPPORT/L
PF 77
CEDMA/L
LEDIND/L
PSWBSEL/L
I/O ADR DECODER
BAND RATE PORT
SWITCHES SELECT
BUS READ ENABLE DCH
BREDCH/H
BWEDCH/L
BWEDCH/H
BUS WRITE ENABLE DCH
I/O ADR
DECODER
SIO.CTC
DS14E682
F
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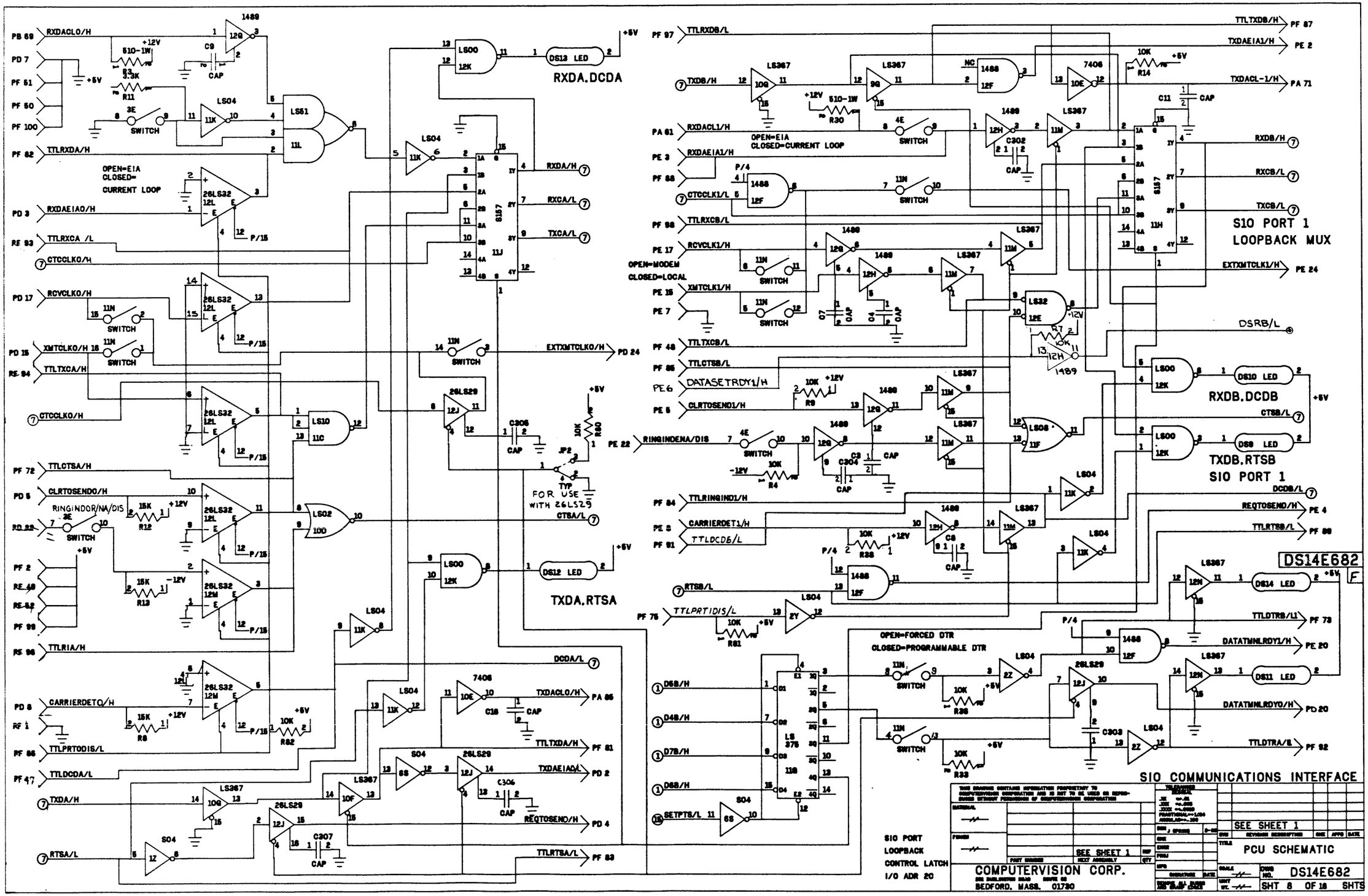
DS14E682
SHT 7 OF 18 SHTS


PB 69 RXDACLO/H
PD 7
PF 51
PF 50
PF 100
PF 82 TTLRXDA/H
PD 3 RXDAEIAO/H
RE 93 TTLRXCA /L
CTCCLKO/H
PD 17 RCVCLKO/H
PD 15 XMTCLKO/H
RE 94 TTLTXCA/H
CTCCLKO/H
PF 72 TTLCTSA/H
PD 5 CLRTOSENDO/H
PD 22 RINGINDOR/NA/DIS
PF 2
RE 48
RE 52
PF 99
RE 96 TTLRIA/H
PD 8 CARRIERDETO/H
RF 1
PF 86 TTLPRTODIS/L
PF 47 TTLDCDA/L
TXDA/H
RTSA/L
1489
510-1W
R3 3.3K
R11
SWITCH
CAP
C9
LS04
LS51
LS10
LS02
LS00
LS367
26LS32
26LS29
S157
OPEN=EIA
CLOSED=
CURRENT LOOP
P/15
RXDA/H
RXCA/L
TXCA/L
EXTXMTCLK0/H
PD 24
DS13 LED
RXDA.DCDA
TXDA.RTSA
DS12 LED
DS10 LED
DS8 LED
C306
C307
C308
C18
JP2
TYP
FOR USE
WITH 26LS29
CTSA/L
DCDA/L
TXDACLO/H
PA 86
TTLTXDA/H
PF 81
TXDAEIAO/L
PD 2
REQTOSEND/H
PD 4
TTLRTSA/H
PF 83
R82
R8
R12
R13
R60
PF 97 TTLRXDB/L
TXDB/H
PA 61 RXDACL1/H
PE 3 RXDAEIA1/H
PF 88
CTCCLK1/L
PF 98 TTLRXCB/L
PE 17 RCVCLK1/H
OPEN=MODEM
CLOSED=LOCAL
PE 15 XMTCLK1/H
PE 7
PF 48 TTLTXCB/L
PF 85 TTLCTSB/L
PE 6 DATASETRDY1/H
PE 5 CLRTOSEND1/H
PE 22 RINGINDENA/DIS
PF 84 TTLRINGIND1/H
PE 8 CARRIERDET1/H
PF 91 TTLDCDB/L
PF 76 TTLPRTIDIS/L
D5B/H
D4B/H
D7B/H
D6B/H
SETPTS/L 11
LS 378
R4
R9
R14
R30
R38
R81
R36
R33
R57
C11
C302
C303
C304
C305
C9
C8
P/4
OPEN=EIA
CLOSED=CURRENT LOOP
OPEN=FORCED DTR
CLOSED=PROGRAMMABLE DTR
TTLTXDB/H
PF 87
TXDAEIA1/H
PE 2
TXDACL-1/H
PA 71
RXDB/H
RXCB/L
TXCB/L
S10 PORT 1
LOOPBACK MUX
EXTXMTCLK1/H
PE 24
DSRB/L
RXDB.DCDB
CTSB/L
TXDB.RTSB
SIO PORT 1
DCDB/L
REQTOSEND/H
PE 4
TTLRTSB/L
PF 86
TTLDTRB/L1
PF 73
DATATMNLRDY1/H
PE 20
DATATMNLRDY0/H
PD 20
TTLDTRA/L
PF 92
SIO COMMUNICATIONS INTERFACE
SIO PORT
LOOPBACK
CONTROL LATCH
I/O ADR 2C
SEE SHEET 1
PCU SCHEMATIC
COMPUTERVISION CORP.
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DS14E682
SHT 8 OF 18 SHTS

DEVICE SELECT PCU

DEVICE SELECT PORT 1

CLOSE TO DISABLE PORT 0

CLOSE TO DISABLE PORT 1

DEVICE CODE LOGIC Z80 BUSY/DONE

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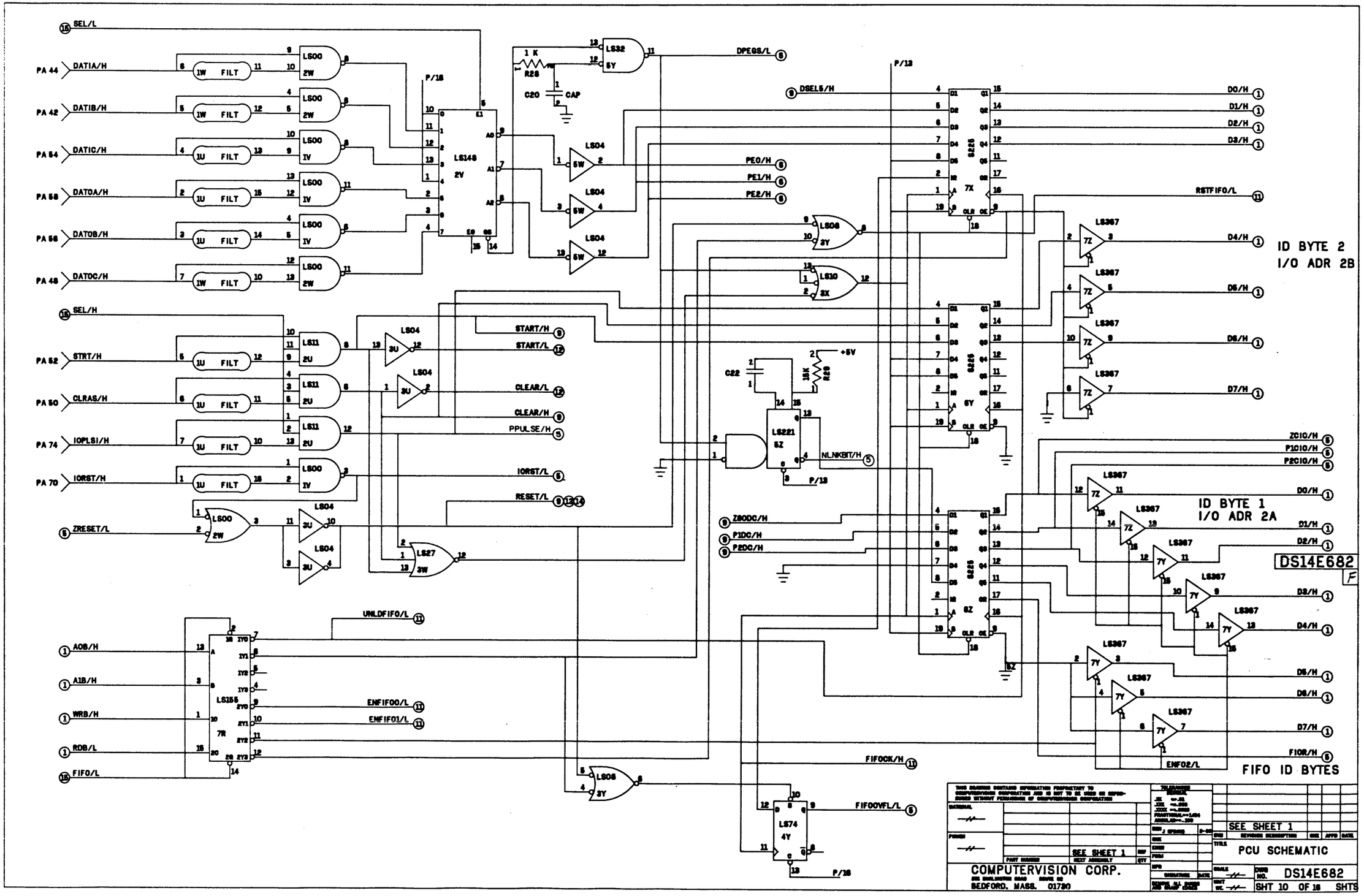
SEE SHEET 1

PCU SCHEMATIC

DS14E682

F

SHT 9 OF 18 SHTS



SEL/L
PA 44 DATIA/H
PA 42 DATIB/H
PA 54 DATIC/H
PA 58 DATOA/H
PA 56 DATOB/H
PA 48 DATOC/H
SEL/H
PA 52 STRT/H
PA 50 CLRAS/H
PA 74 IOPLSI/H
PA 70 IORST/H
ZRESET/L
A0B/H
A1B/H
WRB/H
RDB/L
FIFO/L
LS148 2V
LS155 7R
LS32 5Y
LS04 5W
LS08 3Y
LS10 3X
LS221 5Z
LS27 3W
LS74 4Y
LS367 7Z
LS367 7Y
S225 7X
S225 6Y
S225 8Z
DPEGS/L
DSEL5/H
PE0/H
PE1/H
PE2/H
START/H
START/L
CLEAR/L
CLEAR/H
PPULSE/H
IORST/L
RESET/L
UNLDFIFO/L
ENFIFO0/L
ENFIFO1/L
FIFOCK/H
FIFOOVFL/L
NLNKBIT/H
Z80DC/H
P1DC/H
P2DC/H
RSTFIFO/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
ZCIO/H
P1CIO/H
P2CIO/H
FIOR/H
ENFO2/L
ID BYTE 2
I/O ADR 2B
ID BYTE 1
I/O ADR 2A
DS14E682
FIFO ID BYTES
SEE SHEET 1
PCU SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DWG NO. DS14E682
SHT 10 OF 16 SHTS

FIFO BYTE 1
I/O ADR 28
(LOW ORDER)

FIFO
BYTE 2
I/O ADR 29
(HIGH ORDER)

CGP TO BUS
TRANSCEIVERS

DCHI DATA REGISTERS

DATA FIFO DCH REGISTERS

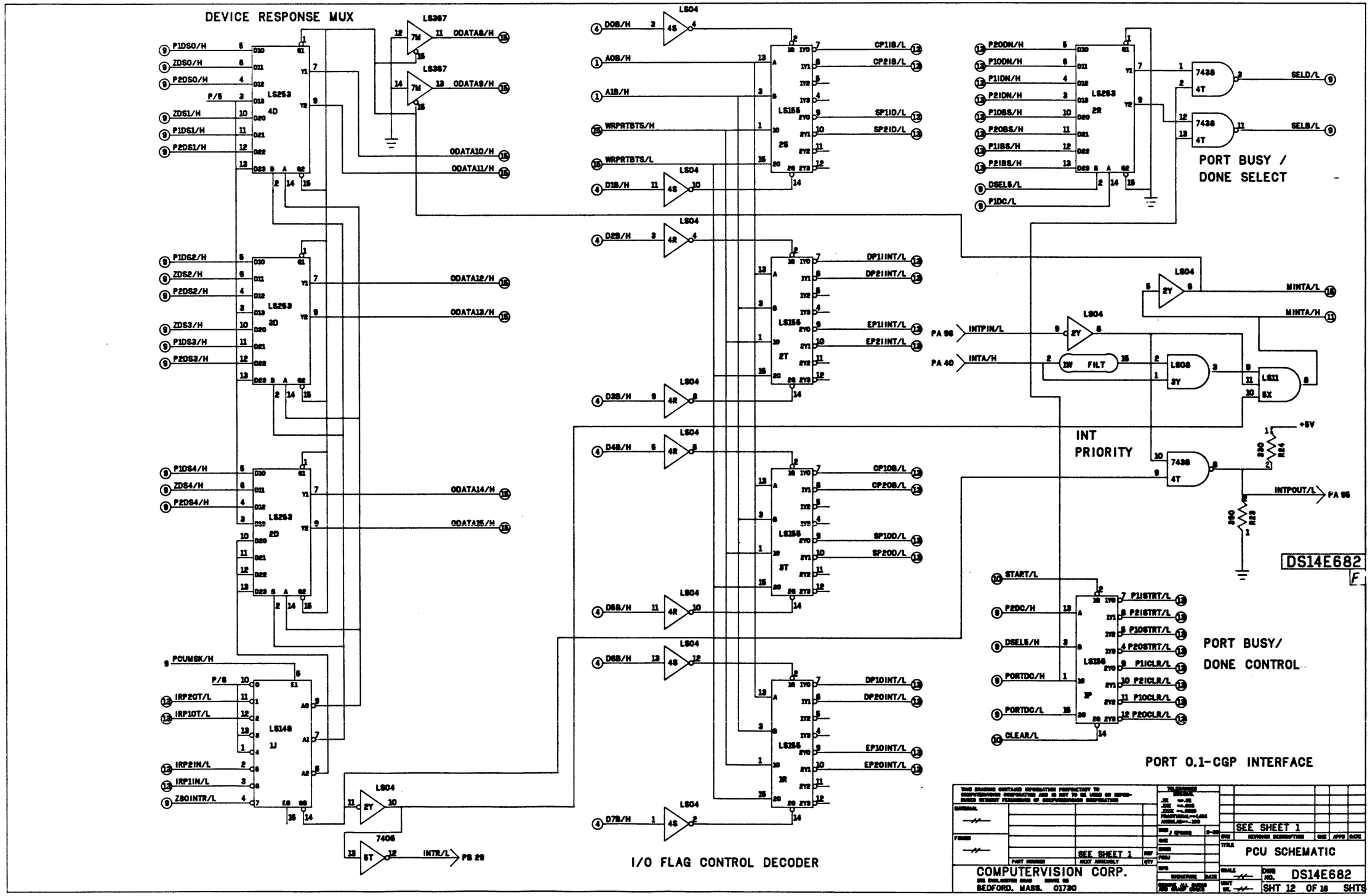
DS14E682
F

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

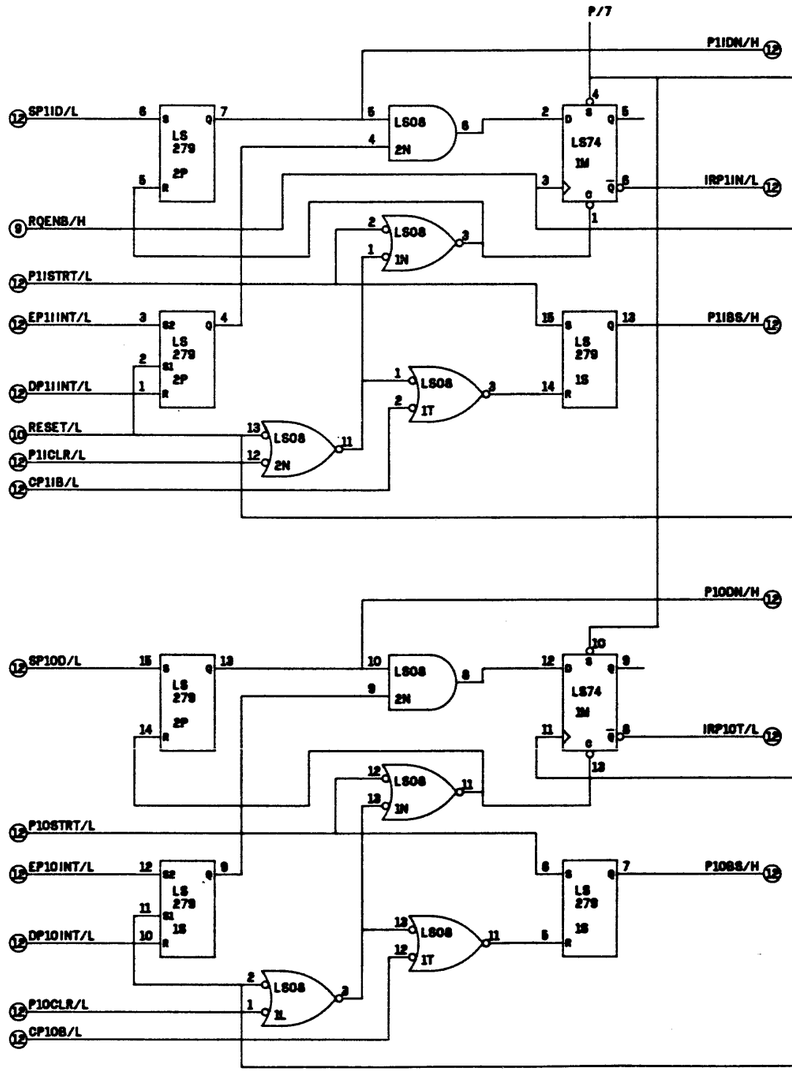
PCU SCHEMATIC

DWG NO. DS14E682

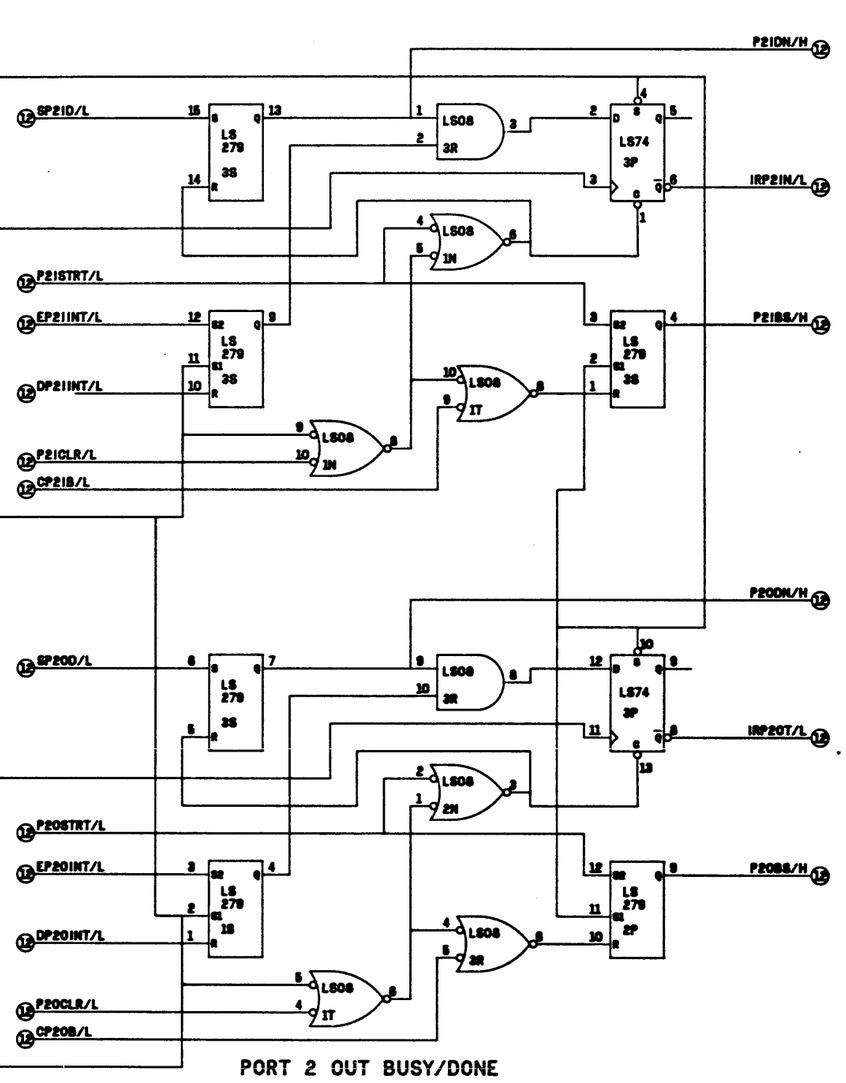
SHT 11 OF 18 SHTS


DEVICE RESPONSE MUX
PORT BUSY / DONE SELECT
INT PRIORITY
PORT BUSY/ DONE CONTROL
PORT 0.1-CGP INTERFACE
I/O FLAG CONTROL DECODER
DS14E682
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
PCU SCHEMATIC
SHT 12 OF 16 SHTS

PORT 0 IN BUSY/DONE



PORT 1 IN BUSY/DONE



PORT 2 OUT BUSY/DONE

PORT 0 OUT BUSY/DONE

PORT 0-1 BUSY/DONE

DS14E682
F

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MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

SEE SHEET 1

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

TOLERANCES UNLESS OTHERWISE SPECIFIED
.XX +-.01
.XXX +-.005
.XXXX +-.0050
FRACTIONAL +-1/64
ANGULAR +-.25

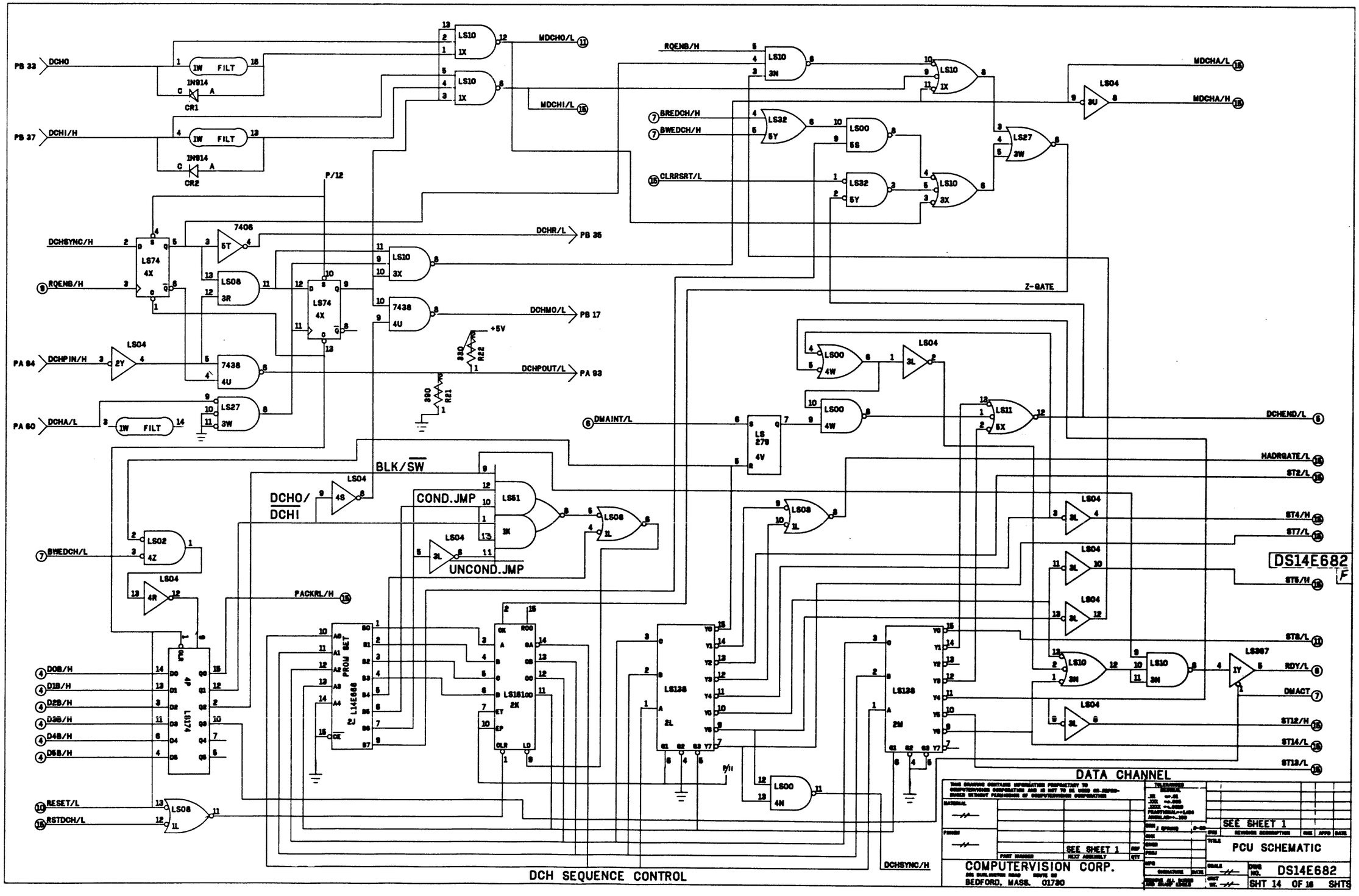
DRN J. SPENCE 2-82
CHK
ENGR
PROJ
APP
DATE

SEE SHEET 1

REV | REVISION DESCRIPTION | ENG | APPD | DATE

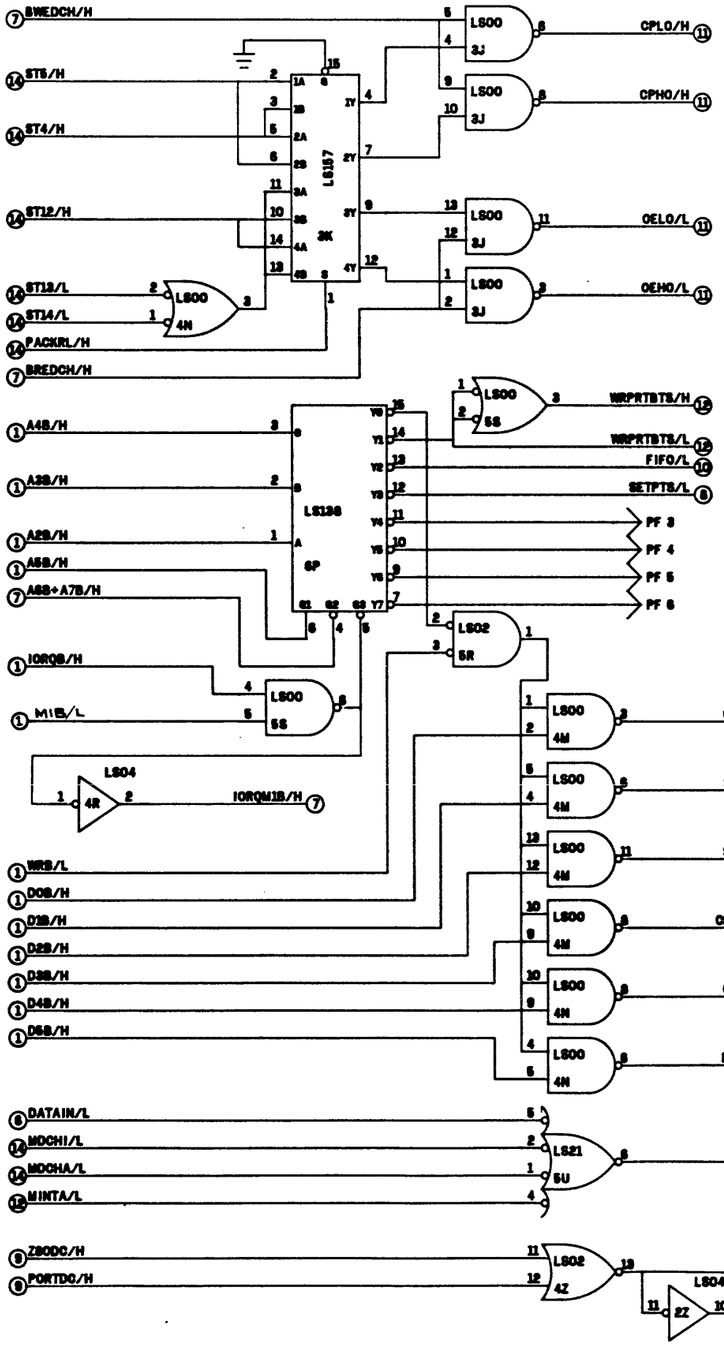
TITLE
PCU SCHEMATIC

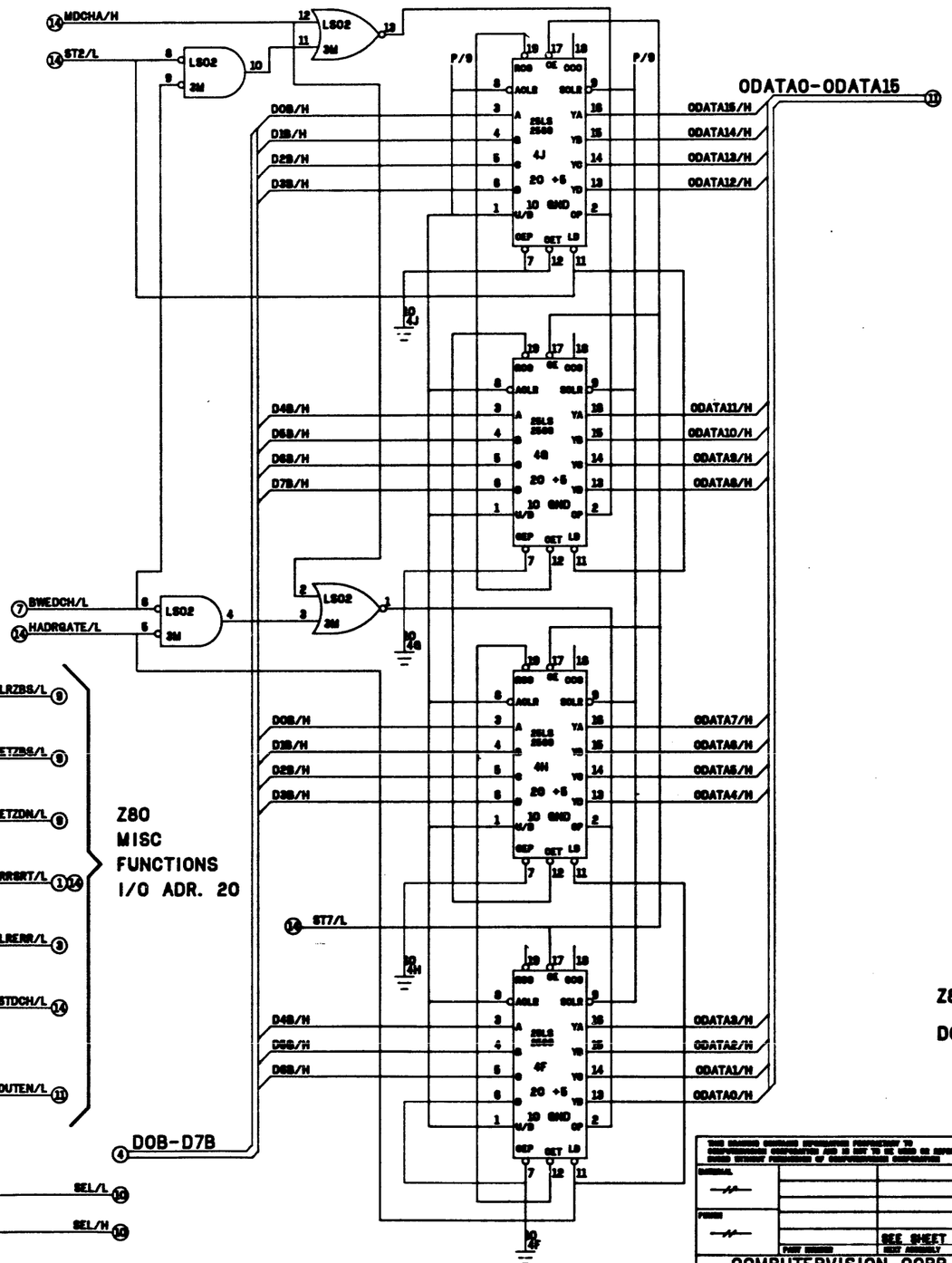
SCALE
DWG NO. DS14E682
SHT NO. SHT 13 OF 16 SHTS



PB 33 DCHO
PB 37 DCHI/H
MDCHO/L
MDCHI/L
RQENB/H
BREDCH/H
BWEDCH/H
CLRRSRT/L
MDCHA/L
MDCHA/H
DCHSYNC/H
RQENB/H
DCHR/L PB 35
DCHMO/L PB 17
DCHPIN/H
DCHPOUT/L PA 93
PA 94
PA 60 DCHA/L
Z-GATE
DMAINT/L
DCHEND/L
HADRGATE/L
ST2/L
ST4/H
ST7/L
ST5/H
ST8/L
RDY/L
DMACT
ST12/H
ST14/L
ST13/L
BLK/SW
DCHO/
DCHI
COND.JMP
UNCOND.JMP
BWEDCH/L
PACKRL/H
D0B/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
RESET/L
RSTDCH/L
DCHSYNC/H
DS14E682
DATA CHANNEL
DCH SEQUENCE CONTROL
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SEE SHEET 1
PCU SCHEMATIC
DS14E682
SHT 14 OF 16 SHTS

BYTE PACKING DIRECTION CONTROL





DS14E682
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Z80 MISC FUNCTIONS
DCH ADDER COUNTER

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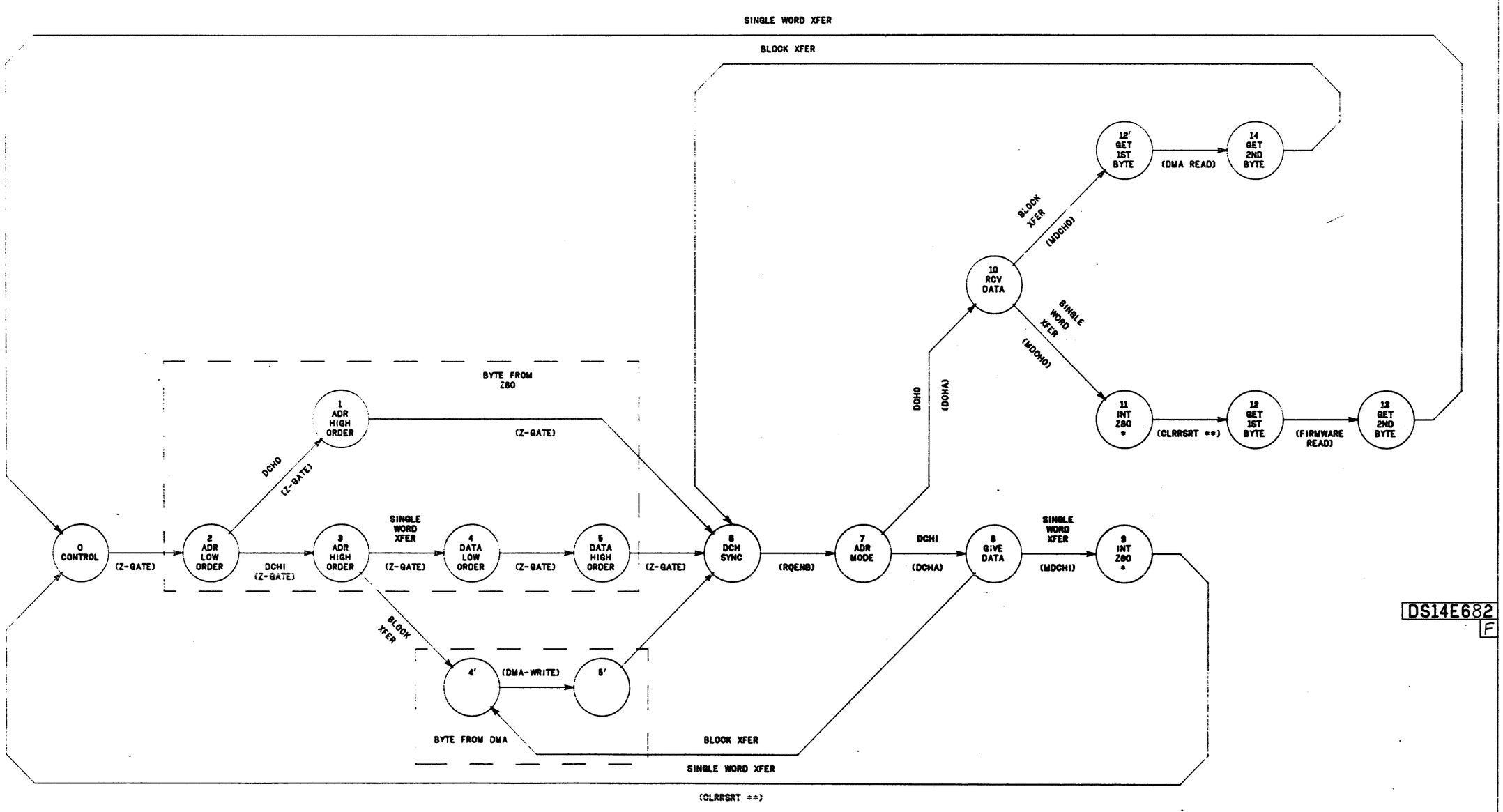
PCU SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DWG NO. DS14E682

SHT 15 OF 16 SHTS



DS14E682
F

* DCHEND INT

** CLEARS DCH INT

SIGNALS IN PARENTHESES CAUSE THE STATES TO ADVANCE.

DATA CHANNEL CONTROLLER STATE DIAGRAM

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MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES
DECIMAL
.XX =±.01
.XXX =±.005
.XXXX =±.0005
FRACTIONAL=±1/64
ANGULAR=±.100

DWG 0 HOURS 0-10
CHK
ENGR 0 DAYS 0-10
PROJ
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES

SYM | REVISION DESCRIPTION | CHK | APPD | DATE

TITLE P.C.U. SCHEMATIC DIAGRAM

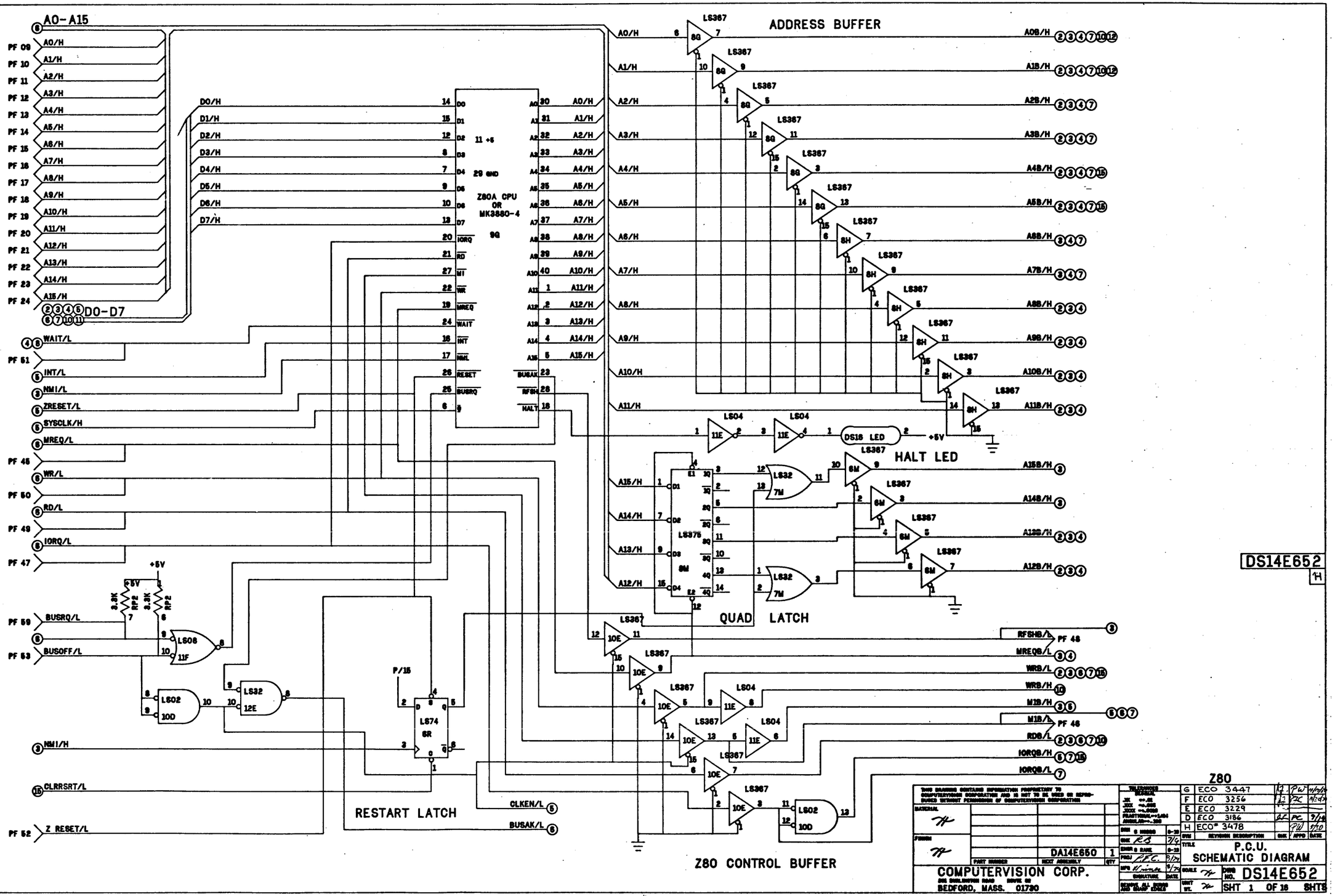
SCALE | DWG NO. DS14E682

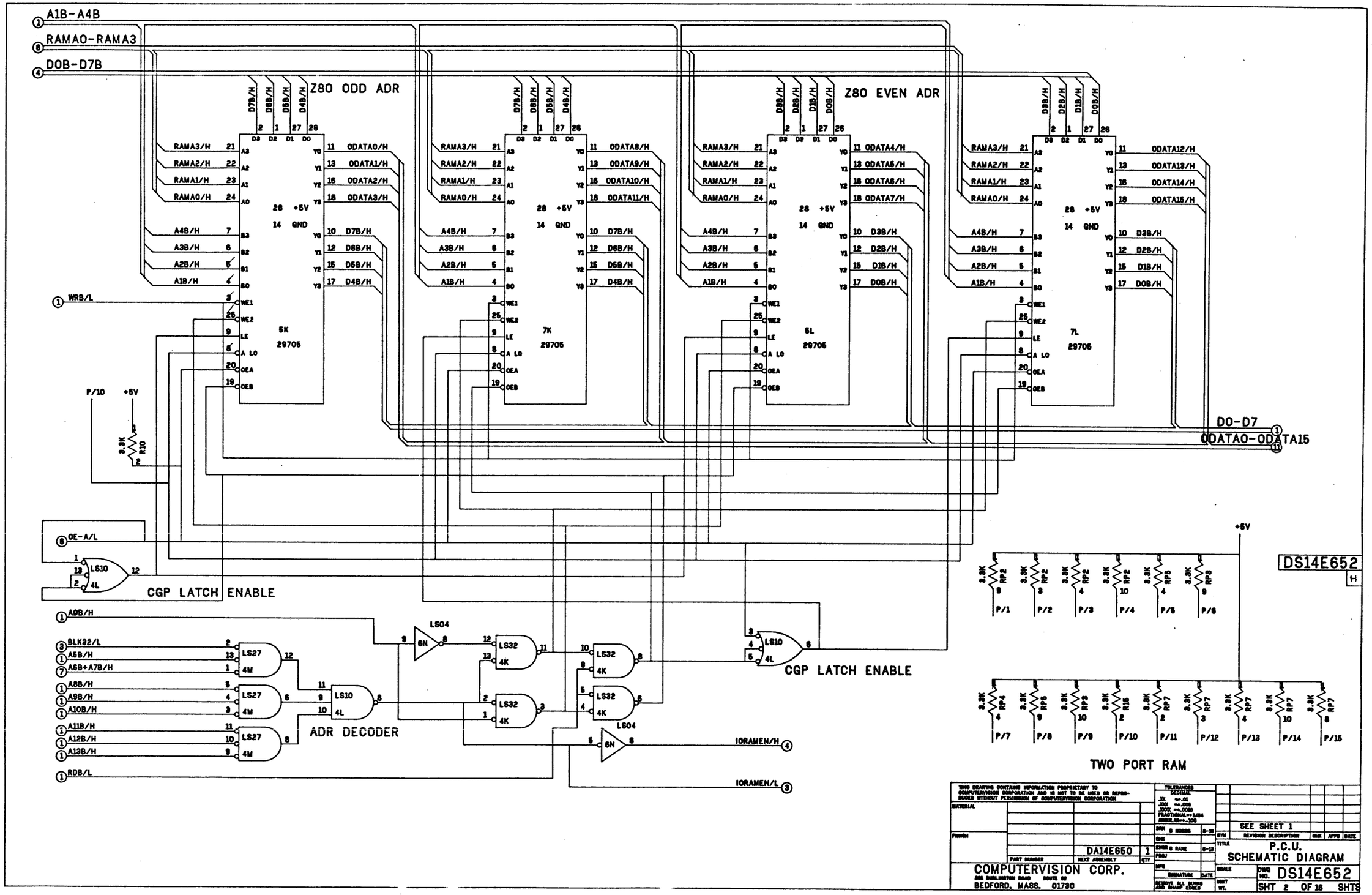
UNIT WT. | SHT 16 OF 16 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

Programmable Communications Unit
(Obsolete)
DS14E652

	Sheet No.
Z80 Circuits (Sheet 1 of 16)	2
Two Port RAM (Sheet 2 of 16)	3
16K RAM Block 0 (Sheet 3 of 16)	4
E PROMS (Sheet 4 of 16)	5
Interrupt Vector Generator (Sheet 5 of 16)	6
DMA Personality Switches, Status Indicator, Two Port RAM Address Decoder (Sheet 6 of 16)	7
I/O Address Decoder, SIO, CTC (Sheet 7 of 16)	8
SIO Communications Interface (Sheet 8 of 16)	9
Device Code Logic, Z80 Busy/Done (Sheet 9 of 16)	10
FIFO ID Bytes (Sheet 10 of 16)	11
Data FIFO, DCH Registers (Sheet 11 of 16)	12
Port 0 and 1 CGP Interface (Sheet 12 of 16)	13
Port 0 and 1 Busy/Done (Sheet 13 of 16)	14
Data Channel (Sheet 14 of 16)	15
Z80 Miscellaneous Functions, DCH Address Counter (Sheet 15 of 16)	16
Data Channel Controller State Diagram (Sheet 16 of 16)	17


A0-A15
PF 09
A0/H
PF 10
A1/H
PF 11
A2/H
PF 12
A3/H
PF 13
A4/H
PF 14
A5/H
PF 15
A6/H
PF 16
A7/H
PF 17
A8/H
PF 18
A9/H
PF 19
A10/H
PF 20
A11/H
PF 21
A12/H
PF 22
A13/H
PF 23
A14/H
PF 24
A15/H
D0-D7
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80A CPU
OR
MK3880-4
11 +5
29 GND
9Q
WAIT/L
PF 51
INT/L
NMI/L
RESET/L
SYSCLK/H
MREQ/L
PF 45
WR/L
PF 50
RD/L
PF 49
IORQ/L
PF 47
+5V
2.2K
RP2
BUSRQ/L
PF 59
BUSOFF/L
PF 53
LS08
11F
LS02
10D
LS32
12E
NMI/H
CLRRSRT/L
PF 52
Z RESET/L
P/15
LS74
6R
RESTART LATCH
CLKEN/L
BUSAK/L
ADDRESS BUFFER
LS367
8G
8H
A08/H
A18/H
A28/H
A38/H
A48/H
A58/H
A68/H
A78/H
A88/H
A98/H
A10B/H
A11B/H
LS04
11E
DS18 LED
HALT LED
A15B/H
A14B/H
A13B/H
A12B/H
LS375
8M
LS32
7M
QUAD LATCH
10E
RFSHB/L
PF 48
MREQB/L
WRB/L
WRB/H
M1B/H
M1B/L
RDB/L
IORQB/H
IORQB/L
LS02
10D
Z80 CONTROL BUFFER
DS14E652
H
Z80
P.C.U.
SCHEMATIC DIAGRAM
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
G ECO 3447
F ECO 3256
E ECO 3229
D ECO 3186
H ECO# 3478
SHT 1 OF 18 SHTS


A1B-A4B
RAMA0-RAMA3
D0B-D7B
Z80 ODD ADR
Z80 EVEN ADR
5K
29705
7K
29705
5L
29705
7L
29705
WRB/L
P/10
+5V
D0-D7
ODATA0-ODATA15
OE-A/L
CGP LATCH ENABLE
A9B/H
BLK32/L
A5B/H
A6B+A7B/H
A8B/H
A9B/H
A10B/H
A11B/H
A12B/H
A13B/H
RDB/L
ADR DECODER
IORAMEN/H
IORAMEN/L
CGP LATCH ENABLE
DS14E652
TWO PORT RAM
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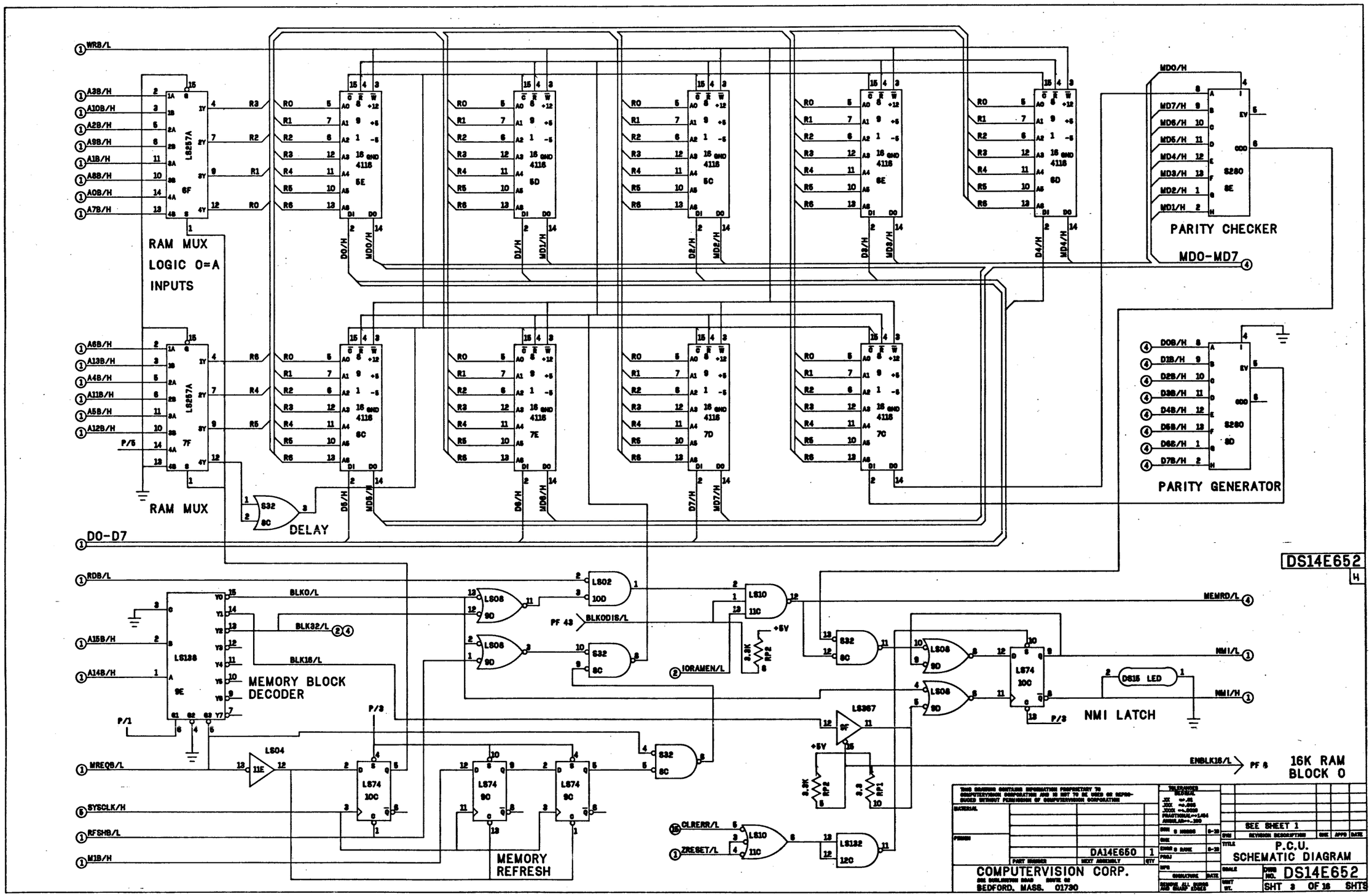
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 2 OF 16 SHTS



RAM MUX
LOGIC 0=A
INPUTS
RAM MUX
DELAY
PARITY CHECKER
MD0-MD7
PARITY GENERATOR
MEMORY BLOCK
DECODER
MEMORY
REFRESH
NMI LATCH
16K RAM
BLOCK 0
DS14E652
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DA14E650
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DS14E652
SHT 3 OF 16 SHTS

MD0-MD7 (3)

ZRESET/L (6)
IORAMEN/H (2)
MREQB/L (1)
SYSCLK/H (6)
LS27 5T
LS74 3S
P/12
7438 3R
WAIT/L (1)

DATA BUFFER

LS367 8J
MD0/H 2 — D0/H
MD1/H 4 — D1/H
MD2/H 6 — D2/H
MD3/H 10 — D3/H
MD4/H 12 — D4/H
MD5/H 14 — D5/H
MD6/H 12 — D6/H
MD7/H 14 — D7/H
(3) MEMRD/L

+5V
10K RPS
LS367 8L
D0/H … D7/H → D0B/H … D7B/H (2 3 8 11 14 15 12)

PF 25 D0/H
PF 26 D1/H
PF 27 D2/H
PF 28 D3/H
PF 30 D5/H
PF 31 D6/H
PF 32 D7/H
PF 29 D4/H
PF 33 … PF 40
D0-D7 (1)

E PROMS

9000-97FF 5J
9800-9FFF 7J
A000-A7FF 5H
A800-AFFF 7H
B000-B7FF 5G
B800-BFFF 7G

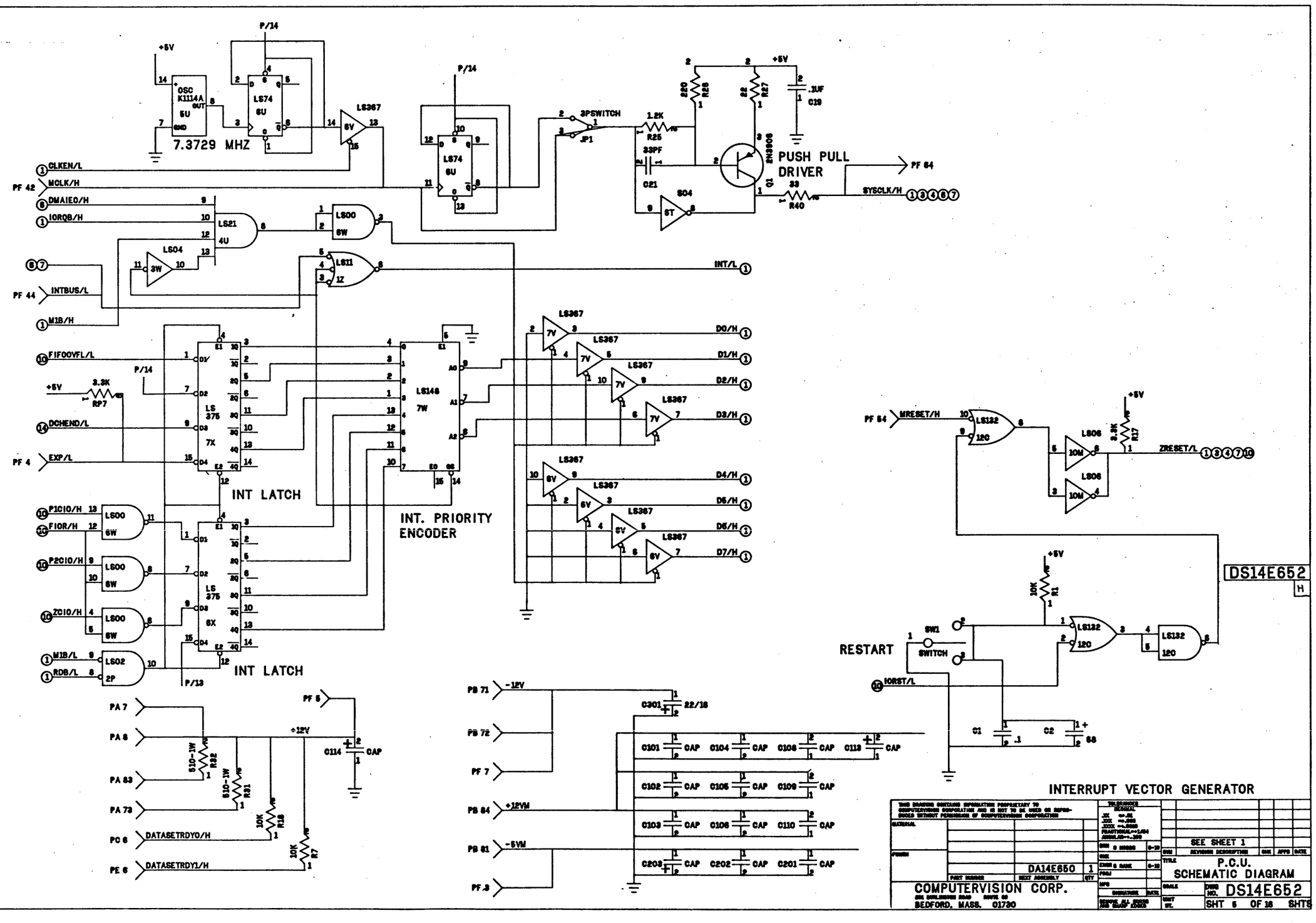
A0B/H 8 … A10B/H 20 → A0 … A10
CS (18)
19+12 / 24+5 / 21-5 / 12 GND
D00 9MD0/H
D01 10 MD1/H
D02 11MD2/H
D03 13MD3/H
D04 14MD4/H
D05 15MD5/H
D06 16MD6/H
D07 17MD7/H

A12B/H (1) 3 — C
A12B/H (1) 2 — B
A11B/H (1) 1 — A
LS138 6F
Y0 15 … Y7 7
G1 6 · G2A 4 · G2B 5
BLK32/L (3)

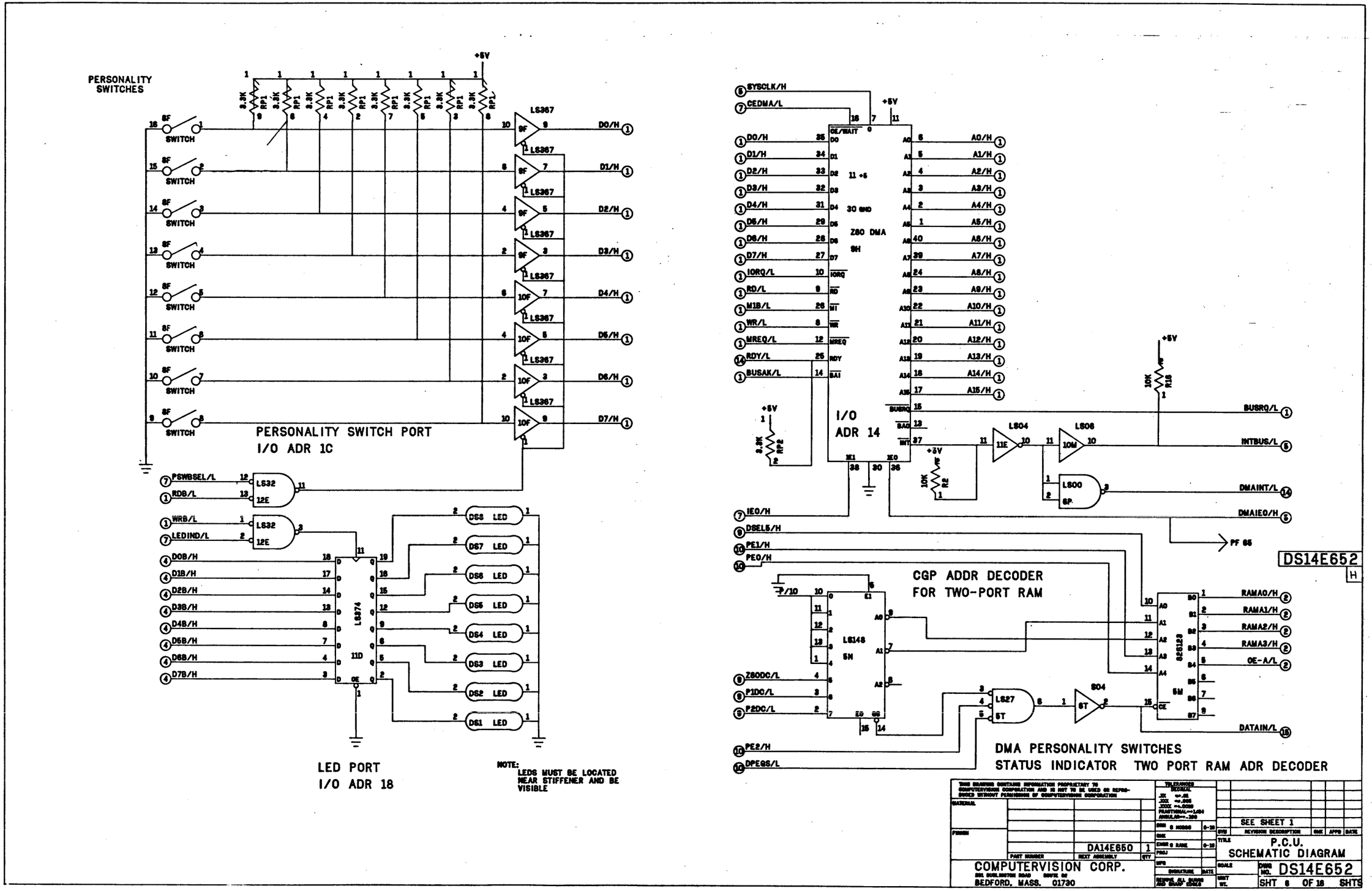
E PROM ADR DECODER
P/5

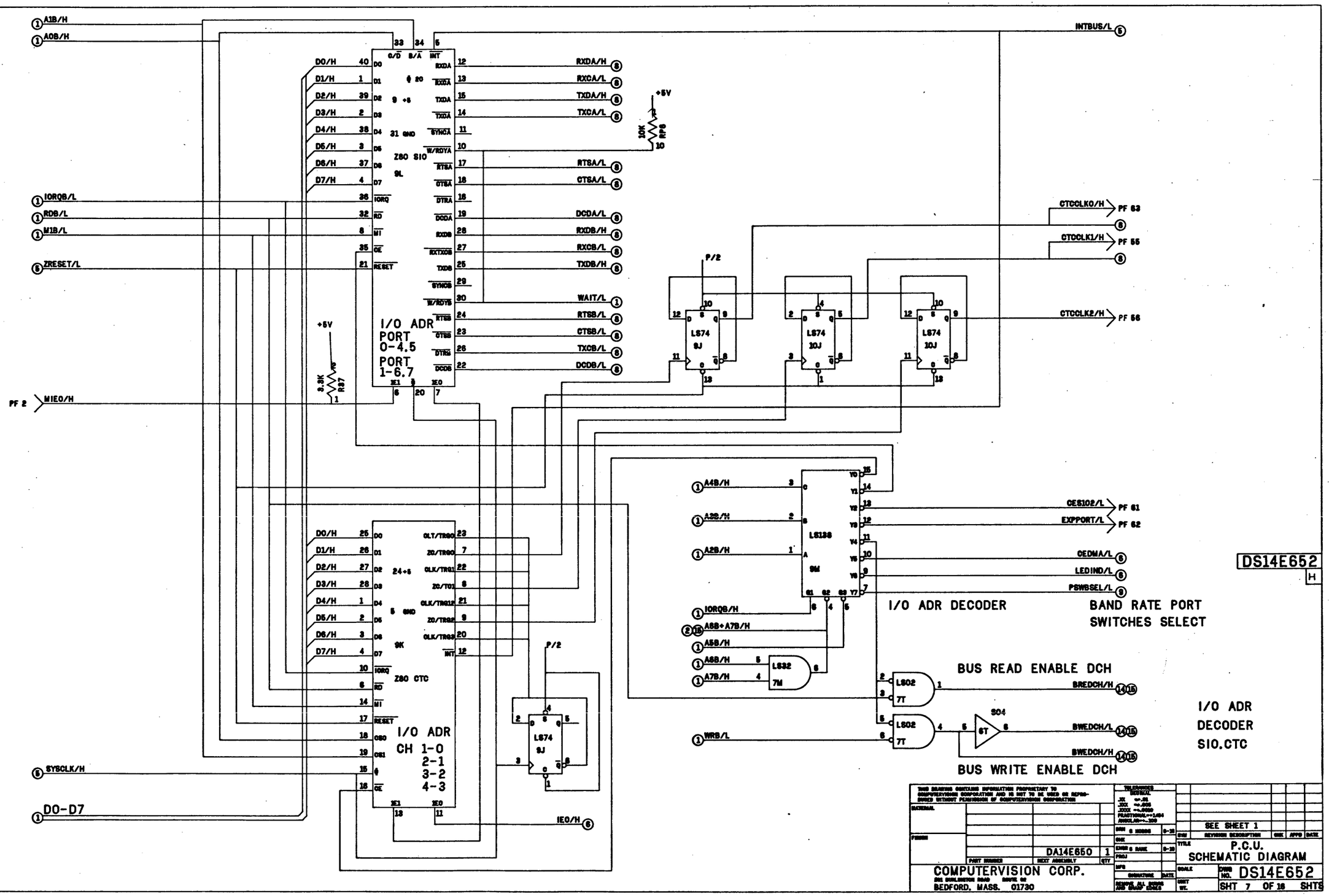
A0B-A10B (1)

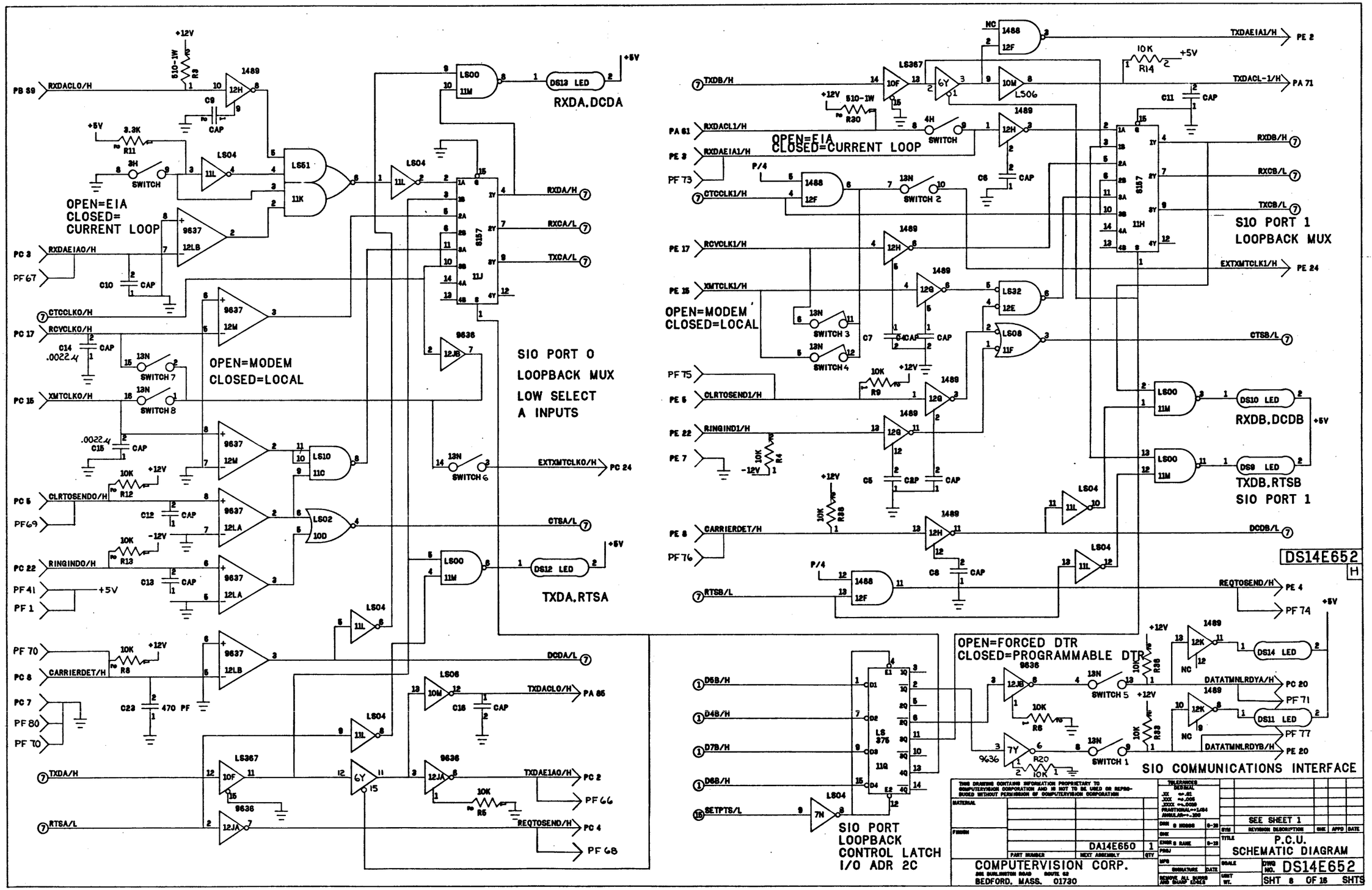
DS14E652 H



7.3729 MHZ
OSC K1114A
LS74 6U
LS367 6V
PUSH PULL DRIVER
2N3906
3PSWITCH
JP1
CLKEN/L
MCLK/H
DMAIEO/H
IORQB/H
INTBUS/L
M1B/H
FIFOOVFL/L
DCHEND/L
EXP/L
P1CIO/H
FIOR/H
P2CIO/H
ZCIO/H
M1B/L
RDB/L
INT/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
INT LATCH
INT. PRIORITY ENCODER
LS148 7W
LS375 7X
LS375 6X
LS00 6W
LS21 4U
LS04 3W
LS11 1Z
LS02 2P
LS132 12C
LS06 10M
MRESET/H
ZRESET/L
SYSCLK/H
RESTART
SWITCH
IORST/L
DS14E652
PA 7
PA 8
PA 83
PA 73
PC 6
PE 6
DATASETRDY0/H
DATASETRDY1/H
PF 5
PB 71
PB 72
PF 7
PB 84
PB 81
PF 3
-12V
+12V
+12VM
-5VM
C301 22/16
C101 CAP
C102 CAP
C103 CAP
C104 CAP
C105 CAP
C106 CAP
C108 CAP
C109 CAP
C110 CAP
C113 CAP
C114 CAP
C201 CAP
C202 CAP
C203 CAP
INTERRUPT VECTOR GENERATOR
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 5 OF 16 SHTS


PERSONALITY SWITCHES
PERSONALITY SWITCH PORT
I/O ADR 1C
LED PORT
I/O ADR 18
NOTE:
LEDS MUST BE LOCATED NEAR STIFFENER AND BE VISIBLE
I/O
ADR 14
Z80 DMA
CGP ADDR DECODER
FOR TWO-PORT RAM
DMA PERSONALITY SWITCHES
STATUS INDICATOR TWO PORT RAM ADR DECODER
DS14E652
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DWG NO. DS14E652
SHT 6 OF 18 SHTS


A1B/H
A0B/H
IORQB/L
RDB/L
M1B/L
ZRESET/L
MIEO/H
SYSCLK/H
DO-D7
INTBUS/L
D0/H
D1/H
D2/H
D3/H
D4/H
D5/H
D6/H
D7/H
Z80 SIO
I/O ADR
PORT
0-4,5
PORT
1-6.7
RXDA/H
RXCA/L
TXDA/H
TXCA/L
RTSA/L
CTSA/L
DCDA/L
RXDB/H
RXCB/L
TXDB/H
WAIT/L
RTSB/L
CTSB/L
TXCB/L
DCDB/L
+5V
10K
RP6
3.3K
R87
P/2
LS74
9J
LS74
10J
LS74
10J
CTCCLK0/H
PF 63
CTCCLK1/H
PF 65
CTCCLK2/H
PF 66
Z80 CTC
I/O ADR
CH 1-0
2-1
3-2
4-3
IEO/H
A4B/H
A3B/H
A2B/H
IORQB/H
A8B+A7B/H
A5B/H
A6B/H
A7B/H
WRB/L
LS138
9M
LS32
7M
CES102/L
PF 61
EXPPORT/L
PF 62
CEDMA/L
LEDIND/L
PSWBSEL/L
I/O ADR DECODER
BAND RATE PORT
SWITCHES SELECT
BUS READ ENABLE DCH
LS02
7T
BREDCH/H
BWEDCH/L
S04
6T
BWEDCH/H
BUS WRITE ENABLE DCH
I/O ADR
DECODER
SIO.CTC
DS14E652
H
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DS14E652
SHT 7 OF 16 SHTS
DA14E650 1
COMPUTERVISION CORP.
BEDFORD, MASS. 01730



OPEN=EIA
CLOSED=
CURRENT LOOP
OPEN=MODEM
CLOSED=LOCAL
SIO PORT 0
LOOPBACK MUX
LOW SELECT
A INPUTS
RXDA.DCDA
TXDA.RTSA
OPEN=EIA
CLOSED=CURRENT LOOP
OPEN=MODEM
CLOSED=LOCAL
SIO PORT 1
LOOPBACK MUX
RXDB.DCDB
TXDB.RTSB
SIO PORT 1
OPEN=FORCED DTR
CLOSED=PROGRAMMABLE DTR
SIO PORT
LOOPBACK
CONTROL LATCH
I/O ADR 2C
SIO COMMUNICATIONS INTERFACE
DS14E652
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DA14E650
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 8 OF 16 SHTS

DEVICE SELECT PCU

CLOSE TO DISABLE PORT 0

CLOSE TO DISABLE PORT 1

DEVICE SELECT PORT 1

DEVICE CODE LOGIC Z80 BUSY/DONE

DS14E652

H

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COMPUTERVISION CORP.
BEDFORD, MASS. 01730

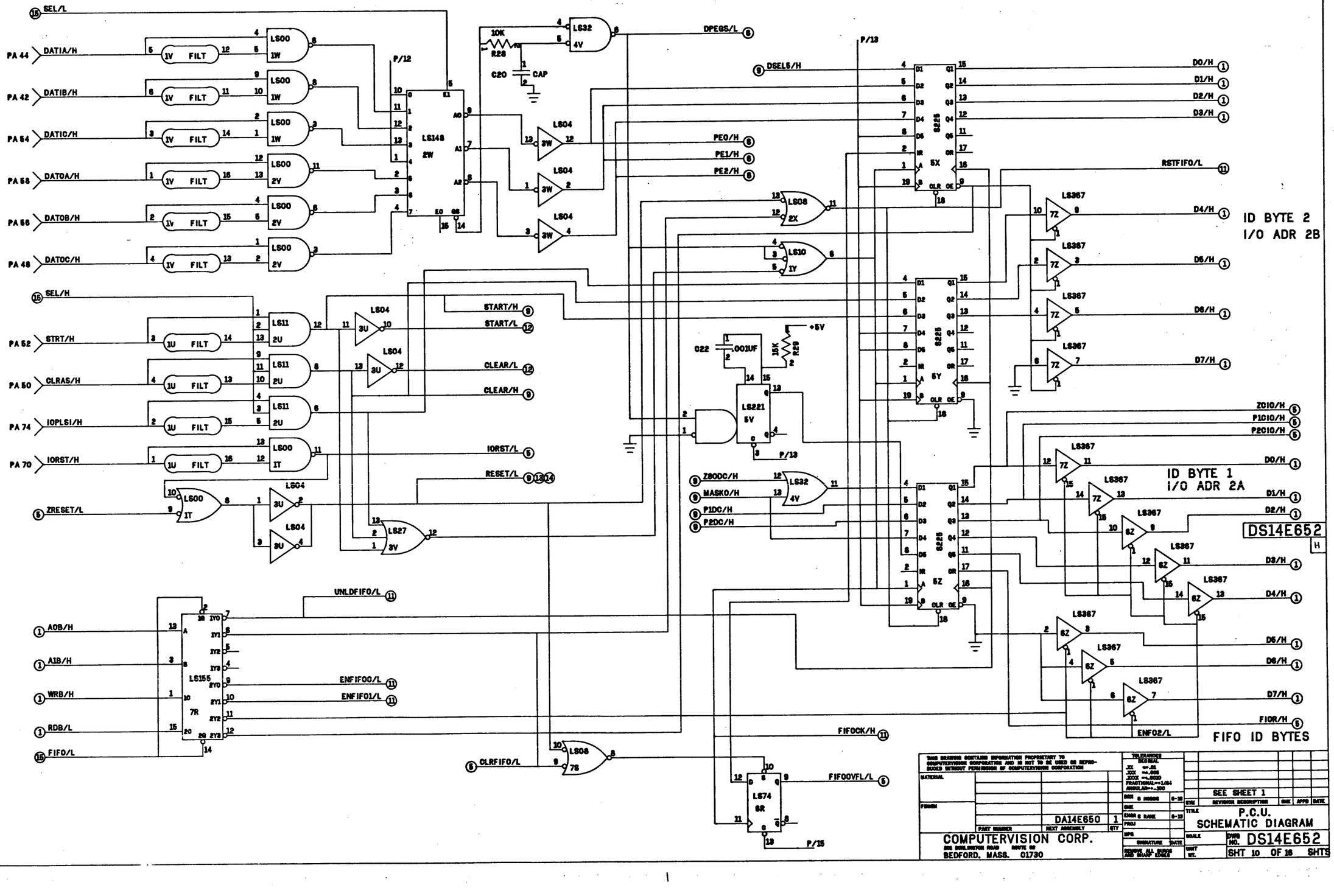
DA14E650 1

SEE SHEET 1

TITLE P.C.U. SCHEMATIC DIAGRAM

DWG NO. DS14E652

SHT 9 OF 16 SHTS


SEL/L
PA 44 DATIA/H
PA 42 DATIB/H
PA 54 DATIC/H
PA 58 DATOA/H
PA 56 DATOB/H
PA 48 DATOC/H
1V FILT
LS00 1W
LS00 2V
P/12
LS148 2W
10K R28
C20 CAP
LS32 4V
DPEGS/L
LS04 3W
PE0/H
PE1/H
PE2/H
DSELS/H
LS08 2X
LS10 1Y
P/13
8225 5X
8225 5Y
8225 5Z
D0/H
D1/H
D2/H
D3/H
RSTFIFO/L
LS367 7Z
D4/H
D5/H
D6/H
D7/H
ID BYTE 2
I/O ADR 2B
SEL/H
PA 52 STRT/H
PA 50 CLRAS/H
PA 74 IOPLSI/H
PA 70 IORST/H
1U FILT
LS11 2U
LS00 1T
LS04 3U
START/H
START/L
CLEAR/L
CLEAR/H
IORST/L
RESET/L
ZRESET/L
LS27 3V
.001UF C22
15K R29
+5V
LS221 5V
Z80DC/H
MASKO/H
P1DC/H
P2DC/H
LS32 4V
ZCIO/H
P1CIO/H
P2CIO/H
ID BYTE 1
I/O ADR 2A
DS14E652
H
AOB/H
A1B/H
WRB/H
RDB/L
FIFO/L
LS155 7R
UNLDFIFO/L
ENFIFO0/L
ENFIFO1/L
ENFO2/L
LS08 7S
CLRFIFO/L
FIFOCK/H
LS74 8R
FIFOOVFL/L
FIOR/H
FIFO ID BYTES
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MATERIAL
FINISH
PART NUMBER DA14E650 NEXT ASSEMBLY 1 QTY
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
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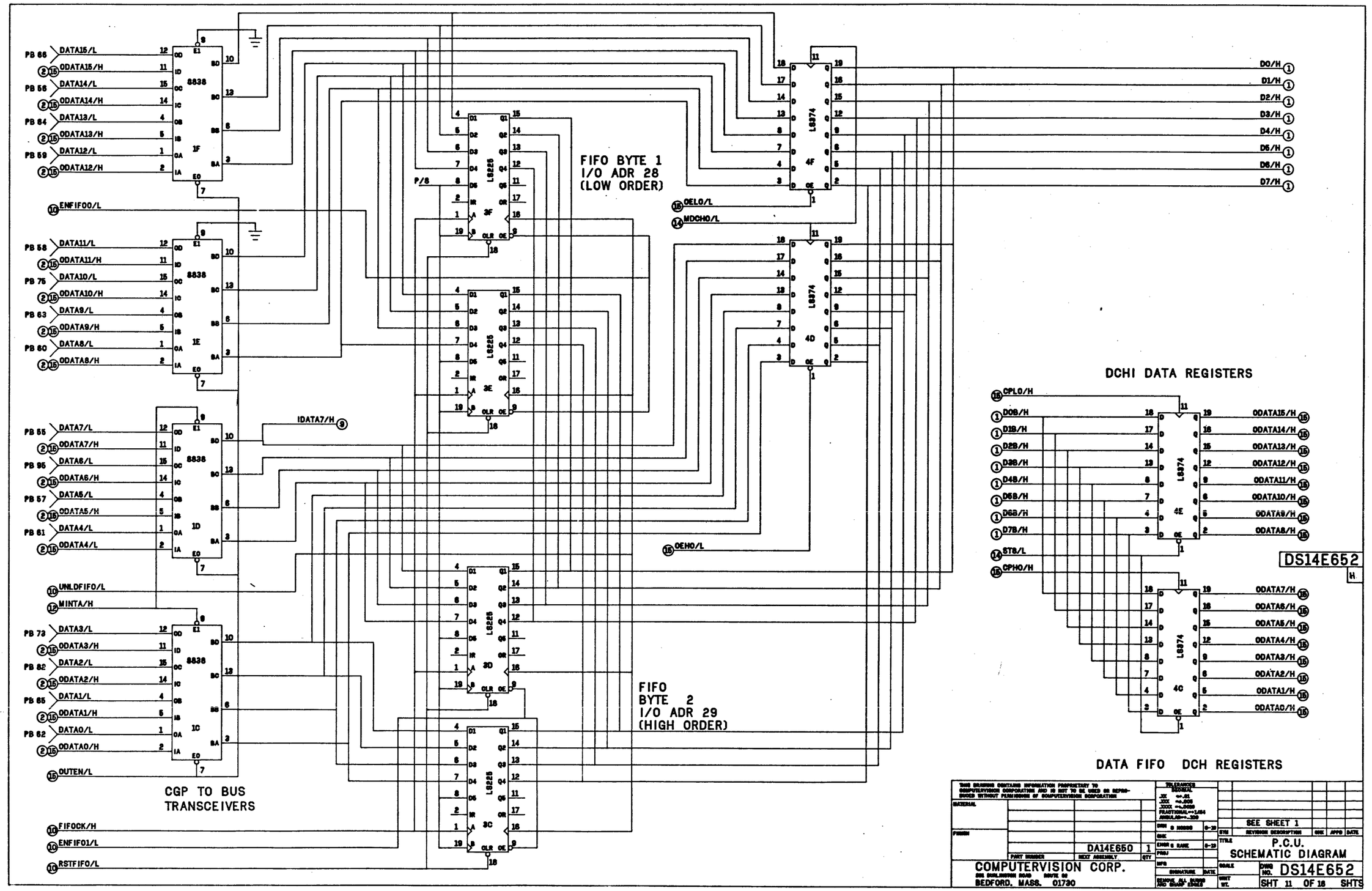
REVISION DESCRIPTION
P.C.U.
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 10 OF 16 SHTS


FIFO BYTE 1
I/O ADR 28
(LOW ORDER)
FIFO
BYTE 2
I/O ADR 29
(HIGH ORDER)
CGP TO BUS
TRANSCEIVERS
DCHI DATA REGISTERS
DATA FIFO DCH REGISTERS
DS14E652
SEE SHEET 1
P.C.U.
SCHEMATIC DIAGRAM
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SHT 11 OF 18 SHTS

DEVICE RESPONSE MUX

LS367 6M — ODATA8/H, ODATA9/H
LS367 6M — ODATA10/H, ODATA11/H
LS253 4G — P1DS0/H, ZDS0/H, P2DS0/H, P/S, ZDS1/H, P1DS1/H, P2DS1/H
LS253 3G — P1DS2/H, ZDS2/H, P2DS2/H, ZDS3/H, P1DS3/H, P2DS3/H — ODATA12/H, ODATA13/H
LS253 2G — P1DS4/H, ZDS4/H, P2DS4/H — ODATA14/H, ODATA15/H
PCUMSK/H
LS148 1G — P/S, IRP2OT/L, IRP1OT/L, IRP2IN/L, IRP1IN/L, Z80INTR/L
LS04 2S — INT/L → PB 29

I/O FLAG CONTROL DECODER

LS04 6N — D0B/H, A0B/H, A1B/H, WRPRTBTS/H, WRPRTBTS/L, D1B/H
LS155 4N — CP1IB/L, CP2IB/L, SP1ID/L, SP2ID/L
LS04 6N — D2B/H
LS155 3N — DP1IINT/L, DP2IINT/L, EP1IINT/L, EP2IINT/L
LS04 6N — D3B/H
LS04 7N — D4B/H
LS155 2N — CP1OB/L, CP2OB/L, SP1OD/L, SP2OD/L
LS04 7N — D5B/H
LS04 7N — D6B/H
LS155 1N — DP1OINT/L, DP2OINT/L, EP1OINT/L, EP2OINT/L
LS04 7N — D7B/H

PORT BUSY / DONE SELECT

LS253 1R — P2ODN/H, P1ODN/H, P1IDN/H, P2IDN/H, P1OBS/H, P2OBS/H, P1IBS/H, P2IBS/H, DSEL5/L, P1DC/L
7438 3R — SELD/L, SELB/L

LS04 2S — MINTA/L, MINTA/H
PA 98 INTPIN/L
PA 40 INTA/H
1V FILT
LS08 7S
LS11 4S

INT PRIORITY

7438 1S
+5V
330 R24
330 R23
INTPOUT/L → PA 96

PORT BUSY/ DONE CONTROL

LS155 2R — START/L, P2DC/H, DSEL5/H, PORTDC/H, PORTDC/L, CLEAR/L
P1ISTRT/L, P2ISTRT/L, P1OSTRT/L, P2OSTRT/L, P1ICLR/L, P2ICLR/L, P1OCLR/L, P2OCLR/L

PORT 0,1-CGP INTERFACE

DS14E652 H

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MATERIAL
FINISH
DA14E650 1
PART NUMBER NEXT ASSEMBLY QTY

UNLESS OTHERWISE SPECIFIED: DIM ± .XX ±.02, .XXX ±.005, .XXXX ±.0050, FRACTIONAL ±1/64, ANGLES ±1°

DRN G MOSS 6-29
CHK
ENGR G BANE 6-29
PROJ
APPD
SIGNATURE DATE

COMPUTERVISION CORP.
200 BOSTON POST ROAD ROUTE 62
BEDFORD, MASS. 01730

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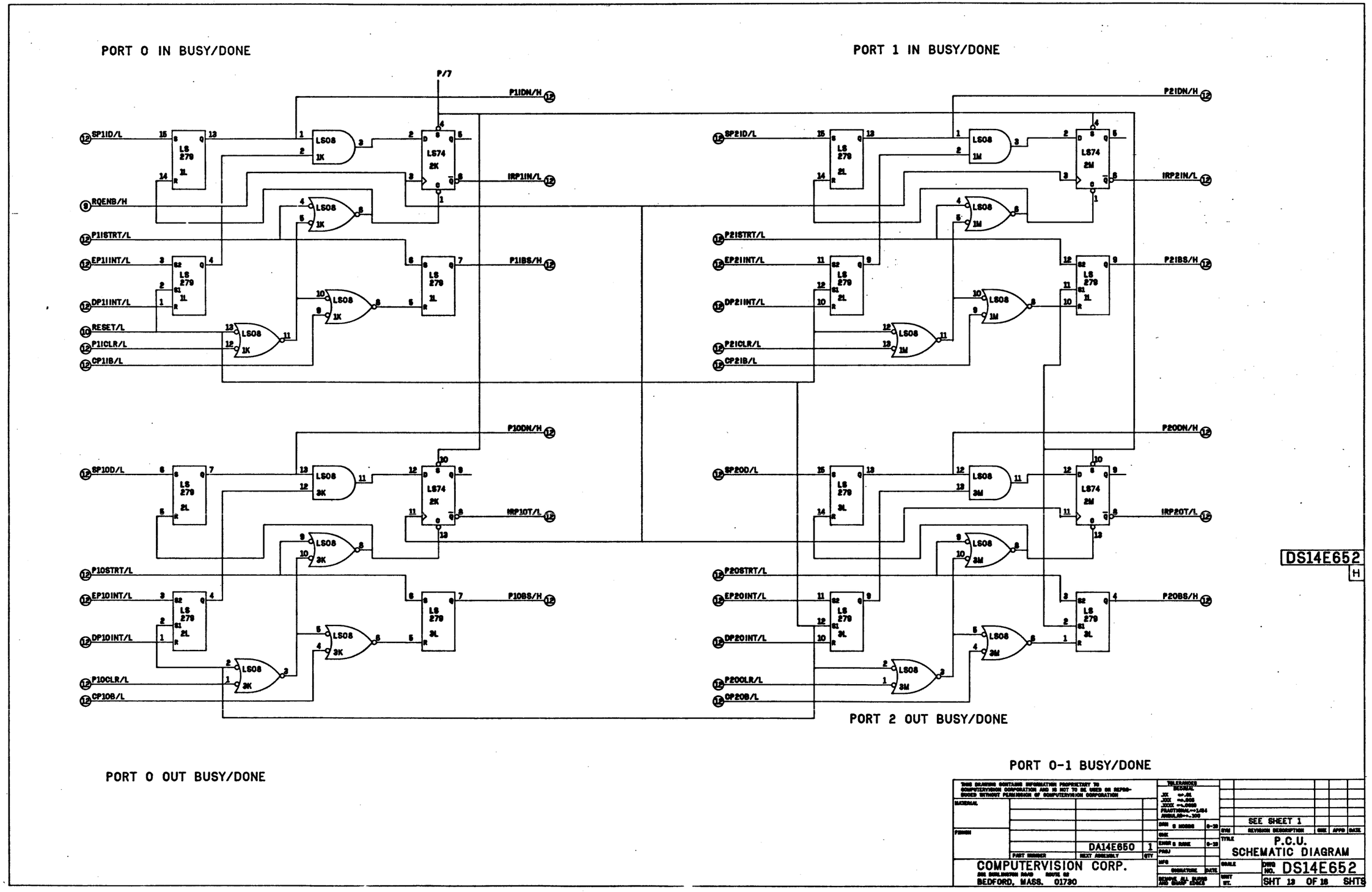
DWG	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE: P.C.U. SCHEMATIC DIAGRAM
SCALE
DWG NO. DS14E652
SHT NO. SHT 12 OF 18 SHTS


PORT 0 IN BUSY/DONE
PORT 1 IN BUSY/DONE
PORT 2 OUT BUSY/DONE
PORT 0 OUT BUSY/DONE
PORT 0-1 BUSY/DONE
P/7
P1IDN/H
IRP1IN/L
P1IBS/H
P10DN/H
IRP10T/L
P10BS/H
P2IDN/H
IRP2IN/L
P2IBS/H
P20DN/H
IRP20T/L
P20BS/H
SP1ID/L
RQENB/H
P1ISTRT/L
EP1IINT/L
DP1IINT/L
RESET/L
P1ICLR/L
CP1IB/L
SP10D/L
P10STRT/L
EP10INT/L
DP10INT/L
P10CLR/L
CP10B/L
SP2ID/L
P2ISTRT/L
EP2IINT/L
DP2IINT/L
P2ICLR/L
CP2IB/L
SP20D/L
P20STRT/L
EP20INT/L
DP20INT/L
P20CLR/L
CP20B/L
LS 279
LS08
LS74
1K
2K
3K
1M
2M
3M
1L
2L
3L
DS14E652
H
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MATERIAL
FINISH
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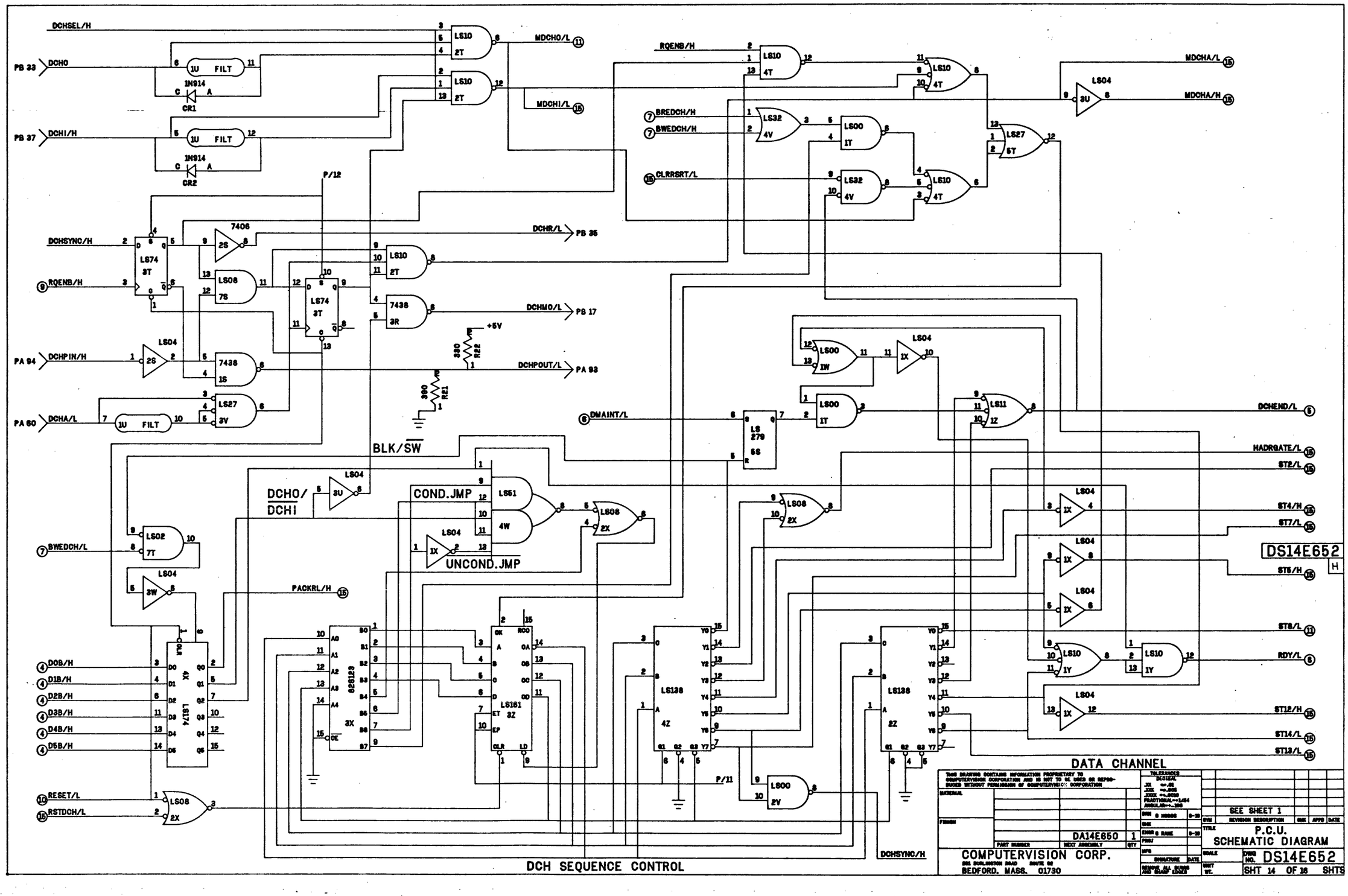
SCHEMATIC DIAGRAM
SCALE
DWG NO. DS14E652
SHT 13 OF 16 SHTS


DCHSEL/H
PB 33
DCHO
PB 37
DCHI/H
1N914
CR1
CR2
FILT
MDCHO/L
MDCHI/L
RQENB/H
BREDCH/H
BWEDCH/H
CLRRSRT/L
MDCHA/L
MDCHA/H
P/12
DCHSYNC/H
RQENB/H
DCHR/L
PB 35
DCHMO/L
PB 17
DCHPIN/H
PA 94
DCHPOUT/L
PA 93
DCHA/L
PA 60
+5V
DMAINT/L
DCHEND/L
HADRGATE/L
ST2/L
ST4/H
ST7/L
ST5/H
ST8/L
RDY/L
ST12/H
ST14/L
ST13/L
BLK/SW
DCHO/
DCHI
COND.JMP
UNCOND.JMP
BWEDCH/L
PACKRL/H
DOB/H
D1B/H
D2B/H
D3B/H
D4B/H
D5B/H
RESET/L
RSTDCH/L
P/11
DCHSYNC/H
DS14E652
DATA CHANNEL
DCH SEQUENCE CONTROL
DA14E650
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
SEE SHEET 1
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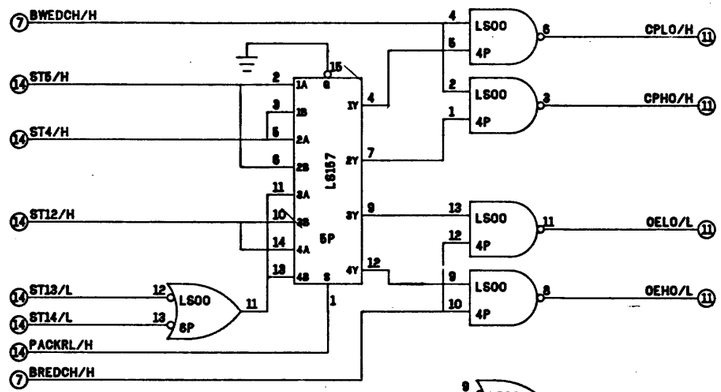
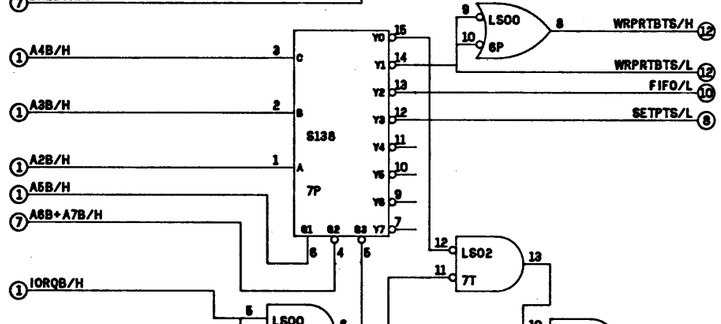
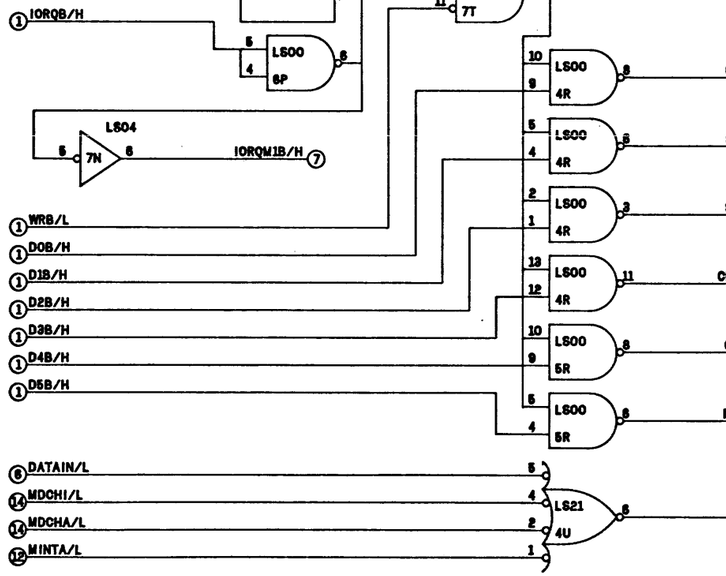
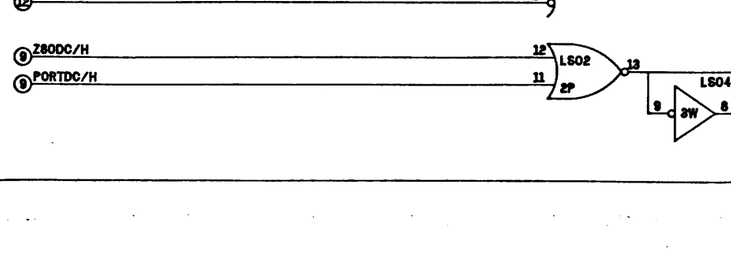
SCHEMATIC DIAGRAM
DWG NO. DS14E652
SHT 14 OF 16 SHTS

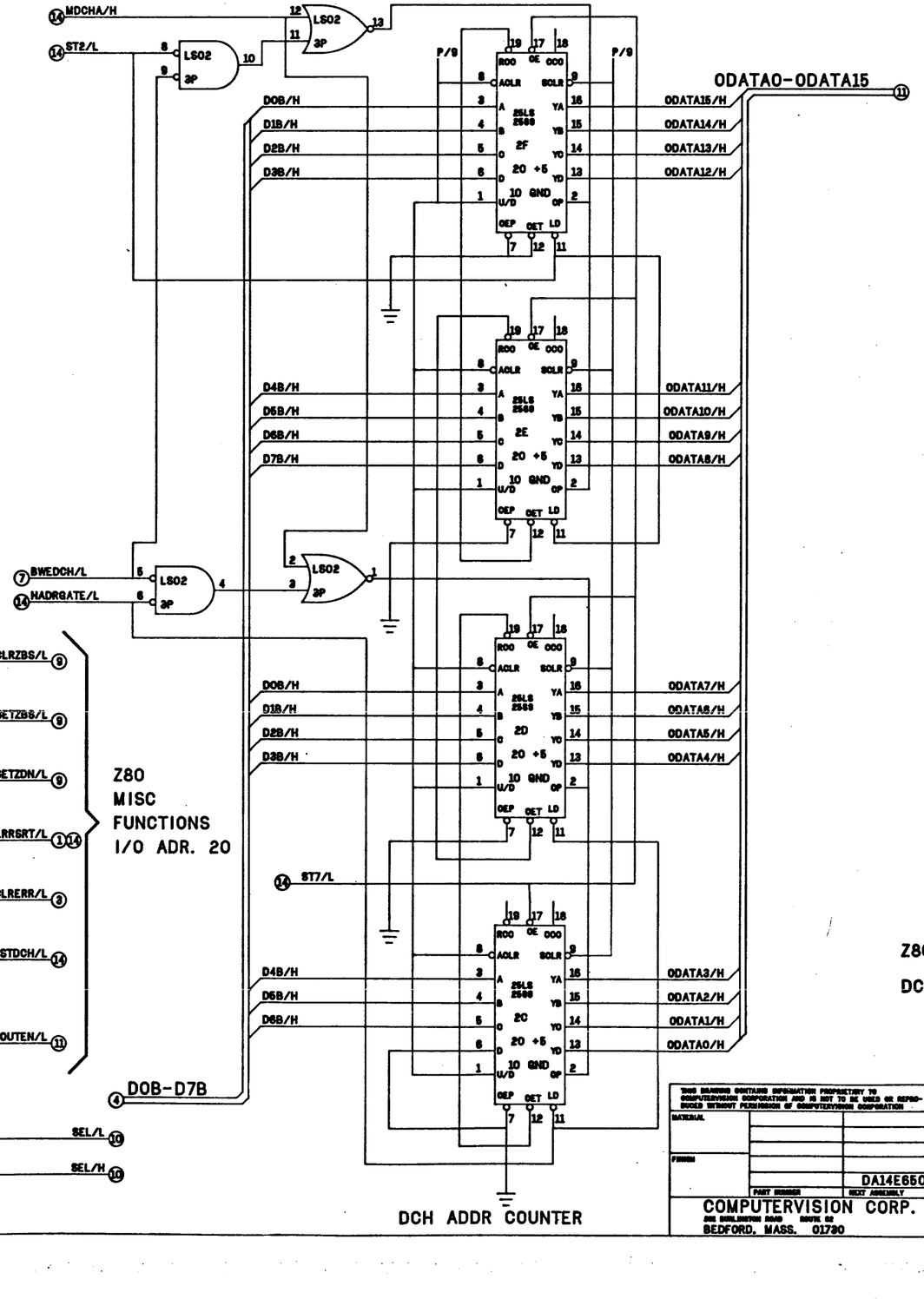
BYTE PACKING DIREOTION CONTROL











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Z80 MISC FUNCTIONS

DCH ADDER COUNTER

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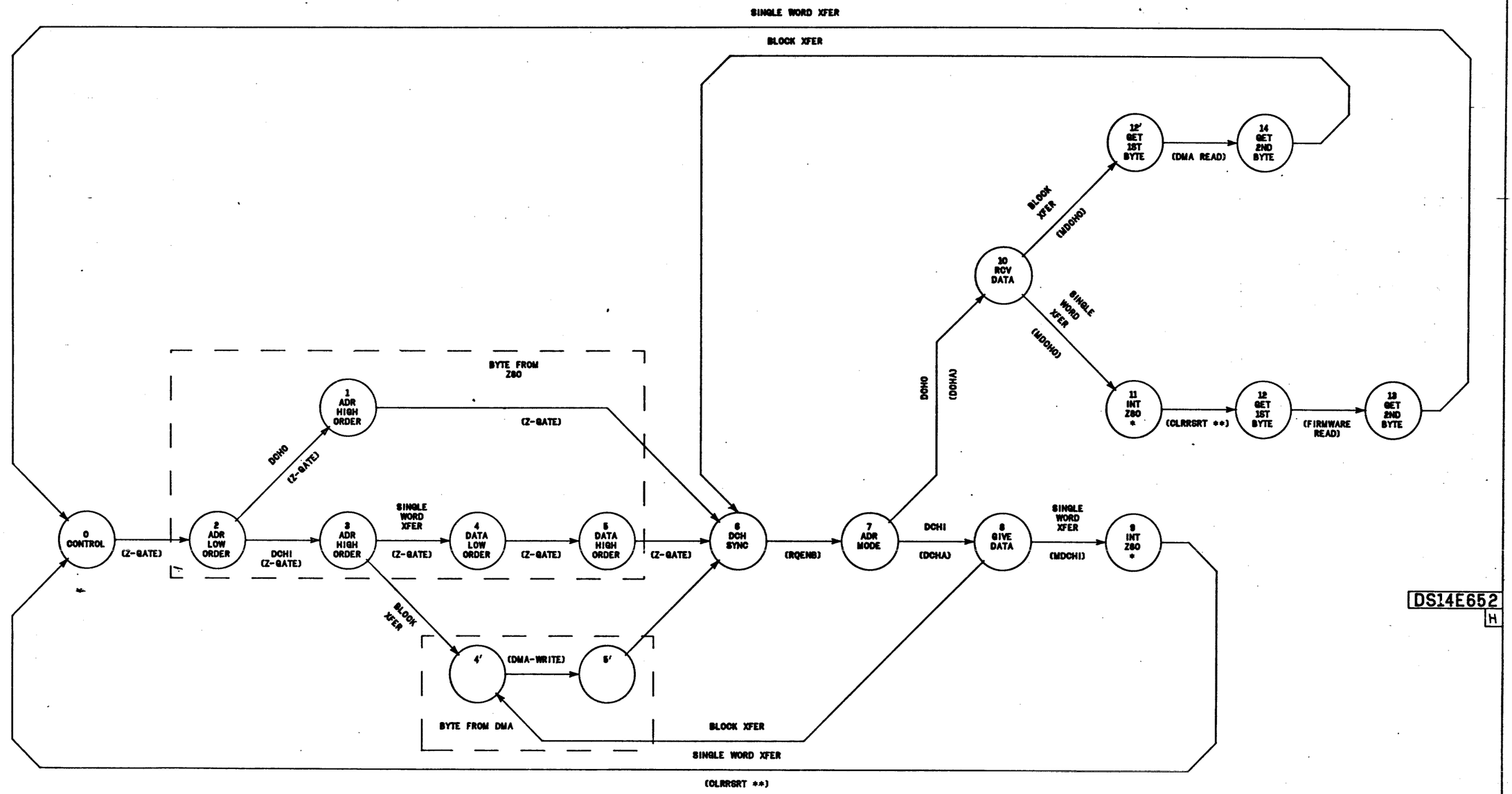
SHT 15 OF 16 SHTS



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* DCHEND INT

** CLEARS DCH INT

SIGNALS IN PARENTHESES CAUSE THE STATES TO ADVANCE.

DATA CHANNEL CONTROLLER STATE DIAGRAM

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300 BURLINGTON ROAD ROUTE 62
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REV	REVISION DESCRIPTION	CHK	APPD	DATE

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