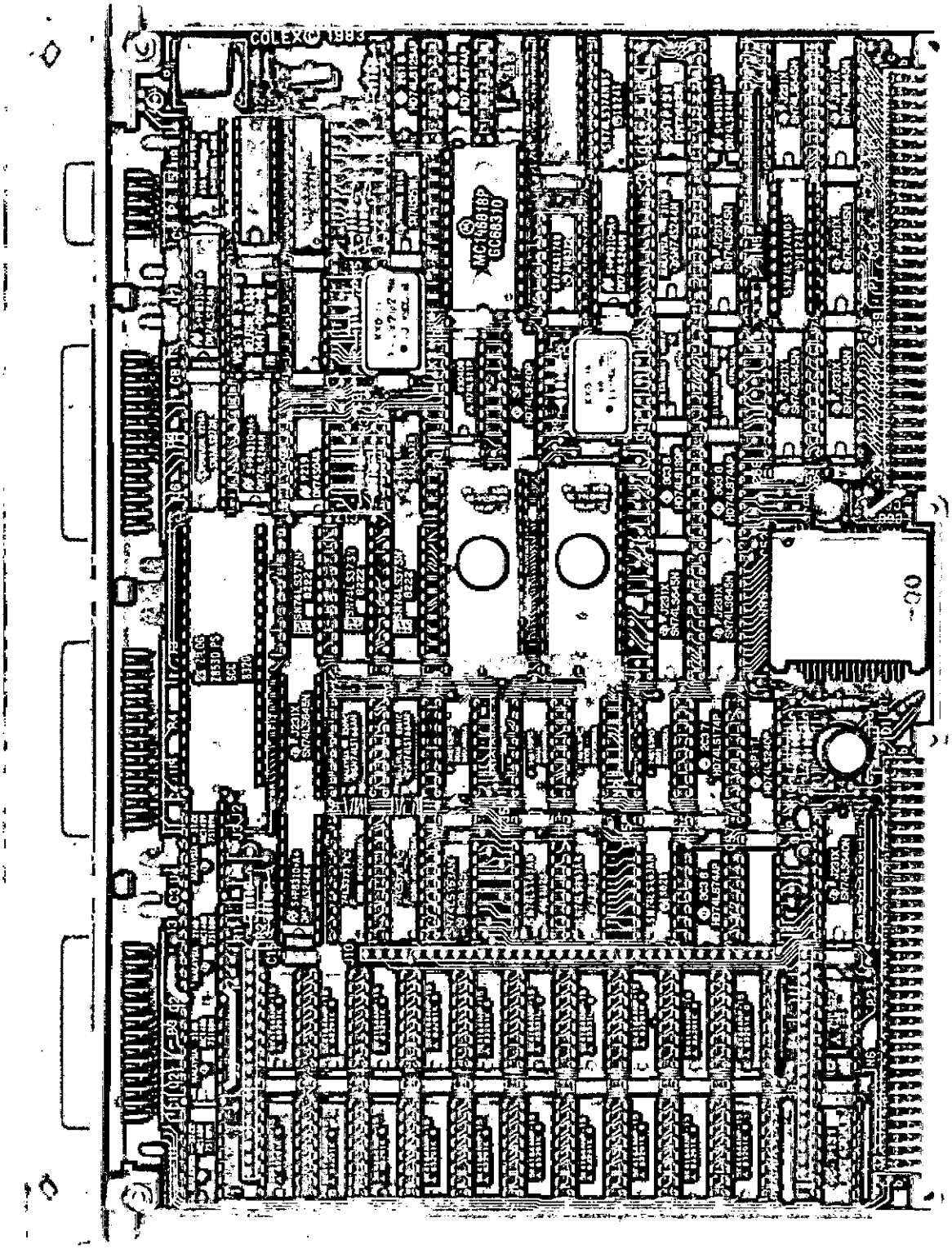
COLEX

VME
80186

TECHNICAL MANUAL



COLEX VME-80186

COLEX's advanced system design has made it possible to bring two of the most popular system concepts of the 80's together onto one board: the Intel 80186 16 bit microprocessor and the VMEbus. By expanding the memory address space to 16 megabytes, adding address modifiers, and providing the proper timing controls, COLEX has made the VME-80186 compatible to the VMEbus standard and to other VMEbus products meeting specification Revision B or later.

The VME-80186 allows, for the first time, the use of the popular operating system MSDOS together with the VMEbus. The 8088/8086 has the widest range of installations among all 16 bit computers. The 80186 incorporates full 8088/8086 upward compatibility while compressing 40 chips into one package. The result is a wide range of software and hardware options for the system builder.

The features of the VME-80186 include:

Processor	80186 CPU
Clock speed	13 MHz
On-board memory	128kb
	2 JEDEC EPROM sockets
Add-on memory	128kb
	Parity for all 256k bytes of memory
Off-board memory	16 megabytes address space
	5 address modifiers
Video output	Optional video controller
Serial I/O	2 RS232 ports with 25 pin connectors
DMA	High speed DMA channel
Printer output	Centronics compatible, 25 pin connector
VMEbus expansion	Full VMEbus interface, slot one functions
	Bus master, slave and controller
Mass storage	SASI interface to floppy and hard disks
Real time clock	With alarm, timer, and battery backup
MultiCPU option	For parallel processing

HIGH PERFORMANCE APPLICATIONS

Applications for the VME-80186 include machine tool control, communications controllers and preprocessors, small business computers, process control, and I/O processor for multi-processor systems. The VME-80186 is compatible with VMEbus products from dozens of vendors, plus other COLEX VMEbus products and can be expanded to use A/D converters, additional mass memory devices, direct industrial interfaces, CMOS RAM modules, graphics display controllers, and many more.

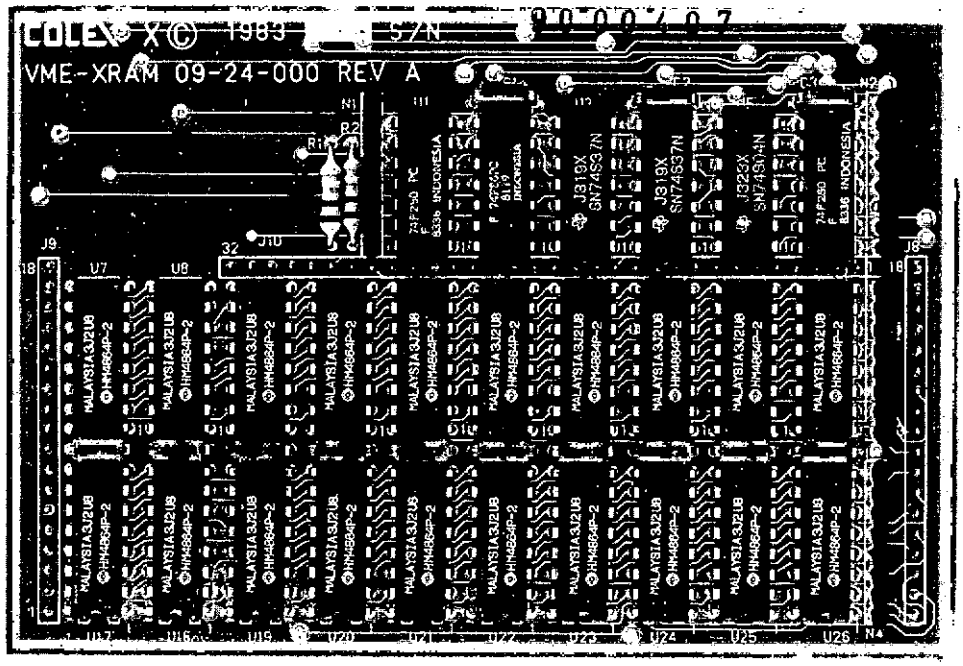
128/256k MEMORY

This memory consists of 128k bytes located on the main board, it can be expanded by an additional 128k bytes by using the XRAM card. Parity logic is provided by the XRAM add-on and performs parity checking on both the main board memory and the plug-on memory. Cycle time of the memory averages 625ns. Refresh for all VME-80186 memory is done by a controller on the VME-80186 card.

The memory map on the VME-80186 card is separated into 5 working segments. Three segments perform actual memory functions, one is for I/O accesses to the VMEbus, the last is to allow VMEbus generated vector interrupts to be read by the 80186 chip.

On-board RAM memory	0- 256Kb	256Kb
Off-board memory	256- 768Kb	512Kb
Vector interrupt input	768- 800Kb	32Kb
VMEbus short I/O	800- 832Kb	32Kb
not used	832- 960Kb	128Kb
On-board EPROM memory	960-1024Kb	64Kb

This mapping is programmable by the 80186 CPU chip. The above mapping is used by COLEX in standard software.



XRAM

The XRAM card adds 128Kb memory and a parity controller to the VME-80186 by way of 3 connector rows. The XRAM card is simply plugged into these connector rows, only one orientation is possible. The memory control logic automatically uses the added-on ram. The parity controller performs parity checking and generation for the entire 256k ram. If an error is detected, a BERR/ signal will be generated. This will cause a 'NON MASKABLE INTERRUPT' to the 80186 if the VME-80186 NMI enable bit is set.

SERIAL PORTS

Serial I/O is possible via the 2 ports on the card. P4 is connected as a DCE for direct connection to a terminal, P3 is wired as DTE for direct connection to a modem, or to another computer. Each port has its own baud rate generator connected to a 3.6864 MHz crystal oscillator. All common baud rates may be used. Multiple protocols are supported, including ASYNC, BYSYNC, HDLC, and SDLC at speeds up to 1 megabaud. The channels can also be programmed for FM, NRZI, and BIPHASE encoding and decoding. Both serial ports are interfaced via 25 pin plugs on the front panel of the card. The serial I/O controller chip used is the ZILOG SCC 853Ø, full programming details can be found in the ZILOG SCC programming manual, a brief summary is provided at the end of this document.

The DTE port (SCC channel A) can be programmed for internal or external clocks, and internal or external sync by the following jumpers:

J1	selects external sync from P3 pin 15
J2	selects the internal baud rate generator from channel B
J3	enables the internally generated sync to P3 pin 15

J1 and J3 should not be inserted at the same time.

P3 pin 17 is connected to the SCC /TRxCA input allowing this to be used as a clock input. With J2 installed, the on-board baud rate generator is connected to both the /RTxCA input and to P3 pin 14 for the clock output.

SCC PROGRAMMING

While the Zilog technical manual is the best source of information on the SCC chip used on the 8Ø186 for all serial I/O, the following quick summary of common programming options can save the user time.

1) Baud rate selection

The source of the baud rate clock is a 3.6864 MHz crystal on channel B from RTXCB to SYNCB. Register 11 should be programmed as follows to use this crystal:

channel A:	56h
channel B:	D4h

This enables the 2, 16 bit divide counters to provide a baud rate to the A and B channels. Both transmit and receive rates will be the same.

Register 14 should be programmed with a Ø1h.

2) Baud rate speed

To calculate the correct divide count for each channel, use the following formula: (BR = required baud rate)

$$= \frac{115200}{BR} - 2$$

Example: $\frac{115200}{9600} - 2 = 10$ for 9600 baud

This is programmed into register 12/13, register 13 is the MSB.

3) Data parameters

Registers 3,4 and 5 determine the parameters used in the character data. For normal operation (7 data bits, no parity, 1 stop bit, ASYNC, DTR and RTS active) the following codes are used:

register	content
3	C1h
4	44h
5	EAh

4) General parameters

To reset the chip, the following data should be written first:

	register	data
channel A:	9	80h
	9	00h
	15	00h
channel B:	9	40h
	9	00h
	15	00h

5) Summary

The byte strings to be outputted to the SCC for 9600 baud operation on both channels would be: (all data hex)

A: 09/80/09/00/03/C1/04/44/05/EA/0B/56/0C/0A/0D/00/0E/01/0F/00
B: 09/40/09/00/03/C1/04/44/05/EA/0B/D4/0C/0A/0D/00/0E/01/0F/00

The first byte is the register, the second is the data.

6) Interrupts

The SCC chip cannot generate interrupts to the 80186.

7) Reading status

The SCC can be polled for data ready or transmitter empty by testing the listed bit.

```
receive ready    = bit 0
transmit ready   = bit 2
```

CENTRONICS INTERFACE

For connection to a printer, a Centronics-compatible interface is provided. The interface is made via P5, a 25 pin connector on the front of the card. This connector matches the lower 25 pins of the standard 36 pin Centronics connector for ease of cable construction. When outputting to the printer, the BUSY and PE (paper empty) signals should be tested, both must be low before data can be sent. After data is outputted to the printer data port, the strobe should be pulsed low for at least 10 us (exact duration depends on the printer used).

VMEbus INTERFACE - Slot 1 functions

The VME-80186 functions as system controller in a VMEbus system. This allows other cards to be plugged into the bus, using the arbitration logic of the VME-80186 to allow data to be exchanged between any two cards on the bus. These 'slot one' functions include: a 16 MHz bus clock; a single-level arbiter of bus requests by the on-board 80186 or any other card; and processing of BERR, ACFAIL, SYSFAIL, INT, and NMI requests. In the arbitration process, interrupt requests have priority over bus requests. The 80186 LOCK function (used typically for bit test and set) is handled as a uninterruptable cycle, allowing orderly interprocessor communication. Interrupt levels 1 and 3 are supported from the bus, bus supplied interrupt vectors can be read by the 80186 in order to form a VMEbus compatible interrupt acknowledge cycle.

Other boards may exchange data on the VMEbus without affecting the throughput of the 80186 CPU.

VMEbus Memory addressing

The 80186 chip normally can address only 1 megabyte of memory. The Colex design adds address modifiers and extra memory address bits to allow the full use of the VMEbus 16 megabyte memory space, with minimal overhead on the part of the programmer.

Two programmable register files added to the 80186 address outputs allow it to address supervisor and user memory spaces, normal and short I/O, separate program/data memory areas, and other user defined address modifiers.

The 4 register files (4 byte dual port memories) allow the 80186 address range of 256-768Kb to be mapped to any 512kb block of memory in the VMEbus memory and address modifier map. This allows 4 types of operations (DMA I/O, DMA memory, CPU I/O and CPU memory) to be automatically correctly mapped to the bus, depending on the cycle being executed, without any output instruction to the register files.

The type of address modifiers defined in the Rev. B VMEbus spec which are supported by the VME-80186 card are shown below. The left column represents the address modifier to be selected from the register file. The right column is the data which must be programmed into the file to generate the address modifier in the left column. Note that AM4 is not generated by the register file (see next section).

VMEbus memory addressing - continued

VMEbus address modifier	bits 5 4 3 2 1 0	register file	bits 2 1 0
Supervisor program	1 1 1 1 1 0		1 0 1
Supervisor data	1 1 1 1 0 1		0 1 1
Supervisor short I/O	1 0 1 1 0 1		0 1 1
User program	1 1 1 0 1 0		1 0 0
User data	1 1 1 0 0 1		0 1 0
User short I/O	1 0 1 0 0 1		0 1 0

Register file codes for common address modifiers

Additionally, any of the 'undefined' codes fitting the model '1x1xxx' may be generated for customized applications, where 'x' is either a 0 or 1. The register file contents are programmable from the CPU by outputing the pattern required to the appropriate port.

With an output instruction, the CPU must write all 8 bits of data to one of the 4 register file ports. Every subsequent VMEbus transfer will use the data stored in the appropriate register file to extend the 80186 addressing to the full VMEbus space. The data byte written to the register file (bits 0 to 7) are sent to the bus as 5 address bits (A19 to A23) and 3 Address Modifier bits. As can be seen from the following table, the address and address modifier data bits must be merged by the program to generate the proper pattern.

Address modifier register files

AM5	AM4	AM3	AM2	AM1	AM0	A23	A22	A21	A20	A19
1	x	1	b0	b2	b1	b7	b6	b5	b4	b3

Note that 'b0' to 'b7' represent the bits in the accumulator of the 80186 CPU.

Also note that AM4 is not directly programmable from the register file. Instead, this bit is driven by a memory select decode line from the 80186 chip. This means it is low when memory addresses are in the range of 768k to 832K, otherwise it is high. AM5 is always driven high during VME-80186 VMEbus accesses in order to disable the unused 32 bit transfer mode of the bus. AM3 is always driven high, as the functions performed by this bit when low are not defined by the VMEbus specification.

VMEbus memory addressing - continued

The 4 register files are loaded by 80186 local output instructions to the appropriate I/O port. The I/O port addresses and their functions are:

Port	Enabled during
200	CPU short I/O address, DMA I/O source address
202	DMA I/O destination address
204	CPU memory address, DMA memory source address
206	DMA memory destination address

Which of the 4 register files are enabled as address modifiers and upper address bits during a VMEbus transfer is determined by 2 functions:

a) Second cycle in a DMA transfer (destination)
b) Short I/O request (80186 local address between 768k and 832k)

This approach allows DMA transfers to be programmed between blocks of VMEbus memory which are separated by more than 512k bytes. This is done by programming the source and destination register files with different memory contents. The scheme also allows the short I/O addresses of the VMEbus to be accessed by the CPU independently of the memory mode (supervisor/user, data/program) selected.

By separating the source and destination address modifiers and upper address bits, the 80186 DMA channel chip has full power to move data anywhere, far beyond the usual 80186 chip addressing limitations.

Interrupt acknowledge cycle

After the CPU receives an interrupt on inputs 1 or 3 from the VMEbus, it can read in the vector from the interrupting device by the following sequence:

Read memory address c0003H if interrupt level 1 vector is to be read
Read memory address c0007H if interrupt level 3 vector is to be read

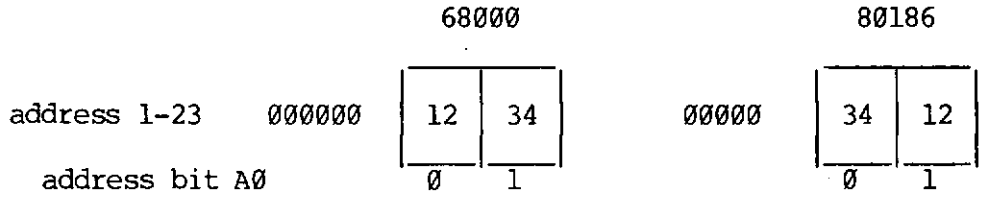
80186 VMEbus byte mode compatibility

Addresses from A1 to A18 are provided directly by the 80186 chip to the VMEbus. The 80186 BHE and A0 lines are translated into VMEbus consistent upper and lower data strobes. Long word transfers are not supported by the VME-80186.

The COLEX VME-80186 card correctly manages the different methods the 80186 chip and VMEbus chip use to define the high and low bytes of a 16 bit word. D0 to D7 of the 80186 chip is connected to D8 to D15 on the VMEbus. Likewise, D8-D15 is connected to D0-D7. Internal connections are not affected by the 'swap' of these data lines. (All I/O on the VME-80186 card is accessable by the 80186 only.) With this translation, a 16 bit word written into memory by a 68000 with be correctly read by the 80186. Without this swap, word transfers would be incompatible. Logic on the VME-80186 card also assures that Byte transfers on the VMEbus are also completely compatible.

Internal Processor memory organization

data = 1234H



The above example shows how the 2 CPU chips store the hexidecimal word '1234' in memory. The swap built into the VME-80186 allows all data interchange between CPU's to be programmer transparent. The 80186 programmer should not write words on odd memory addresses if the 68000 is to correctly read this data, since the 68000 chip itself cannot support this feature.

80186 chip initialization

The internal registers of the 80186 require initialization on power-on for correct operation of the chip and the VMEbus interface described in this specification. The complete list of registers and the data required is listed below:

name	address	data	function
control block			defaults to 0FF00H after reset
upper chip select	0FFA0H	0F038H	EPROM at last 64K bytes no wait states external ready
lower chip select	0FFA2H	03FF8H	RAM at 0 to 256K external ready
peripheral select	0FFA4H	00E3BH	I/O base address at E000, 3 wait states for pcs 0-3
midrange chip select	0FFA6H	0C1FBH	Interrupt acknowledge cycle via access to 768k - 800k short I/O via 800k - 832k 3 wait states and ready
MPCS	0FFA8H	090BBH	7 I/O chip selects, not memory mapped I/O 3 wait states for pcs 4-6 4 x 32k byte segments

Timer and DMA registers are not listed, these do not affect basic operation of the board. The INTEL 80186 chip manual should be referred to for more detail.

ADDRESS MODIFIER INITIALIZATION

The address modifiers are initialized to allow the 80186 address space in the range of 256k-768k to access the VMEbus memory from 0 to 512k. Also, the short I/O space is set up.

PORT	DATA	FUNCTION
0E200	03	Short I/O space
0E202	03	Short I/o space
0E204	05	Supervisor space, address 0
0E206	05	Supervisor space, address 0

GENERAL PURPOSE I/O

P6 is a 9 pin connector on the front panel which may be used for connection of the VME-80186 card to external signals. On the connector are 2 of the 3 counter/timers of the 80186 and 5 single bit TTL compatible inputs.

In addition, P2 contains one interrupt input, a TTL input, and a TTL output bit for custom applications.

SASI INTERFACE

For interfacing the 80186 card to floppy disks, hard disks, cartridge tapes and other mass storage devices, the VME-80186 includes a DMA controlled SASI port via the board's P2 connector. Necessary control of hard disk error management is included to interrupt and stop DMA transfers should a disk error occur. The VME-80186 does not latch the SASI data in either direction, instead the SASI interface is provided with a wait generator to assure that the SASI device has transferred the data before the 80186 processor is allowed to continue. Since an I/O cycle to the SASI port will normally not be started until the SASI device has issued a request, no timeout is required. J11 controls whether or not wait states are generated by the hardware during the select sequence. With J11 installed, the interface adheres to the SASI bus specifications. If a SASI controller is used (for example XEBEC 1410) which will respond with BUSY is less than 800 ns (the maximum 80186 built-in wait state timeout), then J11 may be removed. This allows automatic system configuration software to sense and check the presence of a variable number of connected controller devices.

The design of the VME-80186 allows multiple cards to share the same SASI interface bus. This allows direct disk to memory transfers without using the VMEbus in multicpu applications. This can significantly improve the system's throughput. The SASI bus can support a wide range of peripherals, including floppy disks, hard disks, tape drives and future storage media including laser disks. COLEX considers the SASI interface combined with the DMA of the 80186 to be the optimal method of system/drive interface.

Direct Memory Access transfers

The VME-80186 includes two DMA channels. One is dedicated for fast, transparent transfers of data between the SASI interface port and memory. Even with the fastest SASI devices, the processor still is operating at 50% throughput. When compared to typical programmed data transfers, the VME-80186 card will transfer data up to 10 times faster than non-dma applications. Also, having the memory on the came card as the SASI port saves bus accesses, resulting in far faster system operation.

The second DMA channel is free for use in memory-memory or memory-VMEbus short I/O transfers. Note that if both DMA channels are used at the same time with the VMEbus, that the same 512Kb block will be used (same register file).

A separate source and destination register file is provided to allow transfers on the VMEbus between different 512Kb blocks. The source register used will be the same as that used for CPU VMEbus accesses, the destination register is unique to the DMA. The card allows the DMA to be used with short I/O ports on the bus. Separate register files are provided for this operation mode.

EPROM SOCKETS

The VME-80186 card contains sockets for 2 EPROM devices of up to 32Kb each. The 80816 chips is programmable for the number of wait states required to allow for access times of a wide range of EPROM devices. The EPROMs are accessible only by the on-board 80186, not by the VMEbus.

Jumper J6 allows the type of EPROM used to be selected. Both EPROMs must use the same jumper connection.

J6

CPU A13	1.	.2	socket pin 26
n/c	3.	.4	+5 volts
CPU A14	5.	.6	socket pin 27

prom type	jumpers
2732	2-4
2764	2-4
27128	1-2
27256	1-2, 5-6

REAL TIME CLOCK

A battery backed-up real time calendar clock chip maintains current time with a 99 year calendar even during power-off conditions. Additionally, a timer interrupt output is available on P2 pin 6c for custom applications.

M3000 REAL TIME CLOCK PROGRAMMING

The programming of the M3000 chip is summarized in attached application note. More details can be found in the M3000 data sheet from MEM Microelectronic-Marin, Switzerland. The chip is organized as 16 byte registers, each accessable via 2, 4 bit (nibble) data transfers.

The M3000 provides a real time clock, alarm and timer function. Only the real time clock is typically used in the VME-80186, thus the 7 bytes used by the timer and alarm can be used as non-volatile ram instead. The clock is updated each second, and the update lasts 6 ms. The M3000 cannot be read during these updates since the data is changing, hence the busy signal should be checked before reading the clock. Once a I/O cycle by the 80186 has been started, the M3000 will not start an update until after the cycle is completed. Each cycle consists of 4 nibble transfers.

Busy can be detected by reading bit 8 of port 180H. The chip is busy when this bit is low. One of 16 addresses can be selected, and the data can be read or written via bit 0 - 3 of the I/O port 100H.

MSDOS SOFTWARE SUPPORT

A preinstalled MSDOS operating system is available to use the VME-80186 in a floppy or hard disk environment. This system allows program development directly on the COLEX VME-80186 card, with assembly and compilation times roughly 4 times faster that the IBM personal computer.

The MSDOS software package can be purchased for use with the VME-80186 in constructing a user assembled system. A turnkey complete packaged computer may also be purchased from COLEX including 10 Mb winchester hard disk, floppy backup, 3 slot VMEbus backplane and power supply in an attractive case.

Built-in firmware

COLEX ships the VME-80186 with a built-in program debugger to assist in testing of user generated programs, especially in applications using customer written software. The features of the debugger include:

Breakpoints set, clear 2 breakpoints
Dump memory in Intel format to the DTE port
Execute program
Fill memory area
Hexidecimal calculations
Load Intel format from DTE port
Memory display, update
Offset, set relative start address
Port display, update
Trace program in memory, display registers and status
eXamine and update register contents
Y turnsthedebugger into a terminal via the DTE port

I/O MAP

The I/O ports of the VME-80186 card are defined in the following table. The I/O ports of the VME-80186 are only accessible by the on-board 80186. All signals are active high unless preceded by a '/'. The polarity matches the signals shown in the connector pinout table. For example, the /STROBE output to the printer will go low when the port 192 is written with bit 0 low.

I/O Address	TYPE	FUNCTION
E000	RD/WR	SASI DATA PORT
		Serial I/O ports A and B
E080	RD/WR	SCC COMMAND CHANNEL B
E082	RD/WR	SCC DATA CHANNEL B
E084	RD/WR	SCC COMMAND CHANNEL A
E086	RD/WR	SCC DATA CHANNEL A
E100	RD/WR	Real Time Clock (RTC)
E180	RD	TTL input port

BIT number	Function
0	P6 X data
1	P6 Y data
2	P6 M data
3	P6 D data
4	P6 G data
5	Printer busy
6	Printer paper empty
7	/SYSFAIL
8	Real time clock busy
9	Colex use only
10	Colex use only
11	/ACFAIL
12	TTL input bit P2 pin 7c

E180	WR	not used
E190	RD	SASI status port

BIT	function
0	/RQ request
1	/MSG message
2	/BUSY busy
3	/I/O Input / Output status

I/O Address	TYPE	FUNCTION
E190-7	WR	Control ports (only bit 0 is used)
E190	WR	TTl output connector P2 pin 5c
E192	WR	not used
E194	WR	/STROBE to printer, active low
E196	WR	NMI enable when high
E198	WR	SASI RST reset, active high
E19A	WR	SASI SEL select, active high
E19C	WR	'FAIL' output to VMEbus, active high
E19E	WR	/LED status LED display, on when low

E200 register files: A19 to A23, plus address modifier

E200	WR	I/O source
E202	WR	I/O DMA destination
E204	WR	Memory source
E206	WR	Memory DMA destination
E280	WR	Printer data port

80816 chip PCS programming

The 80186 Programmable Chip Select (PCS) lines are programmed to provide the following addresses for on-board I/O. The above addresses assume the following programming is used.

PCS	DISPLACEMENT	PCS	DISPLACEMENT	
0	0	4	200H	
1	80H	5	280H	
2	100H	6	300H	not used
3	180H			

80186 INTERRUPTS

The 80186 has 5 interrupt inputs. They are used on the VME-80186 card as follows:

int0	VMEbus interrupt line 3
intl	P2 pin 6a
int2	VMEbus interrupt line 1
int3	SASI interface
int4	ACFAIL, BERR, Parity error

80186 TIMER COUNTERS

The 80186 chip has 3 counter/timer channels. The 2 full counter/timers are connected to 2 of the 7 input bits from P6. The third timer channel is used as a 1 ms clock input in the COLEX debugger and MSDOS. It is available for use in non MSDOS applications.

timer 0	P6 input 'X interrupt'
timer 1	P6 input 'Y interrupt'

VMEbus signal description

The signals used by the VME-80186 are:

/ACFAIL	input		indicates that the power supply is going to fail
/IACKIN	input		not used by slot 1 cards
/IACKOUT	output	TS	same as /IACK (slot 1)
Am0-AM5	output	TS	driven during bus cycles only
/AS	I/O	TS	address strobe
A01-A23	I/O	TS	addresses
/BBSY	output	OC	driven during bus cycles
/BCLR	output	TS	driven when VME-80186 wants bus
/BERR	I/O	OC	driven by parity error during slave cycles driven by bus timeout logic for all cycles
/BG3OUT	output	TS	acknowledge bus to requester
/BGxIN	input		not used by slot 1
/BR3	input output	 OC	starts bus arbitration driven low when the 80186 starts a bus access
/DS0	I/O	TS	low data byte transfer
/DS1	I/O	TS	high data byte transfer
/DTACK	I/O	TS	acknowledges end of cycle
D00-D15	I/O	TS	data bits
/IACK	output	TS	active when memory location c0000-c0007 is addressed
/IRQ1	input		request interrupt level 1
/IRQ3	input		request interrupt level 3
/LWORD	input		disables accesses to VME-80186
/SYSFAIL	I/O	OC	driven by 'FAIL' bit from 80186 readable by 80186 cpu
/SYSRESET	input		TTL input resets the card when low
/WRITE	I/O	TS	indicates write cycle on bus
/SYSCLK	output		16 MHz bus clock

VMEbus connector P1

pin	row a	row b	row c
1	D00	BBSY/	D08
2	D01	BCLR/	D09
3	D02	ACFAIL/	D10
4	D03		D11
5	D04		D12
6	D05		D13
7	D06		D14
8	D07		D15
9	Ground		Ground
10	SYSCLK		SYSFAIL/
11	Ground	BG3OUT/	BERR/
12	DS1/		SYSRESET/
13	DS0/		LWORD/
14	WRITE/		AM5
15	Ground	BR3/	A23
16	DTACK/	AM0	A22
17	Ground	AM0	A21
18	AS/	AM0	A20
19	Ground	AM0	A19
20	IACK/	Ground	A18
21			A17
22	IACKOUT/		A16
23	AM4	Ground	A15
24	A07	IRQ7/	A14
25	A06	IRQ7/	A13
26	A05	IRQ7/	A12
27	A04	IRQ7/	A11
28	A03	IRQ7/	A10
29	A02	IRQ7/	A09
30	A01	IRQ7/	A08
31	-12V	+5V Standby	+12V
32	+5V	+5V	+5V

Signals not listed are not used by the VME-80186 card.

INPUT / OUTPUT CONNECTORS P2 PINOUT

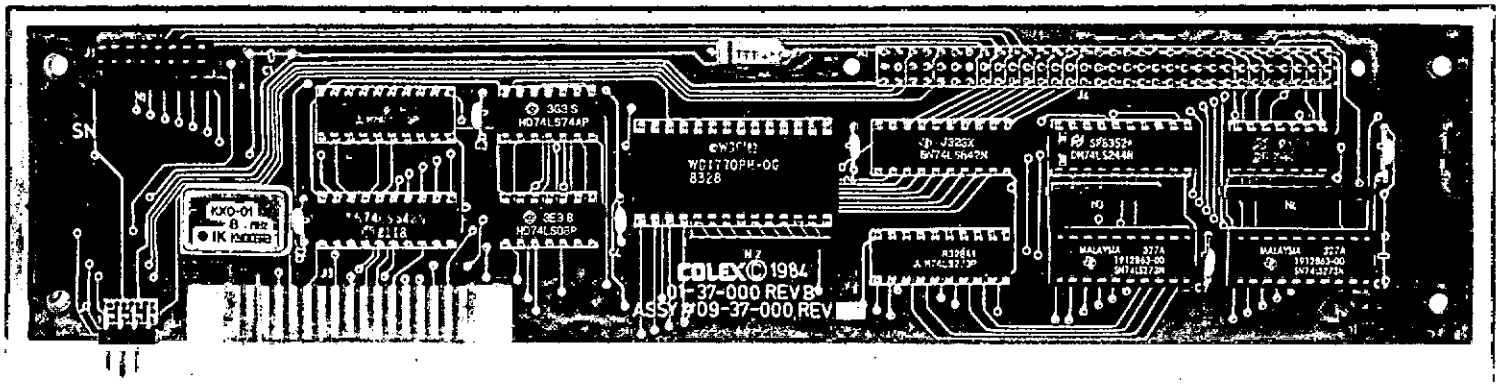
The VME-80186 board uses the second VME bus connector (P2) rows A and C for connections to system functions which would typically be found inside a computer chassis. P3 to p6 are on the front panel for ease of connection to terminals and modems. No connections to off-board functions are made from the card except via these front and back edge connectors.

Row b of P2 is not used by the VME-80186.

	Row a	Row c
pin	function	function
1	+5 volts	Ground
2	Ground	do not connect
3	do not connect	Ground
4	Ground	do not connect
5	do not connect	TTL output bit
6	Interrupt input bit	RTC Interrupt Request
7	Ground	TTL input bit
8	SASI DØ/	Ground
9	SASI Dl/	Ground
10	SASI D2/	Ground
11	SASI D3/	Ground
12	SASI D4/	Ground
13	SASI D5/	Ground
14	SASI D6/	Ground
15	SASI D7/	Ground
16		Ground
17		Ground
18		Ground
19		Ground
20		Ground
21		Ground
22		Ground
23		Ground
24		Ground
25	SASI BUSY/	Ground
26	SASI ACK/	Ground
27	SASI RESET/	Ground
28	SASI MSG/	Ground
29	SASI SEL/	Ground
30	SASI C/D/	Ground
31	SASI REQ/	Ground
32	SASI I/O/	Ground

FRONT PANEL CONNECTOR PINOUT

	DTE serial	DCE serial	Printer	Interrupts
	P3	P4	P5	P6
1	ground	ground	/STROBE	+5 volts
2	Transmit data	Receive data	data Ø	Y interrupt
3	Receive data	Transmit data	1	Y data
4	RTS out	RTS in	2	X interrupt
5	CTS in	CTS out	3	X data
6	DSR in	DSR out	4	ground
7	ground	ground	5	M data
8	-	-	6	D data
9	-	-	7	G data
1Ø	-	-	-	
11	-	-	BUSY	
12	-	-	PAPER EMPTY	
13	-	-	-	
14	clock out	-	ground	
15	sync I/O	-	ground	
16	-	-	ground	
17	clock in	-	ground	
18	-	-	ground	
19	-	-	ground	
2Ø	DTR out	DTR in	ground	
21	-	-	ground	
22	-	-	ground	
23	-	-	ground	
24	-	-	ground	
25	-	-	ground	



LFLP

For low cost addition of a floppy disk drive to the VME-80186 card, COLEX offers a SASI port-compatible floppy disk card. This controller card supports full double density operation and can use the DMA channel of the 80186 card's SASI port. It offers one-to-one direct pinout connection to the floppy disk units. It is supported by the VME-80186 built-in debugger and by MSDOS.

LFLP is mounted behind the VME backplane, it plugs directly into P2, and provides for a SASI interface connector to be installed for other mass storage controllers. An alternate version (XFLP) is available with a form factor for direct mounting onto the side of a 5.25" floppy disk.

Overview of jumpers

J1	DTE sync in
J2	DTE on-board clock
J3	DTE sync out
J4	Select VMEbus address
J5	Select VMEbus address
J6	EPROM type
J7	COLEX use only (strap pins 2-3)
J8	XRAM interface
J9	XRAM interface
J10	XRAM interface
J11	SASI wait on select
J12	Enable slot 1 functions
J13	selects either /BR3 or /BCLR for VMEbus access request

MECHANICAL SPECIFICATIONS

233.4 x 160 mm double eurocard.
Two 96 pin DIN 41612 connectors
20.8 mm height
Metal front panel with 4 'D' type connectors
Two hand grips for board removal

ELECTRICAL SPECIFICATIONS

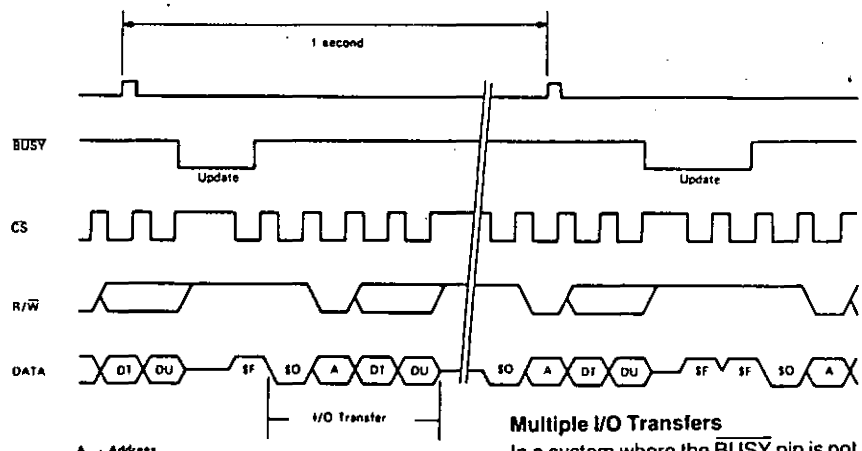
Power requirements

5V @ 5%	6.0 A
12V @ 5%	0.1 A
-12V @ 5%	0,1 A

ORDERING INFORMATION

VME-80186	Card as described with 128kb RAM. Includes manual and debugger in PROM.
XRAM	Plug-on 128kb RAM expansion card with parity. Includes installation instructions.
LFLP	Add-on low cost floppy controller with manual.
MSDOS	Floppy disk with MSDOS, MSDOS user manuals. Requires LFLP and system with 5.25" floppy disk or winchester hard disk.
VME-SYSCON	VME-80186 compatible card with full graphics video output.
COLEX-2000	Transportable computer with the VME-SYSCON, 10 Mb hard disk, 720Kb floppy disk, power supply, 3 slot VMEbus backplane, built-in video display, keyboard, MSDOS software and complete user manuals.
COLEX-2100	Desktop computer with the VME-SYSCON, 10 Mb hard disk, 720Kb floppy disk, power supply, 3 slot VMEbus backplane, MSDOS software and complete user manuals. Optional full graphics terminal and keyboard.
VME-MMCPU	68010 based UNIX processor card.
UNIX	System V Uniplus+ operating system. Can be installed into either the COLEX-2000 or 2100 system.

I/O Transfer Wateforms



A - Address.
DT - Data, tens
DU - Data, units

* Not available externally.

Status Control (Address F)

This address contains the information for setting the mode of operation of the M 3000. To set the required mode of operation, the information must be written into address F of the M 3000, according to the typical read/write sequence shown in the flow diagram.

Data Control (Address O E)

Data may be written or read at these addresses according to the typical read/write sequence shown in the flow diagram.

Mode of Operation

In the M 3000, depending on the status word contents, an up-date cycle occurs every second and lasts for a maximum of 6 ms. During the up-date cycle, the M 3000 clears the multiplexer (MUX) and sets the $\overline{\text{BUSY}}$ signal (pin 14) to "low". If a read-out is performed during the up-date cycle, the data will be "F", corresponding to the code "busy". A conflict between an up-date cycle and an I/O transfer may thereby be avoided. Before any I/O transfer, the processor should test the busy signal either by a read-out or by test of the busy signal at pin 14. If the M 3000 is not busy, the RAM is allocated to the external bus and an I/O transfer can be initiated (refer to fig. 4). If an internal up-date request occurs during an I/O transfer, the M 3000 waits until the end of the I/O transfer before initiating the up-date cycle. Therefore, the I/O transfer must be completed within one second to allow RAM access for the internal up-date cycle. If an I/O transfer is not completed, an internal up-date cycle is forced after a maximum of 2 seconds

I/O Address Locations

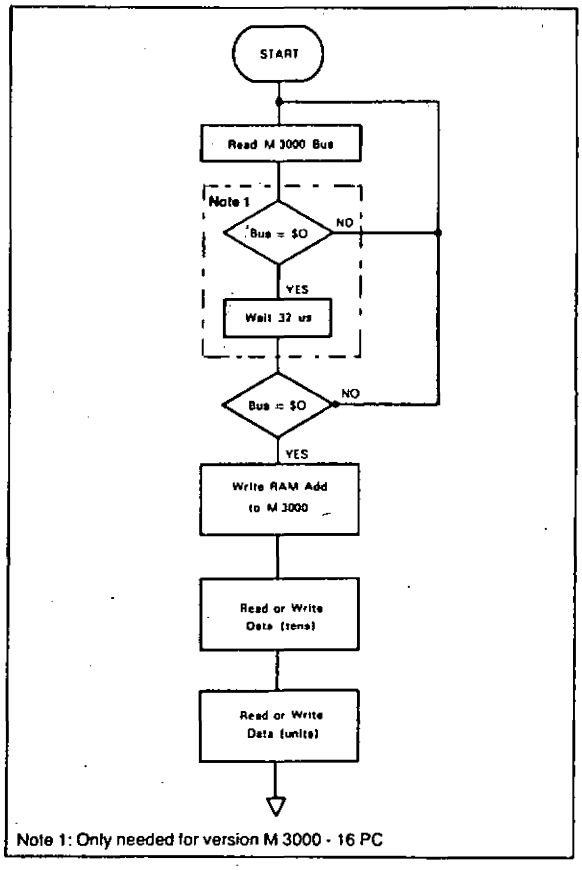
Address	Data	Group	Max. Value★	Operations
0	Seconds	WATCH	59	Time data locations
1	Minutes		59	incremented
2	Hours		23	by internal timing
3	Date		28, 29, 30, 31	circuitry under
4	Month		12	control of status Bit 0
5	Year		99	
6	Week day		07	
7	Week no.		53	
8	Seconds	ALARM	59	Alarm data locations
9	Minutes		59	preset by user
A	Hours		23	to provide IRQ output
B	Date		28, 29, 30, 31	at specified time
C	Seconds	TIMER	59	Timer data locations
D	Minutes		59	incremented under
E	Hours		23	control of status bit 4
F	Status	STATUS		Control

★ Only applicable to WATCH, ALARM and TIMER data. RAM locations not used for timing information may be used as NON-Volatile RAM. The RAM accepts data in hexadecimal format (possible contents 00 to FF). For example in a system where no ALARM or TIMER facility is needed, RAM address 0-7 are required for basic timekeeping leaving RAM addresses 8-E available as Non Volatile RAM.

Multiple I/O Transfers

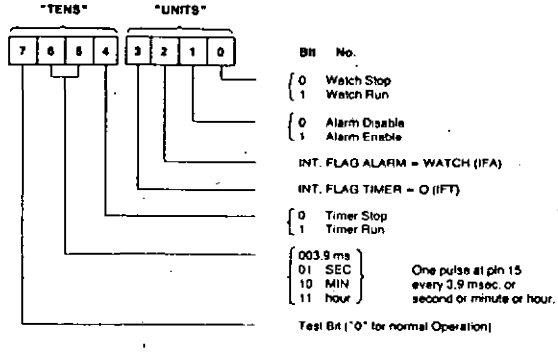
In a system where the $\overline{\text{BUSY}}$ pin is not used and many consecutives I/O transfers are required, eg. seconds, minutes, hours, date; it is necessary to read out the seconds again at the end of the I/O transfers. This is to ensure that no internal update has occured during two successive transfers.

Typical Read/Write Sequence



Note 1: Only needed for version M 3000 - 16 PC

Status Word Bit Allocations



COLEX LIMITED WARRANTY FOR STD BUS BOARDS

COLEX warrants this product against defects in materials or workmanship for one year from the date of purchase from COLEX. This limited warranty is subject to the following terms and conditions:

A. If the product has defects in materials or workmanship, COLEX will repair or replace the product, at COLEX's sole option, at no charge to you for the duration of this warranty.

(1) To obtain service under this warranty, obtain a return authorization number. In the United States contact the Colex Service Center for a return authorization number. Outside of the United States contact your local sales agent for a return authorization number

(2) Complete the REQUEST FOR WARRANTY SERVICE form included with the product. You must complete all items in this form. Send the product to your nearest COLEX service center, include the original of the REQUEST FOR WARRANTY SERVICE form, keep a copy of the form for yourself, and send a copy to the nearest COLEX regional headquarters. The regional headquarters addresses are printed on the REQUEST FOR WARRANTY SERVICE form.

(3) You must send the product postage prepaid and insured. You must enclose the product in an anti-static bag to protect the product from damage by static electricity. COLEX is not responsible for damage to the product due to static electricity.

B. This warranty does not apply to any products which have been modified, altered, or tampered with; to any products which have been subjected to abuse, accident, improper installation or misuse; to any products whose serial numbers have been removed; or to any products which have been repaired or serviced by other than an authorized representative of COLEX.

C. For the repair or replacement of any products not covered by this warranty, COLEX will repair or replace such products, at COLEX's sole option, at COLEX's then current charges for labor and materials.

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