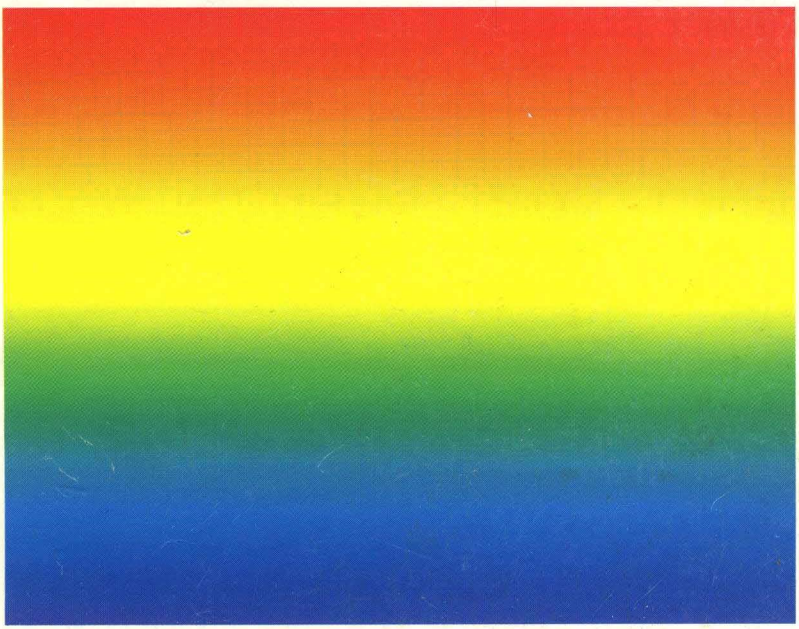
DCME-Q Series
User Information Manual

CLEARPOINT



DCME-Q Series

User Information Manual

Revision 1.1

If my memory serves me right . . . It must be Clearpoint®.

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Contents

Chapter 1 Introduction

1.1 Manual Overview

This manual is written for the individual with basic computer knowledge and some technical experience. If you have no technical background, it is suggested that you obtain the assistance of a technically-knowledgable individual before proceeding with the installation. If you do not have such access, call Clearpoint's Product Support line (see Chapter 4, page 28, for phone numbers) and request assistance.

— STATIC DISCHARGE WARNING —

All Clearpoint products are exhaustively tested prior to shipment to insure superior field performance. Failures in the field are largely attributed to component failure due to improper handling. Be sure to take all necessary precautions during installation, particularly for grounding to protect against ESD damage (electro-static discharge).

The manual covers the steps for installation of the board(s) in the system (Chapter 2), description of the CSR (Chapter 3), what to do in the event of a problem (Chapter 4), and supplementary information in Appendices A, B, C, and D.

1.2 Product Overview

1.2.1 Product Features

This manual supplies user information for the DCME-Q Series of memory modules. DCME-Q modules provide high density, low cost per bit storage for systems which utilize the Digital Equipment Corporation (hereafter referred to as DEC) Q-BUS. 256 Kb[1] MOS RAMS are used as individual storage devices to provide up to 4MB[2], or 64 Kb MOS RAMS for up to 1 MB, on a single quad-height or dual-height board.

1.2.2 Table 1 - DCME-Q Series Products

Product Number	Quad Height Board Size	DRAM Type
DCME-Q4B/4MB	4 MB	256 Kb MOS RAMS
DCME-Q4B/3.5	3.5 MB	256 Kb MOS RAMS
DCME-Q4B/2MB	2 MB	256 Kb MOS RAMS
DCME-Q4B/1MB	1 MB	256 Kb MOS RAMS
DCME-Q4B/1MB	1 MB	64 Kb MOS RAMS
DCME-Q4B/512KB	512 KB	64 Kb MOS RAMS
Product Number	**Dual Height Board Size**	**DRAM Type**
DCME-Q2B/2MB	2 MB	256 Kb MOS RAMS
DCME-Q2B/1MB	1 MB	256 Kb MOS RAMS
DCME-Q2B/512KB	512 KB	64 Kb MOS RAMS
DCME-Q2B/256KB	256 KB	64 Kb MOS RAMS
DCME-Q2A/512KB	512 KB	64 Kb MOS RAMS
DCME-Q2A/256KB	256 KB	64 Kb MOS RAMS

The DCME-Q Series offers the following features:

- Up to 4 MB memory capacity
- Jumper selectable 18- or 22-bit addressing
- Parity generation and checking on board
- Complete DEC software-hardware compatible, parity control and status register on-board locatable at any of 8 assigned I/O page addresses
- Battery back-up support [3]
- Single 5 volt power supply
- Starting address programmable at any 64KB, 256KB, or 512KB boundary
- Parity error LED provides visual indication of board failure
- Block Mode DMA on the Q2B and Q4B boards
- Factory upgrade available up to 2 MB for Q2B boards, up to 4 MB for Q4B boards

[1] Mb and Kb represent megabits and kilobits.
[2] MB and KB represent megabytes and kilobytes.
[3] Battery backup on the DCME-Q2A is available as a special revision from Clearpoint.

1.2.3 Specifications

Characteristics	Specifications		
	DCME-Q4B	DCME-Q2B	DCME-Q2A
Read access time	200 ns typ.	85 ns typ.	225 ns typ.
Write access time	50 ns typ.	60 ns typ.	50 ns typ.
Memory cycle time	450 ns typ.	300 ns typ.	450 ns typ.
+5V operating current typ.-max.	1.9-2.1 amp	1.6-2.0 amp	1.4-1.8 amp
+5V BBU current	0.9 amp typ.	0.7 amp typ.	0.7 amp typ.
Operating temperature	0° to +65° C		
Storage temperature	-40° to +85° C		
Relative humidity	0 to 90% (non-condensing)		
Voltages required	+5V +5% pins BU1,AA2,BA2		
BBU voltage	+5V +5% pins AV1,AS1*,AE1*		

* optional spares available on backplane

1.2.4 Physical Description

The DCME-Q module is a single quad-height or dual-height memory module which interfaces to the LSI-11 Q-BUS. All timing and control logic for the memory, refresh circuitry, parity control, and status register are contained on board. The MOS memory array consists of up to eight rows of 262,144 X 1 bit dynamic RAM devices with 18 devices per row [65,536 X 1 bit for the 64 Kb MOS RAM boards]. Each row will accept 262,144 18-bit words [65,536 18-bit words for the 64 Kb MOS RAM boards] consisting of (two) eight-bit bytes and two parity bits (one per byte). Circuitry for refresh of the MOS memory devices is provided on board and operates transparently to the user.

1.3 Backplane Pin Utilization

Table 2 contains the backplane power pins required for DCME-Q4B. Table 3 designates the pins used for other signals.

1.3.1 Table 2 - Backplane Power Pins Required

Voltage	Pin
+5 normal	BV1
	AA2
	BA2
Ground	AT1
	BT1
	AC2
	BC2
+5 battery (if used)	AV1
+5 Battery spare (if used)	AS1
	AE1

1.3.2 Table 3 - Backplane I/O Signal Pins

Signal	Pin
AC1	BDAL 16
AD1	BDAL 17 L
BA1	BDCOK H
BC1	BDAL 18 L
BD1	BDAL 19 L
BE1	BDAL 20 L
BF1	BDAL 21 L
AE2	BDOUT L
AF2	BRPLY L
AH2	BDIN L
AJ2	BSYNC L
AK2	BWTBT L
AM2	BIAKI L
AN2	BIAKO L
AP2	BBS7 L
AR2	BDMGI L
AS2	BSMGO L
AU2	BDAL 00 L
AV2	BDAL 01 L
BE2	BDAL 02 L
BF2	BDAL 03 L
BH2	BDAL 04 L
BJ2	BDAL 05 L
BK2	BDAL 06 L
BL2	BDAL 07 L
BM2	BDAL 08 L
BN2	BDAL 09 L
BP2	BDAL 10 L
BR2	BDAL 11 L
BS2	BDAL 12 L
BT2	BDAL 13 L
BU2	BDAL 14 L
BV2	BDAL 15 L

Chapter 2 Hardware

2.1 Chapter Overview

Chapter 2 provides information for configuring the DCME-Q4B, DCME-Q2B and DCME-Q2A jumper options prior to system installation. Following the configuration sections, installation and checkout procedures are explained.

— Static Discharge Warning —

It is important that you protect the memory boards from static discharge. An undetected static charge can damage a board and cause apparent system failure and data corruption. Be sure to be properly grounded before handling any memory board.

2.2 Preparation for Installation - Inspection

1. Before removing memory board(s) from the protective anti-static plastic container, be sure that you are grounded, either with a wrist or heel strap for that purpose.
2. Once you are properly grounded, remove the memory board from the anti-static plastic container and carefully examine it for any damage (bent corners, loose chips, etc.). If there is any visible damage, call Clearpoint immediately. (See Chapter 4 for details about Clearpoint's Product Support Engineering.)
3. Copy the DCME-Q Series Revision letter(s) and Serial number (found on the yellow bar code sticker) from each board into Chapter 4, page 28 of this manual. (See Figure 2, 3, or 4 which illustrates the location of these letters/numbers on your board.)
4. Return each board to the plastic container until you are ready for installation.

2.3 Configuring the DCME-Q Series Jumpers

All DCME-Q Series boards have jumpers that need to be configured in order for the system to recognize the memory size and other options. The figure below shows these configuration options. The board comes with jumper plugs installed. Sections 2.4, 2.5, and 2.6 provide explanation of the appropriate settings for the DCME-Q4B, DCME-Q2B amd DCME-Q2A boards.

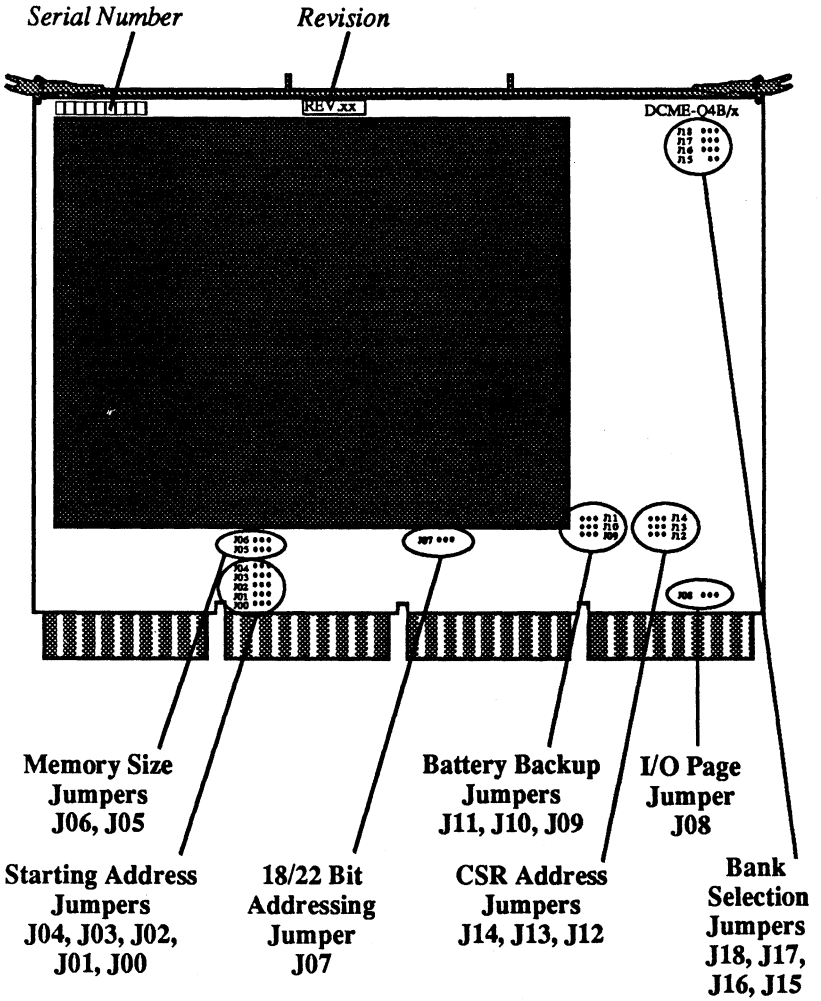
To change a jumper setting, use a needle-nose pliers to remove the cap and re-position it as directed in the relevant diagram.

2.3.1 Figure 1 - Jumpers Description

2.4 DCME-Q4B Jumper Settings

Figure 2 provides the locations of the various DCME-Q4B option jumpers. The module should be inspected prior to installation to ensure that it has been properly configured. Section 2.4 describes the various DCME-Q4B jumper options.

2.4.1 Figure 2 - DCME-Q4B Jumper Indentification



2.4.2 Starting Address Selection

The memory starting address may be programmed at any 128 KB boundary using jumpers J00 through J04.

BDALxx refers to the address line that the memory board responds to. The jumpers for each board correspond to a particular address, so must be configured for the appropriate starting address. Use Table 4 below to identify the DCME-Q4B jumpers which correspond to the address lines used to set the starting address. Then **Appendix A** (p.29) is used to determine the jumper configurations by starting address. Write the jumper names from Table 4 into the Table headings of **Appendix A** above the corresponding address lines. Draw a line across the **Appendix A** Table under the starting address for this installation. This will underline the jumper configurations to be set.

Example: For an installation with 2 MB of existing resident memory, write in J04 through J00 above BDAL21 through BDAL17 in **Appendix A.** Draw a line across under 2048 KB (2 MB) in the Starting Address column. The settings for this installation are J04 - Left, J03 - Right, J02 - Right, J01 - Right, J00 - Right

2.4.3 Table 4 - DCME-Q4B Starting Address Jumpers

J04	J03	J02	J01	J00
BDAL21	BDAL20	BDAL19	BDAL18	BDAL17

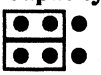
2.4.4 Board Size Selection

Jumpers J05 and J06 are used to configure the board size. DCME-Q4B boards have up to eight rows of 262,144 x 1 bit or 65,536 x 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 262,144 (256 KB) or 65,536 (64 KB) 18-bit words. A DCME-Q4B may provide 256, 512, 1024, 2048, or 4096 KB. J05 and J06 must be configured, as shown in Table 5, to match the size of the memory array on board.

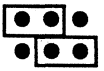
2.4.5 Table 5 - Memory Size Jumpers

Board Memory Capacity

4 MB J06 J05

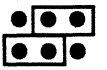


2 MB J06 J05

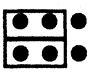


1 MB J06 J05

512 KB J06 J05



256 KB J06 J05



To configure jumpers for the DCME-Q4B/3.5 MB board, see ***Appendix C.***

2.4.6 18/22 Bit Selection

DCME-Q4B addressing logic is capable of either 22- or 18-bit operation. J07 is used to select the desired addressing mode as follows:

18-Bit Address J07 

22-Bit Address J07 

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18-bit addressing mode is selected and the board may not be configured to respond to addresses above 256 KB.

2.4.7 I/O Page Selection

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-BUS. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4 KW[1] I/O page space. BBS7 is asserted whenever an I/O page transfer is requested. The memory board should ignore all transfers requested within the I/O space. If, however, there are few peripherals on the system and it is desired by the user to reserve only 2 KW of the I/O page space, jumper J08 may be used as follows:

4 KW I/O Page J08 

2 KW I/O Page J08 

2.4.8 Battery Backup Option

The MOS memory, unlike core memory, requires the 5 volt supply to retain data. If the 5V power is removed from the board, system memory data is lost.

The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5V input pin. Table 6 shows the various configurations of the battery backup mode select jumpers J09, J10, and J11.

2.4.9 Table 6 - Battery Backup Mode Jumpers

No Backup

J11 

J10 

J09 

Battery Backup +5 AV1, AS1

J11 

J10 

J09 

Backup +5 AVI (AS1, AE1 unused)

J11 

J10 

J09 

Battery Backup +5 AV1, AE1

J11 

J10 

J09 

[1] KW represents KWord.

2.4.10 CSR Address Selection

The parity control and status register (hereafter referred to as CSR) has an I/O page address in the top 4KW of memory. This address may be any one of eight specific locations reserved by DEC for this purpose. Jumpers J12, J13, and J14 are used to select one of the reserved addresses. Table 7 illustrates the use of these jumpers. Note that each memory board used in a system must be configured to a different address.

2.4.11 Table 7 - CSR Address Jumpers

CSR Address			CSR Address		
772100	J14		772110	J14	
	J13			J13	
	J12			J12	
772102	J14		772112	J14	
	J13			J13	
	J12			J12	
772104	J14		772114	J14	
	J13			J13	
	J12			J12	
772106	J14		772116	J14	
	J13			J13	
	J12			J12	

No CSR or Parity -To disable parity, remove J12, J13, and J14 jumper caps.

2.4.12 Bank Selection

To enable bank selection, jumpers J15, J16, J17, and J18 (see Figure 2) are used. If all of these jumpers are "out" (see Figure 1), the bank select feature is disabled. For further discussion of the bank selection option, see Appendix D, p. 33.

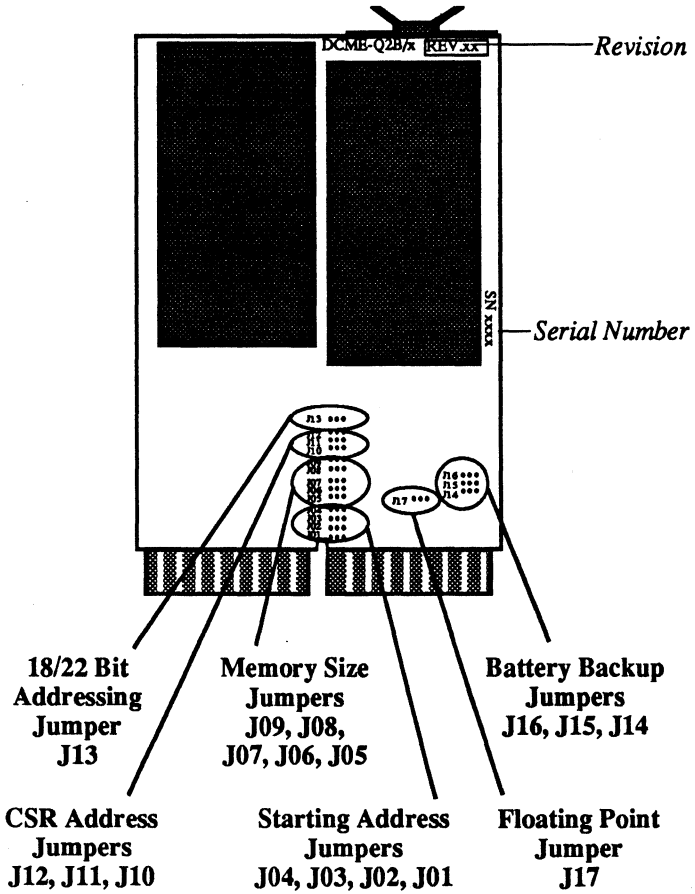
Jumper Configurations are complete.

Proceed to Section 2.7 Hardware Installation, p. 23.

2.5 DCME-Q2B Jumper Settings

Figure 3 provides the locations of the various DCME-Q2B option jumpers. The module should be inspected prior to installation to ensure that it has been properly configured. Section 2.5 describes the various DCME-Q2B jumper options.

2.5.1 Figure 3 - DCME-Q2B Jumper Identification



2.5.2 Starting Address Selection

The memory starting address may be programmed at any boundary which is a multiple of the board size using jumpers J01 through J04. The 256 KB board may be set at any 256 KB boundary, the 512 KB board at any 512 KB boundary, the 1 MB board at any 1024 KB boundary. **The DCME-Q2B can only be placed over resident memory sizes that are multiples of the DCME-Q2B board size.**

BDALxx refers to the address line that the memory board responds to. The jumpers for each board correspond to a particular address, so must be configured for the appropriate starting address. Use Table 8 below to identify the DCME-Q2B jumpers which correspond to the address lines used to set the starting address. Then **Appendix A** is used to determine the jumper configurations by starting address. Write the jumper names from Table 8 into the Table headings of **Appendix A** above the corresponding address lines. Draw a line across the **Appendix A** Table under the starting address for this installation. This will underline the jumper configurations to be set.

Example: For an installation with 2 MB of existing resident memory, write in J04 through J01 above BDAL21 through BDAL18 in **Appendix A.** Draw a line across under 2048 KB (2 MB) in the Starting Address column. The settings for this installation are J04 - Left, J03 - Right, J02 - Right, J01 - Right.

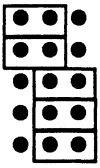
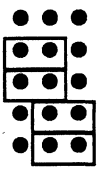
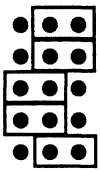
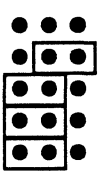
2.5.3 Table 8 - DCME-Q2B Starting Address Jumpers

J04	J03	J02	J01
BDAL21	BDAL20	BDAL19	BDAL18

2.5.4 Board Size Selection

Jumpers J05, J06, J07, J08, and J09 are used to configure the board size. DCME-Q2B boards have up to four rows of 262,144 x 1 bit or 65,536 x 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 262,144 (256 KB) or 65,536 (64 KB) 18-bit words. A DCME-Q2B may provide 256, 512, 1024, or 2048 KB. J05 through J09 must be configured, as shown in Table 9, to match the size of the memory array on board.

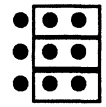
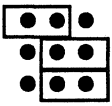
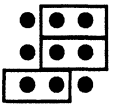
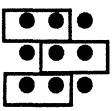
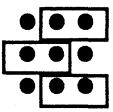
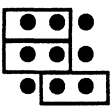
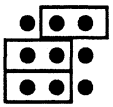
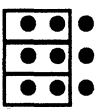
2.5.5 Table 9 - Memory Size Jumpers

2 MB	J09		1 MB	J09		Use 256 Kb DRAMs
	J08			J08		
	J07			J07		
	J06			J06		
	J05			J05		
512 KB	J09		256 KB	J09		Use 64 Kb DRAMs
	J08			J08		
	J07			J07		
	J06			J06		
	J05			J05		

2.5.6 CSR Address Selection

The parity control and status register (hereafter referred to as CSR) has an I/O page address in the top 4KW of memory. This address may be any one of eight specific locations reserved by DEC for this purpose. Jumpers J10, J11, and J12 are used to select one of the reserved addresses. Table 10 illustrates the use of these jumpers. Note that each memory board used in a system must be configured to a different address.

2.5.7 Table 10 - CSR Address Jumpers

CSR Address			CSR Address		
772100	J12		772110	J12	
	J11			J11	
	J10			J10	
772102	J12		772112	J12	
	J11			J11	
	J10			J10	
772104	J12		772114	J12	
	J11			J11	
	J10			J10	
772106	J12		772116	J12	
	J11			J11	
	J10			J10	

No CSR or Parity -To disable parity, remove J12, J11, and J10 jumper caps.

2.5.8 18/22 Bit Selection

DCME-Q2B addressing logic is capable of either 22- or 18-bit operation. J13 is used to select the desired addressing mode as follows:

18-Bit Address	J13	
22-Bit Address	J13	

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18-bit addressing mode is selected and the board may not be configured to respond to addresses above 256 KB.

2.5.9 Battery Backup Option

The MOS memory, unlike core memory, requires the 5 volt supply to retain data. If the 5V power is removed from the board, system memory data is lost.

The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5V input pin. Table 11 shows the various configurations of the battery backup mode select jumpers J14, J15, and J16.

2.5.10 Table 11 - Battery Backup Mode Jumpers

No Backup

J16 
J15 
J14 

Battery Backup +5 AV1, AS1

J16 
J15 
J14 

Backup +5 AVI (AS1, AE1 unused)

J16 
J15 
J14 

Battery Backup +5 AV1, AE1

J16 
J15 
J14 

2.5.11 Floating Point Compatibility

The DCME-Q2B is configured to run with the Floating Point compatibility enabled. To run the DCME-Q2B in a system without floating point move the jumper J17 to the Disable position.

Floating Point Enabled	J17	
Floating Point Disabled	J17	

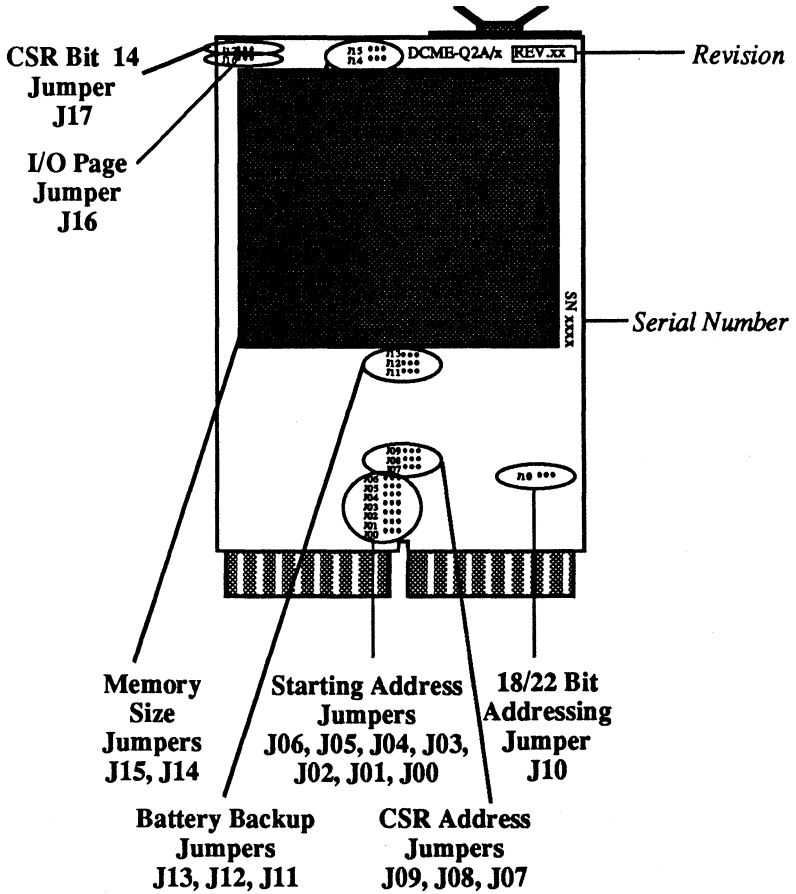
Jumper Configurations are complete.

Proceed to Section 2.7 Hardware Installation, p. 23.

2.6 DCME-Q2A Jumper Settings

Figure 4 provides the locations of the various DCME-Q2A option jumpers. The module should be inspected prior to installation to ensure that it has been properly configured. Section 2.6 describes the various DCME-Q2A jumper options.

2.6.1 Figure 4 - DCME-Q2A Jumper Identification



2.6.2 Starting Address Selection

The memory starting address may be programmed at any 32 KB boundary using jumpers J00 through J06.

BDALxx refers to the address line that the memory board responds to. The jumpers for each board correspond to a particular address, so must be configured for the appropriate starting address. Use Table 12 below to identify the DCME-Q2A jumpers which correspond to the address lines used to set the starting address. Then **Appendix A** (p. 29) is used to determine the jumper configurations by starting address. Write the jumper names from Table 12 into the Table headings of **Appendix A** above the corresponding address lines. Draw a line across the **Appendix A** Table under the starting address for this installation. This will underline the jumper configurations to be set.

Example: For an installation with 1 MB of existing resident memory, write in J06 through J00 above BDAL21 through BDAL15 in **Appendix A.** Draw a line across under 1024 KB (1 MB) in the Starting Address column. The settings for this installation are J06 - Right, J05 - Left, J04 - Right, J03 - Right, J02 - Right, J01 - Right, J00 - Right.

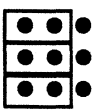
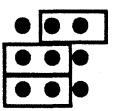
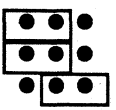
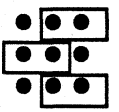
2.6.3 Table 12 - DCME-Q2A Starting Address Jumpers

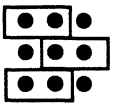
J06	J05	J04	J03	J02	J01	J00
BDAL21	BDAL20	BDAL19	BDAL18	BDAL17	BDAL16	BDAL15

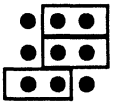
2.6.4 CSR Address Selection

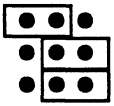
The parity control and status register (hereafter referred to as CSR) is accessed at the top portion of memory. This address may be any one of eight specific locations reserved by DEC for this purpose. Jumpers J07, J08, and J09 are used to select one of the reserved addresses. Table 13 illustrates the use of these jumpers. Note that each memory board used in a system must be configured to a different address.

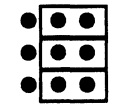
2.6.5 Table 13 - CSR Address Jumpers

CSR Address			CSR Address		
772100	J09		772110	J09	
	J08			J08	
	J07			J07	
772102	J09		772112	J09	
	J08			J08	
	J07			J07	

772104 J09 J08 J07 

772114 J09 J08 J07 

772106 J09 J08 J07 

772116 J09 J08 J07 

No CSR or Parity -To disable parity, remove J09, J08, and J07 jumper caps.

2.6.6 18/22 Bit Selection

DCME-Q2A addressing logic is capable of either 22- or 18-bit operation. J10 is used to select the desired addressing mode as follows:

18-Bit Address J10 

22-Bit Address J10 

BDAL 18, BDAL 19, BDAL 20, and BDAL 21 are ignored if 18-bit addressing mode is selected and the board may not be configured to respond to addresses above 256 KB.

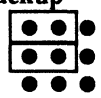
2.6.7 Battery Backup Option

On the DCME-Q2A, the battery backup option is available as a special revision pre-wired by the manufacturer. If you purchased this revision, you should confirm the correct configuration of the battery backup jumpers.

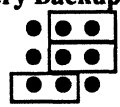
The battery backup option is used if battery power is available to maintain system memory data during power failures. Battery backup 5V must be available on backplane pin AV1. AS1 or AE1 may be used as an additional battery backup 5V input pin. Table 14 shows the various configurations of the battery backup mode select jumpers J11, J12, and J13.

2.6.8 Table 14 - Battery Backup Mode Jumpers

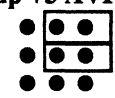
No Backup

J13 J12 J11 

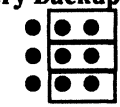
Battery Backup +5 AV1, AS1

J13 J12 J11 

Backup +5 AVI (AS1, AE1 unused)

J13 J12 J11 

Battery Backup +5 AV1, AE1

J13 J12 J11 

2.6.9 Board Size Selection

Jumpers J14 and J15 are used to configure the board size. DCME-Q2A boards have up to four rows of 65,536 x 1 bit dynamic RAM devices with 18 devices per row. Each row will accept 65,536 (64 KB)18 bit words. A DCME-Q2A may have 1, 2, 3, or 4 rows of memory chips corresponding to 128, 256, 384, or 512 KB respectively. J14 and J15 must be configured, as shown in Table 15, to match the size of the memory array on board.

2.6.10 Table 15 - Memory Size Jumpers

512 KB J15 
J14 

384 KB J15 
J14 

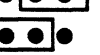
256 KB J15 
J14 

128 KB J15 
J14 

2.6.11 I/O Page Selection

The BBS7 signal is used during the address portion of a data transfer cycle on the Q-BUS. It indicates that the bus master is requesting a data transfer with one of the I/O devices in the 4 KW[1] I/O page space. BBS7 is asserted whenever an I/O page transfer is requested. The memory board should ignore all transfers requested within the I/O space. If, however, there are few peripherals on the system and it is desired by the user to reserve only 2 KW of the I/O page space, jumper J16 may be used as follows:

4 KW I/O Page J16 

2 KW I/O Page J16 

2.6.12 CSR Bit 14 Selection

For software which requires bit 14 of the CSR to be read only and always 0, jumper J17 is provided.

CSR bit 14 may be set J17 

CSR bit 14 is always 0 J17 

Jumper configurations are complete.

Proceed to Section 2.7 Hardware Installation, p. 23.

[1] KW represents KWord.

2.7 Installation Procedure

The following procedure should be followed when a DCME-Q Series board is received.

1. Visually inspect the module to make sure that it has arrived in good condition.
2. Set up jumper configuration options for required operation.
3. Verify that the required power connections are available on the backplane (see Table 2, p. 8).
4. Power down the system. Make sure that the system is powered off before plugging in any module.
5. Plug the module into the Q-Bus. Some DEC literature suggests that memories be installed in sequential slots following the CPU. However, any place in the backplane is sufficient. Do make sure that the module is not being inserted backwards; the component side must face in the same direction as other modules in the system.
6. Power up the system and run any DEC memory diagnostic as an initial test. If available, use the following diagnostics:

   MAINDEC-11 CVMSA (22-bit system diagnostic)

   MAINDEC-11 CZKMA (18-bit system diagnostic)

Chapter 3

CSR Description

3.1 Chapter Overview

When any byte is written to DCME-Q Series boards with parity option, a parity bit is generated which is stored along with the byte of data in the memory array. Whenever a byte of data is read, the parity logic checks it against the stored parity bit. If parity is bad, an error has occurred and data is assumed to be bad.

In order for software to utilize the parity generation and checking circuitry in the DCME-Q Series board, a control and status register (CSR) is provided. The CSR is assigned an address in the I/0 page which may be accessed by software. When a parity error is detected, the upper address bits of the bad memory location (All to A21) are latched in the CSR. Control bits are provided in the CSR to enable *interrupt on error* and *write of bad parity* for diagnostic purposes.

3.2 CSR Bit Assignment

The CSR is a 16-bit register located in the I/O page. The function of the 16 bits in the CSR are as follows:

1. Bit 0 - Parity error interrupt enable

   If set to 1, the memory board will interrupt the processor on error, by setting bits BDAL 17 and BDAL 16 along with the data bits BDAL 0 to BDAL 15. This will result in an LSI-11 processor trap to location 114. BUS INIT clears this bit.

2. Bit 1 - UNUSED

3. Bit 2 - Write wrong parity

   If this bit is set to 1, any word or byte written to the array will be stored along with an incorrect parity bit. This is for maintenance purposes. It enables diagnostics to check the boards' ability to detect parity errors and interrupt when enabled. This bit is cleared by BUS INIT.

4. Bit 3 - UNUSED

5. Bit 4 - UNUSED

6. Bit 5 THRU 11 - Latch address bits

   When a parity error is detected, the upper address bits of the failing location are latched. These bits are not cleared by BUS INIT, but are writeable, as well as readable. When an error is detected, address bits 11 to 21 are displayed in these bits. Since there are only 7 bits and there are 11 latched address bits, they are multiplexed. Bit 14 in the CSR controls which of the latched address bits are on display. (See Table 16 below.)

7. Bit 12 - UNUSED

8. Bit 13 - UNUSED

9. Bit 14 - Extended CSR read enable

   (See Table 16.) This bit is used to multiplex the extended latched address bits A18 to A21 into the CSR bits 5 to 11. This bit is cleared by BUS INIT. Jumper J17 may be used to disable setting of bit 14. If jumper J17 is on, CSR bit 14 is always 0.

3.2.1 Table 16 - CSR Bits 5 to 11

CSR Bit	If CSR Bit 14=0	If CSR Bit 14=1
05	Latched A11	Latched A18
06	Latched A12	Latched A19
07	Latched A13	Latched A20
08	Latched A14	Latched A21
09	Latched A15	0
10	Latched A16	0
11	Latched A17	0

10. Bit 15 Parity error flag

    This bit is set if a parity error is detected and remains set until cleared either by being written over or by invoking BUS INIT command.

Chapter 4 Problems?

4.1 Chapter Overview

Clearpoint offers a lifetime warranty. In the event a board does not work, call one of the numbers listed on the next page, and Clearpoint's Product Support Engineering will help you solve your problem with immediate telephone support, on-call 24 hours/day, 7 days/week.

Clearpoint's Lifetime Warranty Policy

Clearpoint warrants this memory product against defects in workmanship and materials for the life of the product. In the event of failure, Clearpoint will repair or replace (at our discretion) the defective memory product.

To obtain service under this warranty, you must call the Clearpoint Product Support Department and obtain a **Return Material Authorization** number. You will then need to provide them with the Clearpoint Product Name, Size, Serial Number, Revision code and symptoms of the problem. You must then ship the defective material to Clearpoint in its **original** packaging with the RMA number written on the outside. Clearpoint will then either ship you a replacement board or repair the defective board.

Shipping and insurance charges from the customer to Clearpoint are to be paid by the customer. Shipping and insurance charges from Clearpoint to the customer are to be paid by Clearpoint.

> **NOTE:** These memory products can be damaged by **Electro-Static Discharge (ESD).** If they are not packaged in the original packaging designed to protect them from ESD, they may be damaged and the warranty may be voided.

THIS WARRANTY IS LIMITED AND DOES NOT APPLY TO CONDITIONS RESULTING FROM IMPROPER USE, IMPROPER INSTALLATION OR UNAUTHORIZED MODIFICATIONS TO THE MEMORY PRODUCTS.

4.3 Calling Product Support

Clearpoint provides its customers with 24-hour Product Support assistance.

In the United States, call toll free, 1-800-332-2578.

In Canada, call toll free, 1-800-243-2578.

In Europe, call The Netherlands, +31-206540250, during business hours.

International, call 1-508-435-7400.

FAX: 508-435-7504

Return of all product must be accompanied by a **Return Material Authorization** number. To obtain this RMA number, call Product Support with the following information:

1. Clearpoint Part Name/Number: DCME-Q/_____
2. Configuration (memory size): _____
3. Serial Number: _____
4. Revision Number: _____
5. Reason for Return: _____
6. Return Ship address: _____

   _____

   _____
7. Bill to Address: _____

   _____

   _____
8. Purchase/Sales Order Number: _____
9. CPU: _____
10. Operating System: _____
11. Other Peripherals: _____

    _____

    _____

APPENDIX A

Starting Address Chart

Jumper Configuration By Starting Address

Note the corresponding jumpers for your board here:

Starting Address	BDAL21	BDAL20	BDAL19	BDAL18	BDAL17	BDAL16	BDAL15
0000	R	R	R	R	R	R	R
32KB	R	R	R	R	R	R	L
64KB	R	R	R	R	R	L	R
96KB	R	R	R	R	R	L	L
128KB	R	R	R	R	L	R	R
160KB	R	R	R	R	L	R	L
192KB	R	R	R	R	L	L	R
224KB	R	R	R	R	L	L	L
256KB .25MB	R	R	R	L	R	R	R
288KB	R	R	R	L	R	R	L
320KB	R	R	R	L	R	L	R
352KB	R	R	R	L	R	L	L
384KB	R	R	R	L	L	R	R
416KB	R	R	R	L	L	R	L
448KB	R	R	R	L	L	L	R
480KB	R	R	R	L	L	L	L
512KB .50MB	R	R	L	R	R	R	R
544KB	R	R	L	R	R	R	L
576KB	R	R	L	R	R	L	R
608KB	R	R	L	R	R	L	L
640KB	R	R	L	R	L	R	R
672KB	R	R	L	R	L	R	L
704KB	R	R	L	R	L	L	R
736KB	R	R	L	R	L	L	L
768KB .75MB	R	R	L	L	R	R	R
800KB	R	R	L	L	R	R	L
832KB	R	R	L	L	R	L	R
864KB	R	R	L	L	R	L	L
896KB	R	R	L	L	L	R	R
928KB	R	R	L	L	L	R	L
960KB	R	R	L	L	L	L	R
992KB	R	R	L	L	L	L	L
1024KB 1.00MB	R	L	R	R	R	R	R

Continued

Note the corresponding jumpers for your board here:

Starting Address	BDAL21	BDAL20	BDAL19	BDAL18	BDAL17	BDAL16	BDAL15
1056KB	R	L	R	R	R	R	L
1088KB	R	L	R	R	R	L	R
1120KB	R	L	R	R	R	L	L
1152KB	R	L	R	R	L	R	R
1184KB	R	L	R	R	L	R	L
1216KB	R	L	R	R	L	L	R
1248KB	R	L	R	R	L	L	L
1280KB [1.25MB]	R	L	R	L	R	R	R
1312KB	R	L	R	L	R	R	L
1344KB	R	L	R	L	R	L	R
1376KB	R	L	R	L	R	L	L
1408KB	R	L	R	L	L	R	R
1440KB	R	L	R	L	L	R	L
1472KB	R	L	R	L	L	L	R
1504KB	R	L	R	L	L	L	L
1536KB [1.50MB]	R	L	L	R	R	R	R
1568KB	R	L	L	R	R	R	L
1600KB	R	L	L	R	R	L	R
1632KB	R	L	L	R	R	L	L
1664KB	R	L	L	R	L	R	R
1696KB	R	L	L	R	L	R	L
1728KB	R	L	L	R	L	L	R
1760KB	R	L	L	R	L	L	L
1792KB [1.75MB]	R	L	L	L	R	R	R
1824KB	R	L	L	L	R	R	L
1856KB	R	L	L	L	R	L	R
1888KB	R	L	L	L	R	L	L
1920KB	R	L	L	L	L	R	R
1952KB	R	L	L	L	L	R	L
1984KB	R	L	L	L	L	L	R
2016KB	R	L	L	L	L	L	L
2048KB [2.00MB]	L	R	R	R	R	R	R

NOTE:

For a starting address above 2 MB, subtract 2 MB from the starting address, set the jumpers according to that value on the table, and set BDAL21 to the Left.

Not all of the above address lines will be used. Select the appropriate address lines for your specific board.

APPENDIX B

Explaining Block Mode DMA

B.1 Introduction

The DCME-Q4B and DCME-Q2B are designed to implement the block mode DMA protocols on the Q-BUS. Block Mode DMA reduces the "hand-shaking" necessary to transfer data and thereby increases the transfer rate by a factor of nearly 2. From the user's perspective there is no difference in the operation or configuration of the DCME-Q4B or DCME-Q2B since the board will operate transparently using whatever form of DMA is invoked by other devices on the bus.

B.2 What is Block Mode DMA?

Under conventional direct memory access (DMA), direct data transfers between I/O devices and memory occur one (16 bit) word at a time or one byte at a time using DATI, DATO or DATO (B) bus cycles. Under block mode DMA, the starting address is followed not only by data for that address, but by data for up to 16 consecutive addresses. By eliminating the assertion of the address for each data word, the transfer rate is nearly doubled.

The DCME-Q4B or DCME-Q2B can also be used in system configurations with non-block mode DMA memory boards (either above or below). Most new Q-BUS peripheral controllers will be supporting block mode protocols and take advantage of the improved bus bandwidth using DATBI and DATBO type bus cycles. For devices already designed that do not use these block mode bus cycles, bus operation is unaffected.

THE DCME-Q4B or DCME-Q2B BLOCK MODE DMA MEMORY BOARD

For a complete technical description of these protocols, refer to the 1983 PDP-11 Micro/PDP-11 Handbook published by Digital Equipment Corporation.

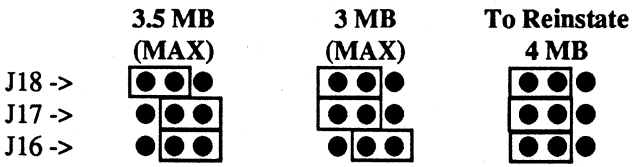
APPENDIX C

Configuring the DCME-Q4B/3.5 MB

Table 17 will allow the user to strap the addressing of the DCME-Q4B (Special Revision) (Order number: DCME-Q4B/3.5MB) to 4 MB, 3.5 MB, 3 MB. These memory configurations are necessary in a MicroVAX I with a graphics card which has 256 KB of memory or any Q-Bus processor which has resident memory. The bank select function is disabled and the bank select jumpers are now used to disable a portion of the high end of memory. This revision of the DCME-Q4B must be ordered pre-wired from Clearpoint for this purpose.

C.0.1 Table 17 - Configuration Table DCME-Q4B/3.5MB

J16, J17, and J18 are used to configure the boards as follows (see Figure 2, page 11 for jumper locations):



The DCME-Q4B/3.5 MB memory board (Special Revision) has 8 rows of memory chips and may be configured as a 3 MB, 3.5 MB, and 4 MB. Jumpers J5 and J6 are configured the same as the 4 MB. Jumpers J16, J17, J18 are used to strap the DCME-Q4B addressing to 4 MB, 3.5 MB and 3 MB.

APPENDIX D

Bank Selection

D.1 Introduction

The bank select feature designed into the DCME-Q4B products is used essentially to increase the available main memory which is addressable in a Q-Bus system. With Clearpoint bank select memory, up to 32 megabytes may be used in a single Q-Bus system with no hardware modifications required.

There is no software available for this application. Each system must be custom tailored to your application.

D.2 Bank Selection

To enable the DCME-Q4B, bank selectability jumpers J15, J16, J17, and J18 (see Figure 2) are used. If all of these jumpers are "out" (see Figure 1), the bank select feature is disabled. To use this feature, J16, J17, and J18 must be installed. J15 may be installed as shown below. Any board which has jumpers J16, J17, and J18 installed will respond to writes (DOUT cycles) to I/O page CSR address 7775100 in one of the following ways:

1. If J15 is not installed, the board will latch bank select bits provided by D5, D6, and D7 in the word being written.
2. If J16, J17, and J18 are all set to the LEFT and J15 is installed; the board will respond with BREPLY L to any write to address 7775100 and latch bank select bits from D5, D6, and D7 in the word being written.
3. J16 jumper in the LEFT position allows 7775100 to be writeable. This WRITE ONLY register allows the effects of the J17 and the J18 jumpers to be negated. By writing a 40 to 7775100 the board becomes a 4 MB board again. 7775100 can not be read.

Since 7775100 is a write only address, the memory boards will not respond to read (DIN cycles) using 7775100 at all.

To verify data being written into bits 5, 6, and 7 of the bank select control status register, data written will be displayed in bits 5 - 11 of the parity control status register for each board.

Bank selectable boards have unique parity CSR addresses as well. Boards which are enabled for bank select have registers as described in Table 18.

D.2.1 Table 18 - CSR Address Selection for Boards Enabled for Bank Select

CSR Address	J14	J13	J12
772120	LEFT	LEFT	LEFT
772122	LEFT	LEFT	RIGHT
772124	LEFT	RIGHT	LEFT
772126	LEFT	RIGHT	RIGHT
772130	RIGHT	LEFT	LEFT
772132	RIGHT	LEFT	RIGHT
772134	RIGHT	RIGHT	LEFT
772136	RIGHT	RIGHT	RIGHT
No CSR or Parity	OUT	OUT	OUT

*Parity may not be disabled for bank selectable boards.

All memory boards in the system must have a unique parity CSR address. Parity must be enabled to use bank select.

The data bits written into CSR 7775100 bits 5, 6, and 7 select which address space and up to eight pages may be available. The following table shows how jumpers J16, J17, and J18 correspond to the selection bits written into 7775100.

D.2.2 Table 19 - Page Selection Options Bank

Select Page No.	CSR Bit 7	CSR Bit 6	CSR Bit 5	J18	J17	J16
0	0	0	0	LEFT	LEFT	LEFT
1	0	0	1	LEFT	LEFT	RIGHT
2	0	1	0	LEFT	RIGHT	LEFT
3	0	1	1	LEFT	RIGHT	RIGHT
4	1	0	0	RIGHT	LEFT	LEFT
5	1	0	1	RIGHT	LEFT	RIGHT
6	1	1	0	RIGHT	RIGHT	LEFT
7	1	1	1	RIGHT	RIGHT	RIGHT

About Clearpoint

Since its inception in 1982, Clearpoint has focused on engineering, developing a first-rate staff and facility for computer-aided design and engineering R&D. Clearpoint applies this expertise to the fields of add-in memory, computer sub-systems and image processing.

The company has developed a unique workplace. Blending individual financial goals with human values, Clearpoint employees are commited to innovation, quality and service. Good people and a good environment combine to make the best product possible.

CLEARPOINT