CIPRICO, INC.

TAPEMASTER

Product
Specification

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TAPEMASTER Product Specification

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REVISION INFORMATION

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C	12-1-81	General Update
D	7-1-83	General Update

REFERENCE DOCUMENTS

The following documents are applicable to the CPC TAPEMASTER and will be of interest to the user:

1. User's Manual for applicable Tape Drive
2. The 8086 Family User's Manual--Intel
3. TAPEMASTER Application Note,

   CPC Publication 21020011
4. Multibus Specification,

   Intel Publication 9800683

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1.0 INTRODUCTION

This document describes the operation of the CPC TAPEMASTER 1/2" Magnetic Tape Drive Adaptor. It provides the information necessary for the user to incorporate the TAPEMASTER into a Multibus-based system. Sections 2 through 5 contain detailed information on the operation of the adaptor.

1.1 GENERAL DESCRIPTION

This section contains a generalized overview of the operation of the TAPEMASTER. Detailed information is contained in later sections.

The TAPEMASTER is an intelligent, fully Multibus compatible 1/2" magnetic tape drive adaptor, capable of handling up to eight 1/2" formatted, start/stop or streaming tape drives. The adaptor functions in 8 or 16 bit systems, single or multiprocessor, with 16, 20 or 24 bit addressing.

Tape operations are controlled through Parameter Blocks placed in system memory by processors requiring use of the adaptor. The location of the Parameter Block is programmable for each operation, i.e., the location is passed to the adaptor at the start of each command or chain of commands. Once an operation has begun, no further system intervention is necessary. The TAPEMASTER will complete the task or tasks assigned, and then become available for the next command.

In addition to tape operations, the TAPEMASTER can perform several powerful data move and diagnostic functions and may be used as a general purpose DMA controller. It may also be used to execute user-written 8089 programs. Refer to later sections for details.

1.2 FEATURES

* Controls up to 8 start/stop or streaming, PE or NRZI formatted drives.
* Programmable for 8 or 16 bit systems.
* Full 24-bit addresing.
* DMA operation.
* Single or multi-master environments.
* Buffered, Direct or Streaming data transfer modes.
* Bus Lock option during DMA transfers.
* Programmable Interrupt option.
* Optional on-board buffer up to 16K bytes.
* Automatic retry for all recoverable errors.
* 64-byte buffer to ease demands on the system bus.
* Powerful Block Move and Exchange commands for generalized data handling.
* Extensive self-diagnostic commands.
* May be used to execute user-written 8089 programs.
* Single 5-volt operation.

2.0 DEFINITION OF TERMS

This section defines the terms used during the detailed description of TAPEMASTER operation.

2.1 CHANNEL ATTENTION

A Channel Attention is an I/O Write to the Multibus address of the TAPEMASTER which is in the system I/O space. It is issued by the system CPU to initiate each TAPEMASTER activity. The I/O address may be set by the user via DIP switches on the board. A Channel Attention must never be issued while the TAPEMASTER is busy (i.e., Gate closed).

Since the least significant bit of the I/O address is not selectable, the TAPEMASTER occupies two addresses. The Channel Attention is defined as the even address. The odd I/O address is defined as the Software Reset. A write to this address resets the TAPEMASTER CPU (see section 3.1.1).

2.2 GATE

The Gate is a byte of data in system memory which controls all access to the TAPEMASTER. It is located in the Channel Control Block in system memory (see section 3.1.4). The Gate may have two values - closed (FFH) or open (00H). A system CPU may only give the TAPEMASTER a command when the Gate is open. Before a system CPU issues a Channel Attention, it should close the Gate using a Test-and-Set type instruction. When the command completes, the TAPEMASTER will open the Gate and will be ready to accept another command.

2.3 POINTER

When system memory addresses are passed to the TAPEMASTER, they must be in the form of a Pointer. Following the Intel 8086 convention, a Pointer consists of two 16-bit words which are combined by the TAPEMASTER to form a 20-bit system memory address. The word at the higher address, or Base, is left-shifted by four bits and added to the lower addressed word, or Offset, to obtain the 20-bit result. Refer to Fig. 2-1 and to the Intel 8086 Family User's Manual for a more detailed discussion of Pointers.

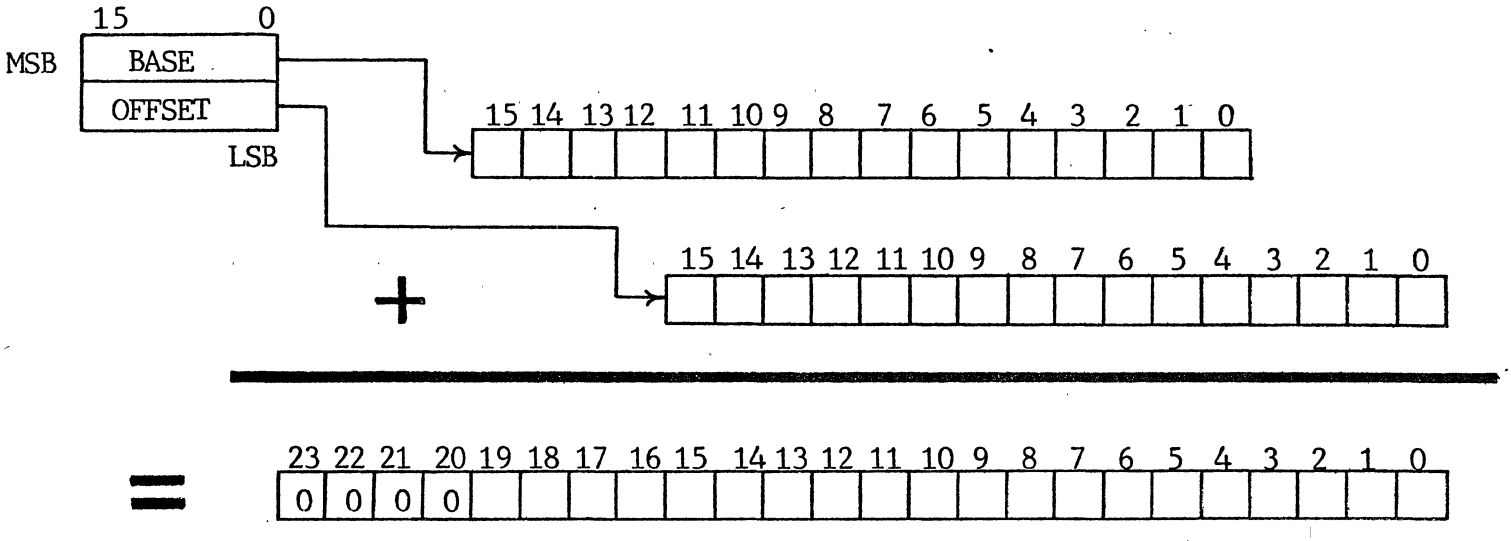


Figure 2-1. Pointer Value

To accomodate 24-bit addressing, the TAPEMASTER uses a 4-bit Page Register, which may be loaded by the user. The Page Register contains system address bits 20-23 (see section 5.1.2).

2.4 PARAMETER BLOCK

A Parameter Block is a short block of consecutively addressed data placed in system memory by a processor in preparation for command execution. The Parameter Block contains information the TAPEMASTER requires to perform the desired operation. The TAPEMASTER command always occupies the first byte of the Parameter Block, which is at the lowest-addressed location.

When execution of a TAPEMASTER command begins, the Parameter Block is read by the TAPEMASTER into Local memory and, just prior to opening the Gate, it is rewritten to system memory with appropriate updates.

3.0 FUNCTIONAL DESCRIPTION

This section contains a detailed description of the operation of the TAPEMASTER.

Operation may be separated into 2 parts: Initialization and Command Execution. All operations are initiated with the issuance of a Channel Attention to the TAPEMASTER.

3.1 INITIALIZATION

Initialization is the procedure through which the TAPEMASTER receives the definition of the system environment from the host. The TAPEMASTER always executes the Intialization procedure when it receives the first Channel Attention after a board reset (sec. 3.1.1).

After the Channel Attention, the TAPEMASTER initializes itself by reading information from three control blocks located in system memory. It is the responsibility of the system to correctly set up these control blocks prior to issuing the first Channel Attention.

The three control blocks are the System Configuration Pointer, the System Configuration Block, and the Channel Control Block. The Initialization process is outlined in Fig. 3-1.

3.1.1 BOARD RESET

The TAPEMASTER board-level Reset may be executed through a system reset or software reset. A system reset occurs when the INIT/ line on the Multibus is activated (low) according to bus convention. A software reset occurs when a write to the higher (odd) I/O address of the TAPEMASTER is executed by a system processor. The two signals are logically "OR'd" together on the board.

3.1.2 SYSTEM CONFIGURATION POINTER

The 6-byte System Configuration Pointer may begin at any system memory address in the lower 1 Mbyte. The only restriction is that the least significant nibble of the address must be 6H (SCP address = XXXX6H). The remaining address bits are set via jumpers on the board.

After the first Channel Attention, the TAPEMASTER reads the first byte of the System Configuration Pointer (SYSBUS) to determine the width of the system bus (initially assumed to be 8 bits). A 00H indicates an 8-bit system bus, 01H a 16-bit bus. Byte 2 is not

used. Bytes 3-6 comprise a Pointer to the next block, the System Configuration Block.

After adjusting for physical bus size, the TAPEMASTER continues to the System Configuration Block and reads that information.

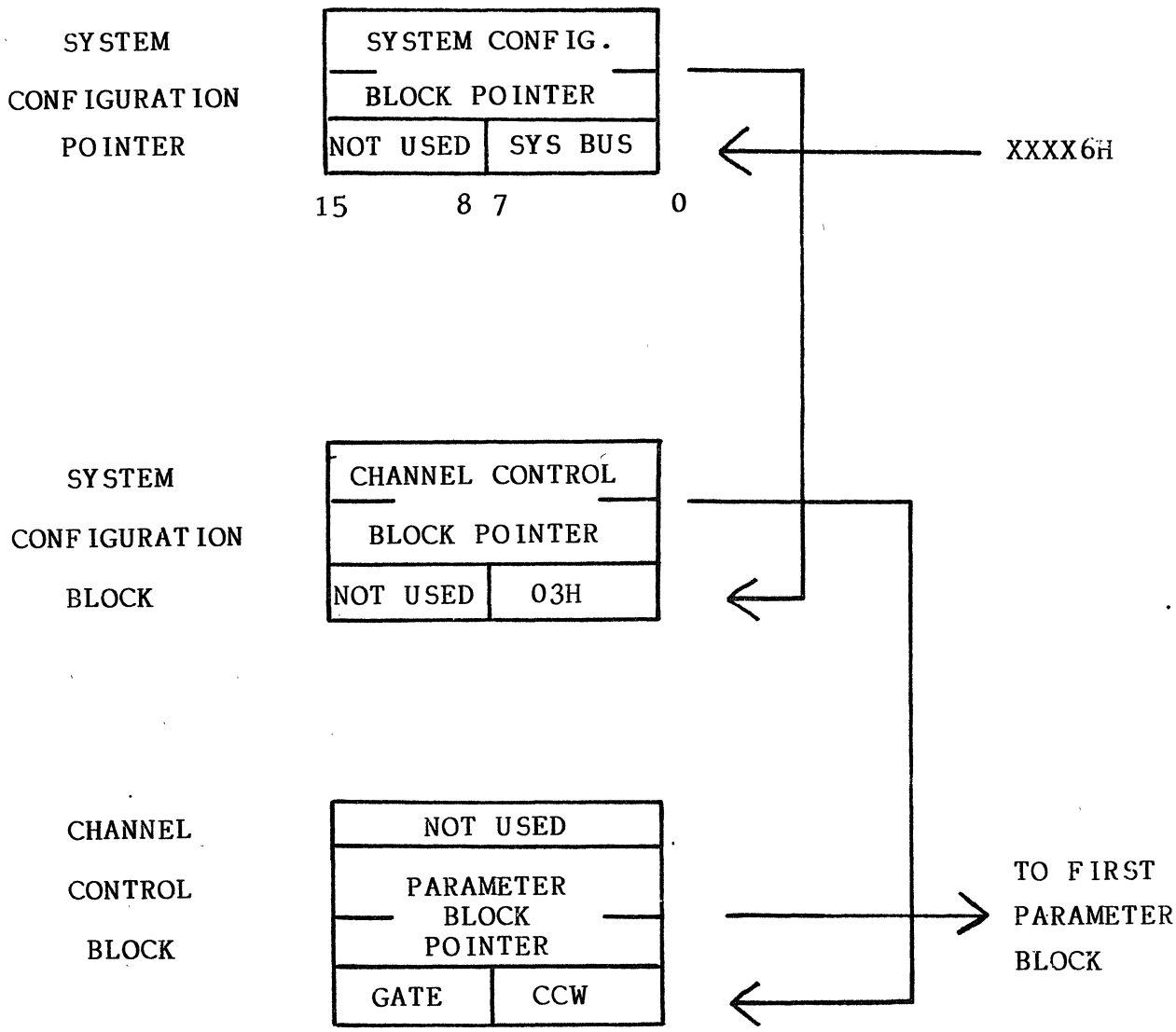


Figure 3-1. Initialization Process

3.1.3 SYSTEM CONFIGURATION BLOCK

The 6-byte System Configuration Block contains one byte whose value is fixed (03H), an unused byte and a 4-byte Pointer to the last Initialization block, the Channel Control Block. After picking up the Pointer in this block, the TAPEMASTER continues to the last block.

3.1.4 CHANNEL CONTROL BLOCK

The 8-byte Channel Control Block contains six bytes around which all TAPEMASTER operations revolve. Byte 1 is the Channel Control Word (CCW), which is used for the interrupt options. It must contain either of two values - 11H for normal operations, or 09H to clear an active non-vectored Multibus interrupt. The CCW may contain other values when executing user-written 8089 programs (See section 3.3 and 3.6 for further details).

Byte 2 is the Gate, which the TAPEMASTER uses to signal its readiness to execute a command. Bytes 3-6 (Parameter Block Pointer) form a Pointer to the location of the LSB of the first Parameter Block.

During the Initialization process, the only byte used in the Channel Control Block is the Gate. It must be set closed (set to FFH) prior to the Initialization process. When the Initialization process has been completed, the TAPEMASTER will open the Gate (set to 00H), indicating that it is now ready to execute commands. The locations used for the System Configuration Pointer and System Configuration Block, if they are RAM-based, may now be reused as required.

3.2 COMMAND EXECUTION

After the completion of the Initialization process, the TAPEMASTER is ready to accept commands, as it now "knows" the programmable locations of the Gate, and of the Parameter Block Pointer. A system processor wishing to execute a command may now do so through the following procedure:

A. Set up the Parameter Block or Blocks in memory.

B. Read the Gate location to determine when the TAPEMASTER is not busy. When the Gate is open (00H), the system processor may take control by setting it closed (FFH).
(Note: In a Multi-procesor system, a Test-and-Set type instruction must be used to close the Gate. This is necessary to prevent one processor from reading the Gate between the read and write of the Gate from a second processor).

C. After closing the Gate, the user sets the Parameter Block Pointer in the Channel Control Block to point at its first Parameter Block. It must also set the Channel Control Word as required.

D. Issue a Channel Attention to the TAPEMASTER.

The TAPEMASTER will then execute the selected command with no additional system intervention. Upon completion of each command, the TAPEMASTER may go on to another Parameter Block, or halt with or without interrupt, depending upon options selected. When it halts, it will open the Gate to signal its readiness to accept another command.

NOTE: The Configure command must be the first command executed after the Initialization process.

3.3 INTERRUPTS

The TAPEMASTER may be programmed, through the CONTROL field in the Parameter Block, to generate an interrupt at the completion of a command, (last command only in a linked chain) or if an unrecoverable error occurs. (If such an error occurs during the execution of an intermediate command in a linked chain, the TAPEMASTER will search through the chain and act on the interrupt options of the last command).

Interrupts may be of two types - Non-vectored Multibus or Mailbox interrupts.

3.3.1 NON-VECTORED INTERRUPTS

Non-vectored interrupts occur when the TAPEMASTER activates one of the eight Multibus interrupt lines. The interrupt will be asserted at the completion of the command or chain of commands for which an interrupt was enabled in the Control field. The interrupt line will remain active until it is cleared by setting the CCW to 09H and executing another TAPEMASTER command. The TAPEMASTER will clear the interrupt before it reads the Parameter Block. The Clear Interrupt command may be used here to avoid the time required for a normal Parameter Block sequence, since this command requires only a 2-byte command code and halts immediately after clearing the interrupt (see section 5.1.8).

3.3.2 MAILBOX INTERRUPTS

A Mailbox interrupt occurs when the TAPEMASTER writes

data to the contents of a reserved memory location (Mailbox) at the completion of a command or chain of commands. The location of the Mailbox is stored in the Interrupt/Link Pointer field of the Parameter Block. When the TAPEMASTER has completed a command for which the Interrupt and Mailbox options were enabled in the Control field, it writes FFH to this Mailbox address. The Mailbox interrupt is most useful in Multiprocessor, position-independent systems.

3.4 DATA TRANSFER

Data can be transferred between system memory and the tape drive in three modes: Buffered, Direct or Streaming.

3.4.1 BUFFERED

During buffered data transfers, the TAPEMASTER completely buffers each block of data in on-board static RAM before transferring the data to the tape (write) or to system memory (read). Maximum block size in this mode is 16K bytes. This mode has the advantage of allowing the system memory to respond completely asynchronously, i.e., data need not be transferred at the speed required by the drive.

3.4.2 DIRECT

Direct data transfers move data directly from system memory, through the TAPEMASTER FIFO to the tape (write), or from the tape, through FIFO to memory (read). Maximum block size in this mode is 65K bytes. System memory must be able to supply or receive data at an average rate equal to or greater than that required by the tape drive.

3.4.3 STREAMING

Streaming data transfers are similar to Direct transfers, in that data is transferred directly between system memory and the tape, through the FIFO. However, unlike the Direct mode, the Streaming mode links multiple data blocks together through a 6-byte header which preceeds each block. This provides the fastest possible data transfer by eliminating the overhead of a full Parameter Block command for each block of data. In addition, the Streaming mode removes all burden of data block synchronization from the system software and accomplishes it in a single command.

3.5 TIME-OUT

The TAPEMASTER contains hardware time-out logic which injects an Acknowledge (ACK/) signal if an expected ACK/

is not received within 4ms after the start of a memory cycle. The time-out may be enabled or disabled by jumper (see Appendix D). It is recommended that TAPEMASTER software drivers be developed with the time-out disabled to more easily identify invalid addresses passed to the TAPEMASTER through the Parameter Blocks.

3.6 USER 8089 PROGRAMS

The TAPEMASTER can execute user-written 8089 programs either from system memory or Local memory. The TAPEMASTER can be directed to execute a user program by placing the starting address of the program (as a 4-byte Pointer) in the location normally occupied by the Command field of a Parameter Block. A Channel Attention begins execution.

For programs residing in system memory, the Channel Control Word in the Channel Control Block (sec. 3.1.4) should be changed from 11H to 13H. This causes the TAPEMASTER to begin execution in system memory rather than Local memory.

For programs residing in Local memory, the code must first be loaded into Local RAM using a Block Move or Exchange command. For such purposes, the TAPEMASTER Local RAM is logically located from Local address C000H. However, user programs should not start below C100H since the TAPEMASTER uses lower RAM locations for variables.

For further information, consult the 8086 Family User's Manual, or contact CIPRICO Inc.

4.0 TAPEMASTER PARAMETER BLOCKS

The TAPEMASTER uses three types of Parameter Blocks: Tape, Block Move, and Exchange. Each Parameter Block is divided into fields which may contain information needed by the TAPEMASTER (Input) and/or status information returned by the TAPEMASTER (Output). The various Parameter Blocks and their fields are described in the following section. Not all fields are used by all commands. Unused fields should be set to zero.

4.1 TAPE COMMAND EXECUTION

Tape commands allow the user to position the tape, write filemarks and to transfer data between the drive and system memory.

4.2 TAPE PARAMETER BLOCK

The normal form of the Tape Parameter Block (Fig. 4-1) contains 22 bytes which form 8 fields.

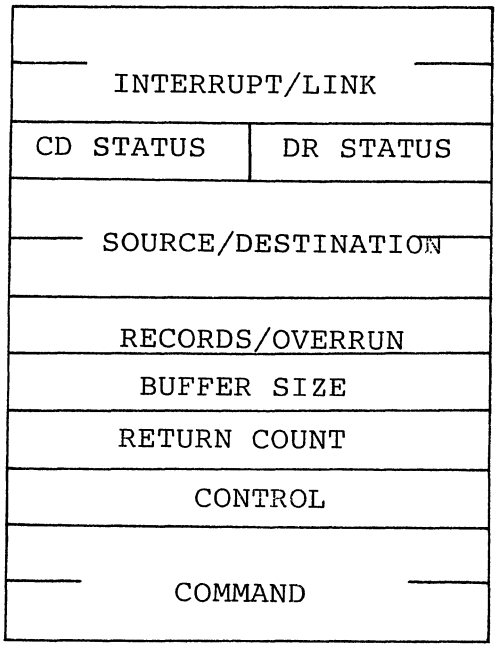


Figure 4-1 Tape Parameter Block

4.2.1 COMMAND (Input)

The lower two bytes of this field contains the hex code of the command to be executed. The upper two bytes must contain 00H for proper operation. (Command hex codes are listed in Appendix F).

4.2.2 CONTROL

This field (Fig. 4-2) contains various options used by the TAPEMASTER during operation. A bit is set if it = 1.

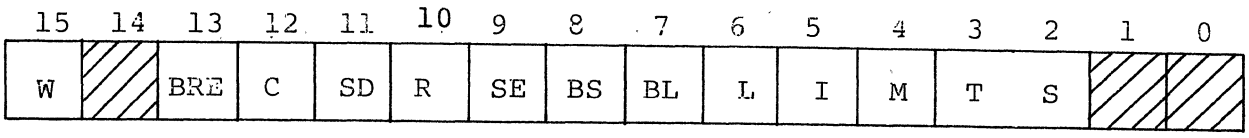


Figure 4-2 Tape Control Field

TS - Tape Select: Selects one of the four tape drives on one bank. (The TAPEMASTER controls two banks composed of four drives each).

00 - Tape Drive 0
01 - Tape Drive 1
10 - Tape Drive 2
11 - Tape Drive 3

M - Mailbox Interrupts: If the I bit is set, the M bit selects Mailbox interrupts. If the M bit is not set, it selects non-vectored Multibus interrupts.

I - Interrupt: Causes the TAPEMASTER to interrupt on the completion of a command.

L - Link: Informs the TAPEMASTER that another Parameter Block follows. (The Link and Interrupt options are mutually exclusive, since each use the Source/Destination Pointer field. If both bits are set, then the Link will take priority).

BL - Bus Lock: Locks the system bus during DMA transfers.

BS - Bank Select: Selects one of the two banks. Physically, this bit is transmitted on the tape interface as the signal FAD/ (Formatter Address), pin J2-48.

0 - Bank 0
1 - Bank 1

SE - Skip EOT: Causes the TAPEMASTER to ignore the EOT signal and allow data transfers past the end of tape marker.

R - Reverse: The operation should proceed in the reverse direction where applicable.

SD - Speed/Density: Selects high speed on dual speed drives such as the Cipher Microstreamer, or low density on remote-selectable dual density drives. If this bit is not set, low speed on dual speed drives or high density on remote-selectable dual density drives is selected.

C - Continuous: Causes the tape to be left moving after a write operation (if the drive supports this feature), effectively extending the acceptable reinstruct window.

BRE - Buffered Read Enable: Allows data to be transferred from TAPEMASTER buffer to system memory when a tape time-out occurs during a Buffered Read command.

W - Width: Selects a 16-bit logical bus width. This bit may be used to force byte transfers on a 16-bit bus. If this bit is not set, the logical system bus width is 8 bits. The logical width must not exceed the physical width selected during Initialization.

4.2.3 RETURN COUNT (Output)

This field contains the block size (in bytes) actually transferred during a data transfer operation. It will also contain the size of the on-board static buffer available for buffered operations, after the execution of a Configure command.

4.2.4 BUFFER SIZE (Input/Output)

This field contains the block size of the tape block to be transferred during a data transfer operation. Maximum block size is 65K bytes (FFFFH). At the completion of a Read Foreign Tape command, this field contains bits 16-31 of the 32 bit block size read from the tape (see section 5.2.2).

4.2.5 RECORDS/OVERRUN (Input/Output)

This field contains a record count, which is required at the start of certain commands, such as the Space Command. At the completion of a Read or Buffered Read command, this field contains the number of bytes actually contained in the tape block just read. This information may be used to indicate that the record just read from the tape contained a fewer or greater number of bytes than requested in the Parameter Block. If the record just read contains more bytes than requested, the Records/Overrun field will contain a larger number than the Return Count and Buffer Size fields. If the record just read contains fewer bytes than requested, the Records/Overrun field will contain the same number as the Return Count field, but a smaller number than

the Buffer Size field.

4.2.6 SOURCE/DESTINATION POINTER (Input)

This field contains the starting system memory address for those commands which access system memory.

4.2.7 DRIVE STATUS (Output)

The bits in this field (Fig. 4-3) reflect the status of the drive at the completion of a command.

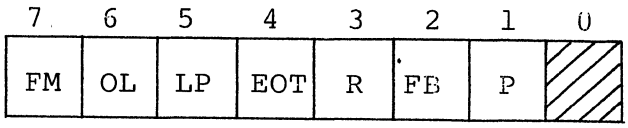


Fig. 4-3 Drive Status Field

P - Write Protect: The tape does not have a write enable ring.
FB - Formatter Busy: The Formatter is busy.
R - Ready: The selected drive is ready.
EOT - End of Tape: The EOT marker was detected.
LP - Load Point: The tape is at Load Point.
OL - On Line: The drive is On Line.
FM - Filemark: A filemark was detected on this operation.

4.2.8 COMMAND STATUS (Output)

The bits in this field (Fig. 4-4) reflect the status of the command.

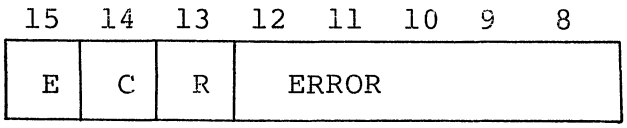


Fig. 4-4 Command Status Field

ERROR - This 5-bit field specifies an error code when a non-recoverable error is encountered. (Error codes are listed in Appendix C).

R - Retry: At least one retry was executed by the TAPEMASTER during this command.

C - Complete: The TAPEMASTER has successfully completed the command outlined in the Parameter Block.

E - Entered: The Parameter Block has been entered by the TAPEMASTER and has begun execution.

4.2.9 INTERRUPT/LINK POINTER (Input)

This field contains the system memory address of the next Parameter Block, if the Link bit is set, or of the Mailbox location, if the Mailbox and Interrupt bits are set.

4.3 BLOCK MOVE COMMAND EXECUTION

The TAPEMASTER can execute a Block Move, or memory-to-memory DMA operation, with many powerful options. The Parameter Block supplies the source address and destination address, either or both of which may be Local (on the TAPEMASTER board) or system memory. The byte count and options are also selected in the Parameter Block.

4.4 BLOCK MOVE PARAMETER BLOCK

The Block Move Parameter Block (Fig. 4-5) contains 28 bytes which form 10 fields.

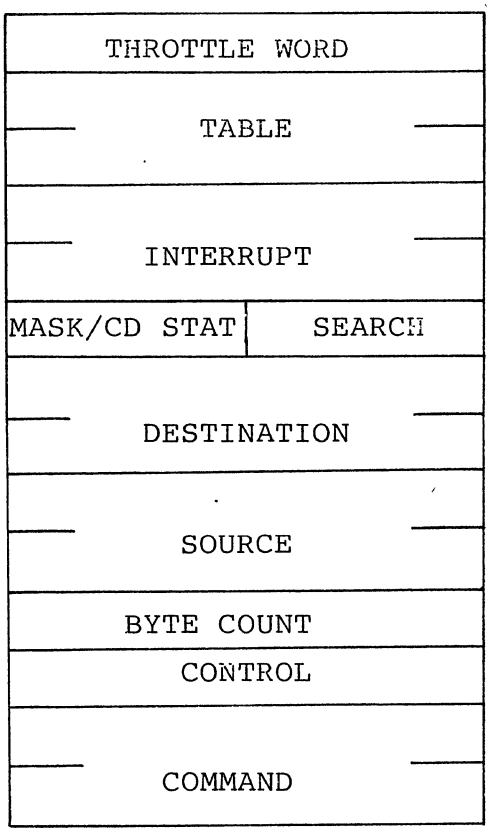


Figure 4-5 Block Move Parameter Block

4.4.1 COMMAND (Input)

The lower two bytes of this field contain the Block Move command hex code, 80H. The upper two bytes must contain 00H for proper operation.

4.4.2 CONTROL (Input)

This field (Fig. 4-6) contains various options used by the TAPEMASTER during the Block Move command. A bit is set if it = 1.

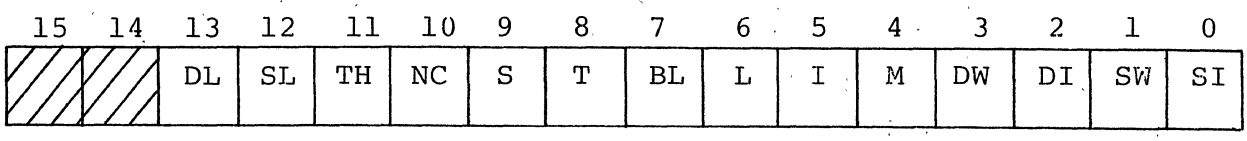


Figure 4-6 Block Move Control Field

SI - Source I/O: Causes the source address of the Block Move to remain constant after each transaction. If this bit is not set, the source address will increment.

SW - Source Width: Selects the logical width of the source as 16 bits. If this bit is not set, the logical width of the source is 8 bits.

DI - Destination I/O: Causes the destination address of the Block Move to remain constant after each transaction. If this bit is not set, the destination address will increment.

DW - Destination Width: Selects the logical width of the destination as 16 bits. If this bit is not set, the logical width of the destination is 8 bits.

M, I, L and BL are the same as for the Tape Control field in section 4.2.3.

T - Translate: Causes each byte from the source to be translated from a look-up table before being moved to the destination.

S - Search: Causes the TAPEMASTER to check each source byte against the Search field during the transfer, and stop on a compare or noncompare (see NC bit). Before the compare is made, each source byte is first masked with the Mask field, so that only desired bits are checked.

NC - Non-compare: If the S bit is set, the NC bit causes a search operation to stop when a source byte and the Search field are different (non-compare). If the NC bit is not set, a search operation will stop when a Source byte and the Search field are identical (compare).

TH - Throttle: Causes the TAPEMASTER to inject a

delay between each byte or word transferred. The length of the delay is specified in the Throttle Word field of the Parameter Block. This option is used to prevent the TAPEMASTER from monopolizing the bus during a non-critical Block Move operation.

SL - Source Local: Specifies the source address as a 16-bit Local address (i.e., on the TAPEMASTER board). If this bit is not set, the source address is a 20 bit system memory address specified by a 4-byte Pointer.

DL - Destination Local: Specifies the destination address as a 16-bit Local address (i.e., on the TAPEMASTER board). If this bit is not set, the destination address is a 20-bit system memory address specified by a 4-byte Pointer.

4.4.3 BYTE COUNT (Input/Output)

At the start of the command, this field contains the number of bytes to be transferred. At the completion of the command, this field contains the number of bytes remaining to be transferred. Normally, this field would contain zeros at the termination of the command, indicating all bytes were transferred. However, if the Search bit is set, the Block Move may terminate on a Compare, and the Byte Count field will contain the number of remaining bytes.

4.4.4 SOURCE POINTER (Input)

This field contains the starting Local or system memory address from which data is to be moved. (If the source is Local, only the lower two bytes of this field are used).

4.4.5 DESTINATION POINTER (Input)

This field contains the starting Local or system memory address to which data is to be moved. (If the destination is Local, only the lower two bytes of this field are used).

4.4.6 SEARCH (Input)

This field contains an 8-bit value which is compared to each source byte, when the Search bit is set in the Control field.

4.4.7 MASK/COMMAND STATUS (Input/Output)

At the start of the command, this field contains an 8-bit value to which each source byte is masked before being compared to the Search field, if the Search bit it set. After the completion of the command, this

field reflects the status of the command. (Fig. 4-7).

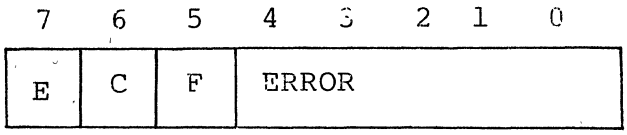


Fig. 4-7 Command Status Field

The E, C, and ERROR fields are the same as for the Tape Command Status field in section 4.2.8.

F - Found: indicates a match was found during a search operation.

4.4.8 INTERRUPT POINTER (Input)

This field contains the location of the Mailbox if the Mailbox and Interrupt bits are set.

4.4.9 TABLE POINTER (Input)

This field contains the starting system memory address of a 256-byte look-up table. If the Translate bit is set, each source byte is used as an index into this table. The entry at that table location is then moved to the destination.

4.4.10 THROTTLE WORD (Input)

This field contains the length of delay between each transferred byte or word, if the Throttle bit in the Control field is set. This 16-bit number is counted down to 0000 before each transfer at a rate of approximately 100 micro-seconds per count.

4.5 EXCHANGE COMMAND EXECUTION

The TAPEMASTER executes an Exchange command which will exchange part or all of the available TAPEMASTER RAM, on a byte basis, with system memory. The Parameter Block supplies the system memory address, the relative current Local address and the byte count to be exchanged.

4.6 EXCHANGE PARAMETER BLOCK

The Exchange Parameter Block (Fig. 4-8) contains 22 bytes which form 9 fields.

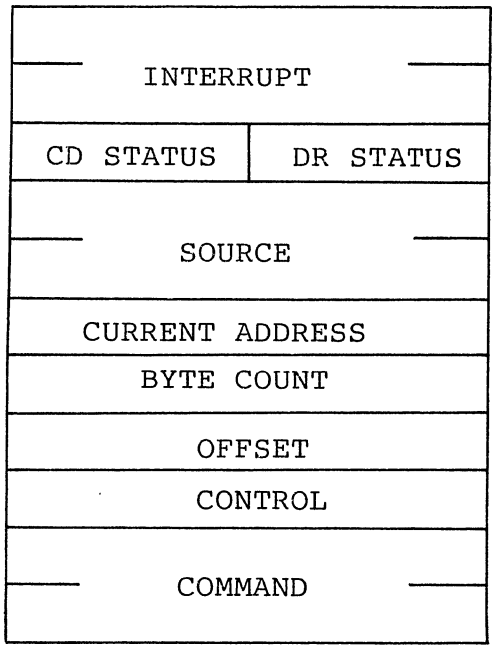


Figure 4-8 Exchange Parameter Block

4.6.1 COMMAND (Input)

The lower two bytes of this field contain the Exchange command hex code, OCH. The upper two bytes must contain 00H for proper operation.

4.6.2 CONTROL (Input)

This field (Fig. 4-9) contains only two options used by the TAPEMASTER during an Exchange command.

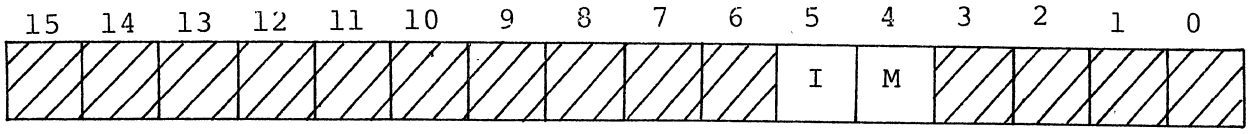


Figure 4-9 Exchange Control Field

M and I are the same as for the Tape Control field in section 4.2.2.

4.6.3 OFFSET (Input)

This field contains the relative address in Local memory where the exchange will start. An offset of zero will result in a physical Local address of C100H.

4.6.4 BYTE COUNT (Input/Output)

At the start of the command, this field contains the number of bytes to be exchanged. At the completion of the command, this field contains the number of bytes remaining to be transferred. If a successful exchange has occurred, this field will contain zeros.

4.6.5 CURRENT ADDRESS (Output)

This field contains the current Local address. It is updated after command completion.

4.6.6 SOURCE POINTER (Input)

This field contains the starting system memory address.

4.6.7 DRIVE STATUS

This field is not used.

4.6.8 COMMAND STATUS (Output)

The bits in this field (Fig. 4-4) reflect the status of the command.

4.6.9 INTERRUPT POINTER (Input)

This field contains the Mailbox location, if the Mail-

box and Interrupt bits in the Control field are set.

5.0 TAPEMASTER COMMANDS

The TAPEMASTER executes 31 commands in five catagories. Refer to the TAPEMASTER Parameter Block descriptions for the contents and significance of the Parameter Block fields. The Command Code (in hex) follows each command.

5.1 CONTROL STATUS COMMANDS

These commands transfer control and status information to and from the TAPEMASTER and/or the drives.

5.1.1 CONFIGURE (00)

This command initializes the on-board registers and memory of the TAPEMASTER, and calculates the buffer space which is available for buffered operations. The buffer size (in hex bytes) is returned in the Return Count field. This command must be the first command to be executed after the Initialization sequence.

5.1.2 SET PAGE REGISTER (08)

This command sets the 4-bit Page Register on the TAPEMASTER. This register, which is cleared on Reset, contains the system memory address bits A20-A23. When this register is set, all TAPEMASTER memory references will use this register as the upper four bits of a 24-bit address. The Page Register contents are specified in bits 0-3 of the Records field.

5.1.3 NOP (20)

No operation. This command executes the mechanics of normal Parameter Block operation.

5.1.4 DRIVE STATUS (28)

This command returns the status of the selected drive in the Drive Status field.

5.1.5 TAPE ASSIGN (74)

This command is reserved to account for differences between formatters from various manufacturers, and to maintain compatibility between the TAPEMASTER and RIMFIRE 38T. For the software revision level referenced by this document, this command is equivalent to a NOP, and requires only the Command Code in the Command field.

5.1.6 SET RETRY (8C)

This command selects the number of times a recoverable error is retried. The number of retries, up to FFH, is specified in the LSB of the Records field. The default value is 6.

5.1.7 DRIVE RESET (90)

This command resets the selected Formatter Enable. It may be used to abort a run-away tape condition.

5.1.8 CLEAR INTERRUPT (9C)

This command clears an active Multibus interrupt and halts if the CCW in the Channel Control Block is set to 09H. The command requires only the Command Code in the Command field. The TAPEMASTER does not update the Parameter Block after the operation is complete.

5.2 TAPE POSITION COMMANDS

These commands move the tape to a known position relative to the read/write head, or perform various other functions which require the tape to be moved. No data is transferred between system memory and the tape.

5.2.1 OVERLAPPED REWIND (04)

This command initiates a Rewind command. Periodic Tape Status commands may then be executed to check for Load Point.

5.2.2 READ FOREIGN TAPE (1C)

This command searches for the next record and counts the bytes in that record. Data is ignored. The byte count is returned as a 32-bit hex number in the Return Count field (bits 0-15) and Buffer Size field (bits 16-31).

5.2.3 REWIND (34)

This command rewinds the tape to Load Point.

5.2.4 OFFLINE/UNLOAD (38)

This command causes the drive to go offline. For the Cipher Data Microstreamer, it also causes the tape to rewind and unload.

5.2.5 WRITE FILEMARK (40)

This command writes a filemark on the tape.

5.2.6 SEARCH FILEMARK (44)

This command searches, forward or reverse, until a filemark is found. If an EOT (forward) or Load Point (reverse) is encountered, this command will terminate early.

5.2.7 SPACE (48)

This command spaces, forward or reverse, a specified number of records. A filemark is counted as a record. The desired number of records is specified in the Records field.

5.2.8 ERASE FIXED LENGTH (4C)

This command erases a fixed length (approximately 3.5 inches) for each record specified in the Records field.

5.2.9 ERASE TAPE (50)

This command erases the entire tape from current position to several feet beyond the EOT.

5.2.10 SPACE FILEMARK (70)

This command is similar to Space except that it terminates early if a filemark is encountered before all the records are spaced over.

5.2.11 SEARCH MULTIPLE FILEMARKS (94)

This command is similar to a Search Filemark except that it proceeds until a specified number of consecutively written filemarks are located. This command is very useful when using double or triple filemarks as file separators. The number of filemarks, up to 255, is specified in the LSB of the Records field.

5.3 DATA TRANSFER COMMANDS

Data Transfer commands transfer data from the tape to system memory (read) or from system memory to the tape (write, edit). The desired data block size, in bytes, is contained in the Buffer Size field. The starting system memory address is contained in the Source/Destination Pointer field.

When the TAPEMASTER has completed the operation, the number of bytes actually transferred is returned in the Return Count field. For successful operations, this field will match the Buffer Size field. For all read commands, the TAPEMASTER will also return the actual number of bytes in the record in the Records/Overrun field.

5.3.1 BUFFERED READ (10)

This command transfers a data block from the tape to system memory in a two-part operation. Data is first moved from the tape to TAPEMASTER buffer, and then from buffer to system memory. This command eliminates any restrictions on system memory response time. Maximum block size is 16K bytes.

5.3.2 BUFFERED WRITE (14)

This command transfers a data block from system memory to the tape in a two-part operation. Data is first moved from system memory to TAPEMASTER buffer, and then to the tape from buffer memory. This command eliminates any restrictions on system memory response time. Maximum block size is 16K bytes.

5.3.3 BUFFERED EDIT (18)

This command edits, in Buffered mode, the record immediately preceeding the current position of the read/write head. Maximum block size is 16K bytes.

5.3.4 DIRECT READ (2C)

This command transfers a data block from the tape to system memory. The system must accept data at an average rate equal to or greater than that of the drive. Maximum block size is 65K bytes.

5.3.5 DIRECT WRITE (30)

This command transfers a data block from system memory to the tape. The system must supply data at an average rate equal to or greater than that of the drive. Maximum block size is 65K bytes.

5.3.6 DIRECT EDIT (3C)

This command edits, in Direct Mode, the record immediately preceeding the current position of the read/write head. Maximum block size is 65K bytes.

5.3.7 STREAMING READ (60)

The Streaming Read command transfers multiple blocks of data from the tape to system memory in the Direct mode. Multiple blocks are used to allow the user to provide a continuous source of data to the tape, which may be necessary to maintain streaming operation.

The Streaming Read requires one or more data blocks in system memory. Each block contains an 8-byte Block Header (Fig. 5-2) and a data area of variable length. The header contains several handshake bits, a byte count and a pointer to the next block, if one follows. Figure 5-1 indicates how multiple blocks, in this case three blocks, can be linked together.

When the TAPEMASTER begins a Streaming Read command, it proceeds to the first block and waits at the Block Gate until the Ready bit is set by the system. When this occurs and no faults are present, it clears "Ready", sets "Busy", reads the next record from the tape and fills the data area in the system memory block. The TAPEMASTER then clears "Busy", sets the "Complete" bit in the Block Gate, proceeds to the next block and repeats the same process, continuing until it enters a block the the "Last Block" bit set. Figure 5-3 diagrams the manner in which the TAPEMASTER handles the Block Gate and enters the block.

The Streaming Read command is useful for high-speed, streaming restore operations and provides for simple synchronization with the destination device (usually a disk).

5.3.8 STREAMING WRITE (64)

The Streaming Write command transfers multiple blocks of data from system memory to the tape in a manner similar to the Streaming Read (see Fig. 5-1, 5-2 and 5-3).

This command is useful for high speed, streaming dump operations and provides for simple synchronization with the source device (usually a disk).

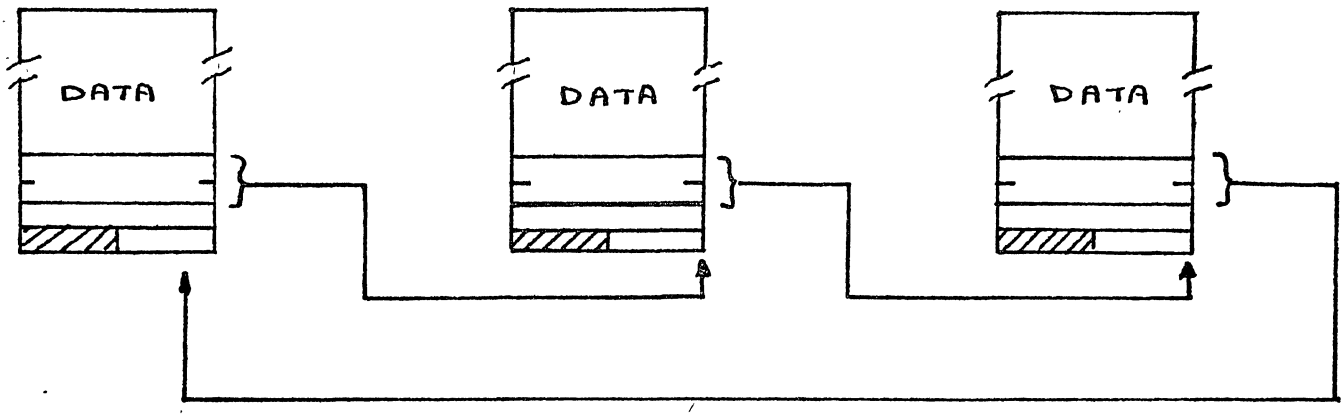


Figure 5-1 Streaming Read or Write

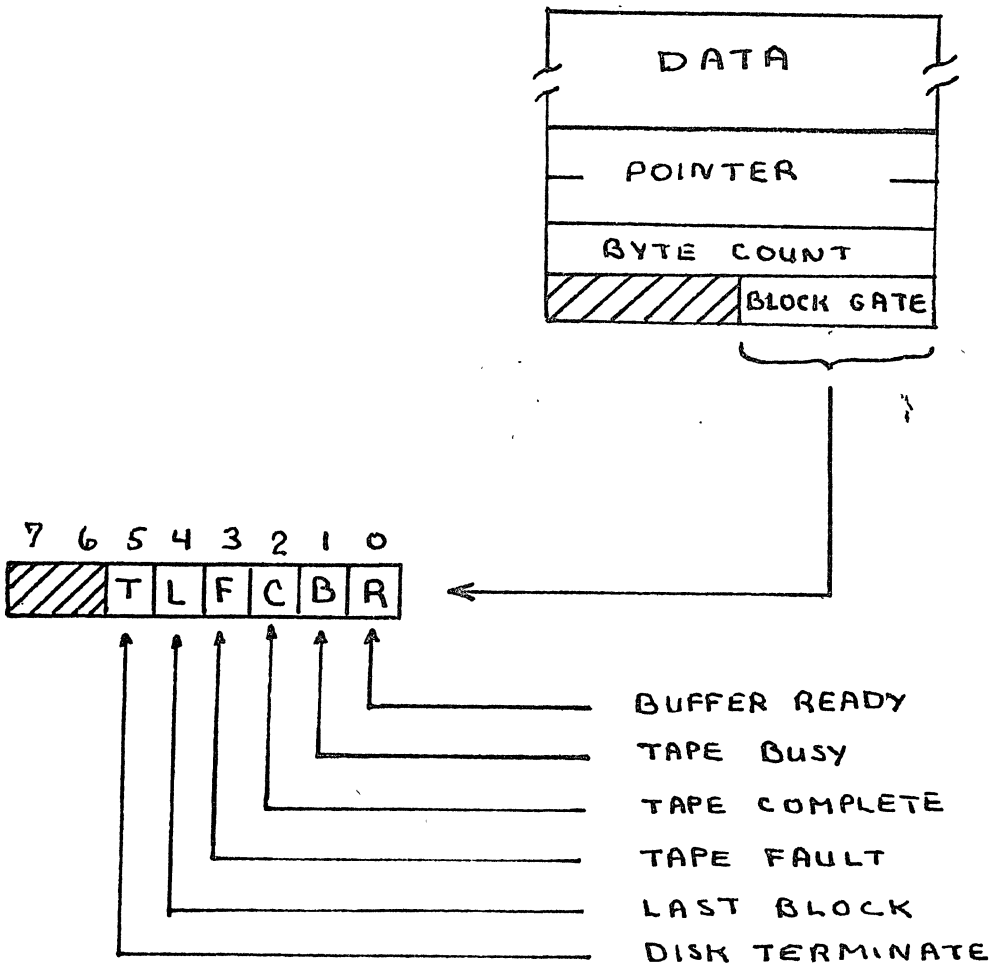


Figure 5-2 Streaming Block Header

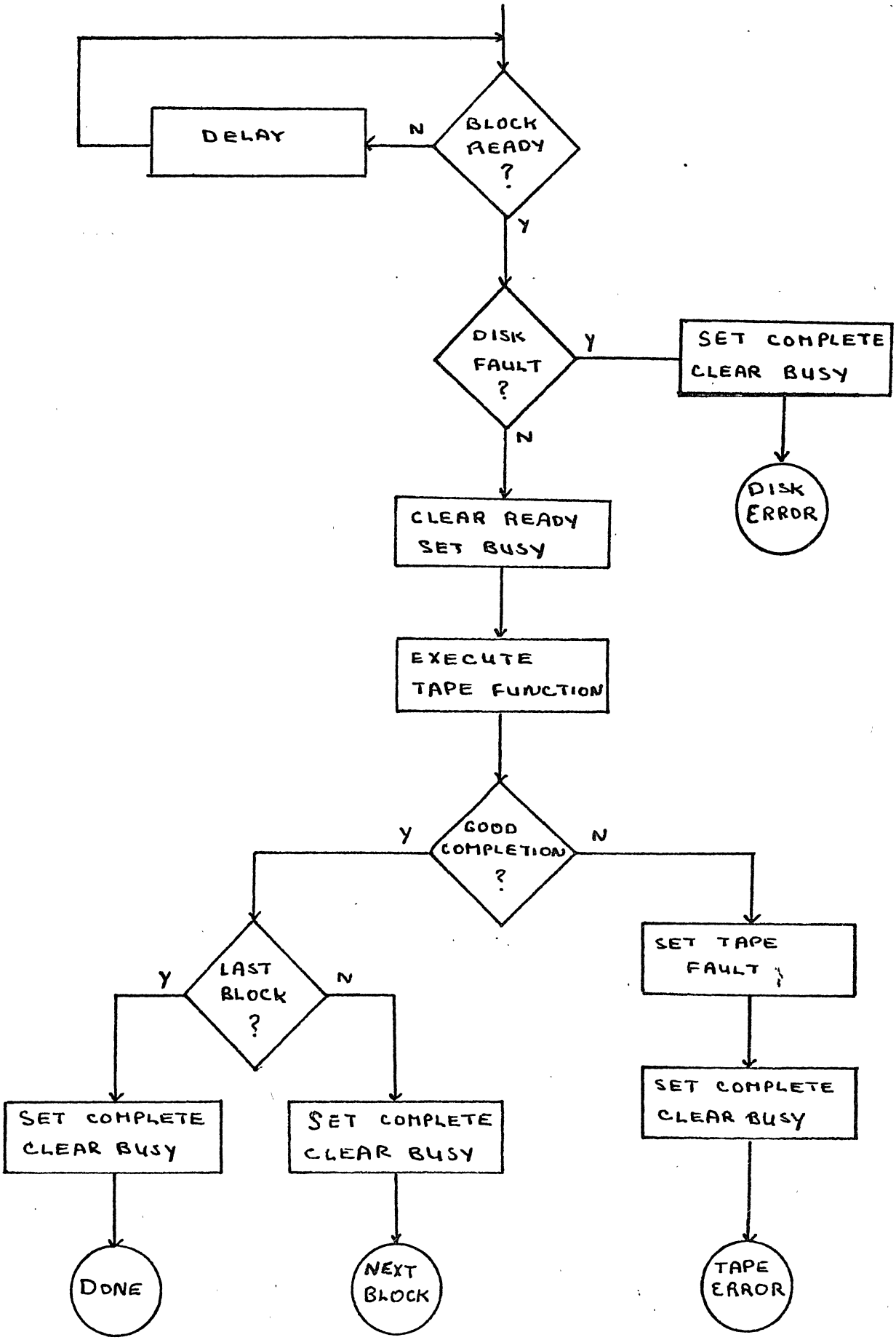


Figure 5-3 Streaming Block Gate Sequence

5.4 SPECIAL COMMANDS

The TAPEMASTER executes two Special commands which are not related to tape functions, and can be executed without the drive connected. These commands are provided to fully utilize the power of the 8089 CPU.

5.4.1 BLOCK MOVE (80)

This command moves up to 65K bytes of data between two memory locations. Either location may be local (on the TAPEMASTER board) or system memory, and may be constant or incrementing.

Several operations may be performed on the data during the Block Move command as outlined in section 4.3.

The Block Move provides a powerful tool for any Multibus system. Some example usages are:

* Extended Memory - Since the TAPEMASTER can address 16 Mbytes (24 address bits), it can be used in conjunction with a compatible memory board to provide access to memory not normally accessible to system processors.

* Memory-mapped I/O - If I/O devices are mapped in memory space, the Block Move can be used to transfer data to or from a peripheral such as a line printer or CRT. By using several of the options, the Block Move could be further extended to perform more complex I/O functions. For example, it could transfer data to a line printer, performing a conversion en route, then monitor the printer status byte and proceed when ready to the next line.

* User 8089 programs - The Block Move may be used to download a user-written 8089 program from system memory to TAPEMASTER RAM for execution (see section 3.6).

5.4.2 EXCHANGE (0C)

The Exchange command exchanges part or all of the available TAPEMASTER RAM with system memory on a byte basis. This command is useful for debugging purposes.

5.5 DIAGNOSTIC COMMANDS

The TAPEMASTER executes two diagnostic commands which are used to test TAPEMASTER RAM. These commands will operate only if jumpers 59-60 are connected on the TAPEMASTER board (see Appendix D). A Configure command must follow the execution of any diagnostic command or commands.

5.5.1 SHORT MEMORY TEST (54)

Consult factory.

5.5.2 LONG MEMORY TEST (58)

Consult factory.

APPENDICES

APPENDIX A - SPECIFICATIONS

Physical:

Height 6.75 in.
Length 12.00 in.

Electrical:

Voltage +5v ±5%

Current	Typical	Maximum
2K	2.55	2.60
16K	3.00	3.10

Capacity: 8 drives

Drives Controlled: All drives complying with industry standard formatted interface.

Transfer Rate: Tape speed to 500 KBps (16 bit system)
to 330 KBps (8 bit system)
(400 ns ACK)

MTBF: 71,000 hours

Environmental: 0-55 degrees ambient (degrees C)

Bus Interface: Fully Intel Multibus compatible

Mating Connectors:

J1, J2 -3M No. 3425 or equivalent
P1 -Viking No. 2VH43/1AV5 or equivalent

APPENDIX B - CABLES

The TAPEMASTER requires two (2) 50-pin flat cables to the tape drive. Cables come in standard 10 and 20 foot lengths. Other lengths are available as special order items. Daisy-chain cables are also available. Part numbers are given in table B-1.

CPC P/N	Length	Function
*******	******	********
81011021	10 ft.	TAPEMASTER J1 to Tape P1
81011022	20 ft.	TAPEMASTER J1 to Tape P1
81011011	10 ft.	TAPEMASTER J2 to Tape P2
81011012	20 ft.	TAPEMASTER J2 to Tape P2
81011041	10 ft.	Daisy-chain cable for Tape P1
81011042	20 ft.	Daisy-chain cable for Tape P1
81011051	10 ft.	Daisy-chain cable for Tape P2
81011052	20 ft.	Daisy-chain cable for Tape P2

TABLE B-1 TAPEMASTER Cable Part Numbers

All cables should be installed such that pin 1 on the drive and the TAPEMASTER are connected.

Some formatters utilize a single 100 pin board-edge connector instead of two 50-pin connectors. In such cases, an adaptor board may be obtained from the manufacturer.

APPENDIX C - ERROR CODES

This section lists the codes for unrecoverable errors detected by the TAPEMASTER during the execution of a command. The code is returned in bits 0-4 of the Command Status field.

Code	Description
00	No unrecoverable error.
01	Timed out waiting for expected Data Busy false.
02	Timed out waiting for expected Data Busy false, Formatter Busy false and Ready true.
03	Timed out waiting for expected Ready false.
04	Timed out waiting for expected Ready true.
05	Timed out waiting for expected Data Busy true.
06	A memory time-out occurred during a system memory reference.
07	A blank tape was encountered where data was expected.
08	An error occurred in the micro-diagnostic.
09	An unexpected EOT was encountered during a forward operation, or Load Point during a reverse operation.
0A	A hard or soft error occurred which could not be eliminated by retry.
0B	A read overflow or write underflow occurred. This error indicates that the FIFO was empty when data was requested by the tape during a write, or full when the tape presented a byte during a read.
0C	Not used.
0D	A read parity error occurred on the byte interface between the drive and the TAPEMASTER.
0E	An error was detected while calculating a checksum on the PROM.
0F	A tape time-out occurred, because the tape drive did not supply an expected read or write strobe. This normally occurs when attempting to read a larger record than was written.
10	Tape not ready.
11	A write was attempted on a tape without a write-enable ring.
12	Not used.
13	The diagnostic mode jumper was not installed while attempting to execute a Diagnostic command.
14	An attempt was made to link from a command which does not allow linking.
15	An unexpected filemark was encountered during a tape read.
16	An error in specifying a parameter was detected by the TAPEMASTER. The usual cause is an entry in the Byte Count field which is zero or too large.
17	Not used.
18	An unidentifiable hardware error occurred. Consult factory.
19	A streaming read or write operation was terminated by the operating system or disk.

APPENDIX D - JUMPER SETTINGS

This section describes the setting of jumpers and DIP switches on the TAPEMASTER board. Factory settings are indicated with an asterisk (*).

1. Jumpers 1-2 (BPRO/)

   These jumpers are set according to the type of bus priority used on the Multibus.

* Serial Priority - Jumper 1-2
  Parallel Priority - No jumper

2. Jumpers 3-5, 51-53 (Bus Arbitration)

   These jumpers control the conditions under which the TAPEMASTER surrenders control of the Multibus during a transfer sequence. Jumpers 3,4,5 allow CBRQ/ to be jumpered low (3-5) or to the Multibus (3-4). Jumpers 51,52,53 allow the ANYQRST input on the 8289 Bus Arbiter to be jumpered high (51-52) or low (52-53). Four configurations are possible.

	Mode	Jumper	Description
	1	3-4 52-53	The TAPEMASTER will surrender the bus to a higher priority master, when that master activates CBRQ/.
	2	3-4 51-52	The TAPEMASTER will surrender the bus to a higher or lower priority master, when that master activates CBRQ/.
*	3	3-5 51-52	The TAPEMASTER will surrender the bus after each transfer cycle.
	4	3-5 52-53	The TAPEMASTER will surrender the bus to a higher priority master after every cycle.

3. Jumpers 18-22 (Maintenance)

   These jumpers are used at the factory to allow the insertion of the CPC 8089 Emulator into the CPU socket.

  Maintenance Mode - Jumper 19-21, 20-22
* Normal Mode - Jumper 18-19, 20-21

4. Jumpers 15-16 (I/O Address Bus Width)

These jumpers select the width of the I/O Address Bus.

* 8-bit address - No jumper
16-bit address - Jumper 15-16

5. Jumpers 23-24

* Not used - must not be jumpered

6. Jumpers 25-30 (Cable parity)

These jumpers control generation and checking of parity on the byte bus between the TAPEMASTER and the drive.

*	Check odd parity	-	Jumper 25-26
	Check even parity	-	Jumper 26-27
*	Generate odd parity	-	Jumper 28-29
	Generate even parity	-	Jumper 29-30

7. Jumpers 31-50 (Initialization Address)

These jumpers allow the user to select the upper 16 bits of the 20-bit System Configuration Pointer address (see sec. 3.1.2). This address is normally set once to the optimum location for a particular system and is not changed thereafter.

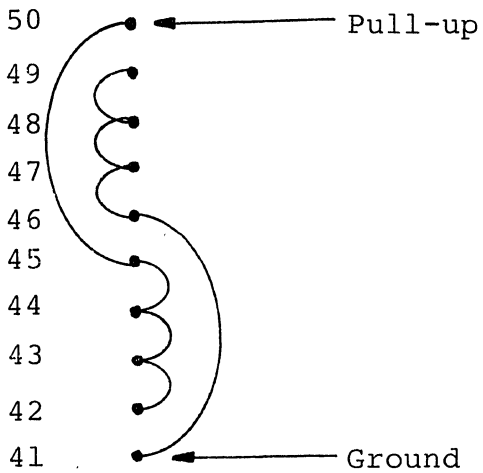
The address is set in two groups of eight bits. Each group is set in a similar fashion. Each group contains 10 pins - 8 pins corresponding to address bits, one pin to a pull-up, and one to a ground. Those address bits which are to be active are daisy-chained to the pull-up, and those which are to be inactive are daisy-chained to the ground.

The pins have the following signficance.

31 - Ground	41 - Ground
32 - A4	42 - A12
33 - A5	43 - A13
34 - A6	44 - A14
35 - A7	45 - A15
36 - A8	46 - A16
37 - A9	47 - A17
38 - A10	48 - A18
39 - A11	49 - A19
40 - Pull-up	50 - Pull-up

As an example, Fig. D-1 indicates the connections necessary to set the address to 0FFF6H. (The lowest nibble is not selectable and must be 6H).

* Factory setting is 0FFF6H, unless requested otherwise.



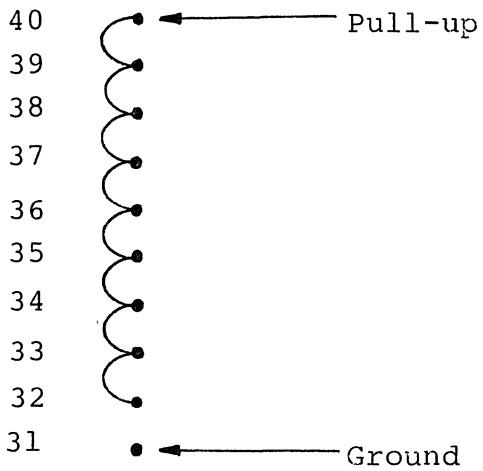


Fig. D-1 Initialization Address 0FFF6H

8. Jumper 51-53 (ANYRQST)

   See paragraph 2 of this Appendix.

9. Jumper 54-56 (PROM type)

   These jumpers select the PROM type, which is 2732(A) for the standard TAPEMASTER.

* 2732(A) PROM type - Jumper 54-55

10. Jumper 57-58 (Bus Time-Out)

    These jumpers enable or disable the system bus time-out.

    Time-out enabled - Jumper 57-58
* Time-out disabled - No Jumper

11. Jumper 59-60 (Diagnostics)

These jumpers allow the execution of the diagnostic commands in section 5.5.

Diagnostic Mode - Jumper 59-60
* Normal Mode - No Jumper

12. Jumper INT, I0-I7 (Interrupts)

These jumpers select the non-vectored interrupt priority level by connecting the INT pin to the appropriate level (I0 = Interrupt 0, I7 = Interrupt 7).

* Factory setting is Interrupt level 7.

13. DIP Switch (Channel Attention, Software Reset, Bus Width)

The two DIP switches are used to select the Channel Attention address, the Software Reset address and the width of the system bus. Bit signficance is marked on the silkscreen on the board. Bit switches "A1" through "A15" select the upper 15 bits of the two I/O addresses and bit switch "8/16" selects the width of the system bus. Since the least significant bit of the I/O address is not selectable, the Channel Attention is defined as the lower or even address and the Software Reset is defined as the higher or odd address. A bit will be decoded as a "1" (active) if the corresponding switch is set towards the "1" on the silkscreen (open).

As an example, Fig. D-2 shows the switch settings for a Channel Attention address of 0FFAAH and a Software Reset address of 0FFABH, using a 16-bit data bus.

* Factory setting is XXAAH, using a 16-bit data bus, unless requested otherwise.

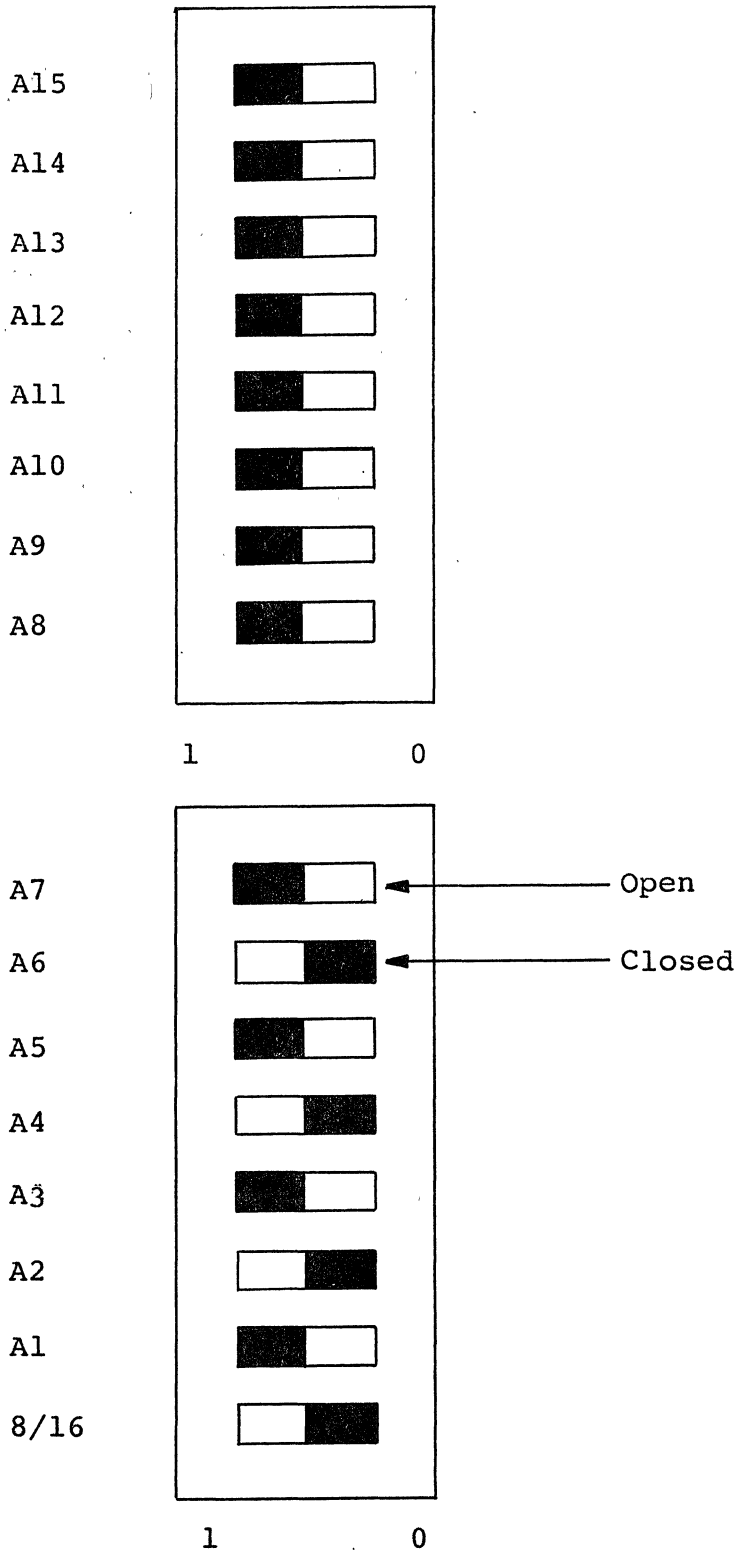


Figure D-2 Channel Attention Address 0FFAAH

APPENDIX E - CONNECTOR PIN-OUTS

J1		J2	
Pin	Signal Description	Pin	Signal Description
1	Ground	1	Read Parity
2	Formatter Busy	2	Read Data 0
3	Ground	3	Read Data 1
4	Last Word	4	Load Point
5	Ground	5	Ground
6	Write Data 4	6	Read Data 4
7	Ground	7	Ground
8	Initiate Command	8	Read Data 7
9	Ground	9	Ground
10	Write Data 0	10	Read Data 6
11	Ground	11	Ground
12	Write Data 1	12	Hard Error
13	Ground	13	Ground
14	Not Used	14	Filemark
15	Ground	15	Ground
16	Not Used	16	CCG/IDENT
17	Ground	17	Ground
18	Reverse	18	Formatter Enable
19	Ground	19	Ground
20	Rewind	20	Read Data 5
21	Ground	21	Ground
22	Write Parity	22	End of Tape
23	Ground	23	Ground
24	Write Data 7	24	Offline/Unload
25	Ground	25	Ground
26	Write Data 3	26	Not Used
27	Ground	27	Ground
28	Write Data 6	28	Ready
29	Ground	29	Ground
30	Write Data 2	30	Not Used
31	Ground	31	Ground
32	Write Data 5	32	File Protect
33	Ground	33	Ground
34	Write	34	Read Strobe
35	Ground	35	Ground
36	Read Threshold 2	36	Write Strobe
37	Ground	37	Ground
38	Edit	38	Data Busy
39	Ground	39	Ground
40	Erase	40	Not Used
41	Ground	41	Ground
42	Write Filemark	42	Corrected Error
43	Ground	43	Ground
44	Not Used	44	On Line
45	Ground	45	Ground
46	Transport Address 0	46	Transport Address 0
47	Ground	47	Ground
48	Read Data 2	48	Formatter Address
49	Ground	49	Ground
50	Read Data 3	50	Speed/Density

APPENDIX F - COMMAND CODES

This section lists the hex codes for all TAPEMASTER Commands.

Group I. Control Status Commands

00 - Configure
08 - Set Page Register
20 - No Operation (NOP)
28 - Drive Status
74 - Tape Assign
8C - Set Retry
90 - Drive Reset
9C - Clear Interrupt

Group II. Tape Position Commands

04 - Overlapped Rewind
1C - Read Foreign Tape
34 - Rewind
38 - Offline/Unload
40 - Write Filemark
44 - Search Filemark
48 - Space
4C - Erase Fixed Length
50 - Erase Tape
70 - Space Filemark
94 - Search Multiple Filemarks

Group III. Data Transfer Commands

10 - Buffered Read
14 - Buffered Write
18 - Buffered Edit
2C - Direct Read
30 - Direct Write
3C - Direct Edit
60 - Streaming Read
64 - Streaming Write

Group IV. Special Commands

80 - Block Move
OC - Exchange

Group V. Diagnostic Commands

54 - Short Memory Test
58 - Long Memory Test