CONTROL DATA®
MP-60 COMPUTER SYSTEM FAMILY

CONTROL DATA
CORPORATION

The CONTROL DATA MP-60 is a computer system architecture for industrial and military applications. Advanced state-of-the-art concepts in microprogramming allow the application engineer to configure the MP-60 in a wide variety of high performance systems. An MP-60 consists of Central Processing Units (CPUs), Input/Output Controllers (IOCs) and memory systems. In addition to executing in the MP-60 native mode, microprogramming features of the hardware allow emulation of other computer systems with cost/performance improvement. The MP-60 standard software product set supports real-time, multiprogramming, multiprocessing systems under the MPX/OS operating system.

The MP-60 is available as a ruggedized industrial package, or a militarized AN/UYK-25(V) package. Both forms of the system hardware are functionally compatible; software is identical.

Control Data offers a wide range of peripheral equipment for the MP-60 System. Additionally, the IOC provides the system user with extensive flexibility in incorporating new peripheral devices, without impacting the software product set. This includes the ability to emulate existing computer systems, thus capturing the software investment, while upgrading processor and peripheral performance.

FEATURES
- User microprogrammable, including emulation features
- Binary, two's complement 32-bit arithmetic; fixed point and single/double precision floating point
- Memory access, through paging, up to 4 million bytes (8 bits); bit, byte, half-word and word addressing with memory protection and parity
- Eight CPU operation states, 32 general-purpose registers per state
- Control Data supported standard software, including MPX/OS operating system, macro and micro assemblers, FORTRAN compiler, on-line debug, file-based structure, system utilities (COSY, PRELIB, FMP, COPYL, etc.) diagnostics
- Local cache memory in the CPU for instructions, look-ahead stack, with a stack per program state

SPECIFICATIONS

Processor –
Type: General-purpose, microprogrammable digital processor
Organization: Microprogrammed control may be used to emulate various architectures
Micromemory Type: Semiconductor, read/write or read only, 70 nanosecond cycle time
Size: 2048 or 4096 32-bit microinstruction for CPUs and IOCs
Arithmetic: Native mode; binary 2's complement, single- and double- precision
Emulation mode; binary 1's or 2's complement (dynamic selection), single- and double-precision
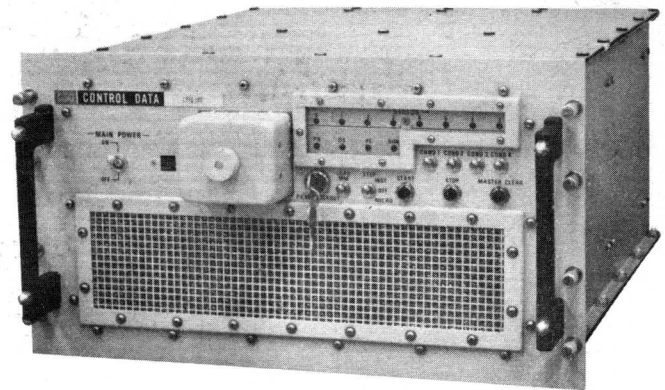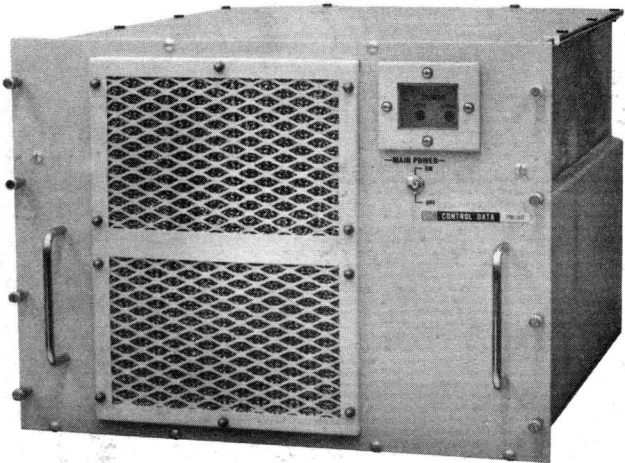
Main Memory –

Large Plane Type: Core storage; configured as 131k bytes or 262K bytes (8-bit data, 1-bit parity), self-contained module (power and cooling)

Interface: Four or eight part continuous scanner per module, daisy-chained modules

Cycle Time: 950 nanoseconds

I/O Controllers: Interfaces to CDC® 1700, CDC 3000 Series; NTDS channels; RS232; others to suit application

Mechanical –

Construction: Rack mounted, modular enclosure standard industrial and AN/UYK-25(V)

Power Requirements (Max) –

CPU: 500 W
IOC: 600 W
Memory Module: 600 W

Physical Characteristics –

	Size	Typical Weight
CPU:	19 x 10.5 x 27.5 in (48.3 x 26.7 x 69.9 cm)	100 lbs (45.4 kg)
IOC:	19 x 10.5 x 27.5 in (48.3 x 26.7 x 69.9 cm)	100 lbs (45.4 kg)
Memory (4-port):	19 x 14 x 23 in (48.3 x 35.6 x 58.4 cm)	125 lbs (56.7 kg)
Memory (8-port):	19 x 15.75 x 23 in (48.3 x 40.0 x 58.4 cm)	135 lbs (61.2 kg)

MTBF: Field reliability data, for various environmental and equipment maturity factors, has demonstrated the following:
CPU: 2700 TO 7860 hours
IOC: 3200 to 17 400 hours
LPM: 3900 to 5700 hours

MTTR (with fault-isolation diagnostics): 30 minutes

Specifications subject to change without notice