Printed Circuit Manual

VOLUME 1

CONTROL DATA

CORPORATION

Pub. No. 60042900
May, 1966

Address comments concerning this manual to:

Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
St. Paul, Minnesota 55112

or use Comment Sheet in back of this manual.

60042900	**Record of Revisions**
REVISION	NOTES
A	Corrections
B	1604 Inverter Ground Rules and Hammer Storage Card
	91 pages added.
C	Long Line Driver and Receiver Cards CA98 and HA26
	pages added.
D	Corrections to card type C64 and C65.
E	Add index tabs, chapter headings, new Table of Contents
	addition to Appendix, type "E" and 1604 cards; and
	Delay Card P13A.
F	Replace the following pages: 3-HA18-1 and 2; 4-C62 and
	C-61-5 and 6; Appendix pages 5 thru 10. Add pages 4-60,
	60A, 62 and 67-1 thru 3; 4-79A-1, 5-97-1 and 2, 5-E10-1.
	Replace page 4-E12-1.
G	6600 Info and Circuit Module Schematics added as Vol. 3.
H	Vol. 1, addition of revised Record of Rev. Vol. 2 add.
	of Record of Rev. Replace the following revised pages;
	Chapter 4 contents page, 4-C62 and C61-1, 4-C62 and
	C61-2, 4-C62 and C61-3, 4-C62 and C61-5, 4-C62 and
	C61-6, 4-C62 and C61-7, 4-P14A & P16A-3, 5-C94-3.
J	Vol. 1, page 2-3600 Inv-3 revised. Vol. 2, Chapter 5,
	second page of contents revised, removed pages 5-PED-1
	thru 5-PED-22. Chapter 6 added and Appendix 1, pages
	16, 17 and 18 removed and new pages added.
K	Publications Change Order 11170. Record of Rev. for
	Vol's. 1 and 2 revised. Removed pages 15 thru 31 of vol.
	2, Appendix 1 and replaced with revised pages.
L	Change Orders 10344 and 10708. Pages v, vi, vii, viii of
(10-5-65)	volume 1 revised. Chapter 4 contents page, 4-HA19-3,
	4-HA37 & HA43-10, 4-P14C & P16A-1, 4-P14C & P16A-2,
	4-P14C & P16A-3, chapter 5 contents pages, 5-C84-1,
	5-C84-2, 5-C84-3 (new page), 3, 4, 7 & 8 (appendix)

60042900

Record of Revisions

REVISION	NOTES
L (Cont'd)	revised. Pages 5-C60-1, 5-C60-2, 5-C60-3, 5-C97-1,
(10-5-65)	5-C97-2, and 5-C97-3 added. Pages 5-HA27 & 5-HA28-1
	and 5-HA27 & 5-HA28-2 revised.
M	Change Order 12131. Appendix 1: pages 16 through 31
(12-13-65)	revised and pages 32 through 47 added.
N	Publication Change Order 12940. New Peripheral
(5-13-66)	Equipment cards added to Chapter 6: ADH, ITA/ITB/ITC,
	ITD, IYA, OJB, OYA and UJB. Revised text for page:
	6-OHA-1. Revised schematic for page 6-IAA, IAB-2.
	Appendix 1 revised. This revision obsoletes all editions
	of Pin Assignments - 1604 & 3600 - Printed Circuit
	Cards, Pub. No. 60106200, which is now included in
	this revision.
P	Publication Change Order 13632. Pages 6-ISC-1 of
(5-13-66)	chapter 6 is revised. The following new cards are
	added to chapter 6: ALA, AMF, AMG, AMH, AMI,
	ANB, ANC, AND, AUA, EUA, EUC, EVB, FCA, FCB,
	FDA, FGA, FHA, FIA, FJA, FKA, FLA, FLB, FMA,
	FNA, FPA, FRA, FSA, FTA, FUA, FVA, FWA, FYA,
	JBA, JCA, JDA, and OTA.
R	Publications Change Order 15800. The following new
(2-13-67)	cards added to Chapter 6: AIB, AKA, AOA, ATA, ATB,
	AVA, AYA, BAA, BAB, BBA, BCA, EEG, EEH, EWA,
	EWB, EZA, FAB, FOA, FOB, FRB, FRC, FRD, FSB,
	FUB, FWB, FXB, GAA, GBA, GCA, GCB, GCC, GCD,
	IOB, IOC, IOD, JEB, JEC, ONA, OUA, OVA, UEA,
	UHB, UIA, UJC, UKA, and UKB.

PREFACE

This manual is for use by design engineers, maintenance personnel, and others who need detailed characteristics of CONTROL DATA* Printed Circuit Cards. A separate manual is available for those interested in schematics only. THE SCHEMATICS INCLUDED IN THIS MANUAL DO NOT NECESSARILY REFLECT THE LATEST REVISIONS.

The descriptions and schematics presented in chapters 2 through 5 are representative of the various types of circuits. Any user who desires more information about a given circuit may order a print of the schematic drawing from the cognizant division, using the drawing number from one of the tables in the appendix section. The schematic drawing bears the name of the designer, who may be contacted for first-hand information.

The appendix section of this manual contains tables listing all printed circuit cards produced by Control Data Corporation. Further up-to-date listings may be obtained by ordering the Standard Printed Circuit Card Index, available from Engineering Services, Computer Division.

Page numbering system used in this manual provides modularity so that additional circuit descriptions may be inserted without affecting the sequential order of page numbers. Additional descriptions may be obtained from the Technical Publications Department as they become available.

Every effort will be made to keep this manual current. Users are requested to notify the Technical Publications Department of any errors or suggestions for improvement.

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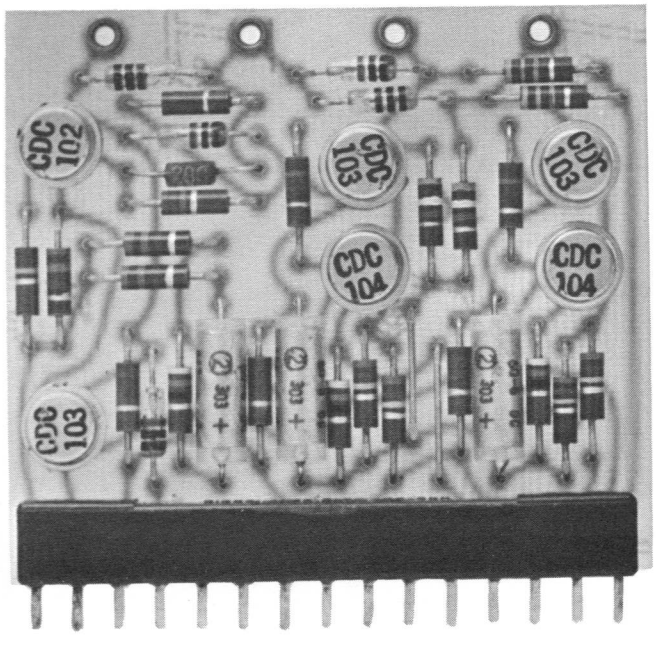
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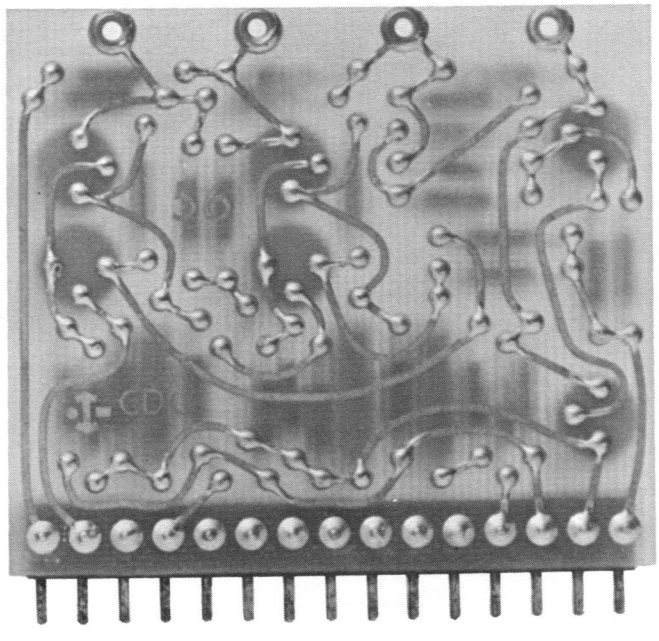


CONTENTS

CARD TYPE		CHAPTER	CARD TYPE		CHAPTER
C61	Receiver	4	E02A	Crosspoint Module	5
C61B	Receiver	4	E03A	Crosspoint Control Module	5
C62A	Transmitter	4	E04A	Crosspoint Control Module	5
C64A	Resync Circuit	5	E05	Decoder	5
C65A	Resync Circuit	5	E06	Terminator	5
C66A	Resync Circuit	5	E07	Terminator	5
C67	Capacitive Delay	5	E08	Single Pulser	5
C68	Capacitive Delay	5	E10	Integrator	5
C69	Capacitive Delay	5	E11	Delay	5
C70C	Capacitive Delay	5	E12	Line Driver	4
C71	Capacitive Delay	5	E13	Line Receiver	4
C75	Modified M^{---} Input	4	E14	Variable Clock	5
C75B	Modified M^{---} Input	4	E15	Line Driver	4
C76	Modified L^{---} Output	4	E19	Terminator	5
C76A	Modified L^{---} Output	4	E20	Resistor Assembly	5
C77	Priority Circuit	5	E61A	Line Receiver	4
C78B	Priority Circuit	5	E62B	Line Driver	4
C79A	Priority Circuit	5	E67A	Line Driver	4
C80	Delay Line, 1 usec	5	H10A	Console Interface	5
C81	Crystal Oscillator	5	H11A	Receiver	4
C82	Crystal Oscillator	5	H12	Delay Line Amplifier	5
C83	Crystal Oscillator	5	H14	Digit Driver	3
C84	Relay Driver	5	H15	Digit Compensator	3
C85	Strobe Shaper	5	H16	Sense Amplifier	3
C86	I/O Sense Amplifier	3	H17	Filter	5
C87	I/O Memory Driver	3	H18	Sense Amplifier	3
C88	I/O Memory Diverter	3	H19	Transmitter	4
C89	Amplifier - Shaper	5	H20	Light Driver	5
C90	I/O Emitter Follower	3	H26	Long Line Receiver	4
C91	Reader Level Amplifier	5	H27	Keyboard Translator	5
C94	Overload Protector	5	H28	Keyboard Translator	5
C97	Channel Disable	5	H31	Level Translator	4
C98	Long Line Driver	4	H32A	Line Driver	4
E00	Jumper	5	H35	Delay Line, 0.1 usec	5
E01A	Crosspoint Module	5			

CHAPTER 1. ELEMENTS OF CONTROL DATA LOGIC

The basic logic element in Control Data computers and peripheral devices is a transistor inverter circuit. A flip-flop (FF) is a combination of two inverters; a control delay is three inverters with clocked inputs. The major portion of a digital computer is built by interconnecting these circuits. Connections of inverters, flip-flops, and control delays form the various units of a digital computer, e. g., registers, counters, adders, complementers, and comparators. To facilitate the diagrammatic representation of these circuits the logic diagram technique is used. This technique emphasizes the functional aspect of a digital computer rather than the electronic aspect.

As a general rule, a digital computer has four main sections: Control, Arithmetic, Storage, and Input/Output. The Control and Arithmetic sections can be grouped under Logic section. Accordingly, the descriptions of the circuits in this manual are presented in four groups: Logic, Storage, Input/Output, and Special Purpose, (Chapters 2, 3, 4, and 5).

PRINTED CIRCUIT CARDS

Control Data electronic circuits are mounted on printed circuit cards (frontispiece). Each card is equipped with a 15 pin male connector for plugging into the equipment chassis. The printed circuit card technique has the advantages of ease of design and maintenance, use of solid state components, greater reliability, and modular construction.

INVERTER

The basic logic building block is an inverter circuit, represented by a rectangle as shown in figure 1-1. This circuit employs a 180^{o} electrical phase shift to produce an inversion; a "1" input results in a "0" output, and vice versa. In addition to use as an inverter, combinations of this basic logic element form bi-stable flip-flops and control delays.

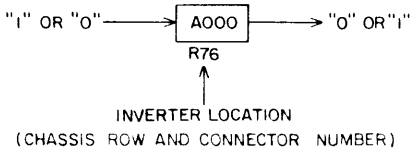


Figure 1-1. Conventional Inverter Symbol

FLIP-FLOP (FF)

A FF is two inverter circuits interconnected as shown in figure 1-2. Each rectangle represents a single inverter. One of the inverters is the set side of the FF; the other, the clear side. The FF is placed in the "1" (set) state by a "1" signal on the set input. Conversely, it is placed in the "0" (cleared) state by a "1" signal on the clear input.

The storage capability of a FF means that the FF remains in the state in which it was placed by the last "1" input. Specifically, if a "1" signal is present at the set input, then the output of inverter K000 (figure 1-2) becomes "0". This output is applied as an input to K001 and its output then becomes "1". The output of K001 is fed back to K000. Thus, when the set input drops to "0", the feedback connection between K000 and K001 permits the storage of the state to which the "1" signal on the set input forced the FF. Should the clear input later receive a "1" signal the output of K001 becomes "0", and the feedback input to K000 is "0". Consequently, K000 furnishes a "1" output which is returned to K001 and replaces the "1" signal at the clear input.

When the FF is set, K001 has a "1" output and K000 has a "0" output. Conversely, when the FF is cleared, K001 has a "0" output, and K000 has a "1" output.

The conventional square or box symbol for a FF is used in figure 1-2 to show the relationship between it and the inverter configuration which forms the FF. The square which represents the FF encompasses the crossover of the outputs.

CONTROL DELAY

The function of the control delay is to synchronize a sequence of logic operations within the computer with the two-phase master clock. Logical "1" inputs are received during one phase time, either odd or even, and "1" outputs are provided during the next phase time, either even or odd. The phase time of the output is opposite the phase time of the input.

DEFINITION OF A CLOCK PHASE TIME

A clock phase time is the time during which an inverter driven by that phase has a "1" output. The input to the inverter is the raw clock signal received directly from the clock card. Thus during a clock phase time, the raw clock signal from that phase is a logical "0".

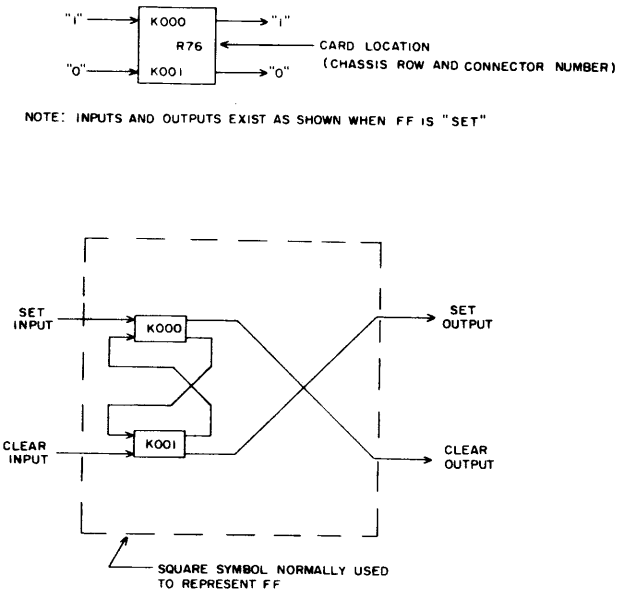


Figure 1-2. Conventional Flip-Flop Symbol

The response time of the inverter is approximately 1/4 to 1/2 a phase time. Thus the clock phase time always lags behind the raw clock signal, due to the delay of the inverter. However, this delay is not shown in the timing diagram of figure 1-4.

DESCRIPTION

The control delay consists of a FF having its feedback ANDed with a raw clock signal, and one or more inverters with two OR inputs each, which are driven by the A section of the FF and by a raw clock signal. The raw clock signal which enables the FF feedback is the phase opposite that which drives the inverter or inverters.

A diagram of a control delay symbol and the circuits encompassed by it is shown in figure 1-3. Figure 1-4 shows the timing of its operation.

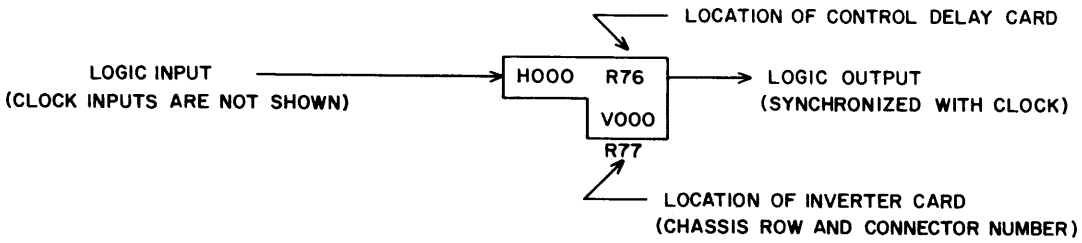
The clock inputs to a control delay are ordinarily not shown on a drawing. It is understood that the output occurs during the odd or even phase time, while the corresponding raw clock signal is a "0", depending upon whether the third superscript digit is odd or even. For example, control delay H100/V100 would have its output during an even clock phase time, while H101/V101 would have its output during an odd clock phase time.

The logic input to a control delay is gated by the external circuitry. Normally, the input drops to "0" shortly after the output appears, and is not repeated. If the input does not drop, then the output of the control delay is a series of pulses from the inverter, since it is driven by the raw clock signal.

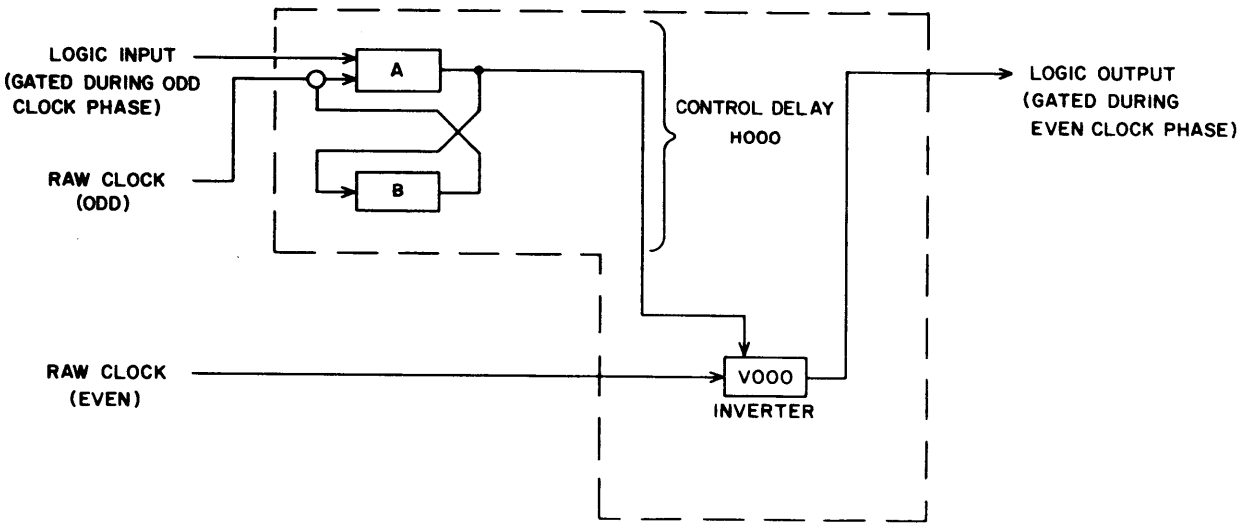
CIRCUIT OPERATION

Figure 1-3 shows that the gated logic input goes directly into the A section of H000. This forces the output of A to "0", resulting in a "1" output from B. The input to A is gated during the odd clock phase time; thus during this time, the odd raw clock signal is "0". When the odd raw clock signal becomes "1", the logic input to A drops, but the feedback path from B to A is enabled so that A continues to have a "0" output until the next odd clock phase time.

Inverter V000 is gated both by the output of A and by the even raw clock signal. With a "0" input from A, inverter V000 provides a "1" output during the even clock phase time, since the even raw clock signal is a "0". The "1" output from V000 continues until the next odd clock phase time disables the FF feedback, and the control delay returns to initial conditions.



NOTE:
INVERTER MAY BE REPRESENTED BY EITHER V---, N---, OR Y---.



NOTE:
LOGIC INPUT IS GATED INTO CONTROL DELAY WHILE ODD CLOCK PHASE IS "1". THE INPUT DROPS WHEN ODD PHASE BECOMES "0" AND IS NOT REPEATED.

Figure 1-3. Conventional Control Delay Symbol

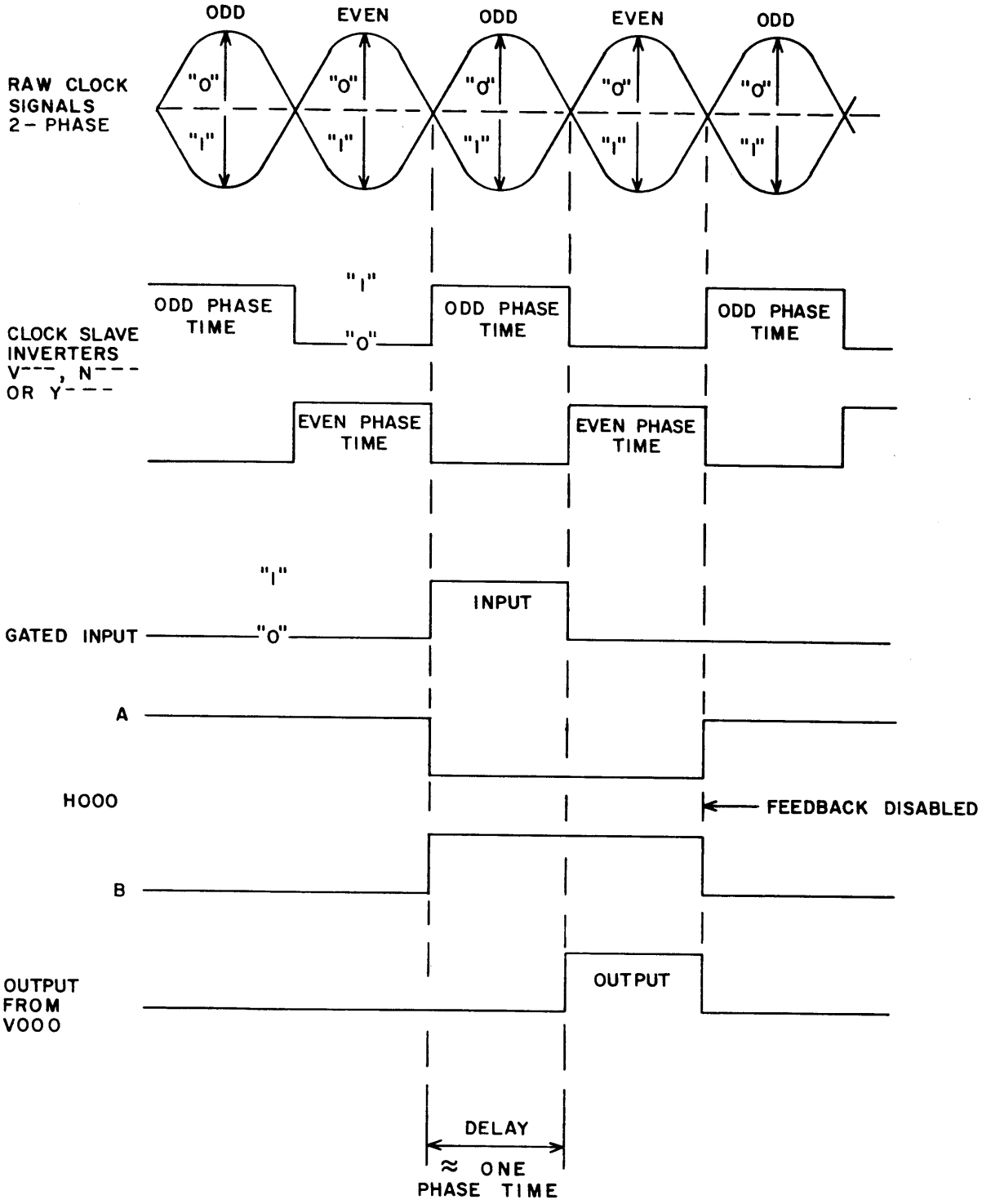


Figure 1-4. Control Delay Timing Diagram

LOGICAL EQUATIONS OF A CONTROL DELAY

A control delay may be represented by a minimum of two logical equations: one equation for the H--- term, and one equation for each V---, N---, or Y--- term. The symbol on the left of the equal sign is the subject term, and the expression on the right describes the configuration of its inputs.

All raw clock and gated logic inputs to a control delay are represented in its equations. The H--- term requires a logic input gated during a clock phase, and a raw clock signal which gates the FF feedback. The V--- term requires a raw clock signal to gate its output, and a logic input from the H--- term. These conditions are covered by the following basic rules:

1. Every input term of an H--- equation must contain one, and only one, clocked symbol such as V---, N---, or Y---.
2. The last term of an H--- equation must be a C--- (raw clock).
3. At least one input term of a V---, N---, or Y--- equation must contain an H--- symbol.
4. The last term of a V---, N---, or Y--- equation must be a C--- (raw clock) symbol.

A set of equations for control delay which would have an output during an even phase time could be written as follows:

H000 = Z024 W005 N001 + C001

V000 = H000 + C000

The symbols in the above equations refer to the following:

H000	A circuit on a control delay card which receives its input during an odd phase time, since the third superscript digit is even.
Z024	A logic input.
W005	A logic input.
N001	A clock slave inverter which provides a "1" input enabling the 3-way AND during an odd clock phase time.
C001	A raw clock signal which is a "0" during odd clock phase times; it is received at the control delay card and gates the FF feedback.
V000	The inverter portion of the control delay which provides a "1" output during an even clock phase time only.
C000	A raw clock signal which is "0" during even clock phase times and drives the control delay inverter.

LOGICAL "AND"

A three-input AND circuit is shown in figure 1-5. The small circle and connections used to represent this circuit on a logic diagram are also shown.

The AND gate requires that all inputs must be a "1" simultaneously. If any one of the AND inputs is a "0", then a "1" on another input is not sensed.

Thus, if the transistors A, B, and C are not conducting, their output diodes are biased in the reverse direction, and the resulting output signals are at the logical "1" level. This condition allows the -20v through the AND resistor to place a negative voltage on the base of transistor D, so that it conducts.

However, if any one of transistors A, B, or C is conducting, its collector goes to approximately ground potential. Its output diode is biased in the forward direction from the -20v through the AND resistor. This prevents the -20v source from applying drive current to transistor D, and transistor D is held in the non-conducting state.

LOGICAL "OR"

A three-input OR circuit is shown in figure 1-6 (the conventional logic diagram representation is also shown). An OR gate allows a "1" signal on any input to be sensed, although a "0" signal may simultaneously appear on another input.

Figure 1-6 shows three single-input ANDs connected to produce three logical OR inputs to transistor D. The input lines are separated by diodes, so that a "1" signal is not nullified by a "0" signal on another input line. Thus, if any one of transistors A, B. or C is not conducting so that it has a "1" output, the -20v through the respective AND resistor applies a negative voltage to the base of transistor D, causing it to conduct.

BASIC THREE-STAGE COUNTER

A counter is essentially a double rank register which increases or decreases the quantity stored, an increment at a time. The three-stage counter circuit shown in figure 1-7 is additive from binary 000 through 111.

A count is stored in two steps:

1. A "1" input on the Advance line sets a FF in rank 1. This occurs in consecutive order and when all three are set, the next

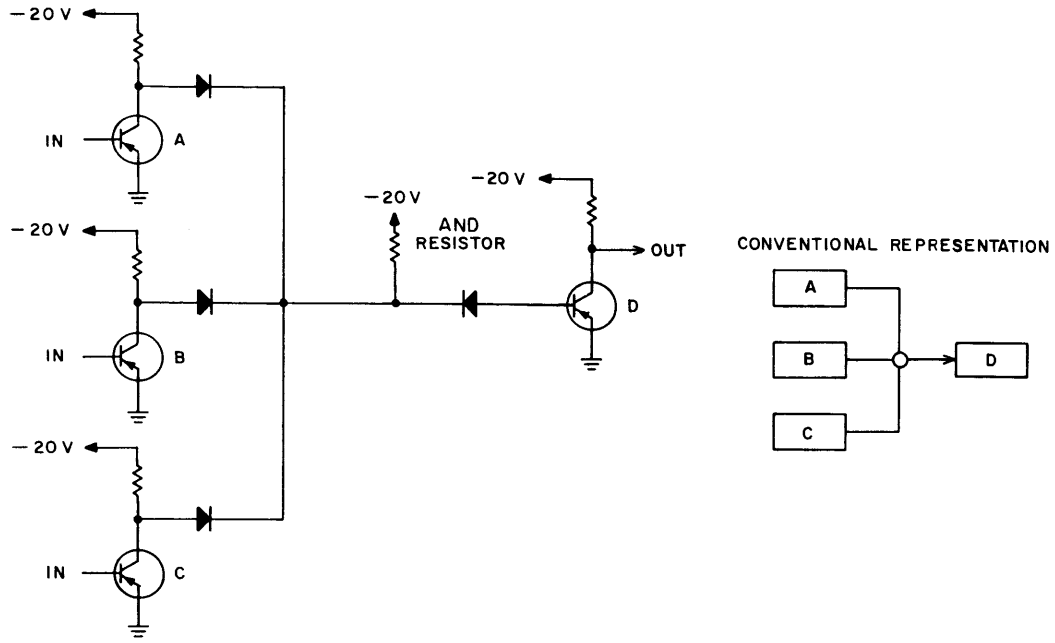


Figure 1-5. Logical AND

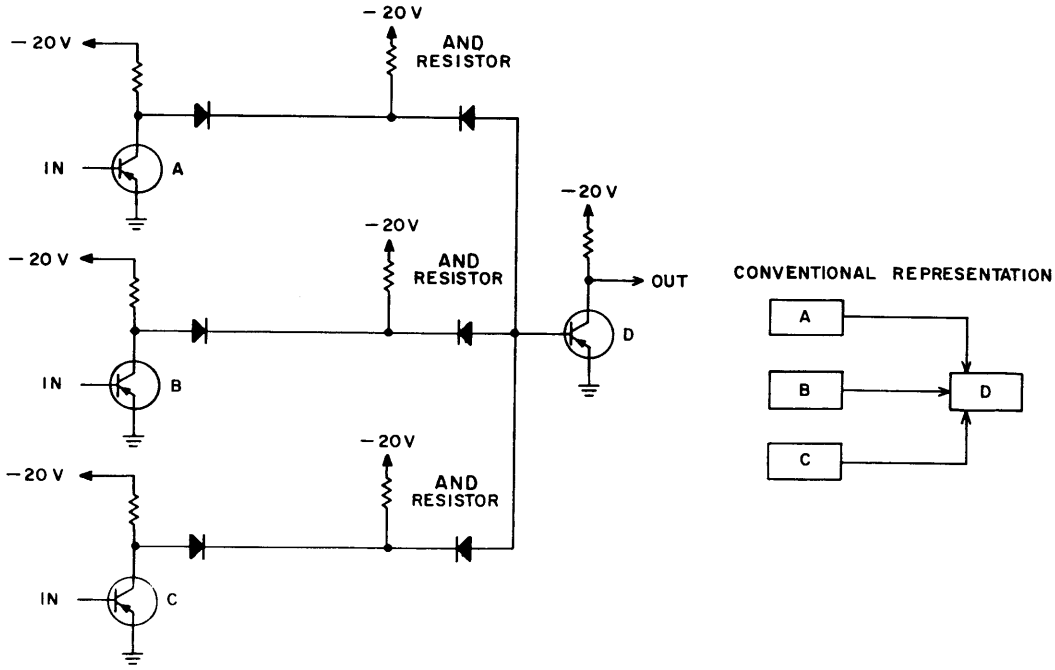


Figure 1-6. Logical OR

input clears them.

2. A "1" input on the Transfer line causes the FFs in rank two to assume the identical states as their corresponding FFs in rank 1.

To analyze the operation of the counter, assume that both ranks are initially cleared, so the count stored is zero. The first Advance command finds the AND gate to K000 enabled and therefore enters the count 001 (octal 1) into rank 1. This partially enables the AND gate to K002 so that the Transfer command enters the count 001 into rank two. The next Advance command finds the AND gate to K001 and K010 enabled and thus enters the count 010 (octal 2) into rank 1. The operation continues in this manner as shown in table 1-1 until the count reaches 111 (octal 7), which is the highest possible count in a three-stage counter. This is followed by a command sequence which returns both ranks to the count 000.

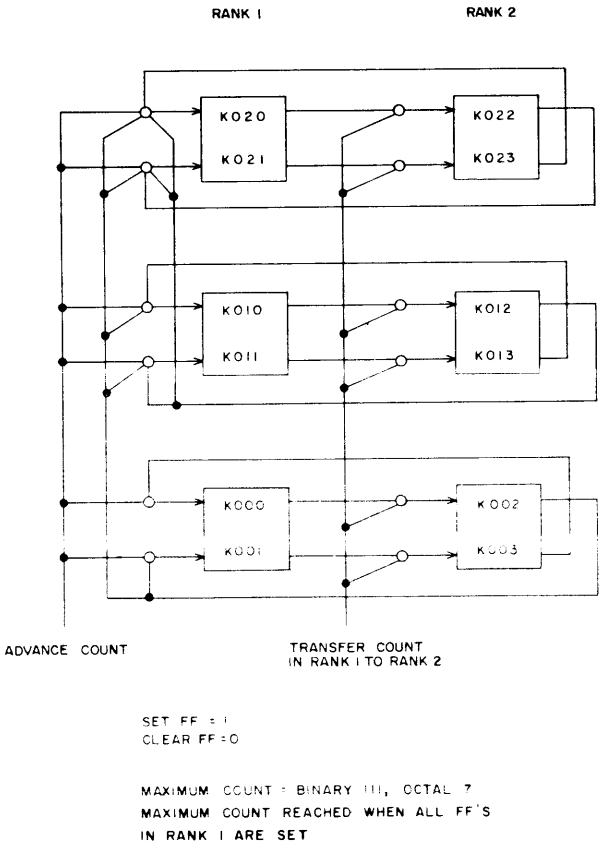


Figure 1-7. Basic Three-Stage Counter

TABLE 1-1. COUNTING SEQUENCE FOR THREE-STAGE COUNTER

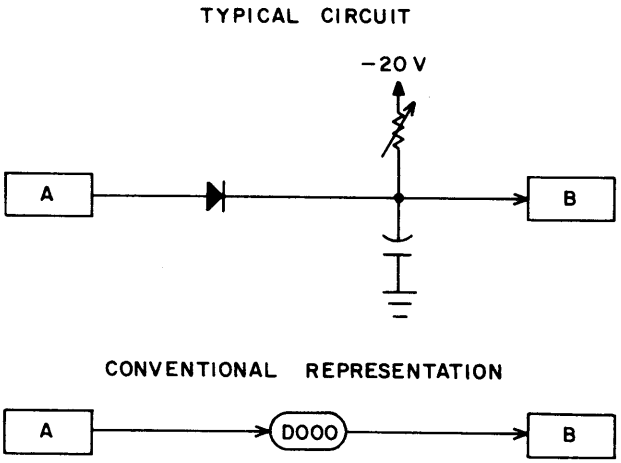
Command	Quantity Stored (Octal)	Rank 1			Rank 2		
		K02-	K01-	K00-	K02-	K01-	K00-
Initial conditions	0	0	0	0	0	0	0
Advance	1	0	0	1	0	0	0
Transfer		0	0	1	0	0	1
Advance	2	0	1	0	0	0	1
Transfer		0	1	0	0	1	0
Advance	3	0	1	1	0	1	0
Transfer		0	1	1	0	1	1
Advance	4	1	0	0	0	1	1
Transfer		1	0	0	1	0	0
Advance	5	1	0	1	1	0	0
Transfer		1	0	1	1	0	1
Advance	6	1	1	0	1	0	1
Transfer		1	1	0	1	1	0
Advance	7	1	1	1	1	1	0
Transfer		1	1	1	1	1	1
Advance	0(or8)	0	0	0	1	1	1
Transfer		0	0	0	0	0	0

CAPACITIVE DELAY

Capacitive delay circuits are constructed by placing a capacitor from the signal line to ground. The delay time is the time required to charge the capacitor when a "1" signal appears on the line. A "0" signal is delayed approximately one tenth as long as a "1". The method of connecting a delay between two logic cards, and the symbols used to represent this connection on a logic diagram are shown in figure 1-8.

Figure 1-8 shows that when the transistor on card A is conducting, its collector is almost at ground potential. Hence, the voltage across the delay capacitor is quite low and it contains very little charge. However, when the output of card A switches to "1" and its transistor stops conducting, the circuitry attempts to bias the input line at the "1" level. Initially this voltage is absorbed by the uncharged delay capacitor, which gradually obtains a charge as shown in figure 1-9.

Two factors govern the delay time: the size of the capacitor and the rate at which it receives charging current. Generally, the larger the capacitor, the longer the delay time. The delay time may be adjusted by varying the resistance in series with the capacitor. Increasing the resistance decreases current flow to the capacitor, increasing the delay time.



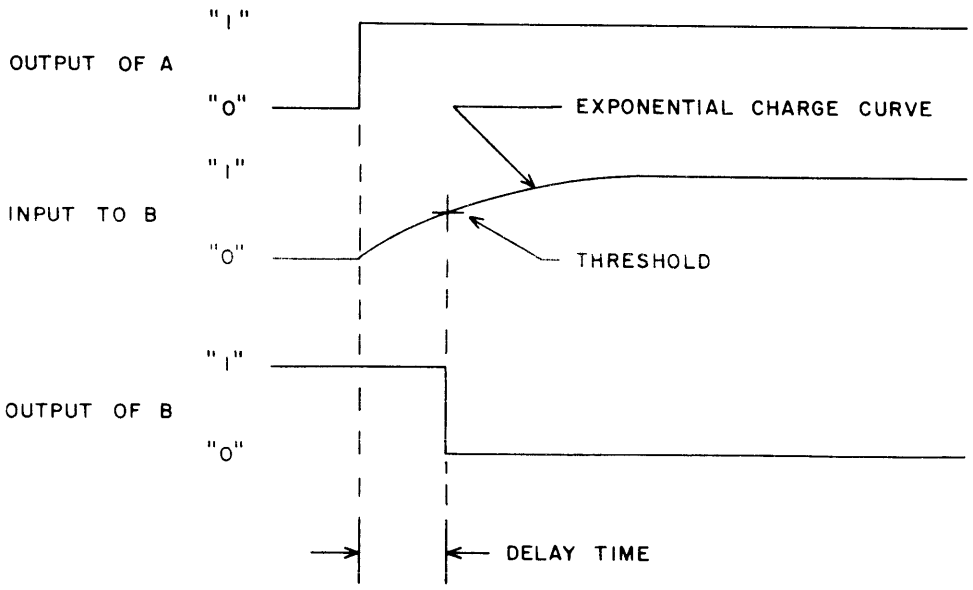
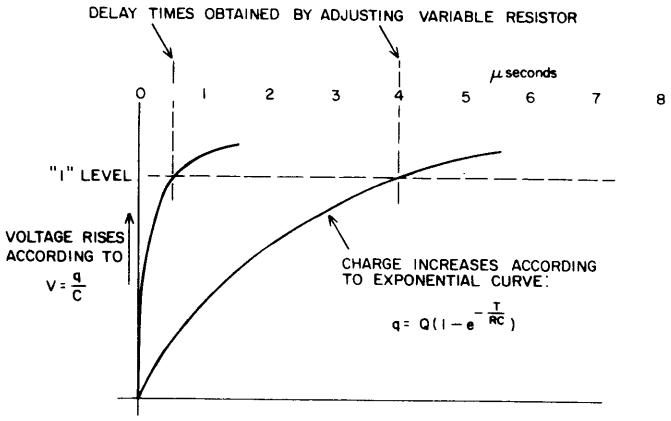


Figure 1-8. Capacitive Delay



NOTE:

SYMBOL	REFERS TO:	UNITS
T	TIME	SECONDS
q	PARTIAL CAPACITOR CHARGE	COULOMBS
Q	FINAL CAPACITOR CHARGE	COULOMBS
R	SERIES RESISTANCE	OHMS
C	CAPACITANCE	FARADS
V	APPLIED POTENTIAL	VOLTS
e	NATURAL LOGARITHM BASE	PURE NUMBER 2.718, APPROX.

Figure 1-9. Capacitor Charge Curve

PULSE FORMING NETWORKS

Many circuits contain pulse forming networks, consisting of two inverters and a capacitive delay, for the purpose of reshaping a steady "1" signal into a short "1" pulse. There are two types: those which produce a pulse upon receipt of a "1" signal and those which produce a pulse when the "1" signal ends. These types are known respectively as "leading edge" and "trailing edge" networks, and are presented in figure 1-10.

When a "1" input is received by a leading edge network, an immediate double inversion occurs, producing a "1" output. However, as soon as the capacitor is sufficiently charged, a "1" is sent directly into A001, and the output of inverter A001 switches to "0".

In the case of a trailing edge network, the steady input signal is fed directly into both inverters. Thus, when this signal goes to "0", the output of both inverters switches to "1". However, the "1" output of A000 does not reach A001 until the capacitor has charged sufficiently; at that time the output of A001 switches to "0".

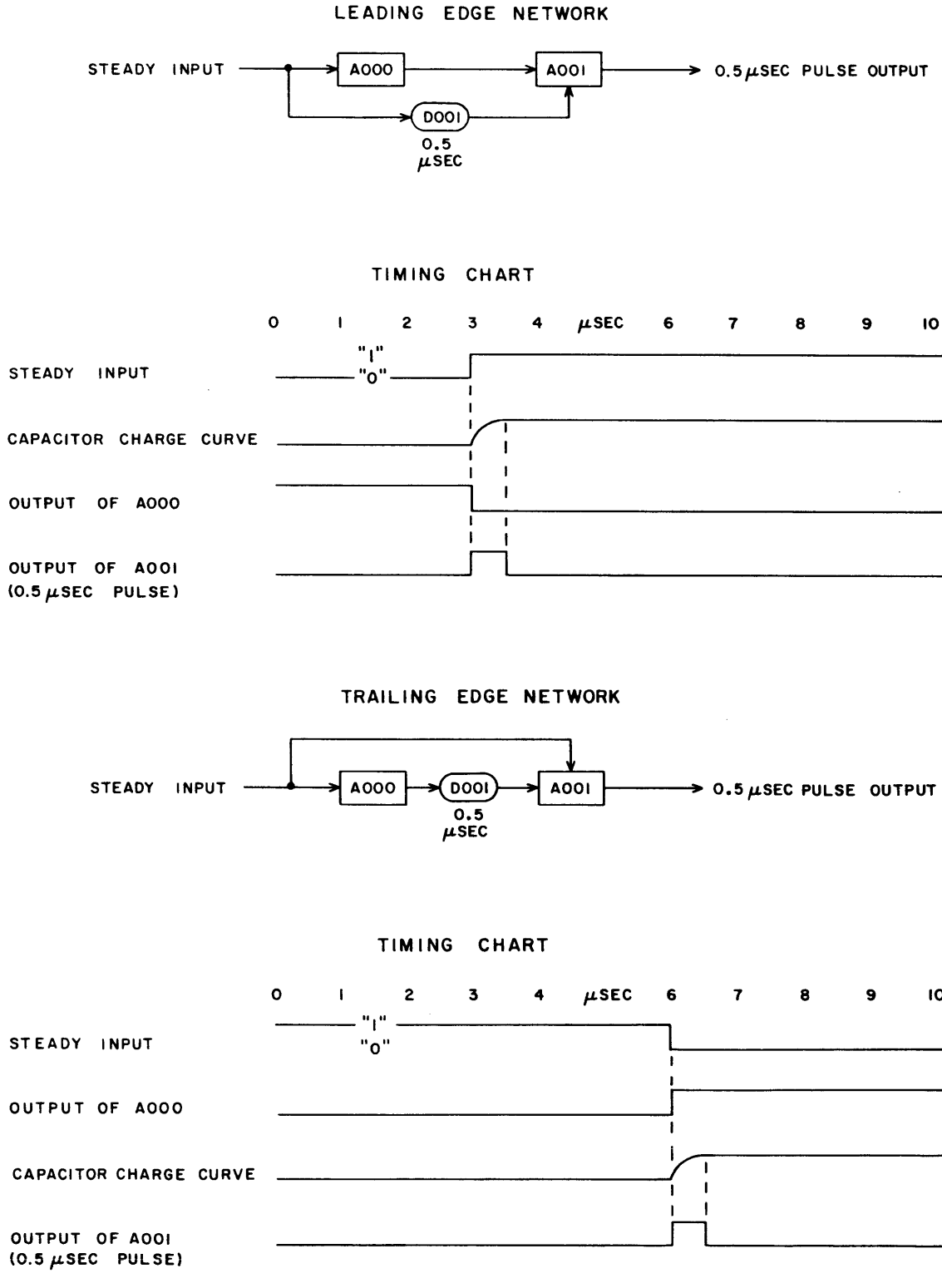


Figure 1-10. Pulse Forming Networks

TIMING CHAIN PULSE GENERATOR

A convenient method of obtaining a series of sequential pulses using flip-flops and delays is shown in figure 1-11.

The two FFs exhibit four distinct sets of conditions at successive time intervals. Initially both are in the clear state. A "1" pulse input to K000 sets K000/001, so that K001 has a "1" output. After a brief delay, this signal sets K002/003. K003 then sends a "1" through a delay to K001, so that K000/001 is cleared. This causes K000 to send a "1" through the third delay to K003, so that K002/003 is also cleared and initial conditions prevail.

These four conditions and the times at which they occur are as follows:

	K000/K001	K002/K003
Time 0	Clear	Clear
Time 1	Set	Clear
Time 2	Set	Set
Time 3	Clear	Set
Time 0 (or 4)	Clear	Clear

The lengths of these time intervals are dependent upon the value of the capacitive delays. In the example shown, all of the times are 0.5 us. However, these may be varied in any manner desired.

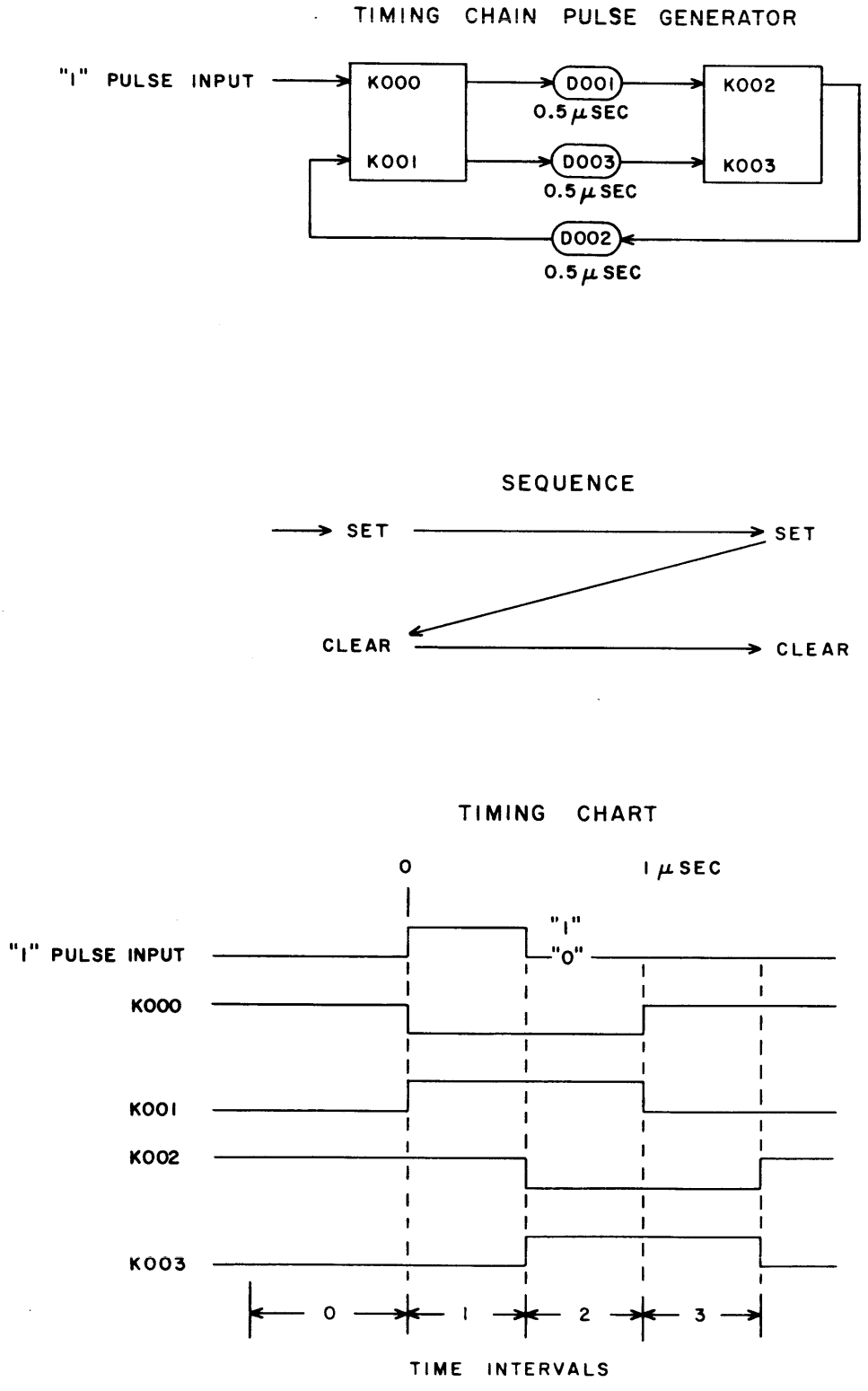


Figure 1-11. Timing Chain

CHAPTER 2. LOGIC CARDS

1604 Inverter Circuit and Ground Rules

3600 Inverter Circuit and Ground Rules

INVERTER CIRCUIT
1604 TYPE

The two signal levels in 1604 type logic are: -3.0v, logical "1", and -0.5v, logical "0". The single inverter inverts these signal levels: a -3.0v input becomes a -0.5v output, and vice versa.

In the standard inverter circuit shown, transistor Q01 is connected as an emitter-follower; Q02, as an amplifier. The collector circuits of the transistors have two feedback loops which prevent the transistors from being driven to cutoff or saturation. As a result, switching from one state to the other is accomplished in from 50 to 100 nanoseconds.

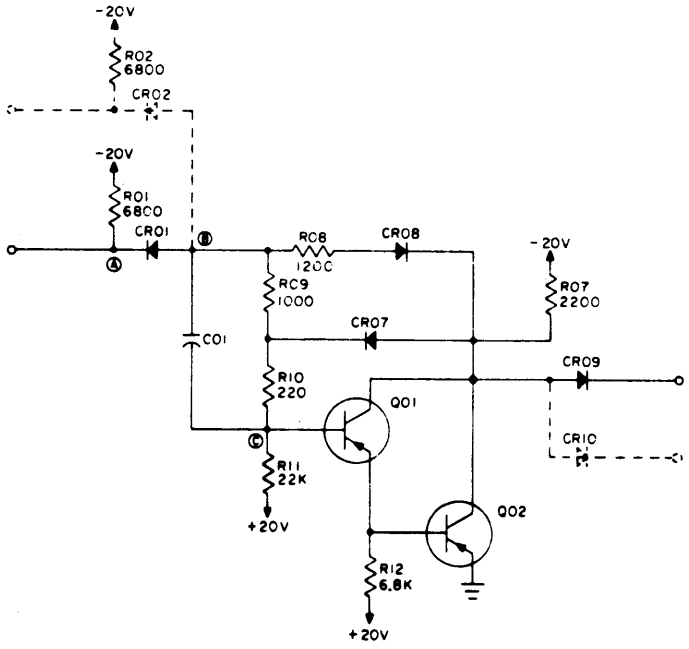
An input signal is applied via isolation diodes CR01 or CR02 to a voltage divider network composed of resistors R07, R08, R09, R10 and R11. An input signal of -0.5v (point A) results in -1.5v at point B and 0.8v at the base of Q01 (point C). CR01 is biased 1v in the backward direction to provide for noise suppression at the input of the inverter. Capacitor C01, between CR01 and the base of Q01, provides rapid coupling of input signal changes to Q01, improving the switching time of the circuit.

Transistors Q01 and Q02 each provide beta* current gains of approximately 100; loop gain of the two transistors is in the order of 10^4. The collector current of Q01 and Q02 develops the output voltage across resistor R07. Output diode CR09 isolates the output line from the other output line connected to CR10.

Diodes CR07 and CR08 form the feedback loops which prevent transistors Q01 and Q02 from being driven to cutoff or saturation. The positive-going limit allows a maximum transistor conduction that is less than saturation; the negative-going limit fixes a minimum conduction for the transistors. When the transistors approach cutoff, their collectors approach -3.0v. The collector potential is coupled back to the base of Q01 through CR08, R09 and R10. As a consequence the base of Q01 always is held at a sufficiently negative voltage to permit some minimum conduction of Q01 and thus Q02.

*The beta current gain is the ratio of collector current to base current.

When the transistors approach saturation, the collectors approach 0v. The collector potential is coupled back to the base of Q01 through CR07 and R10. The base of Q01 is thus prevented from becoming so negative that saturation occurs.



Schematic Diagram of 1604 Type Inverter Circuit

GROUND RULES

The following ground rules for usage of the basic 1604 inverter circuit are intended as guidelines in obtaining optimum performance. They are not intended to be excessively restrictive, because it is often found that a circuit will operate satisfactorily in a configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic and timing considerations, and are the responsibility of the designer.

1) A maximum of eight outputs may be taken from a single inverter.

2) An inverter will drive a maximum of six simultaneously gated AND loads.

3) The total number of inputs and outputs of a single inverter must not exceed 12.

4) The number of OR inputs to an inverter is limited to a maximum of six.

5) For high speed operation, the number of AND connections which can be made to a single OR input should be limited to four. If timing is not critical, the maximum number of AND connections can be increased to six.

6) All unused input pins must be grounded.

7) The minimum switching time for a mesa transistor inverter driving one load is approximately 30 nanoseconds. This will increase to about 75 nanoseconds as additional loads are added.

8) The minimum switching time for a drift transistor inverter driving one load is approximately 50 nanoseconds. This will increase to about 100 nanoseconds as additional loads are added.

9) An inverter will drive a load having 0.015 uf of capacitance. This may be increased at the discretion of the designer; however, long capacitive delays (greater than 10 usec) should be constructed using card type 97.

10) A capacitive delay should not be driven directly by a flip-flop, especially a flip-flop using mesa transistors, unless the discharge time of the capacitance is appreciably shorter than the duration of the input to the flip-flop.

3600 INVERTER CIRCUIT

NOTE

Type CA cards having OR inputs have been discontinued and should not be used for new design.

AVAILABLE CARD TYPES

Three series of printed circuit cards have been produced during development of the 3600 family of computing systems. The initial prototype series was designated Type C. Later, after the design had been approved, the physical size of the phenolic board was increased slightly and the cards went into production as the Type CA series. Except for the addition of more test points, there was no change in the circuit.

As shown in figure 1, logical OR inputs on Type CA inverters consist of only the OR diode without any connection to -20 volts. This was intended to eliminate the requirement for grounding unused OR inputs, since an open OR input will not drive the circuit output to "0". In actual practice, however, it was found that the distributed capacitance of large numbers of open OR inputs could result in a delay in switching time. In addition, since OR inputs did not provide the clamping action of AND inputs, the circuits tended to respond excessively to transients on the signal line. These conditions brought about the development of two new series of cards, called Type HA and Type K. Both of these have the same basic inverter circuit as the Type CA inverter, but the inputs are modified. The logical AND and OR input configuration of a Type K card is identical to the corresponding Type CA number, but all OR's have been converted to single-way AND's including the feedback of flip-flops. Cards in the Type HA series are built with a limited number of inputs, e. g., an HA 07 card contains two inverters with each having only one single-way AND input. Type CA cards have since been discontinued and should not be used in new design.

BASIC INVERTER CIRCUIT

The basic inverter circuit consists of two transistor stages, as shown in figures 1 and 2. Transistor Q01 is a grounded emitter stage which supplies AND current to the load, and transistor Q02 is an emitter follower stage which supplies OR current to the load.

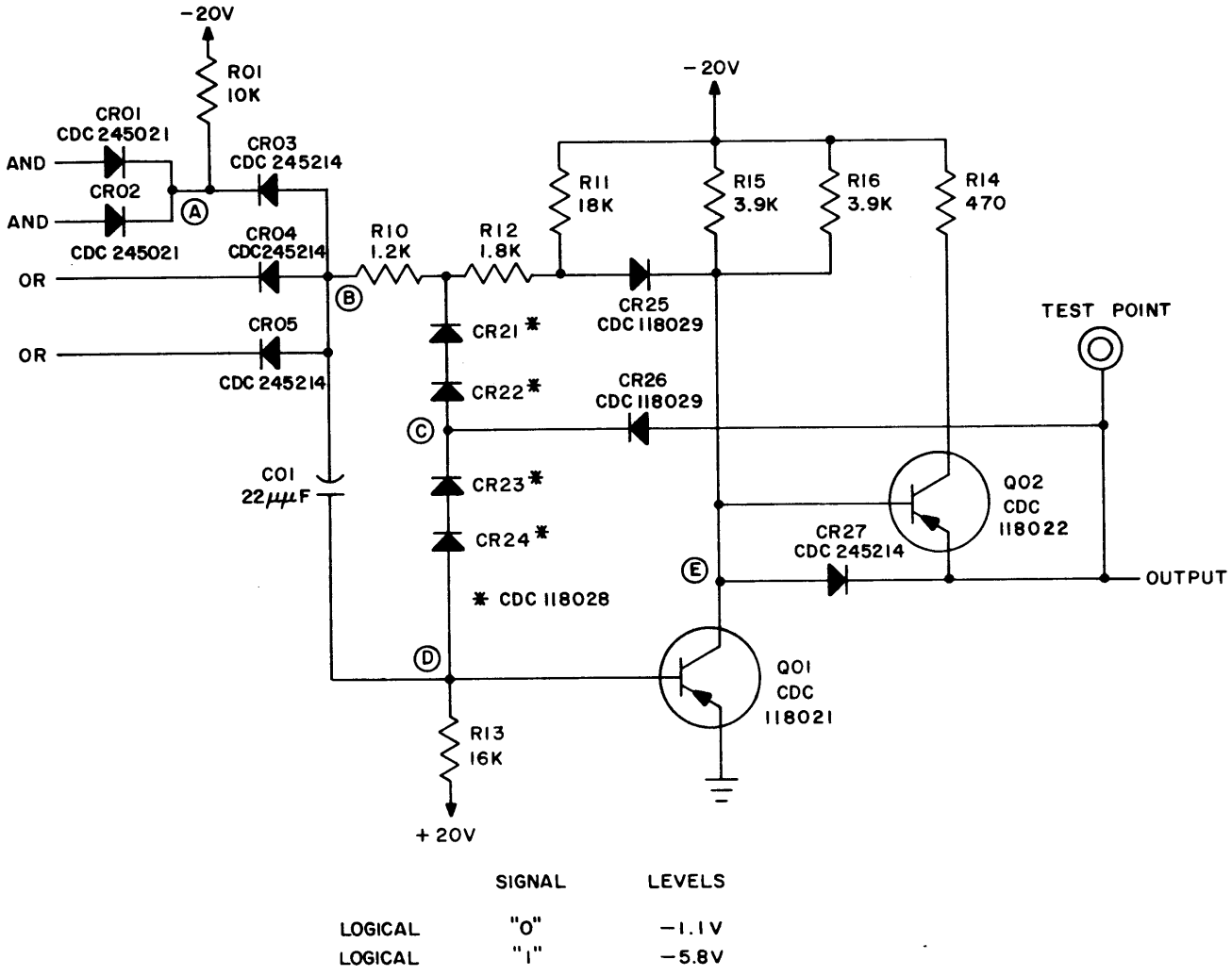


Figure 1. Schematic Diagram Type CA Inverter Circuit
(Not to be used for new design)

The input to the circuit consists of two levels of diode logic. The maximum number of inputs is limited by the number of available input pins on a circuit card; however, the maximum number of individual inputs to any single AND cannot exceed 6.

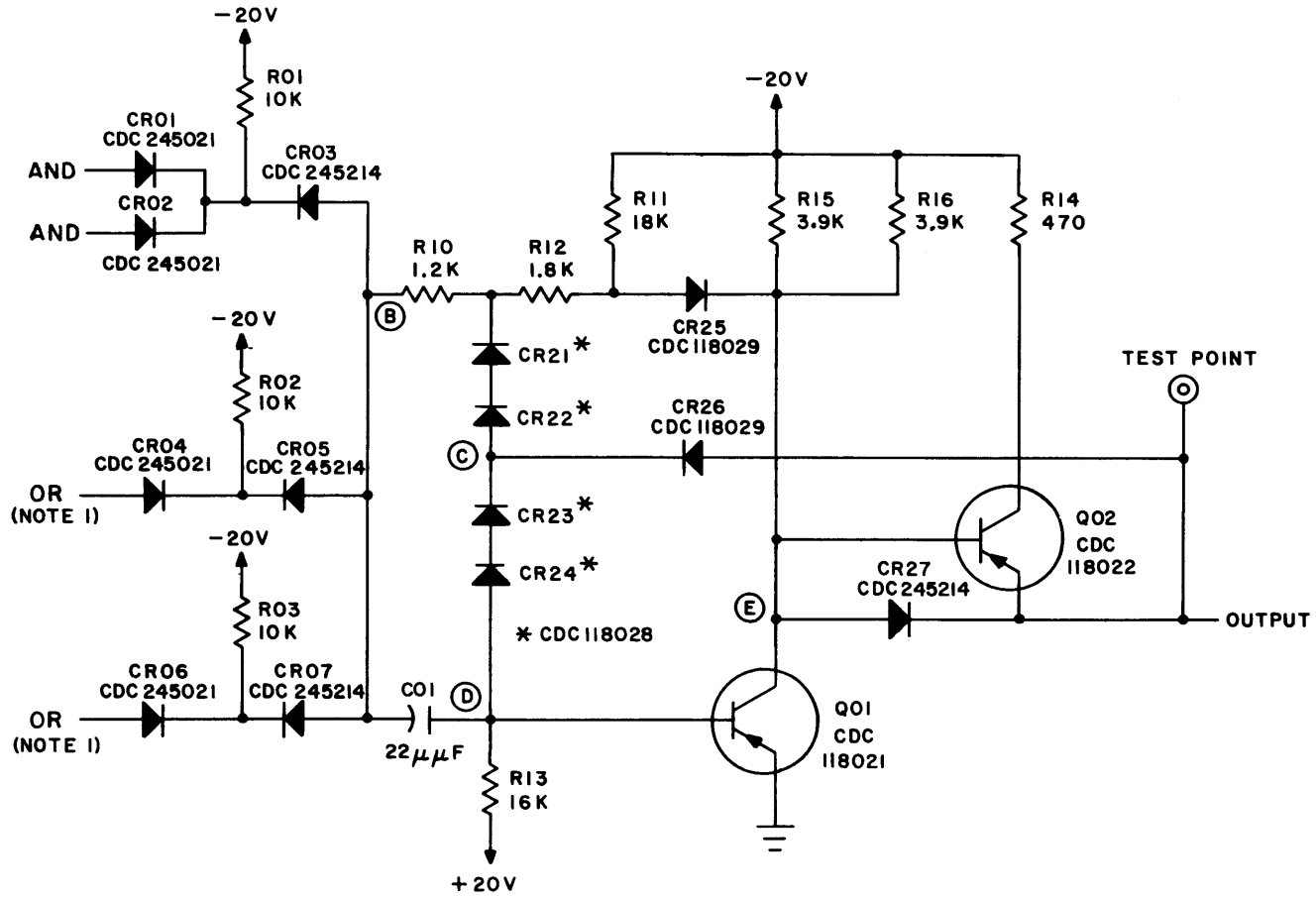


Figure 2. Schematic Diagram of Type K and Type HA Inverter Circuit

The input logic diodes are medium speed germanium devices. Initially, Hughes HD2969 diodes were used, and a set of graphs is included in this report which show the comparative recovery time of these diodes.

The response of an AND input is a function of the time constant of the AND resistor R01, shunt circuit capacitance at point (A) and the recovery speed of the input diodes. Because additional AND diode inputs increase the shunt capacitance, it is necessary to decrease the size of the AND resistor a proportionate amount as the number of inputs to the AND increases beyond 3.

The transition speed of the AND circuit varies inversely with the recovery speed of the AND diodes. Slow diodes allow additional recovery current to be drawn. This, in effect, allows a larger turn-on current in the first transistor stage.

The input resistor and diode network of transistor Q01 establishes the clamping levels for the output signal. This network also provides feedback to the base of Q01 which stabilizes the two quiescent values of the output voltage.

The input network establishes an input threshold level of approximately -3 volts. Thus, the input signal must be more negative than -3 volts before transistor Q01 turn-on current is allowed to flow. Silicon forward drop diodes CR21 through CR24 are used in the input network to obtain a constant d-c level for signal threshold. These diodes also have a low dynamic impedance which causes little attenuation of the input signal current.

The 22 uuf speed-up capacitor C01 on the input of the first stage bypasses the 1.2 k resistor R10 and the diode network during the initial rise or fall of the input signal. This provides additional drive to the base of Q01 during the input signal transition, thereby speeding the switching of this stage.

Feedback is accomplished through two high speed silicon diodes, CR25 and CR26, which have very low stored charge characteristics. If these diodes were capable of storing excessive charge, there would be additional delay in switching. By using diodes with very low storage, the initial switching speed is greatly improved.

When the grounded emitter stage Q01 is turned on, collector current flows out of the circuit through the series diode CR27. In this state, Q01 can supply current to 8 AND loads. Transistor Q01 is clamped out of saturation by the silicon feedback diode CR26, and the output voltage settles at a nominal value of -1.1 volt. The voltage drop across diode CR27 insures a back bias being applied to the base-emitter junction of Q02, thereby keeping this stage turned off.

When Q01 turns off, the collector voltage starts to rise toward -20 volts. Since the voltage across the load cannot change as quickly as the collector voltage of Q01, the series output diode CR27 is back biased and the output emitter follower stage Q02 is turned on.

The turn-on current is applied to the base of Q02 at the rate at which Q01 turns off. The turn-on current is the current that is drawn through the first stage collector resistors R15 and R16. This current is available to turn on the output stage only as fast as it is turned off in the first stage.

Transistor Q02 in the on state proceeds to drive the output voltage negative. At about -5.8 volts, the output is fed back to the input of the first stage by diode CR25 to start the clamping action. Since this process has delay associated with it, the output signal overshoots the -5.8 volt mark and may carry as far as -8 volts. The circuit then settles the voltage back to the -5.8 volt level. In this state, transistor Q02 provides a low impedance path to the -20 volt supply.

GROUND RULES

(Effective November 21, 1963)

The following ground rules for usage of the basic 3600 inverter circuit are the result of tests performed by the Special Projects Department, Government Systems Division of Control Data Corporation. Inquiries concerning these ground rules should be addressed to the above department.

The ground rules are intended as guidelines in obtaining optimum circuit performance. They should not be considered as being excessively restrictive, because it is often found that a circuit will operate satisfactorily in a less than optimum configuration which may deviate considerably from one or more of the ground rules. Decisions as to when a ground rule may be violated must be based upon various electronic considerations, and are the responsibility of the designer.

Definition: Minimum Usage Inverter

The minimum usage inverter referred to in the following rules is defined to be an inverter driving one load and having one input. The inverter which drives the minimum usage inverter must drive no other loads. All wire lengths are kept as short as possible, voltages are adjusted to proper levels, and temperatures are allowed to stabilize.

LOADING

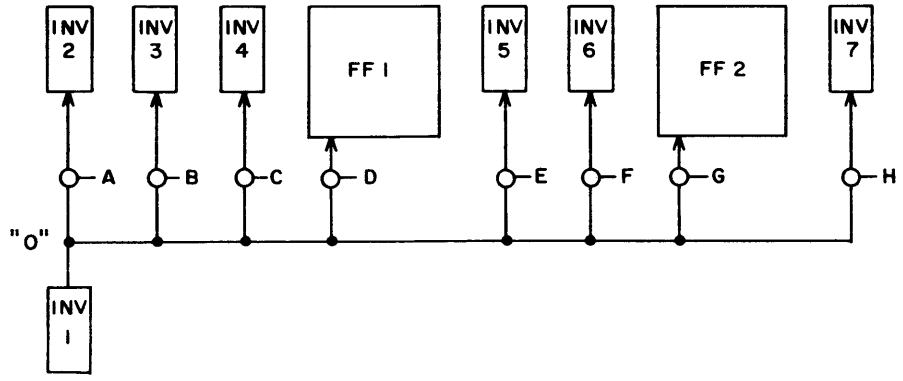
Any single input to a recipient inverter, regardless of whether it is a part of a 1, 2, 3, 4, 5, or 6 input AND or an OR input, is considered to be one load.

1) An inverter may simultaneously drive eight AND loads, eight OR loads, or any combination up to eight loads total.

2) A flip-flop or a control delay may drive only seven loads, because it is required to provide its own feedback which constitutes one load.

Exception to Rule

Inverter 1 is normally capable of maintaining a logical "0" on eight input AND gates. However, there is one exception when all the points, A through H, are driven to a "1" simultaneously. The current demand on inverter 1 is of such magnitude that the "0" condition is lost momentarily, allowing runt pulses to occasionally set a flip-flop or be amplified through an inverter. This condition can be avoided by limiting the inverter to a total of six loads as opposed to the usual eight loads.



UNUSED INPUTS

3) In case an entire AND input group is unused, at least one of the inputs must be grounded.

4) All unused OR inputs must be grounded, if using type C or CA cards.

5) All unused single-way AND inputs must be grounded.

NOISE SUPPRESSION

6) When a noise condition cannot be alleviated by the following suggestions or if an interconnecting lead is over 80 inches in length use logic level clamp card CA02.

   a) Maintain wire runs as short as possible.

   b) When possible, drive heavily loaded inverters from a lightly loaded source.

   c) When possible, use cards with 1, 2, 3, or 4 input AND gates as opposed to 5 and 6 input AND gates.

   d) Avoid using OR inputs unless the OR is a single-way AND.

7) All drive lines from H--- terms to N---, V---, and Y--- terms must be clamped, regardless of length, and must enter the recipient N---, V---, and Y--- terms through AND inputs.

8) N---, V---, and Y--- terms having a clock signal on an AND input must use one of the special card types numbered K72, CA73, K74, K92, K93, and HA06.

The clock input must be on the following pins:

Card Type	Inverter A	Inverter B
CA72	5 or 6	13 or 14
K72	2, 5, or 6	10, 13, or 14
CA73	2 or 3	10 or 11
CA74	5 or 6	13 or 14
K74	5 or 6	13 or 14
K92	2	
K93	2 or 3	
HA06	5 or 6	13 or 14

Exception to Rule

a) A clock input must come in on an AND; if the listed pins do not lend themselves to conditions, another AND input can be used.

b) The restriction of using only the above card types may be violated in applications where the logic circuits are heavily loaded.

PROPAGATION DELAYS AND TIMING ALLOWANCES

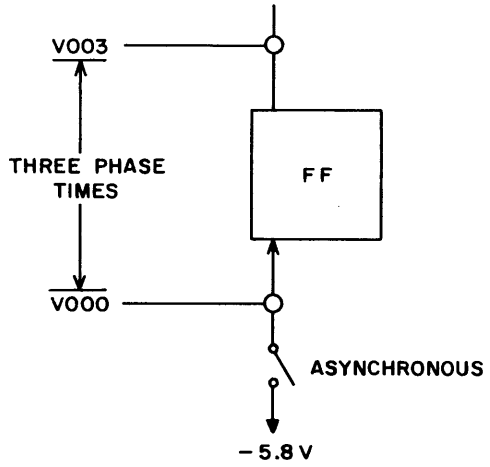
9)	Allow 17×10^{-9} seconds	To switch from "0" to "1" any minimum usage inverter using any type input.
10)	Allow 11×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverter using a 1, 2, 3, or 4-way AND input.
11)	Allow 8×10^{-9} seconds	To switch from "1" to "0" minimum usage inverters where equal numbers of AND and OR inputs are involved in a string of inverters.
12)	Allow 6×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverters using a 5 or 6-way AND input.
13)	Allow 5×10^{-9} seconds	To switch from "1" to "0" any minimum usage inverters using OR inputs.
14)	Allow 2×10^{-9} seconds per foot	For propagation time from point to point through all lengths of wire.
15)	Add 1×10^{-9} seconds	To each inverter switching time for each additional load beyond one.
16)	Add 2×10^{-9} seconds	To each inverter switching time for each foot of wire attached to the output.

17) The transition times from -1.1v "0" to -5.8v "1" and from -5.8v "1" to -1.1v "0" range from 20×10^{-9} to 50×10^{-9} seconds and 15×10^{-9} to 35×10^{-9} seconds, respectively. These times are highly influenced by loading effects.

18) If two inverters are cross coupled to perform as a flip-flop and the load on either side of the flip-flop is two loads or less, the cross-coupling must come into AND inputs.

19) The length of cross-coupling leads of inverters to be used as a flip-flop must not exceed six inches.

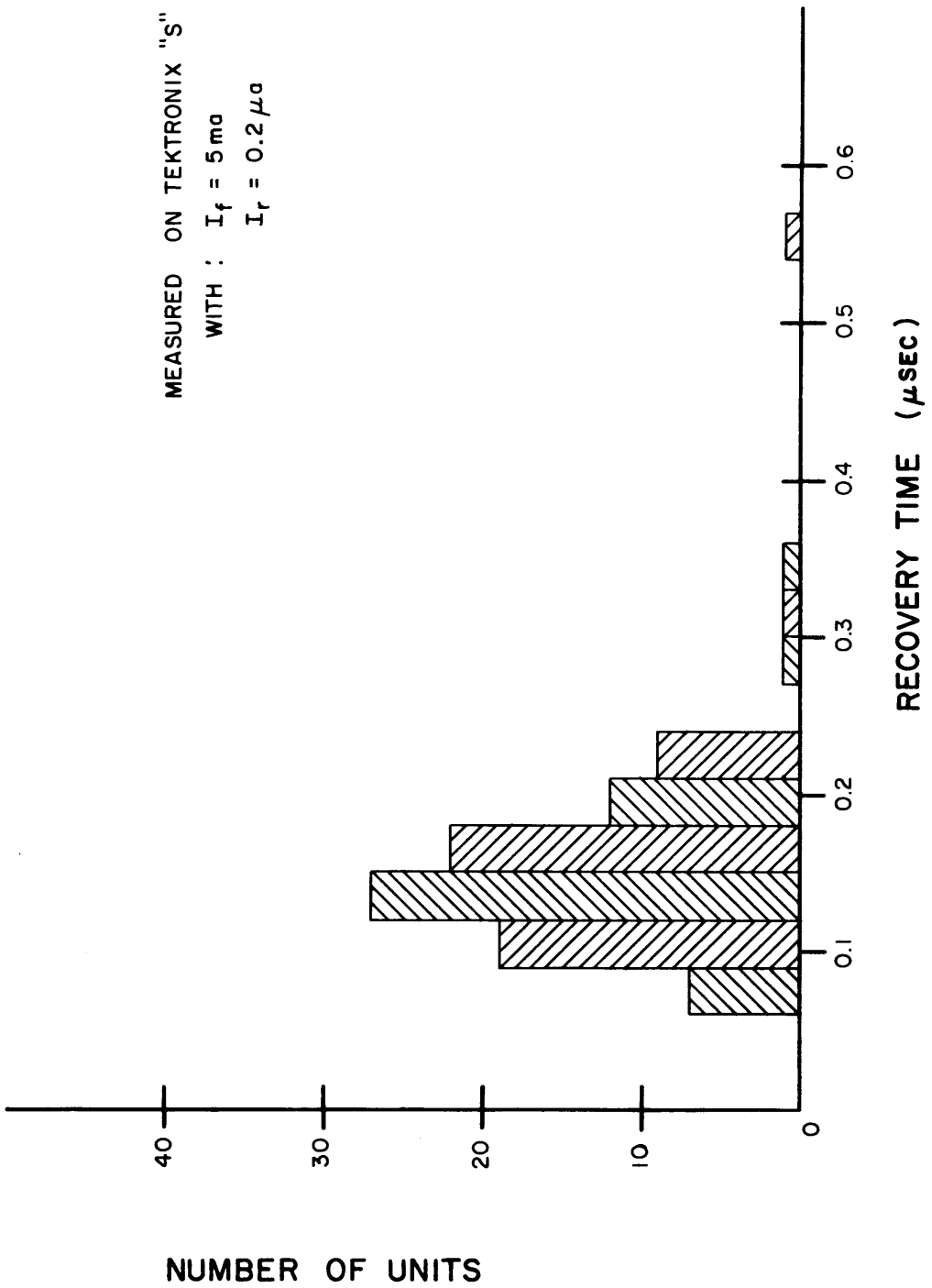
20) In applications where an asynchronous signal forms an AND gate with an N---, V---, or Y--- term, allow a minimum of three clock-phase times (187.5×10^{-9} sec) before probing the flip-flop output for reliable information.



TEST RESULTS

The following pages contain graphs showing the comparative recovery time of the logic diodes and the margins over which the +20v and -20v supplies may vary.

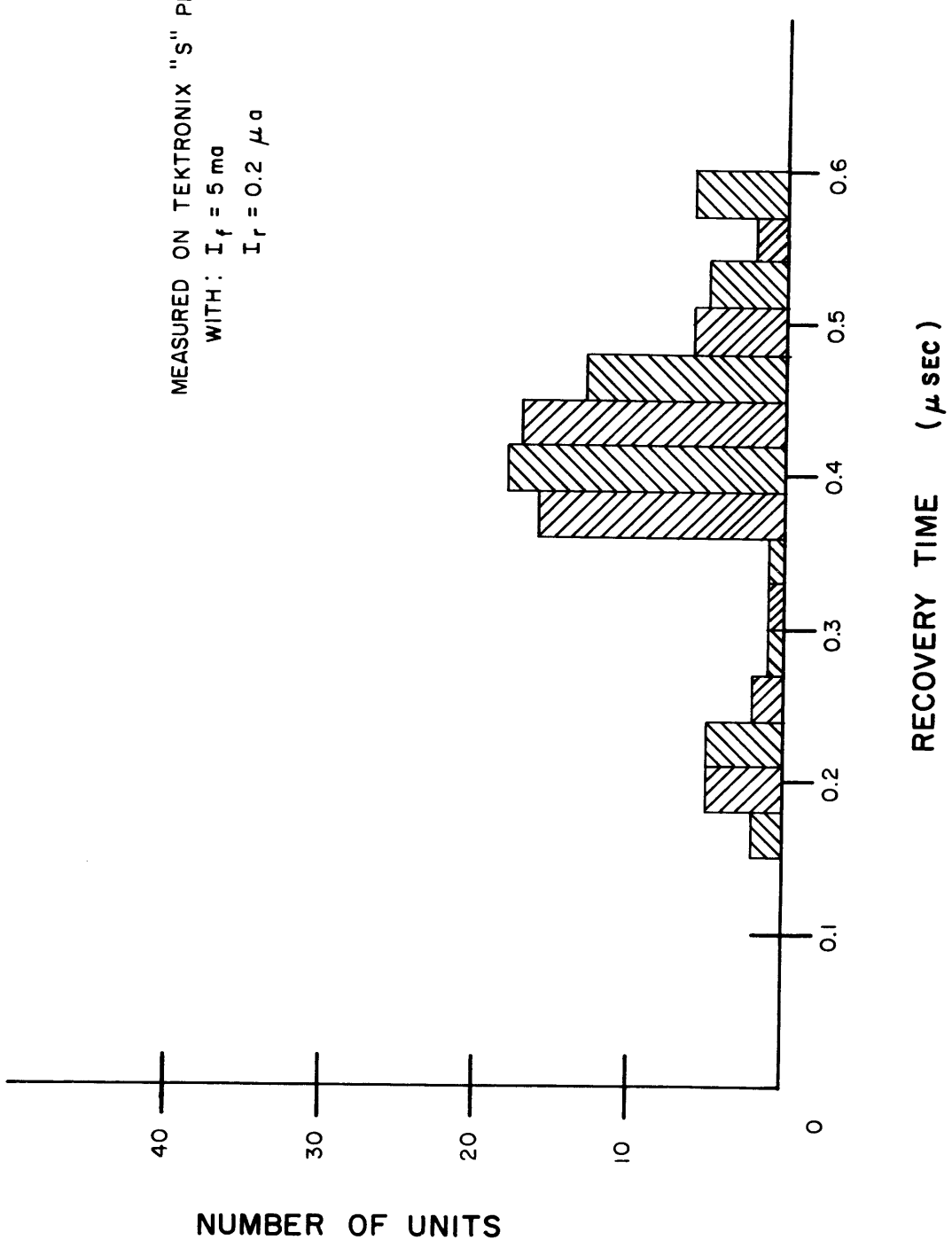
The voltage margin tests were made by varying the supply voltage of an entire chassis until failure occurred. The final version of the inverter circuit was tested in a chassis composed of 1170 cards which contained 2046 inverters.



Clevite CGD 899 Diodes
Distribution of Reverse Recovery Time

2-3600 Inv-10

REV. A

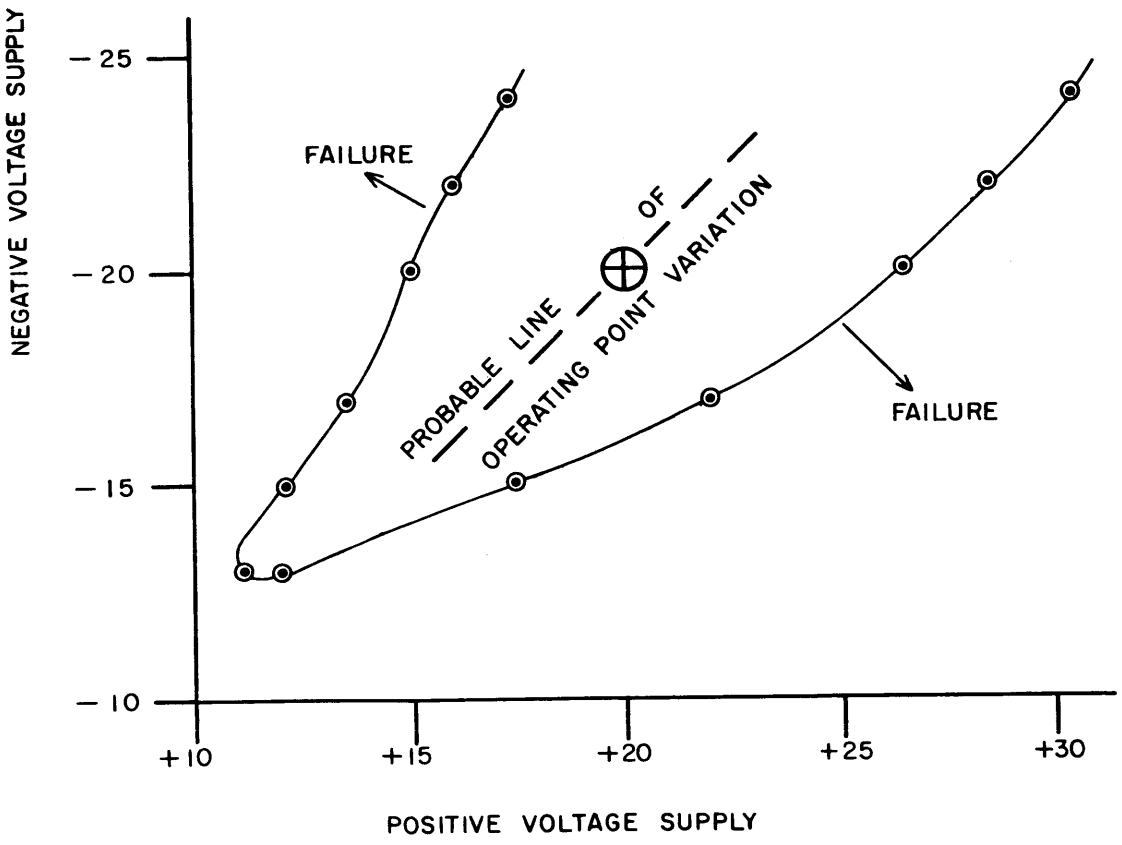


Hughes HD 2969 Diodes
Distribution of Reverse Recovery Time

2-3600 Inv-11

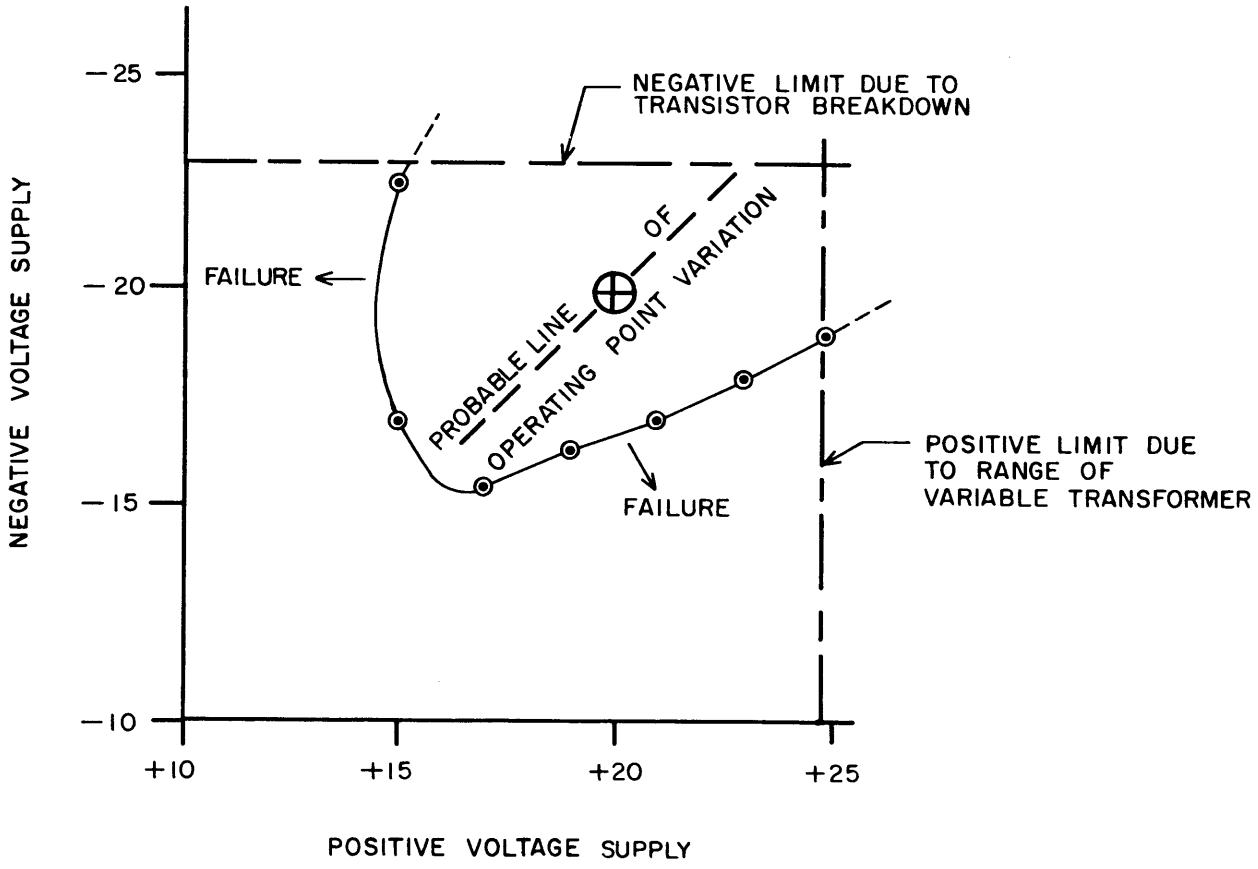
REV. A

8 mc "P" COUNTER CONTAINING 43 CARDS
LOGIC DIODES HD 1804



Voltage Margins

TEST CHASSIS CONTAINING 1170 CARDS (2046 INVERTERS)
FINAL VERSION OF CIRCUIT AS SHOWN IN 2-3600 INV-2



Voltage Margins

2-3600 Inv-13

REV. A

CHAPTER 3. STORAGE CARDS

Drive Generator	51, 51A
Diverter	52, 52A
Selector	53
Current Source	54, 74
Inhibit Generator	55, 55A, 58, 58A, 59, 59A
Sense Amplifier	56
Sense Amplifier	57
Even Plane Inhibit Driver	C00
Line Driver	C03
Odd Plane Inhibit Driver	C04
Gate	C05
Sense Amplifier	C06
Inhibit Compensator	C09
Drive Line Transformer	C10
I/O Sense Amplifier	C86
I/O Memory Driver	C87
I/O Memory Diverter	C88
I/O Emitter Follower	C90
Digit Driver	H14
Digit Compensator	H15
Sense Amplifier	H16
Sense Amplifier	H18
Memory Driver	P51
Memory Diverter	P52
Sense Amplifier	P56

DRIVE GENERATOR
Card Types 51 and 51A

The driver generator (page 3-51-2) develops the R/W current which is applied to the memory drive lines selected (designated H and V in the 1604 computer). Two identical channels feed opposite ends of the primary winding of transformer T01. Each channel consists of transistor Q01, connected as an emitter-follower, and transistors Q02 and Q03, connected in parallel as amplifiers. The input signal is an AND combination of two selector (card type 53) outputs. A -1v input results in approximately 0v at the base of Q01. The emitter of Q01 is clamped to ground by CR03, so neither Q02 nor Q03 conducts. Consequently, no current flows in the primary of T01.

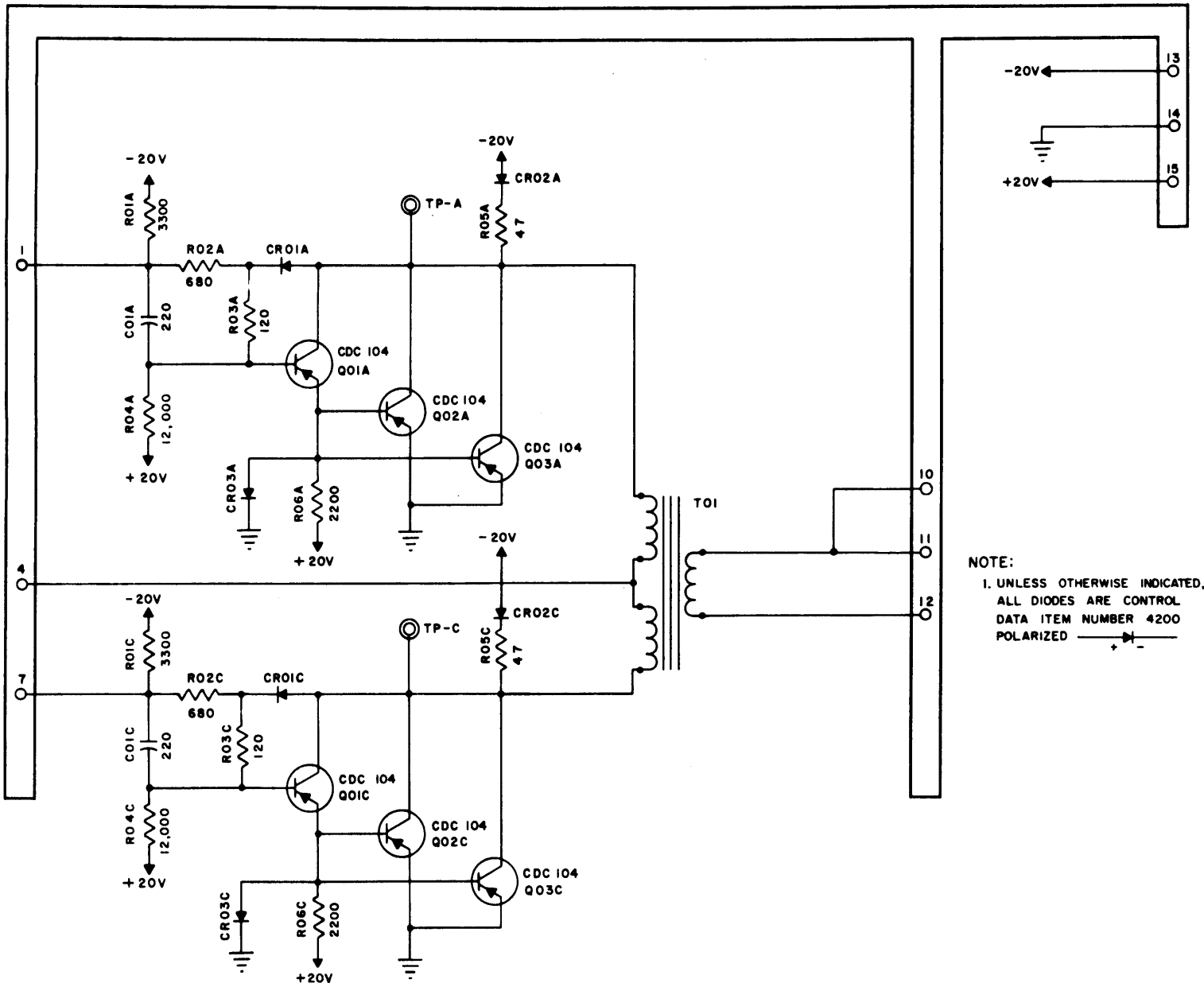
Note: Transistor Q03 is not used on card type 51A.

A -12v input signal causes Q01 to conduct; however, the conduction is held below saturation by feedback diode CR01. The negative voltage developed across R06 is applied to the bases of Q02 and Q03, causing these transistors to conduct. Current flows from the current sources through the emitters of Q02 and Q03 to the collectors, through the primary of T01, to the current sources. The current pulse from the secondary of T01, amplified by the step-down action of T01, is applied to the drive line of the memory plane assembly. It then flows through the selected diverter and back to the secondary of T01.

The polarity of the output current from T01 is determined by the direction of the current flow in the primary. The direction of current flow, in turn, is determined by the selected channel. For example, if channel A receives a -12v input, a read pulse is generated; a channel B input generates a write pulse. Acceptable switching times are as follows:

Negative to positive $\leq$ 0.15usec

Positive to negative $\leq$ 0.2 usec


-20V
13
14
15
+20V
-20V
CR02A
TP-A
R05A
47
R01A
3300
R02A
680
CR01A
C01A
220
R03A
120
CDC 104
Q01A
CDC 104
Q02A
CDC 104
Q03A
R04A
12,000
+20V
CR03A
R06A
2200
+20V
T01
10
11
12
-20V
CR02C
TP-C
R05C
47
R01C
3300
R02C
680
CR01C
C01C
220
R03C
120
CDC 104
Q01C
CDC 104
Q02C
CDC 104
Q03C
R04C
12,000
+20V
CR03C
R06C
2200
+20V
NOTE:
1. UNLESS OTHERWISE INDICATED, ALL DIODES ARE CONTROL DATA ITEM NUMBER 4200 POLARIZED

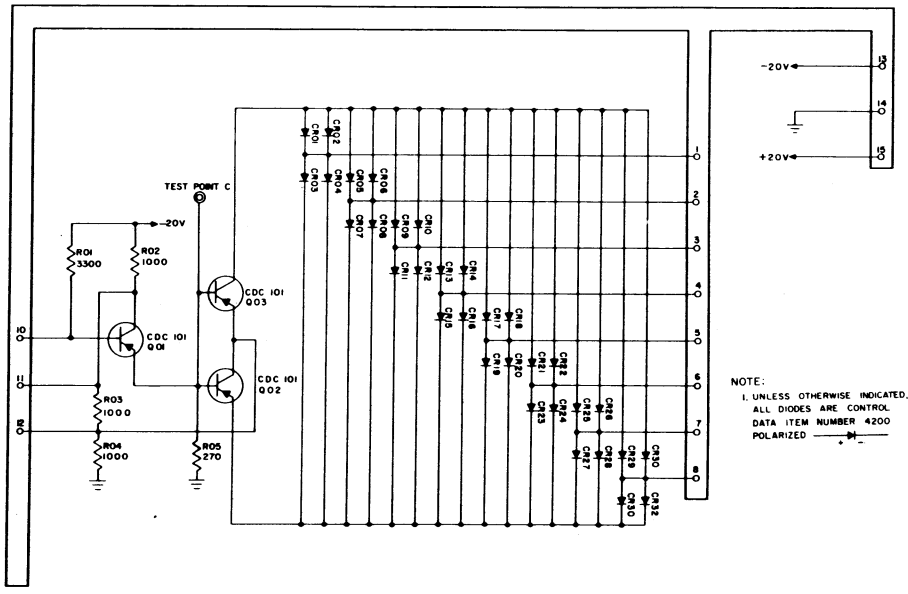
DIVERTER

Card Types 52 and 52A

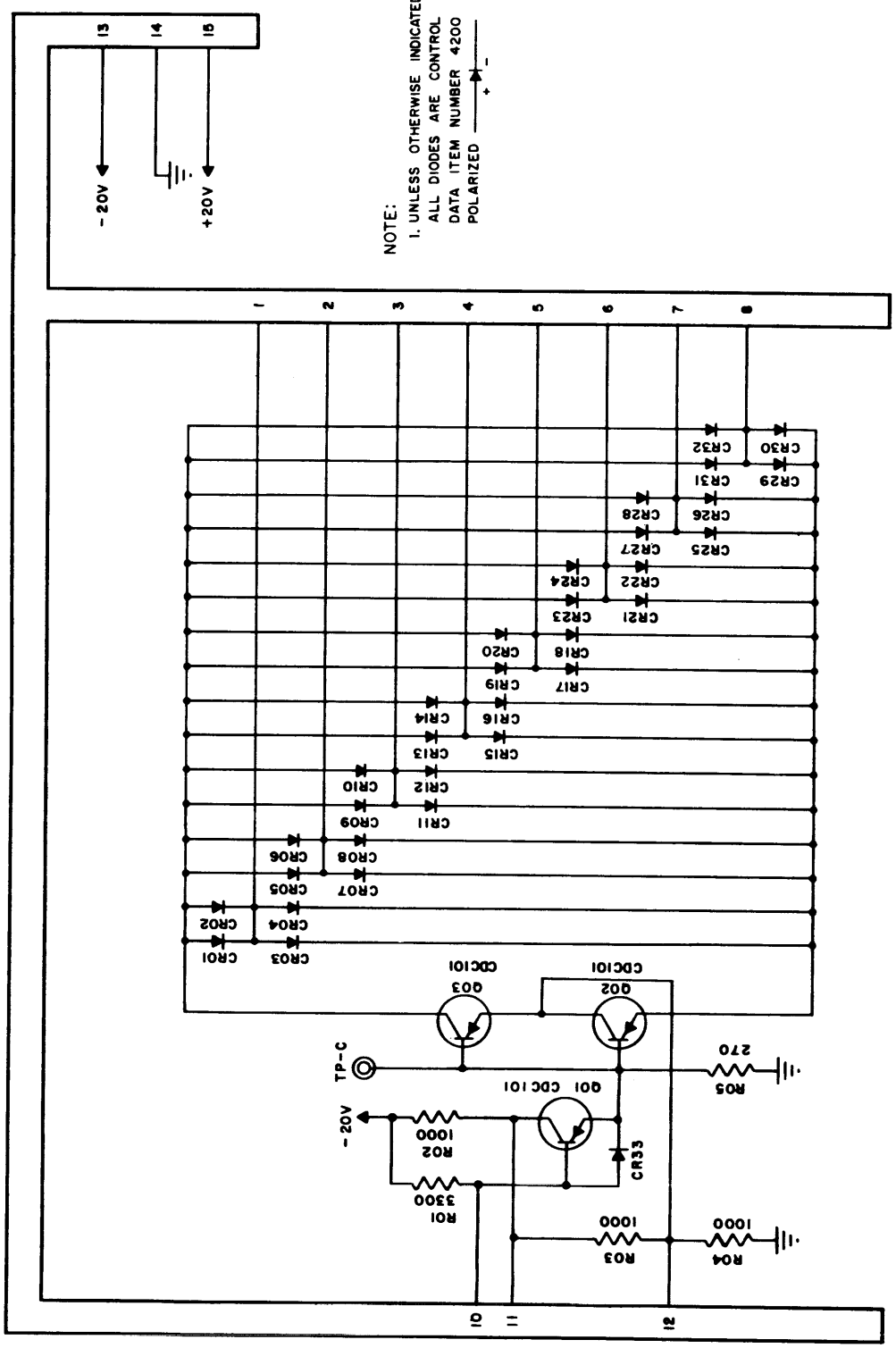
DIVERTER (Type 52)

The diverter circuit serves as an electronic switch in series with a drive line of the memory plane assembly. Transistor Q01 is connected as an emitter follower, and transistors Q02 and Q03 as switches. A -3v input causes Q01 to conduct; the negative signal from Q01 enables Q02 and Q03. One or the other transistor passes the current pulse on the drive line to which the diverter is connected.

A positive pulse passes one of the pairs of diodes CR03/CR04, CR07/CR08, CR11/CR12, etc., depending upon the driver selection, and passes Q02. A negative pulse passes one of the pairs of diodes CR01/CR02, CR05/CR06, etc., and passes Q03. In either case, the current pulse is returned to the R/W driver. The bleeder networks of all diverters are connected in parallel via terminals 11 and 12 to equalize the current flow through the bleeders and reduce heating.



Diverter 52

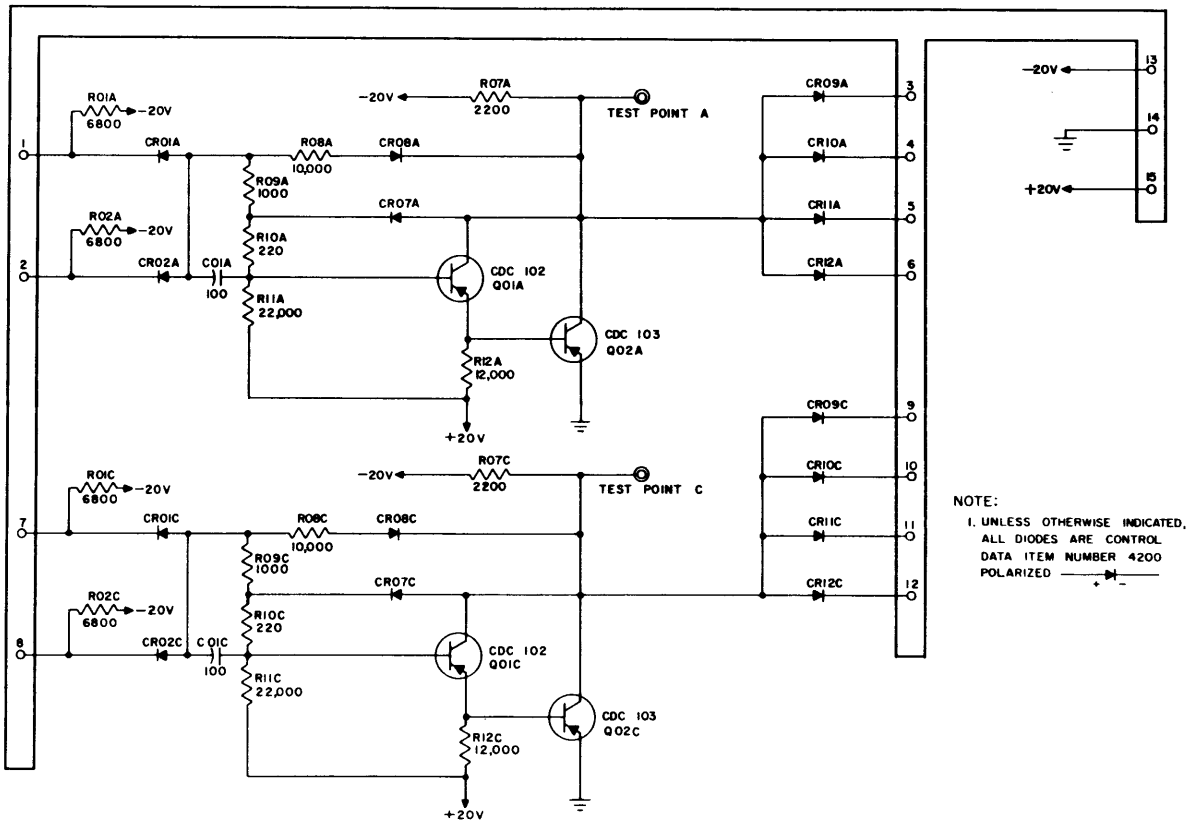


Diverter 52A

SELECTOR

Card Type 53

Each selector card consists of two identical circuits designed to feed a drive generator circuit. A selector circuit is similar to the 1604 type inverter except that the resistance results in output signal levels of -1v and -12v. Each selector circuit has two input diodes CR01/CR02 and four output diodes CR09/CR10/CR11/CR12.



Selector 53

CURRENT SOURCE

Card Types 54 and 74

A current source card consists of banks of parallel resistors, each of which connects an output pin and the -20v supply. The function of this card is to provide the resistances needed to hold memory drive and inhibit currents to the desired amplitude.

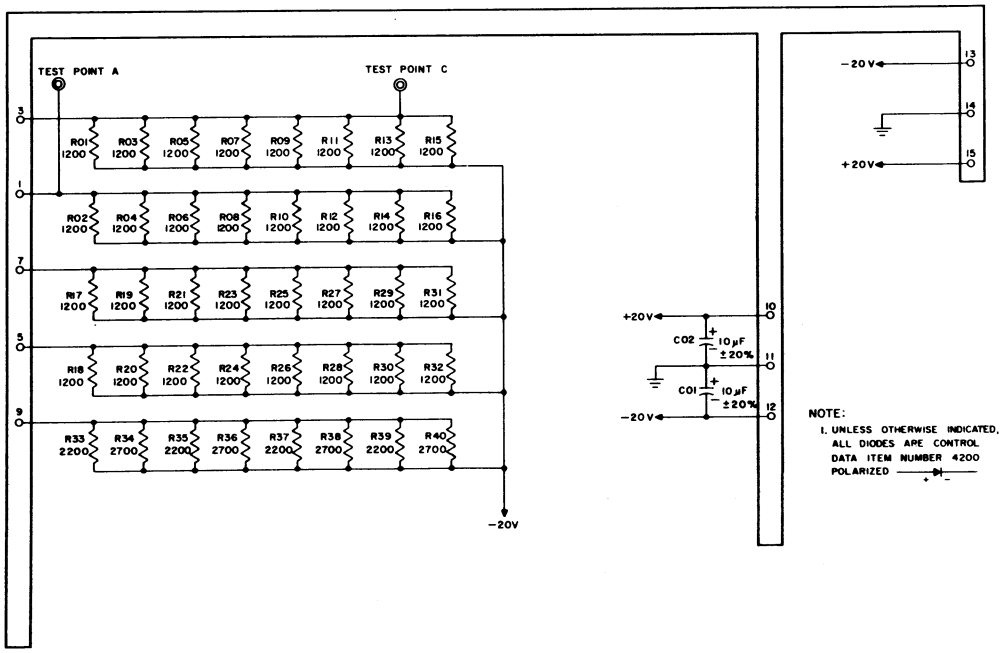
The available resistances are as follows:

Card Type 54

pins 1, 3, 5, 7	150 ohms
pin 9	303 ohms

Card Type 74

pins 1, 3, 5, 7	257 ohms
pin 9	**303 ohms**



Current Source 54

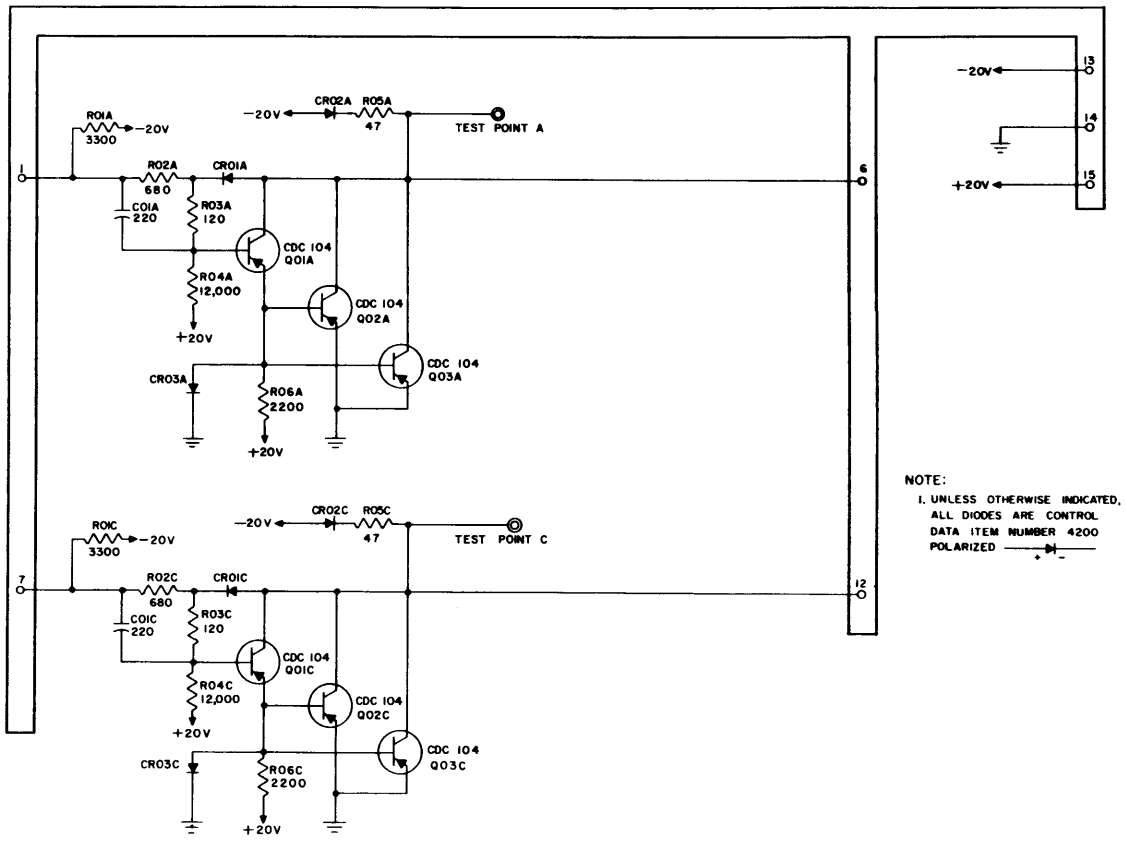
INHIBIT GENERATOR

Card Types 55, 55A, 58, 58A, 59, 59A

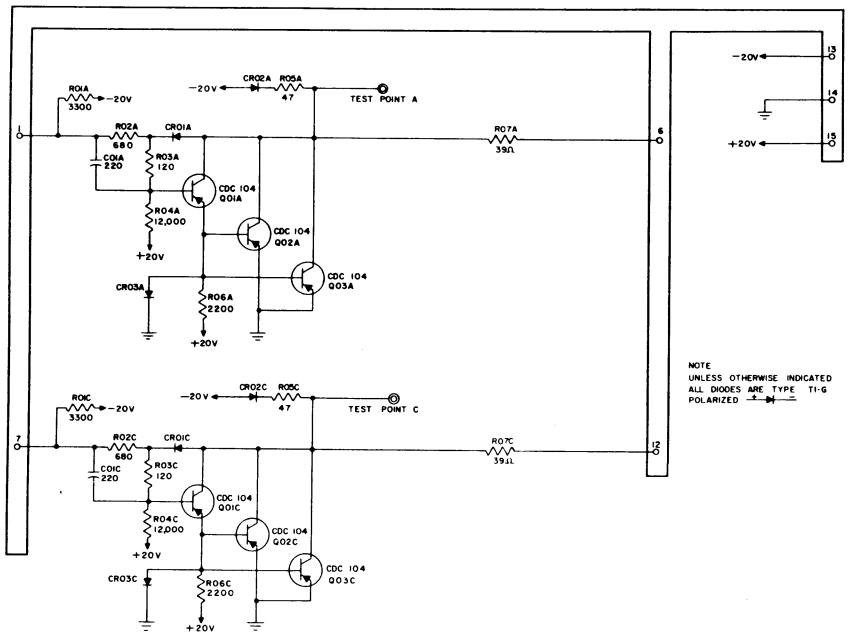
Note: Transistor Q03 is not used on card types 55A, 58A, and 59A.

Each inhibit generator card has two generator circuits which are similar to the type 51 drive generator channels except for the absence of an output transformer. The output of each channel is independently connected to a terminal of the card.

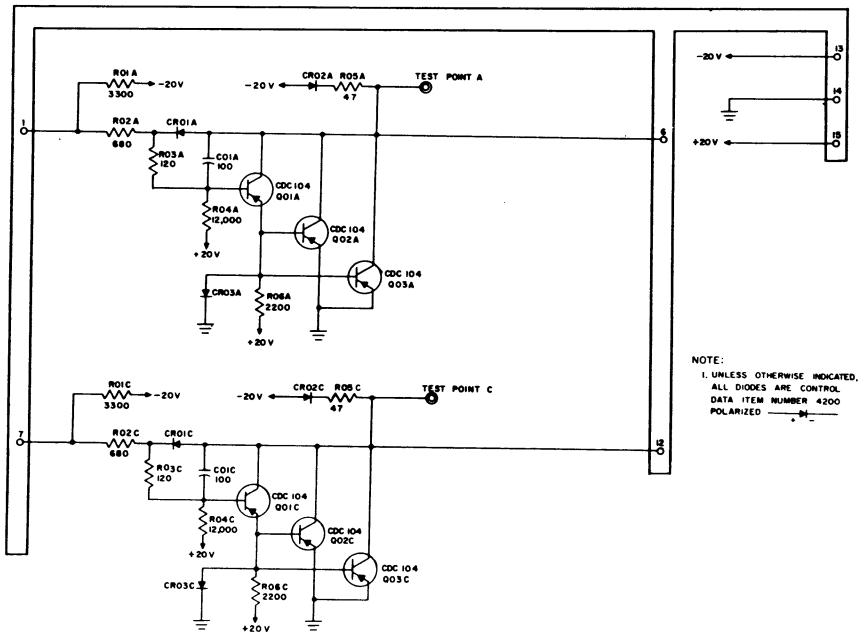
A -12v input signal to either generator of a type 58 card causes Q01 to conduct and thus enable Q02 and Q03. Current from the external source connects to the generator via terminal 6 or 12 and passes through Q02 and Q03 to ground.



Inhibit Generator 55



Inhibit Generator 58



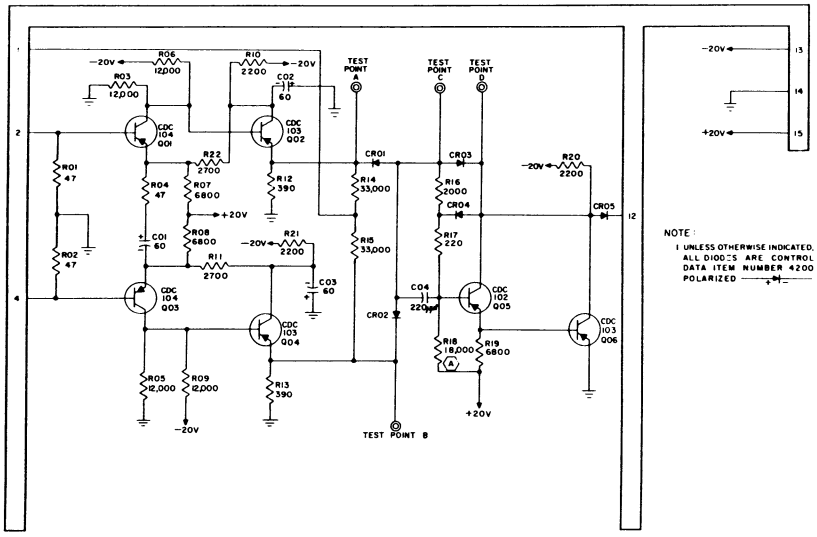
Inhibit Generator 59

SENSE AMPLIFIER

Type 56

The 56 card amplifies the signals from a memory plane as the result of a read pulse, and produces a "0" output when a core switches. Transistors Q01 to Q04 are connected in a differential amplifier circuit. The signals from either end of the sense windings are applied to Q01 and Q03. The emitters are held at the difference voltage by a difference network composed of R04 and C01; noise voltages on the sense line are cancelled.

Capacitors C02 and C03, in the collector circuits of Q02 and Q04, provide d-c stabilization. Diodes CR01 and CR02 pass the negative-going components of the signals from Q02 and Q04, and serve as clippers. The bias across these diodes, and thus the clipping level, is adjustable by the Margin Switch on the operator's console. When the switch is up, +20v is applied to the junction of R14 and R15 raising the reference voltage across the input diodes to the last stage. When the switch is down, -20v is applied to R14 and R15 making the circuit more sensitive to the signal from the sense line which tends to make spurious pulses look like "1's". Transistors Q05 and Q06 are connected in an amplifier-inverter circuit. The output, a signal from CR05, as a result of a "1" signal from the sense wire, is -0.5v.



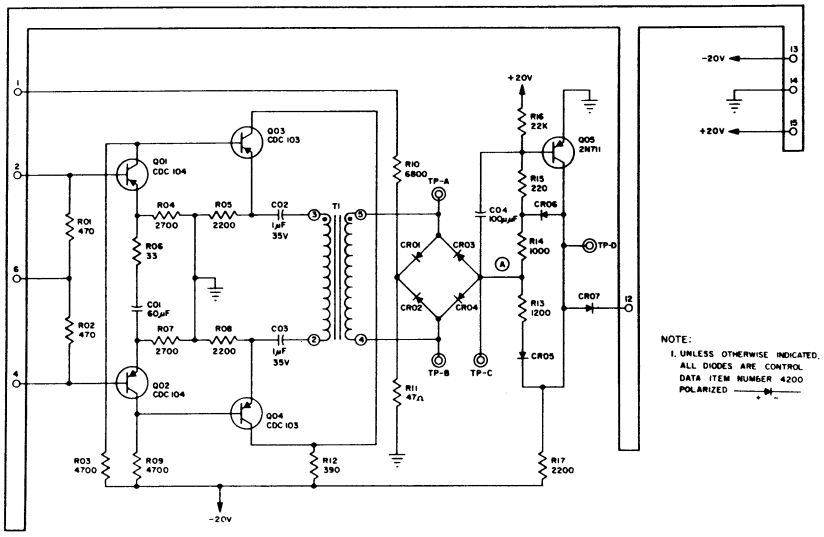
Sense Amplifier 56

SENSE AMPLIFIER

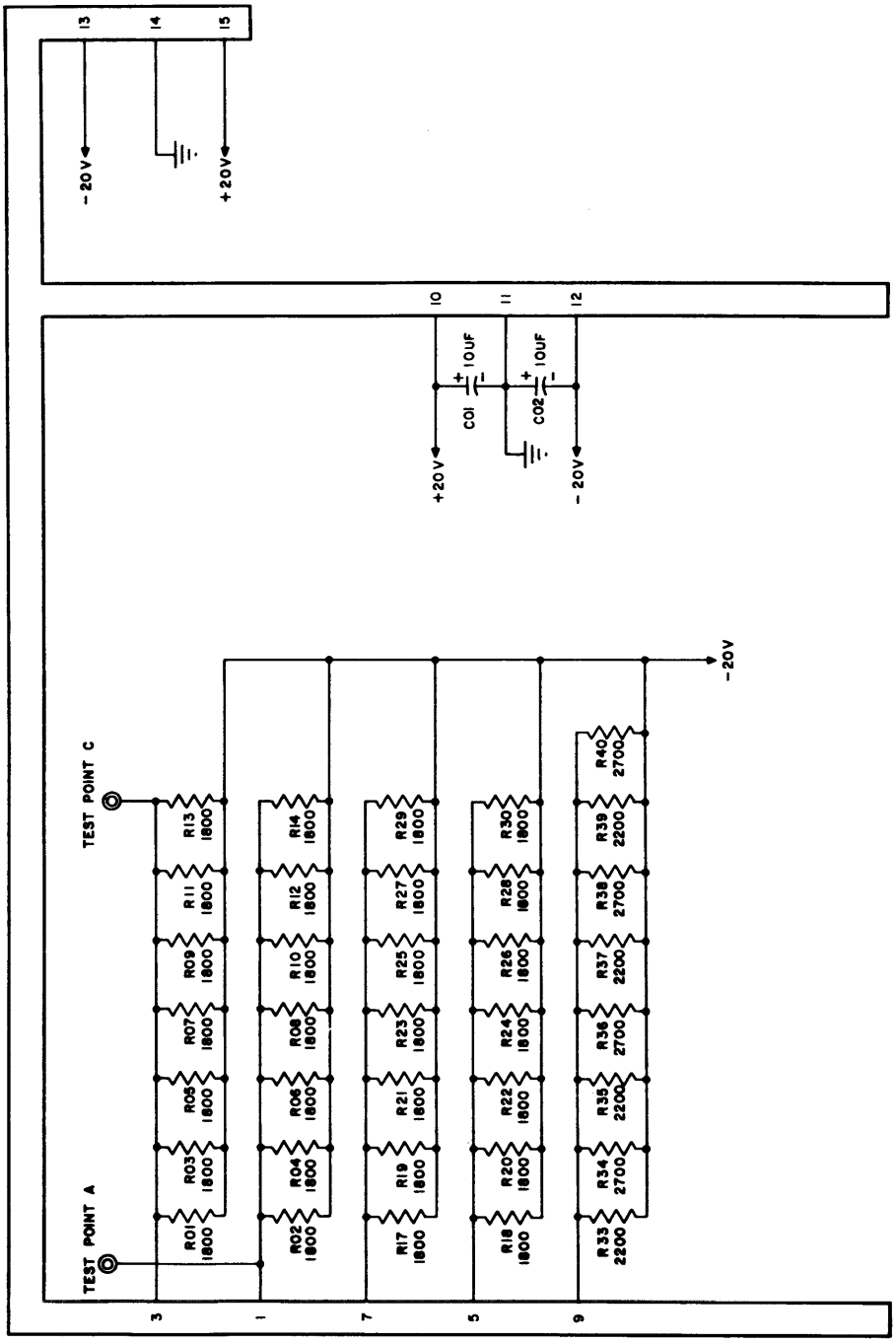
Type 57

The sense amplifier below amplifies the signal from a memory plane (pins 2 and 4) as the result of a read pulse, and produces a "0" output when a core switches. Transistors Q01, Q02, Q03, and Q04 form a differential amplifier which feeds T1 through coupling capacitors C02 and C03. The secondary of T1 is connected to a bridge detector so that the signal polarity at (A) is always the same. The Q05 network is a standard inverter circuit providing normal output logic levels of -3.0v and -0.5v.

Gain from the differential amplifier for the common mode component of the input signal is about 2; for the differential mode component, across R06 - C01, gain is about 100. Detector bias is determined by the Margin switch on the console. With the switch at HI, the +20v applied to pin 1 raises the reference level of the detector making it less sensitive; weak signals tend to be dropped. With the switch at LO, -20v appears at pin 1 and the detector is more sensitive to spurious pulses. No connection to pin 1 is made when the switch is in the normal, center position. Pin 6 is connected to the diverter bus (-7.0v) to provide bias for input transistors Q01, Q02. The output from Q05, as the result of a "1" signal on the sense lines, is -0.5v.



Sense Amplifier 57



Tape Current Source 74

EVEN PLANE
INHIBIT DRIVER
Card Type C00

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from the +40v source at pin 6 to the inhibit winding at pin 1 or pin 15. This occurs whenever all inputs to the respective circuit are at the logical "1" level of -5.8v. The inhibit circuit contains a series 120-ohm resistor so that the resulting current is approximately 340 ma.

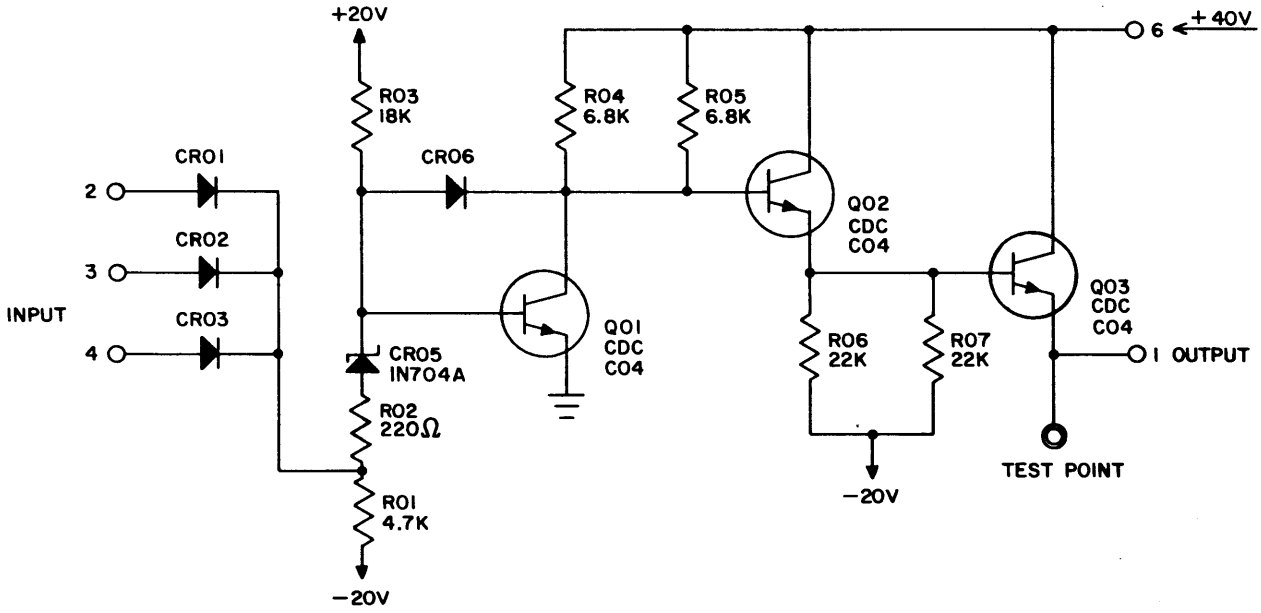
OPERATION

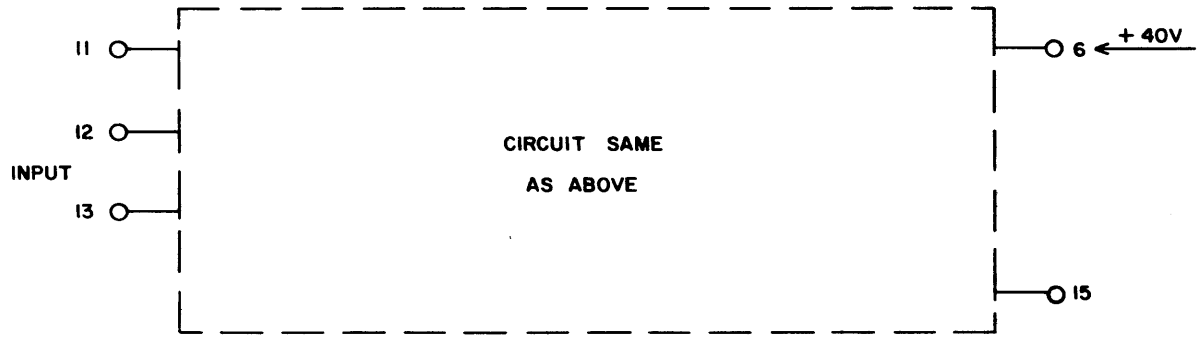
Each circuit has a three-way logical AND input, meaning that all inputs must be at the -5.8v "1" level in order for an input to be sensed. A -1.1v "0" signal on any input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

A level-shifting action is provided to the base of Q01 by resistors R01, R02, R03, and the 4.1v zener diode CR05. The zener diode CR05 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When a -1.1v "0" signal appears at an input, the zener diode CR05 places a forward bias on the base of Q01. Transistor Q01 then switches to a state of heavy conduction. It is held out of saturation by the feedback diode CR06 and its collector voltage is approximately +0.4v. The low collector voltage of Q01 is also the base voltage of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is equal to its +0.4v base voltage minus its base-emitter junction drop, and is approximately -0.3v. This provides sufficient forward bias so that a minimum conduction is maintained through Q02. Transistor Q03 is connected as an emitter follower with the inhibit winding load in series with the emitter. The emitter of Q03 is connected to ground through the inhibit line. The base-emitter junction is therefore reverse biased by the -0.3v input, so that Q03 is cut off. This disables the current path from the +40v supply to the inhibit winding.

With the AND input satisfied by -5.8v "1" signals, the base of Q01 is biased at approximately -1.5v and Q01 is cut off. The collector voltage of Q01 rises to approximately +38.5v (40v minus the IR drop across R03 and R04). This provides drive to the





NOTES:

1. EACH CIRCUIT HAS THREE "AND" INPUTS.
2. TRANSISTORS Q02 & Q03 CONDUCT WHEN ALL INPUTS ARE -5.8V "1".
3. ALL DIODES ARE HD2969 UNLESS OTHERWISE INDICATED.

EVEN PLANE

Inhibit Driver C00

base-emitter junction of Q02. Transistor Q02 is connected as an emitter follower; thus its emitter voltage becomes approximately +38v. This provides a strong forward bias to the base of Q03, causing Q03 to conduct heavily. The voltage applied to the inhibit line is the emitter voltage of Q03 and is approximately +37.5v. The 340 ma inhibit current is also the emitter current of Q03, and is allowed to flow when Q03 switches to the conduction state.

LINE DRIVER

Card Type C03

FUNCTION

The function of the circuits on this card is to enable 450 ma of positive current to flow from the output pins 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. Pins 1 and 15 connect to the two ends of the primary windings of eight memory driver transformers. During the memory cycle, one transformer will be center-tapped to +20v; thus current flow in either direction may be obtained by selecting one of the circuits on the C03 card.

The output pins 1 and 15 are connected as shown on page 3-C03-2 by capacitor C03 and resistor R06, which form a series differentiating network. This connection transmits only those signals having a high rate of change, such as a sharp noise spike, and blocks entirely a steady d-c voltage. Thus, a noise spike appearing at pin 1 also appears at pin 15, and their total effect is to cancel each other. However, the d-c levels of pins 1 and 15 are completely separated if either circuit switches to the conduction state while the other remains cut off.

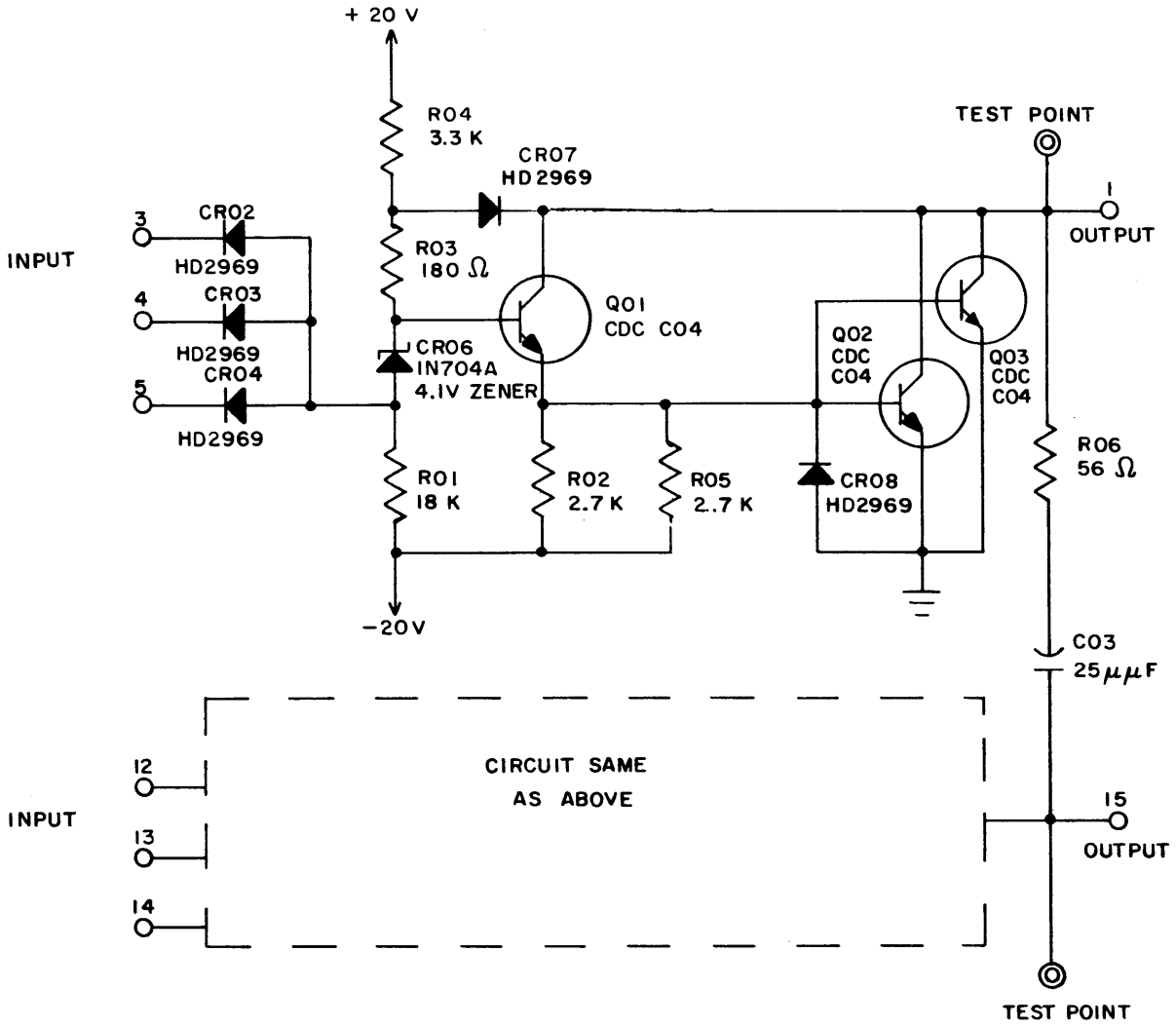
OPERATION

The two circuits on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit; however, the component numbers mentioned are those appearing in circuit A.

A level shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and it is cut off. The bases of Q02 and Q03 are held at approximately -0.3v by the forward drop of diode CR08, and they are likewise cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing



NOTES:

1. EACH CIRCUIT HAS 3 "OR" INPUTS.
2. TRANSISTORS SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

Line Driver C03

through the transformer primary into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a positive voltage. This forward bias is sufficient so that Q01 conducts heavily, but it is held out of deep saturation by diode CR07 and resistor R03. Transistor Q01 in its conduction state allows the +20v source, which connects to pin 1 through the transformer primary, to bias the bases of Q02 and Q03 at a positive potential. Thus they also conduct heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of approximately 1v across Q02 and Q03.

Transistors Q02 and Q03 are grounded emitter stages driven by the emitter follower stage Q01. Their base drive is taken directly from the emitter of Q01; thus the input to Q02 and Q03 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the bases of Q02 and Q03 well into the positive voltage domain, so that they also switch on and conduct heavily. Likewise, when Q01 switches off, Q02 and Q03 also switch off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junctions of Q02 and Q03 so that they are well into the cut off region.

ODD PLANE
INHIBIT DRIVER
Card Type C04

FUNCTION

The function of the circuits on this card is to allow a 340 ma inhibit current to flow from pin 1 or 15 to ground, whenever all inputs to the respective circuit are at the logical "0" level of -1.1v. The inhibit wires are energized by a source of +40v, and each inhibit circuit contains a series 120-ohm resistor so the resulting current is approximately 340 ma. The odd plane inhibit wires terminate at either pin 1 or pin 15 of a C04 card, and the path is completed to ground allowing current to flow, if the respective inhibit generator circuit switches to its conduction state.

OPERATION

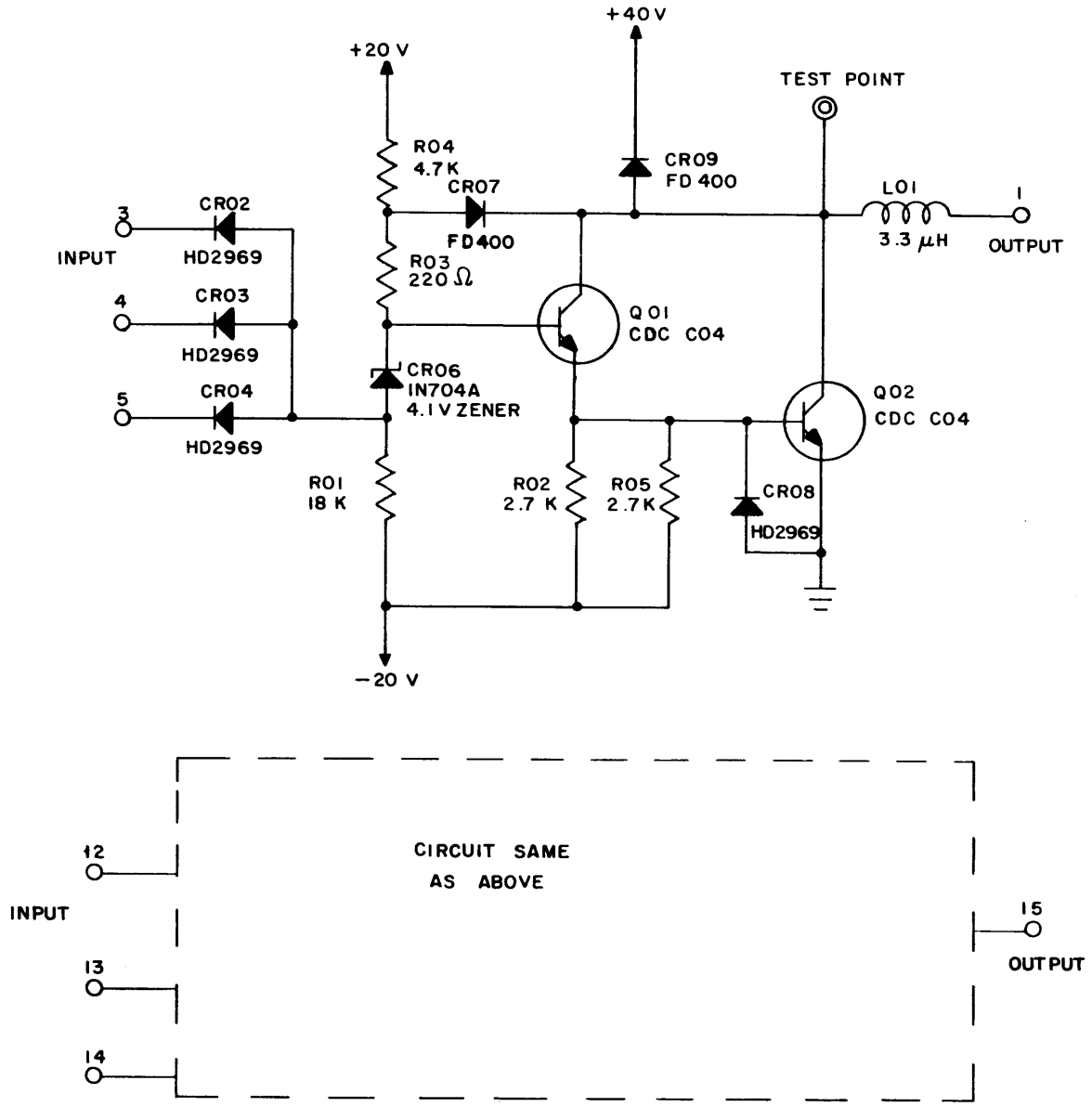
The two circuits contained on the card are identical and are labeled A and B. The following discussion of operation applies to either circuit but the component numbers mentioned are those appearing in circuit A.

A level-shifting action is provided to the base and emitter of Q01 by resistors R01, R03, R04, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

Each circuit has three logical OR inputs, meaning that a -5.8v "1" signal on any input is sensed, although a -1.1v "0" signal may be present simultaneously at another input. Any unused input acts as a steady "0", regardless whether it is grounded or left open.

When a -5.8v "1" signal appears at an input, the base of Q01 is biased at about -1v and Q01 is cut off. The base of Q02 is held at approximately -0.3v by the forward drop of diode CR08, and Q02 is also cut off. Thus, except for negligible leakage effects, pin 1 is completely isolated from ground and rises to a high positive voltage. Diode CR07 therefore provides a blocking action, preventing current from flowing through the inhibit wire into pin 1.

If all of the circuit inputs are at the -1.1v "0" level, zener diode CR06 holds the base of Q01 at a sufficiently positive voltage so Q01 conducts heavily. In this state, diode



NOTES:

1. EACH CIRCUIT HAS THREE "OR" INPUTS.
2. A CIRCUIT WILL SWITCH TO ITS CONDUCTION STATE WHEN ALL INPUTS ARE −1.1 V "0".

ODD PLANE

Inhibit Driver C04

CR07 holds Q01 out of saturation. Transistor Q01 in its conduction state allows the +40v source, which connects through the inhibit wire to pin 1, to bias the base of Q02 at a positive level. Thus transistor Q02 also conducts heavily, and positive current is allowed to flow from pin 1 to ground with only a drop of 1v across Q02.

Transistor Q02 is a grounded emitter stage driven by the emitter follower stage Q01. The base drive for Q02 is taken directly from the emitter of Q01; thus the input to Q02 follows the input to Q01 and is increased by the gain of Q01. When Q01 switches on, it attempts to bias the base of Q02 well into the positive voltage domain, so Q02 also switches on and conducts heavily. Likewise, when Q01 switches off, Q02 also switches off, and the voltage drop across diode CR08 applies a reverse bias of approximately 0.3v to the base-emitter junction of Q02 so it is well into the cut off region.

The connection of diode CR07 and the +40v source provides a clamp for the collector voltage of the transistors. When the transistors switch to the non-conducting state, the inductance of the inhibit wire tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode.

The 3.3 uh inductor in series with the output pin is for reducing ringing on the inhibit wire. The inductor increases the current rise time and hence reduces the overshoot.

GATE
Card Type C05

FUNCTION

The function of the Gate circuit is to enable a current path from a +20v source through which current of the order of 900 ma flows to the primary windings of two memory driver transformers. Pin 4 connects to +20v and pins 1, 2, and 3 provide the output. The path from pin 4 to the output is enabled only when all inputs to the Gate circuit are at the logical "0" level of -1.1v.

The function of the Discharger circuit is to ground the primary windings of the two memory driver transformers previously energized. This removes stored charge from the windings and neutralizes the transformers. The Discharger circuit is enabled by a -1.1v "0" input.

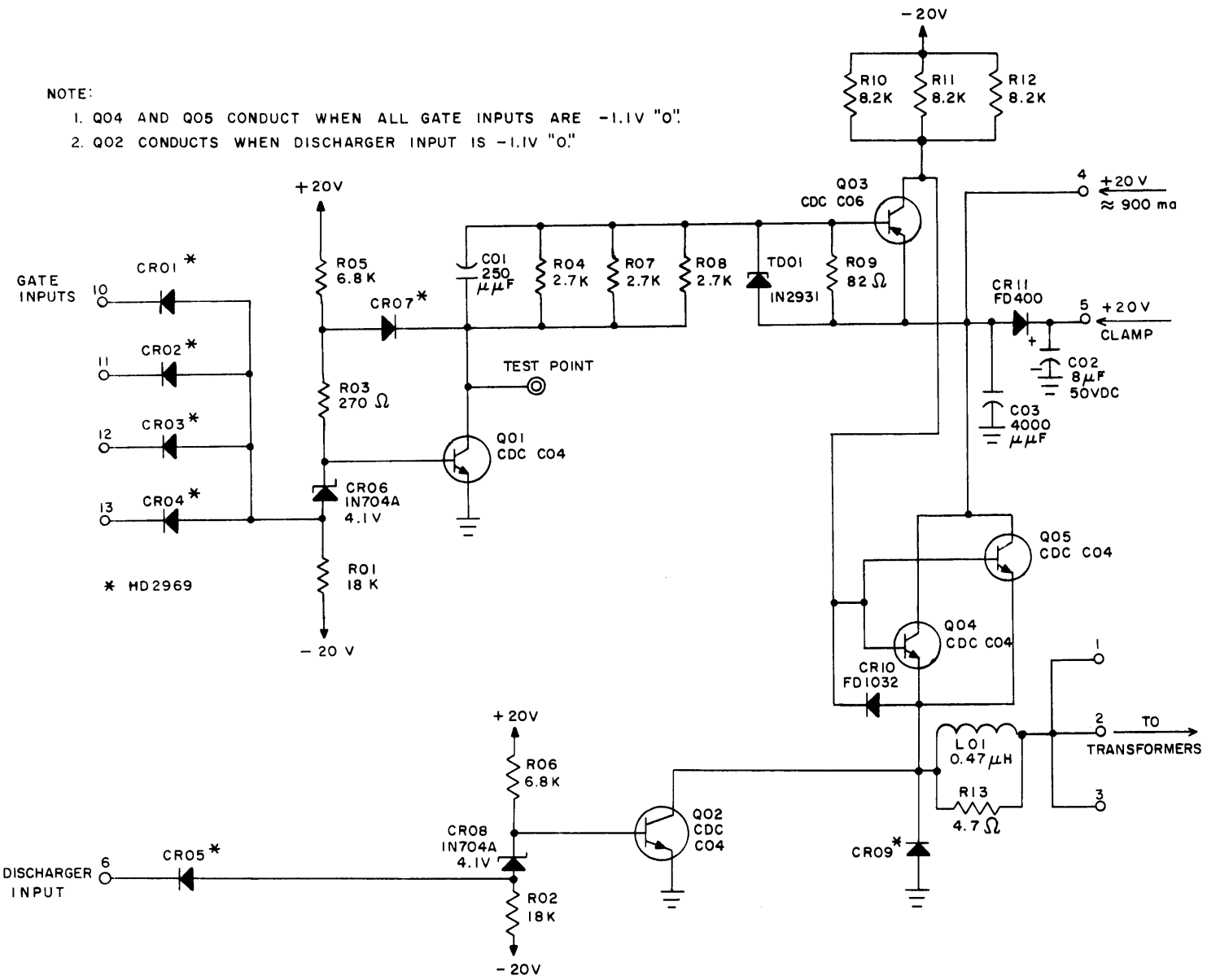
OPERATION

Pins 10 through 13 provide four logical OR inputs to the Gate circuit, and pin 6 provides an OR input to the Discharger. An unused input is interpreted as a steady "0", regardless whether it is grounded or left open.

A level-shifting action for the Gate inputs is performed by resistors R01, R03, R05, and the 4.1v zener diode CR06. The zener diode CR06 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations. Resistors R02, R06, and zener diode CR08 perform the level-shifting action for the Discharger.

With open circuits or logical "0" signals on all Gate inputs, the base of Q01 is at an approximate potential of +0.7v. It is prevented from going more positive by the low forward base-emitter impedance of Q01. During this time, Q01 is in the conduction state. However, if any input receives a -5.8v "1", the zener diode CR06 holds the base of Q01 at approximately -1.7v and Q01 is cut off.

During the time that Q01 is cut off by a "1" signal, its collector potential is raised to a high positive value by the +20v source attached to pin 4. Since no appreciable current now flows through the 82-ohm resistor and tunnel diode between base and emitter of Q03, it is also essentially cut off.


NOTE:
1. Q04 AND Q05 CONDUCT WHEN ALL GATE INPUTS ARE -1.1V "0".
2. Q02 CONDUCTS WHEN DISCHARGER INPUT IS -1.1V "0."
-20V
R10 8.2K
R11 8.2K
R12 8.2K
+20V
Q03 CDC C06
4 +20V ≈ 900 ma
GATE INPUTS
10
11
12
13
CR01 *
CR02 *
CR03 *
CR04 *
R05 6.8K
CR07 *
C01 250 μμF
R04 2.7K
R07 2.7K
R08 2.7K
TD01 IN2931
R09 82 Ω
CR11 FD400
5 +20V CLAMP
C02 8μF 50VDC
C03 4000 μμF
TEST POINT
R03 270 Ω
Q01 CDC C04
CR06 IN704A 4.1V
R01 18 K
* MD2969
- 20 V
Q05 CDC C04
Q04 CDC C04
CR10 FD1032
1
2 TO TRANSFORMERS
3
L01 0.47μH
R13 4.7 Ω
CR09 *
+20V
R06 6.8K
CR08 IN704A 4.1V
Q02 CDC C04
DISCHARGER INPUT
6
CR05 *
R02 18K
-20V

When Q01 switches to its conducting state, current is allowed to flow from the +20v source at pin 4 through the tunnel diode and 82-ohm resistor between emitter and base of Q03, through the three parallel 2.7k resistors, and through Q01 to ground. A threshold level is provided by the tunnel diode, since in its low-voltage state, it does not allow Q03 to conduct. However, when current through the tunnel diode increases to 10 ma, it switches to its high-voltage state. This places approximately 0.8v forward potential on the base of Q03 causing it to switch to its conduction state. This enables the series circuit from +20v at pin 4 through Q03 and through the three parallel 2.7k resistors to -20v. The base drive for Q04 and Q05 is taken from the collector of Q03, and when Q03 conducts, turn-on current is provided for Q04 and Q05 so that they switch to the conduction state. Thus the circuit is completed, allowing positive current to flow from pin 4 to the output. When Q03 switches off, the voltage drop across diode CR10 applies a reverse bias of approximately 0.6v to the base-emitter junctions of Q04 and Q05, cutting them off.

Transistors Q04 and Q05 control a current of the order of 900 ma flowing in a highly inductive load. Diode CR09 is therefore provided so that when Q04 and Q05 interrupt the current, the induced high-voltage transient is dissipated with no effect on other transistors.

Diode CR11 acts as a clamp against positive voltage surges at the collectors of Q04 and Q05 when current is interrupted. Pin 5 connects to a separate +20v bus and prevents pin 4 from becoming more positive than +20.6v, taking into account the 0.6v drop across the silicon diode.

Capacitors C02 and C03 provide a smoothing filter for spikes and ripple in the +20v sources at pins 4 and 5. The 8 microfarad capacitor C02 is sufficient for ripple and low frequency fluctuations; however, it exhibits a certain amount of inductive reactance due to its large area. For this reason, it is necessary to include C03 which has negligible inductive reactance and is therefore effective in filtering high frequency spikes.

The Discharger circuit is enabled by a -1.1v "0" input on pin 6. This causes zener diode CR08 to apply sufficient forward bias to the base of Q02 so that Q02 switches to its maximum conduction state. Transistor Q02 thus provides a low impedance path to ground for any stored charge remaining in the primary windings of the two memory driver transformers.

SENSE AMPLIFIER

Card Type C06

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "0" output on pin 15.

The circuit may be conveniently divided into two sections: a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -13.6v. The output of -13.6v represents a logical "1" which changes to a logical "0" when a memory core switches its magnetic state. The following logic card interprets any signal more positive than -3v as a logical "0", however the discriminator output approaches -1.6v when a core switches.

AMPLIFIER

The differential voltage amplifier is the symmetrical portion of the circuit to the left of the diode bridge, as shown in the accompanying diagram. Input signals from the sense winding are received on pins 4 and 5. The ends of the sense winding are connected to these two pins, forming a series loop which threads all memory cores in a plane quadrant. The only ground reference to this loop is through the 1000-ohm resistor R02, thus the nominal 30 mv potential induced in the sense winding by the switching of a core is applied equally and oppositely to both input pins. This is amplified into a 3v signal which appears across the diode bridge.

The amplifier circuit is sensitive only to the difference in potential between pins 4 and 5, which is produced by the application of a double-ended signal from the sense winding. A simultaneous shift of the d-c reference level of both input pins produces only a negligible effect. It is possible for both inputs to fluctuate simultaneously by as much as 2v without producing more than 0.2v fluctuations at the diode bridge.

"Common mode rejection ratio" refers to the number used to represent the degree of sensitivity exhibited by a differential amplifier to potential differences between its inputs and simultaneous shifts of both inputs in the common mode. The number for this circuit is of the order of 40,000.

Resistors R01 and R03 are connected in series across the two inputs as shown. This relatively low resistance is in parallel with the input impedance of the amplifier, so that the total terminating impedance across the sense line is reduced. This has the effect of making the amplifier less sensitive to noise induced by the flow of inhibit current.

The 3.3 uh inductors in the emitter circuits of Q02 and Q03 determine the high frequency roll-off of the amplifier. This inductance reduces the gain at high frequencies and prevents the amplifier from responding to noise spikes.

The signals produced by the memory cores are received and amplified in the double-ended fashion. As an example of operation, assume that the 30 mv potential from the memory core is in a direction so that pin 4 shifts negative 15 mv and pin 5 shifts positive 15 mv from the rest state. These potentials are applied to the bases of Q02 and Q03, causing Q02 to conduct more heavily while conduction through Q03 decreases. This action is further regulated by the constant-current source through Q01, so an emitter current increase in Q02 must be accompanied by a decrease in Q03.

Due to the action described above the collector of Q02 becomes more positive and the collector of Q03 becomes more negative. This, in turn, causes transistors Q04 and Q06 to conduct less heavily while conduction through Q05 and Q07 increases. The collectors of Q04 and Q06 therefore shift approximately 1.5v in the negative direction and the collectors of Q05 and Q07 shift a similar amount in the positive direction. A potential difference of 3v then exists across the diode bridge.

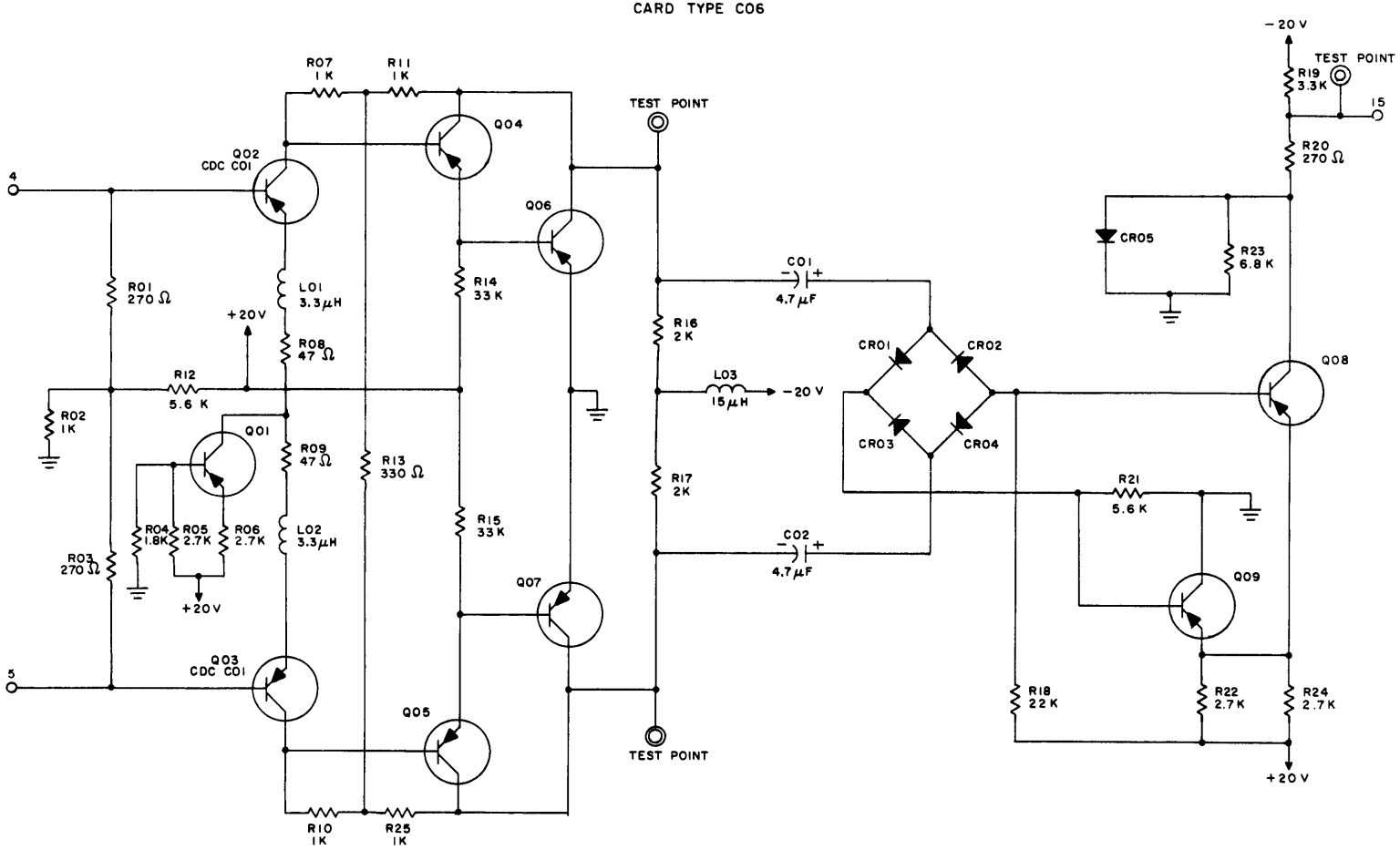
The signals from the collectors of Q02 and Q03 are amplified by a factor of 100 by Q04 and Q06, and by Q05 and Q07, respectively, which are connected as an emitter follower and a grounded emitter amplifier. Depending upon their particular characteristics, the two transistors are capable of providing a maximum available gain of the order of 1000. To insure stable operation, this is reduced to around 30 by the negative feedback connection of the two 1000-ohm resistors from collector to base. A portion of this negative feedback, however, is nullified by the 330-ohm resistor connecting the two feedback lines, so the over-all voltage gain of each of the stages is approximately 100.

DISCRIMINATOR

The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The

SENSE AMPLIFIER

CARD TYPE C06



NOTE:

1. ALL DIODES FD 1032.
2. ALL TRANSISTORS CDC C02, UNLESS OTHERWISE INDICATED.

output of the discriminator is from pin 15 and is approximately -13.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -1.6v which is interpreted as a logical "0".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q08 is held at around 1.2v higher positive potential than the base of Q09. Transistor Q09 thus conducts quite heavily while Q08 conducts very little. Under these conditions the output at pin 15 is around -13.6v, due to the voltage dividing action of R19, R20, and R23. Transistor Q09 provides a low impedance path to ground, so the emitter of Q08 cannot rise to a high positive potential when it is in a state of low conduction.

The diode bridge rectifies the potential across it, so an input of either polarity results in a negative input to the base of Q08 and a positive input to the base of Q09. This has the effect of causing Q08 to conduct heavily while Q09, in turn, conducts very little. Transistor Q08 thus enables a low impedance path from +20v to ground through diode CR05, which is a silicon diode having a forward drop of approximately 0.6v. The anode of CR05 is therefore at approximately +0.6v, so that pin 15 is biased at approximately -1.6v by resistors R20, R19, and the -20v source. This output voltage level is interpreted as a logical "0".

INHIBIT COMPENSATOR
Card Type C09

FUNCTION

The function of the circuits on this card is to enable a 340 ma current to flow from pin 1 or 15 to ground, whenever at least one input to the respective circuit is a -1.1v "0". The inhibit compensator circuits are energized by a +40v supply. Each circuit contains a series 133-ohm resistor external to the circuit on the card. Each inhibit compensator circuit terminates at either pin 1 or pin 15 of a C09 card, and the path is completed to ground allowing current to flow if the respective circuit attached to that pin switches to its conduction state.

OPERATION

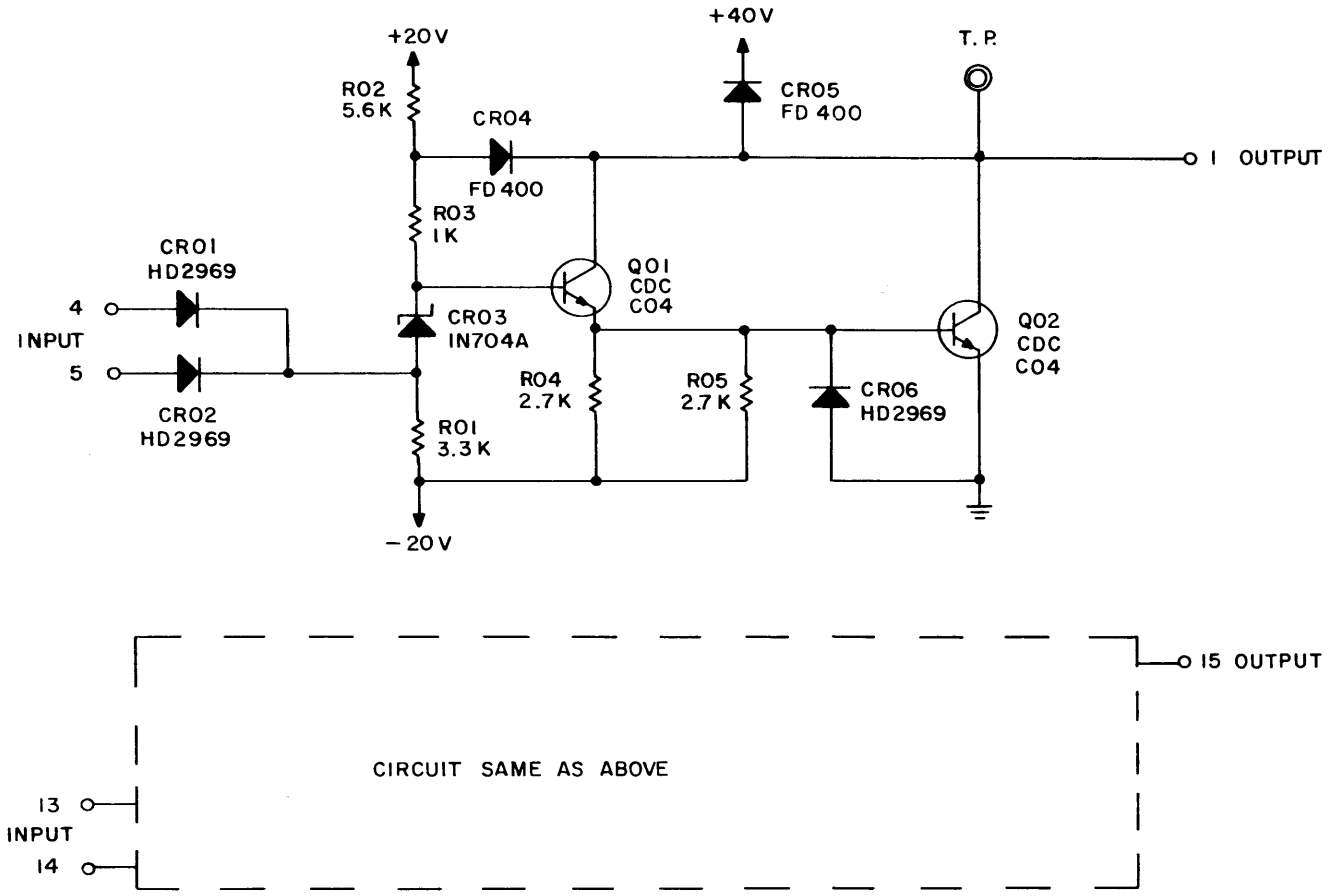
Each circuit has a two-way logical AND input, meaning that both inputs must be at the -5.8v "1" level for an input to be sensed. A -1.1v "0" signal on either input disables the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

The transistors are disabled if the AND is satisfied by two -5.8v "1" inputs, preventing current from flowing. If either input receives a -1.1v "0", the transistors switch to the conduction state and current is allowed to flow from the output pin to ground.

A level-shifting action is provided by the 4.1v zener diode CR03. This diode is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

When the AND is satisfied by -5.8v "1" inputs, this voltage level plus the forward drop of diodes CR01 and CR02 holds the anode of CR03 at approximately -6.1v. The base of Q01 is therefore at approximately -2v. The emitter of Q01 is held at approximately -0.3v by the forward drop of CR06. This places a reverse bias of 1.7v across the base-emitter junction of Q01, so it is well into the cut off region. In addition, the 0.3v drop of CR06 reverse biases the base-emitter junction of Q02, so that it is also cut off. Thus, except for negligible leakage effects, the output pin is completely isolated from ground.

When either input receives a -1.1v "0", the anode of CR03 is held at approximately -1.4v. The 4.1v voltage differential across the zener diode CR03 attempts to hold the



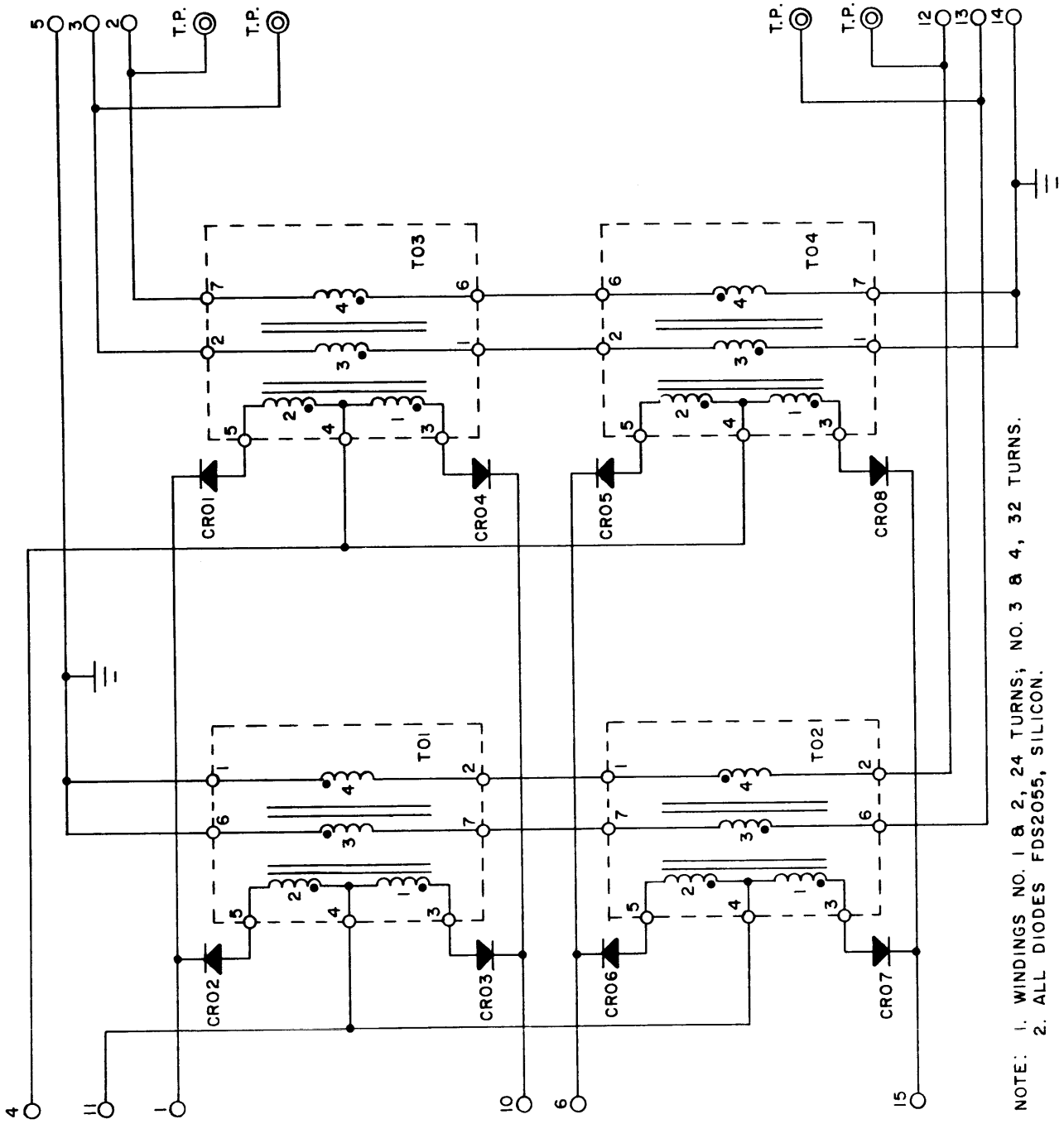
NOTES:

1. EACH CIRCUIT HAS A TWO-WAY "AND" INPUT.
2. A -1.1V "0" ON EITHER INPUT ENABLES CIRCUIT TO CONDUCT.
3. -5.8V "1's" ON BOTH INPUTS PREVENT CIRCUIT FROM CONDUCTING.

Inhibit Compensator C09

base of Q01 at approximately +2.7v. This causes Q01 to switch on and conduct heavily, but it is clamped out of saturation by CR04. The emitter voltage of Q01 rises to approximately +2.2v, providing drive to the base of Q02. Transistor Q02 thus switches to the conduction state, allowing current to flow from the output pin to ground.

The connection of diode CR05 and the +40v supply provides a clamp for the collector voltage of the transistors. When the transistors switch to the nonconducting state, the inductance of the load tends to induce high-voltage transients; however, these inductive transients are clamped at +40v plus the drop across the silicon diode CR05.



Memory Drive Line Transformer C10

To produce +44v at pin 12, the external circuitry would connect card pins 10 and 15 to ground, allowing 450 ma to flow through windings # 1 of T01 and T02. The primary voltage is of the order of +18v, due to the drop across the silicon diode and external circuitry; however, the 3:4 transformer step-up produces a secondary voltage of approximately +22v.

It is seen that windings # 4 of T01 and T02 are connected in series so the voltages are additive, resulting in +44v at pin 12. It is further seen that windings # 3 are connected oppositely, so the voltages cancel and only a negligible effect is produced at pin 13. However, +44v appears at pin 13 with negligible voltage at pin 12 if the external circuitry grounds pin 6 instead of pin 15.

If it is desired to produce -44v at pin 12, then pins 1 and 6 are grounded; and if the -44v is to appear at pin 13, pins 1 and 15 are grounded.

Under the preceding sets of conditions, the voltages appearing on pins 12 and 13 appear on pins 2 and 3, if the source of +20v is gated into pin 4 instead of pin 11.

The various outputs available at pins 2, 3, 12, and 13 and the conditions necessary to produce them, are listed below. Pin 5 provides a common return for pins 12 and 13, and pin 14 provides a common return for pins 2 and 3.

Gate +20v into:	Enable Ground Connection From:	Resulting Voltages at: Pin 2	Pin 3	Pin 12	Pin 13
Pin 4	Pins 6 and 10	+44v			
Pin 4	Pins 1 and 15	-44v			
Pin 4	Pins 10 and 15		+44v		
Pin 4	Pins 1 and 6		-44v		
Pin 11	Pins 10 and 15			+44v	
Pin 11	Pins 1 and 6			-44v	
Pin 11	Pins 6 and 10				+44v
Pin 11	Pins 1 and 15				-44v

DRIVE LINE TRANSFORMER
Card Type C10

FUNCTION

The function of this card is to provide half-currents of 340 ma at approximately 44v to the memory stack when supplied with primary power at the +20v level. The card contains four 3:4 voltage step-up transformers, each having two secondary windings of 32 turns and a center-tapped primary of 48 turns. The transformers are connected so that two operate simultaneously with their primary windings energized in parallel from +20v and their secondaries connected in series. The output voltages are therefore additive, resulting in levels of approximately 44v.

This card operates in conjunction with three other cards; a gate card which switches a source of +20v into the center taps of the transformer primaries, and with two transformer driver cards which allow current to flow from one of the primary windings to ground.

OPERATION

A schematic of the circuit contained on card type C10 is presented in the accompanying diagram, with the transformers indicated by dashed outlines. The transformers are identical, each having four windings and seven connecting pins as shown. Silicon diodes at transformer pins 3 and 5 provide isolation so current cannot flow through a primary winding in the wrong direction and prevent interaction between transformers.

The dots on the transformer windings indicate polarities according to the usual convention. For example, if current flows into the dotted end of the primary winding, current must flow out of the dotted end of the secondary winding. If a voltage is impressed across the primary winding so that the dotted end is positive, the dotted end of the secondary will also be positive.

As an example of operation, assume that card pin 11 is energized from a source of +20v. This is fed to the center tap of the primary windings of transformers T01 and T02. Then, by connecting card pins 1 or 10, and 6 or 15 to ground, it is possible to produce either +44v or -44v at either pin 12 or pin 13 while the other pin remains at essentially zero potential. The positive and negative potentials correspond to the memory cycle, in which a current of one polarity is used to read and the other to write.

I/O SENSE AMPLIFIER
Card Type C86

FUNCTION

The function of the circuits on this card is to detect, amplify, and shape the pulse induced in the sense winding when a magnetic memory core switches state during the Read phase of the memory cycle. The pulse produced during the Write portion of the cycle is not detected.

During the rest state, the circuit output is a logical "1" of approximately -5.7v. When a core is read, the output switches to a logical "0" of approximately -0.5v.

The circuits are restricted to driving AND loads only.

OPERATION

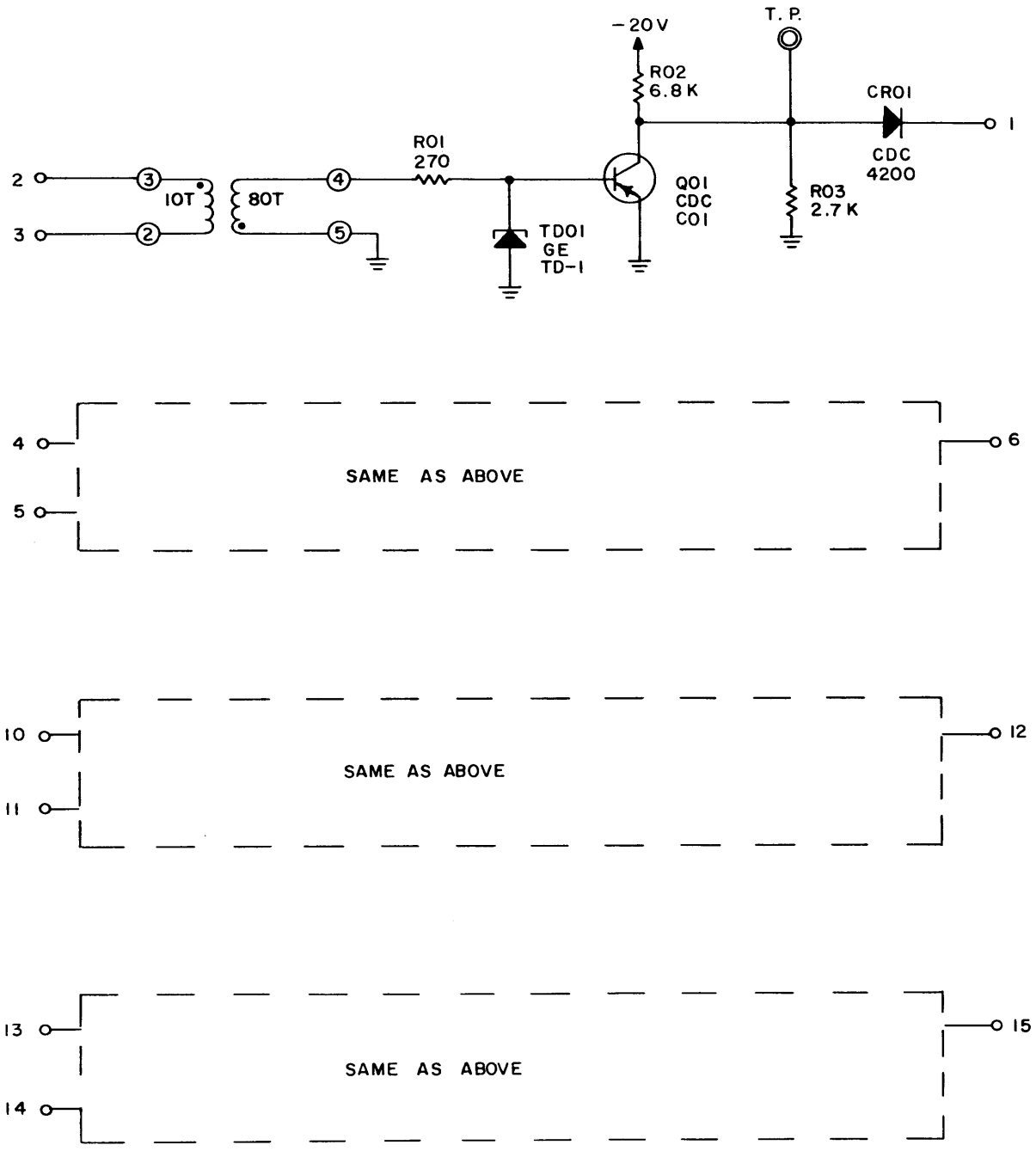
The Sense Amplifier circuit consists of a grounded emitter PNP transistor with a tunnel diode between base and ground. The tunnel diode provides a noise threshold rejection level and results in an essentially square output from the circuit.

In its low-voltage state, the tunnel diode holds transistor Q01 cut off. The circuit output is then produced by the voltage-dividing action of R02 and R03 and stabilizes at approximately -5.7v. The effect of the load is negligible, since the circuit is restricted to driving AND loads only.

The tunnel diode in its high-voltage state places a forward bias of approximately 0.5v across the base-emitter junction of Q01, causing Q01 to switch on and conduct heavily. The output voltage becomes equal to the collector voltage of Q01 plus the drop across diode CR01 and is approximately -0.5v.

The output produced when a memory core switches state is approximately 47 mv. During the Read phase, the core outputs are of a polarity such that pin 4 of the input transformer goes negative. The 47 mv input is increased by the 1 : 8 voltage step-up of the input transformer.

Initially, the tunnel diode is in its low-voltage state and the circuit is providing a "1" output. The tunnel diode remains in its low-voltage state as current through it increases, until it reaches the peak of its characteristic curve where I and V are approximately 1 ma and 65 mv, respectively. A slight increase in current puts the tunnel diode in the regenerative region and the voltage increases almost instantaneously to



NOTE:

A SENSE AMPLIFIER IS RESTRICTED TO DRIVING "AND" LOADS, ONLY.

I/O Sense Amplifier C86

500 mv. This causes Q01 to conduct and the circuit output switches to "0". The tunnel diode remains in the high-voltage state until current through it decreases to approximately 0. 12 ma. This is the characteristic curve valley, and at this point, the voltage drops almost instantaneously to approximately zero. This cuts off transistor Q01 and the circuit output returns to "1".

I/O MEMORY DRIVER
Card Type C87

FUNCTION

The function of this circuit is to provide drive current to a memory unit upon receipt of a -5.8v "1" input. The output may be either a half-current of approximately 200 ma, or a full current of up to 800 ma. In order to obtain a maximum current from pin 14 pin 10 must be grounded.

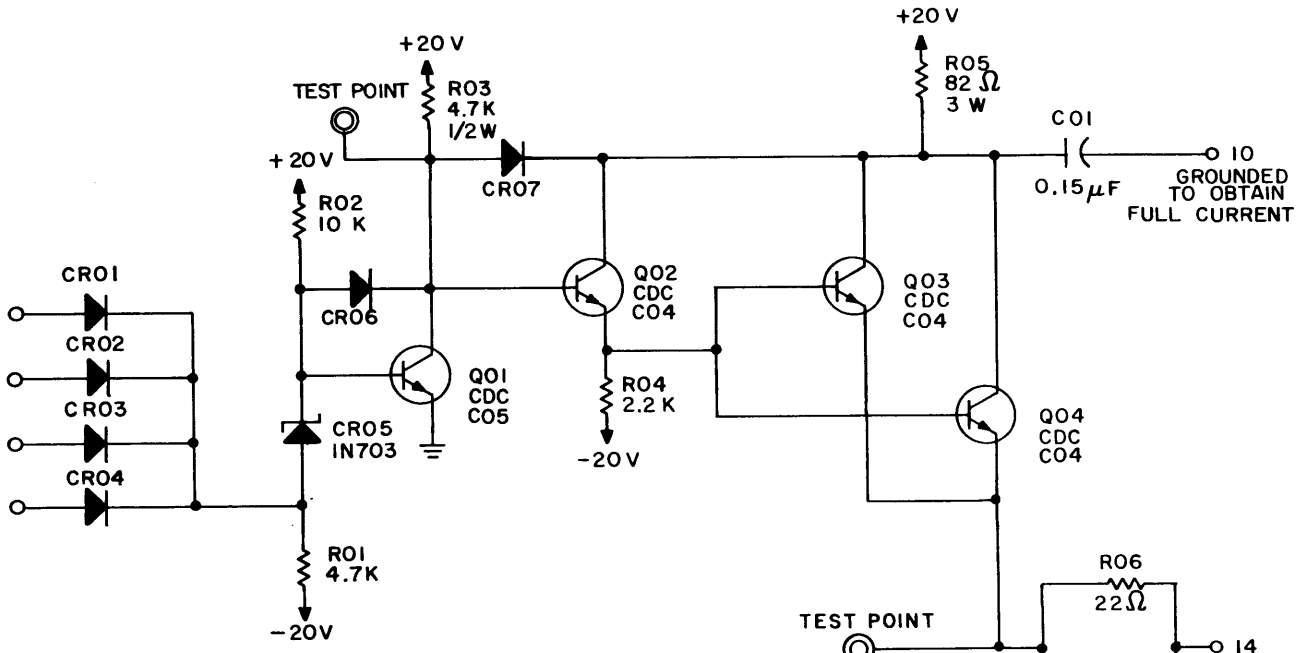
OPERATION

The circuit has a four-way logical AND input, meaning all inputs must be at the -5.8v "1" level in order for an input to be sensed. A 1.1v "0" on any input will disable the AND. An unused input acts as a steady "1" if left open, or as a steady "0" if grounded.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 3.5v zener diode CR05. The zener diode CR05 is reverse biased so that its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 3.5v positive with respect to the anode regardless of current fluctuations.

With -1.1v "0" inputs, zener diode CR05 holds the base of Q01 sufficiently positive so that it conducts heavily. Transistor Q01 is held out of deep saturation by CR06, and its collector voltage is approximately +0.5v. The collector voltage of Q01 is applied to the base of Q02, which is connected as an emitter follower. The emitter voltage of Q02 is therefore equal to its base voltage less the base-emitter junction drop, and is approximately -0.1v. The emitter voltage of Q02 is applied to the bases of Q03 and Q04, which are also connected as emitter followers. The emitter circuits of Q03 and Q04 thread the memory plane and terminate at a Diverter circuit; thus the emitter voltage of Q03 and Q04 is approximately +0.9v. The -0.1v input from Q02 therefore back biases the base-emitter junctions of Q03 and Q04, cutting them off.

A -5.8v "1" input results in approximately -2.3v at the base of Q01, so Q01 is cut off. If the circuit is providing a half-current, pin 10 is not grounded and resistors R05 and R08 limit the current to approximately 200 ma. In addition, the voltage drop across R05 holds the collector voltage of the transistors at a relatively low level. The collector of Q01 rises to approximately +3.5v, providing drive to Q02. The emitter voltage of Q02 becomes approximately +2.9v, causing Q03 and Q04 to switch to the conduction state. Transistor Q02 is held out of deep saturation by CR07. Q03 and Q04 are held out



NOTES :

1. ALL DIODES CDC 4200, UNLESS NOTED.
2. CIRCUIT HAS A FOUR—WAY "AND" INPUT.
3. −5.8V "1's" ON ALL INPUTS CAUSE Q03 AND Q04 TO CONDUCT.

of deep saturation by the voltage drop across Q02. The emitter voltage of Q03 and Q04 is applied to the drive lines and is approximately +2. 2v. The emitter currents of Q03 and Q04 combine to provide the memory drive current.

In order to obtain a peak value of full current from the circuit, pin 10 must be grounded. This allows capacitor C01 to become charged while the circuit is not providing drive current. When transistors Q03 and Q04 switch on, C01 discharges into the drive line, providing an initial high current surge. With Q01 cut off, its collector voltage rises to approximately +19v, providing drive to Q02. The emitter voltage of Q02 rises to approximately +18. 4v, causing Q03 and Q04 to switch on and conduct heavily. The voltage applied to the drive lines is the emitter voltage of Q03 and Q04, and is approximately +17. 8v during the initial high current surge. As capacitor C01 becomes discharged, the voltage levels within the circuit decrease toward the values given in the preceding paragraph.

I/O MEMORY DIVERTER
Card Type C88

FUNCTION

The function of this circuit is to enable memory drive current to flow from one of the output pins to ground, whenever all inputs are at the logical "0" level of -1.1v. The drive lines are energized with half-currents of 200 ma or full currents of up to 800 ma peak by the circuit contained on a Driver card C87. Each drive line terminates at one of the output pins of a Diverter card, and the circuit is completed to ground allowing current to flow when transistors Q02 and Q03 switch to the conduction state.

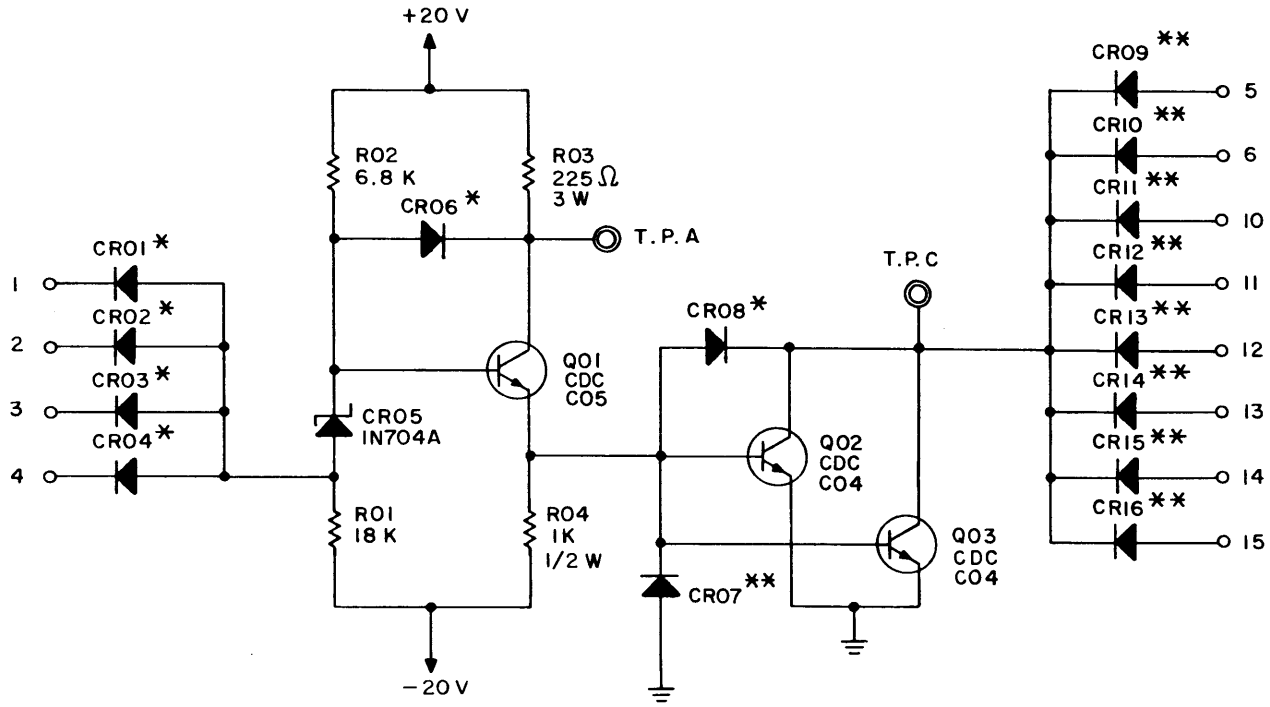
OPERATION

The circuit has four logical OR inputs, and transistors Q02 and Q03 switch to the conduction state only when all inputs are -1.1v "0". A -5.8v "1" on any input holds Q02 and Q03 in the cut off state.

An input level-shifting action is provided to the base of Q01 by resistors R01 and R02, and the 4.1v zener diode CR05. The zener diode CR05 is reverse biased so its operating point is beyond the knee of the breakdown region; thus the cathode remains approximately 4.1v positive with respect to the anode, regardless of current fluctuations.

A -5.8v "1" input results in approximately -1.5v at the base of Q01. This cuts off Q01, since its emitter is clamped at approximately -0.6v by diode CR07. The bases of Q02 and Q03 are also clamped at approximately -0.6v by diode CR07, and since their emitters are grounded, they are cut off.

If all inputs are at the -1.1v "0" level, zener diode CR05 holds the base of Q01 at approximately +1.4v. This causes Q01 to switch to a state of heavy conduction, but it is held out of deep saturation by diode CR06. Transistor Q01 is connected as an emitter follower; thus its emitter voltage rises to approximately +0.7v, providing drive for Q02 and Q03. The +0.7v input from Q01 causes Q02 and Q03 to switch on and conduct heavily, but they are held out of deep saturation by diode CR08.



* CDC 4200 (HD 2969)

** CDC 4211 (FD 400)

NOTES :

1. CIRCUIT HAS FOUR "OR" INPUTS.
2. TRANSISTORS Q02 AND Q03 SWITCH TO CONDUCTION STATE WHEN ALL INPUTS ARE −1.1V "0".

I/O EMITTER FOLLOWER
Card Type C90

FUNCTION

The function of the circuits on this card is to convert the outputs from the brushes of a punched card reader into memory drive currents of approximately 200 ma. The circuit output is in series with a memory drive line, which connects to a -20v supply. The circuit input is driven by one of the brushes at a card reading station. When the brush senses a hole in the card, transistor Q01 conducts heavily, enabling memory drive current to flow.

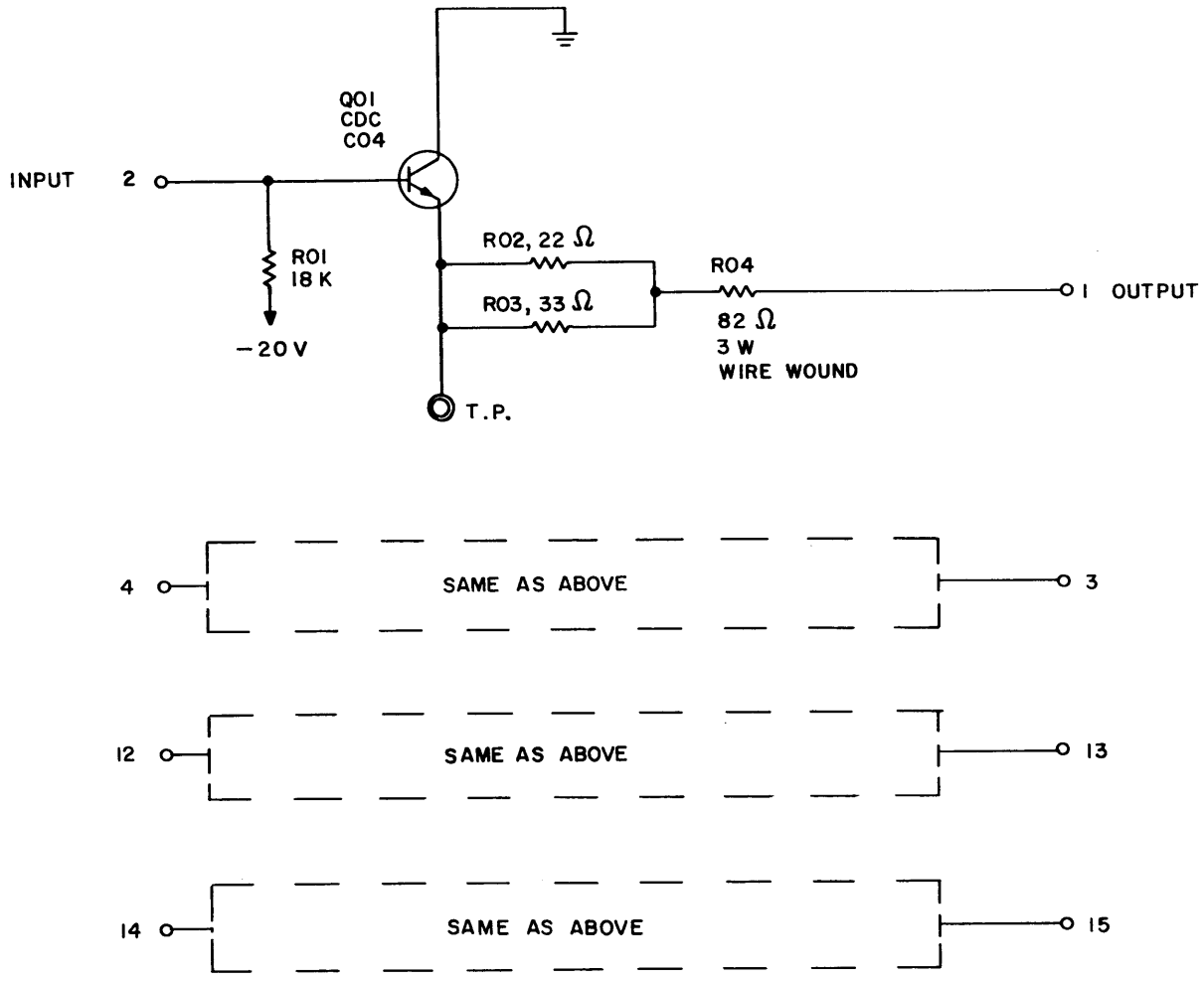
OPERATION

Inputs to the circuit are provided by a brush at the card reading station, and the signal levels are open circuit and approximately ground. The ground signal results when a hole in the punched card allows the brush to touch a metallic roller which is at approximately ground potential. If a hole is not present, the insulating effect of the card produces an open circuit.

The metallic roller at the reading station is held at approximately ground potential by a Relay Driver card type C84. The roller is thus at a potential equal to the saturation voltage of the Relay Driver transistor which is approximately -0.6v.

An open circuit input allows the base voltage of Q01 to rise toward -20v. The emitter of Q01 is also at -20v, since it connects through the memory drive line to a -20v supply. This puts Q01 in the cut off condition, and memory drive current is prevented from flowing.

An input of approximately ground allows Q01 to switch on and conduct heavily. The voltage applied to the drive line is -20v, less the drop across the Relay Driver transistor and the base-emitter voltage of Q01, and is approximately -18.5v. The memory drive current is also the emitter current of Q01 and is limited by resistors R02, R03, and R04 to approximately 200 ma. The base current of Q01 is equal to the 200 ma emitter current divided by h_{FE} and is approximately 8.5 ma. The brush at the reading station is therefore required to carry the base current of Q01 plus enough additional current so that the voltage drop across R01 is approximately 19.4v; a total of approximately 9.5 ma.



NOTES:

1. INPUT SIGNAL LEVELS ARE:
   - A. OPEN CIRCUIT, Q01 CUTS OFF.
   - B. ≈ GROUND, Q01 CONDUCTS HEAVILY.

I/O Emitter Follower C90

DIGIT DRIVER
Card Type HA14

FUNCTION

The function of this circuit is to provide bi-directional 400 ma drive currents through a digit winding in a word organized memory. The two ends of the winding connect to pins 14 and 15. Pin 13 connects through a power resistor to +20 v.

The circuits are activated by -1.1v "0" inputs. Each circuit has a 2-way AND input and pin 12 acts as a gate. The receipt of -1.1 v "0" inputs at pins 10 and 12 will cause pin 15 to go positive and 14 to go negative; with "0" inputs at pins 11 and 12, pin 14 will go positive and 15 will go negative.

OPERATION

The filter network consisting of L01, L02, and C04-C08 performs a decoupling function. The current carried by pins 14 and 15 is of the order of 400 ma. The decoupling network prevents voltage surges and fluctuations on the circuit input which could result from heavy current switching at the output.

The two input circuits are identical, as shown in the accompanying diagram. The components mentioned here are those associated with test point A.

The input of each circuit is a 2-way AND, and -1.1 v "0" inputs allow transistor Q01 to conduct. A level-shifting action is provided by the 4.1 v zener diode CR05. A -5.8 v "1" input at either pin 10 or 12 will result in approximately -1.2 v at the base of Q01, so that Q01 is cut off. With both inputs at the -1.1 v "0" level, zener diode CR05 will bias the base of Q01 well into the conduction region.

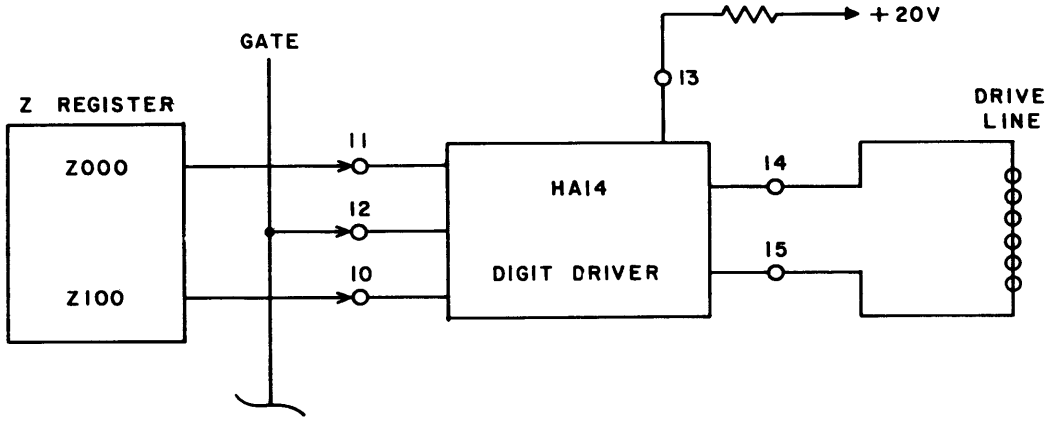
Transistor Q01 in its conduction state allows current flow to increase through the primary winding of transformer T1. In this state, current through the 16-turn primary of T1 will be approximately 2 ma. This results in about 8 ma in each of the 4-turn secondaries and provides forward drive current for Q03 and Q06, causing them to switch.

Transistors Q03 and Q06 in their conduction state cause pin 15 to go positive and 14 to go negative. The 100-ohm resistor R15 provides a blocking action, causing practically all of the current from Q03 to flow out of pin 15, through the 2-ohm drive line resistance, back into pin 14, and through Q06 to -20 v.

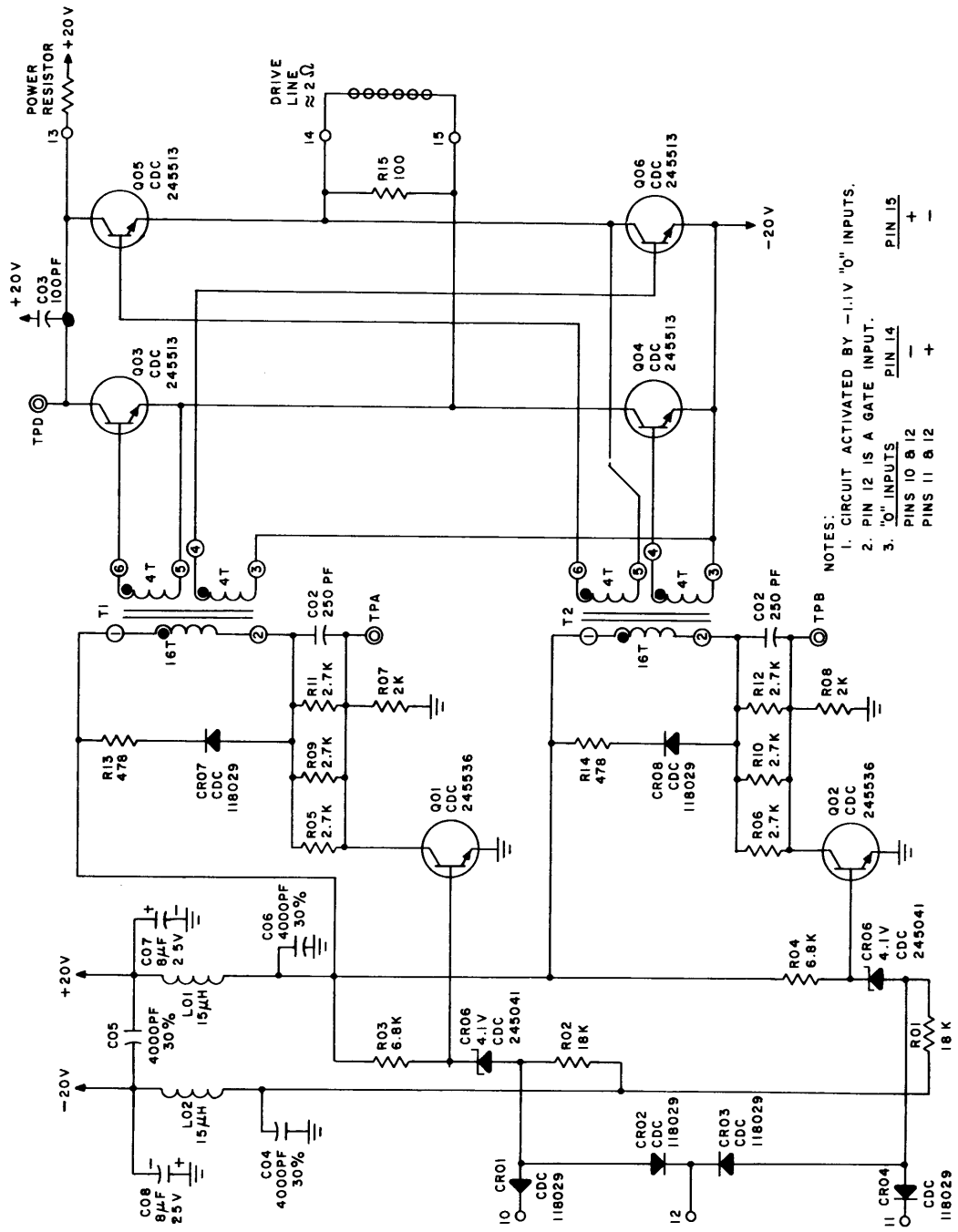
(Note that with "0" inputs at pins 11 and 12, transistors Q04 and Q05 will conduct producing an output current of the opposite polarity.)

Capacitor C03 performs a speed-up function, providing an initial surge of high current when the transistors switch on. This gives a sharper leading edge to the output waveform.

The connection of R13 and CR07 provides a clamp for the transformer primary. This dissipates any inductive transient which could result when Q01 switches off.



TYPICAL APPLICATION



Digit Driver HA14

DIGIT COMPENSATOR
Card Type HA15

FUNCTION

This circuit operates in conjunction with the drive hardware of a word-organized memory. Its purpose is to provide a constant load for the -20v power supply by driving a 400 ma current through a load resistor during times when no drive lines are energized.

The load resistors are external to the circuits on the card and are connected in series from pins 1 and 15 to -20v. Current is allowed to flow whenever at least one of the inputs to the respective circuit is a -5.8v "1".

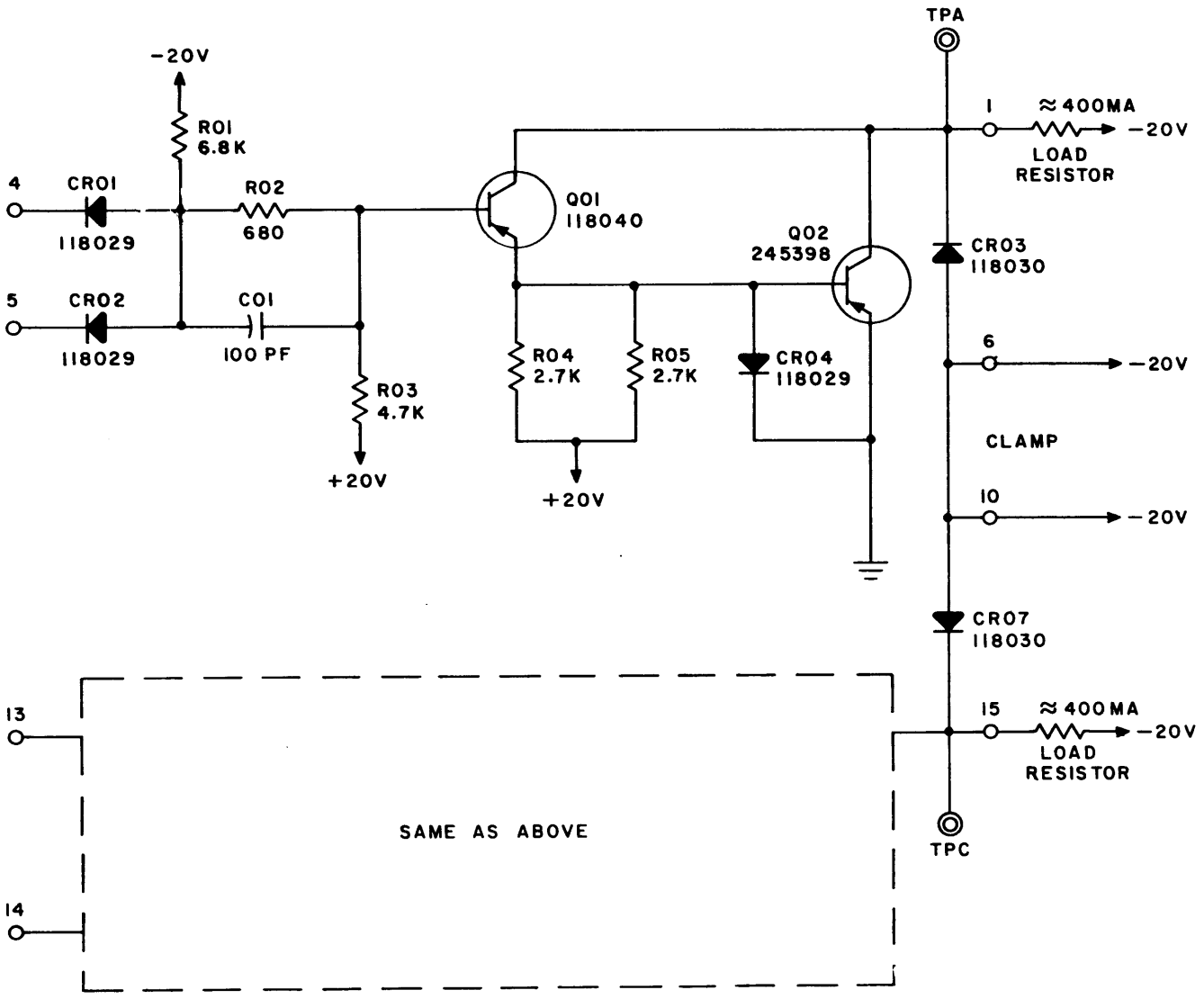
OPERATION

Each circuit has two OR inputs, and a -5.8v "1" on either input will cause the circuit to conduct. If both inputs are left open, the base of Q01 will rise toward approximately +4.5v and the circuit will be cut off.

A -1.1v "0" on both input will hold the circuit in the OFF state. This results in approximately +2v at the base of Q01. The emitter of Q01 and the base of Q02 are held at +0.5v by the forward drop across CR04, so that both transistors are cut off.

A -5.8v "1" on either input holds the base of Q01 at approximately -2v. The base drive for Q02 is taken from the emitter of Q01. A negative-going input to Q01 causes it emitter current to increase. Initially, this current is supplied from the +20v source through R04 and R05. However, the voltage drop across R04 and R05 is clamped at about 0.3v by the base-emitter junction drop of Q02. Resistors R04 and R05 are therefore able to supply only about 0.22 ma, and a further increase in the emitter current of Q01 will draw drive current through Q02, causing it to switch to its conduction state.

Diodes CR03 and CR07 provide clamps for the collector voltage of the transistors. This clamp connection should be used when driving an inductive load.



NOTES: 1. EACH CIRCUIT HAS TWO "OR" INPUTS.
2. TRANSISTORS CONDUCT WHEN EITHER INPUT RECEIVES A −5.8V "1".

SENSE AMPLIFIER
Card Type HA16

FUNCTION

This card is designed for use as a sense amplifier in a word-organized memory. It consists of a differential amplifier driving a discriminator with a strobe input. Pins 4 and 5 connect to the two ends of the sense line, pin 15 provides the output, and pin 12 is the input for the -1.1v "0" strobe pulse. In the quiescent state, the output at pin 15 is about +0.3v which is interpreted as a logical "0".

The polarity of the differential 0.1 v input signal determines whether the output at pin 15 will be "1" or "0". If pin 4 goes positive with respect to pin 5, the strobed output at pin 15 will be a "1" of approximately -5.8 v. If pin 4 goes negative with respect to pin 5, the output at pin 15 remains at a +0.3 v."0".

The strobe input at pin 12 is a -1.1 v "0" pulse. This input must be present in order to allow the circuit to produce a -5.8 v "1" output. If pin 12 is held at -5.8 v "1", the output at pin 15 will be held at +0.3 v "0".

OPERATION

Since this circuit is a direct coupled amplifier, regulated voltages must be used. A connection to -18 volts is made at pin 2 and a connection to -6.8 v is made at pin 13. The -18 v may be obtained from an 18-volt zener diode and a 4.5-ohm resistor in series to -20 v, and the -6.8 v may be obtained using a 6.8-volt zener diode and a 30-ohm resistor in series to -20 v.

The 200-ohm resistors R01 and R04 terminate the sense line, while R02 and R03 provide bias for Q01 and Q02. The 100 mh inductor in the emitter circuit of Q01 and Q02 greatly increases the emitter impedance and improves the common mode characteristics.

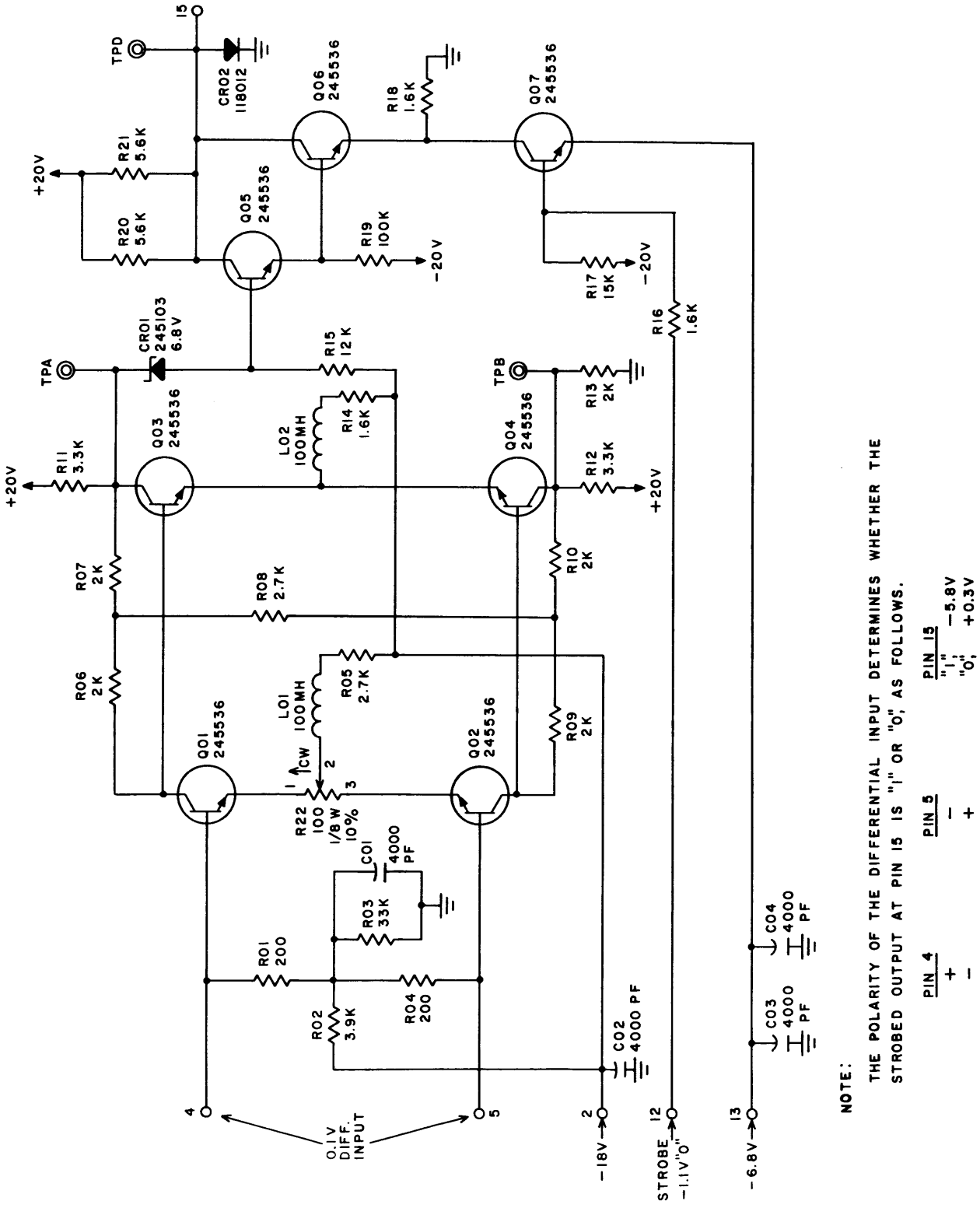
The 2K resistors in the collector circuits of the amplifier provide negative feedback. A portion of this is nullified by the positive feedback connection of R08.

The load resistances of Q01 and Q02 consist of the two 2K resistors plus the 3.3 K resistor. The load of Q03 is the 3.3 K resistor in parallel with the output circuit, while the load of Q04 is the 3.3 K resistor and the 2 K resistor in parallel.

Level translation is performed by the 6.8v zener diode CR01, which drives the input of the Darlington amplifier consisting of Q05 and Q06.

Transistors Q06 and Q07 perform an AND function. If both conduct at the same time, the -6.8v at pin 13 will produce approximately -5.8v at pin 15, allowing for voltage drop across the transistors. Transistor Q06 is driven to its conduction state by a differential input which causes pin 4 to become positive with respect to pin 5. Transistor Q07 is driven to conduction by a -1.1v "0" strobe pulse at pin 13.

If the AND condition of simultaneous conduction by Q06 and Q07 is not met, the voltage at pin 15 will be a logical "0" at approximately +0.3v. This is produced by the forward drop across CR02.



NOTE:

THE POLARITY OF THE DIFFERENTIAL INPUT DETERMINES WHETHER THE STROBED OUTPUT AT PIN 15 IS "1" OR "0", AS FOLLOWS.

PIN 4	PIN 5	PIN 15	
+	−	"1"	-5.8V
−	+	"0"	+0.3V

Sense Amplifier

SENSE AMPLIFIER
Card Type HA18

FUNCTION

This card amplifies and detects the pulses induced in a sense winding when a magnetic memory core switches polarity. The two ends of the sense winding are connected to pins 4 and 5, and when a core switches its magnetic state, the circuit produces a logical "1" output at pin 15.

The circuit may be conveniently divided into two sections; a differential voltage amplifier having a gain of approximately 100, and a discriminator having an output of approximately -1.6v. The output of -1.6v represents a logical "0" which changes to a logical "1" when a core switches. The following logic card interprets any signal more negative than -3v as a logical "1", however the circuit output approaches -14.6v when a core switches.

AMPLIFIER

The differential voltage amplifier portion of the circuit is similar to card type C06, which is discussed elsewhere. However, the overall gain is approximately 100 so that the nominal 30 mv induced in the sense winding by the switching of a core results in approximately 3v at the diode bridge.

DISCRIMINATOR

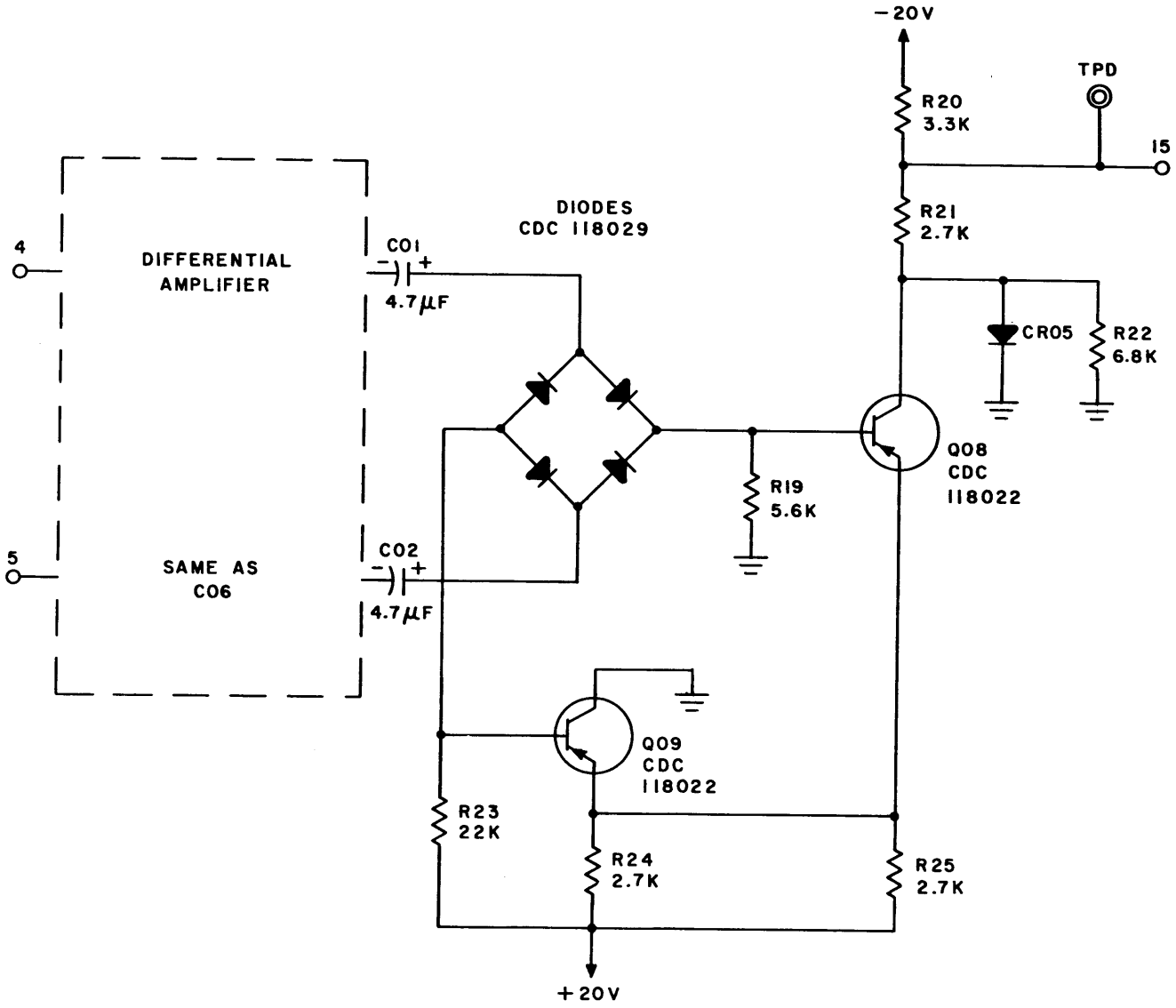
The discriminator is the portion of the circuit to the right of the diode bridge. Its function is to provide outputs at voltage levels suitable for use by logic circuits. The output of the discriminator is from pin 15 and is approximately -1.6v during the rest state. However, when a voltage appears across the diode bridge, the output at pin 15 approaches -14.6v which is interpreted as a logical "1".

The diodes used in the bridge are high speed silicon devices having a forward voltage drop of the order of 0.6v. Therefore, during the rest state, a voltage-dividing action is provided from +20v to ground through the 22,000-ohm resistor R18, the diode bridge, and the 5600-ohm resistor R21. Due to the forward drop of the diodes, the base of Q09 is held at around 1.2v higher positive potential than the base of Q08. Transistor Q08 thus conducts quite heavily while Q09

conducts very little. Under these conditions the output at pin 15 is around -1.6 v, due to the voltage dividing action of R20, R21, and the -20 v source. Diode CR05 is in a state of heavy forward conduction, being forward-biased by the +20 v source through R25 and Q08. In this state, the anode of CR05 is at approximately +0.6 v.

The diode bridge rectifies the potential across it, so an input of either polarity results in a positive input to the base of Q08 and a negative input to the base of Q09. This has the effect of causing Q09 to conduct heavily while Q08, in turn, conducts very little.

The output of -14.6 v is established by the voltage-divider action of R20, R21, and R22. Transistor Q09 provides a low impedance path to ground, so that the emitter of Q08 cannot rise to a high positive potential.



NOTE: PRODUCES "1" OUTPUT WHEN CORE SWITCHES.

Sense Amplifier HA18

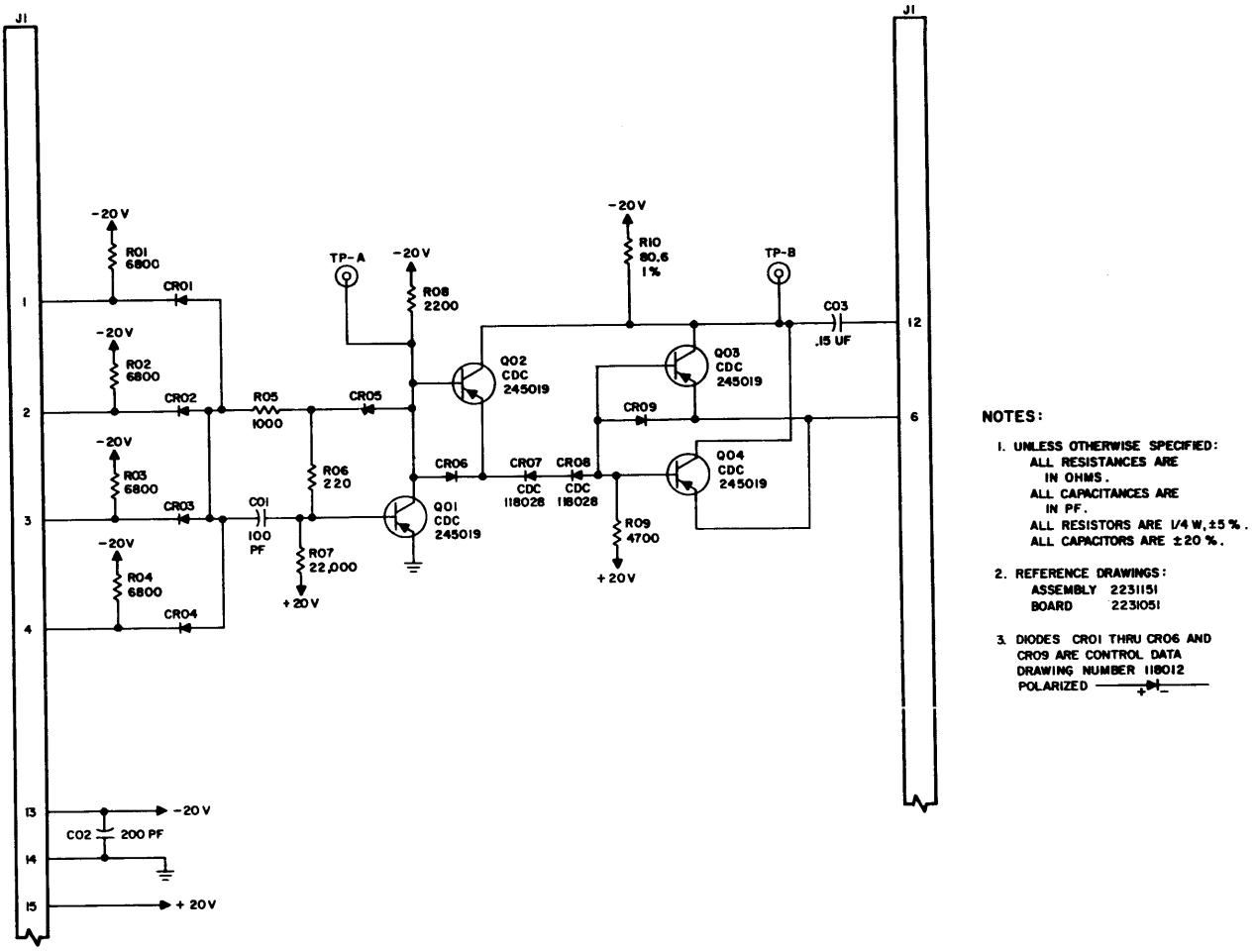
MEMORY DRIVER
Card Type P51

Card P51 provides either 200 ma half-current or 400 ma full-current (with pin 12 grounded) pulses to the wires threading the magnetic cores in the memory unit by enabling transistors Q03 and Q04, so positive current may flow from pin 6 to -20v.

This card is controlled by logic inputs on pins 1, 2, 3, and 4. Inputs are either -3v, logical "1", or -0.5v, logical "0". Transistors Q03 and Q04 are cut off if any of the card inputs receives a logical "1" and conduct only if all inputs are a logical "0".

Assume that input pins 2, 3, and 4 are grounded ("0") and that a -3v signal appears on the collector of the transistor on the preceding logic card, which is connected to input pin 1 of the P51 card. This level is sufficiently negative to cause the output diode on the logic card to cut off and permit the input diode on pin 1 of the P51 card to conduct. This biases the emitter-base junction of Q01 in the forward direction. With Q01 in a conduction state, its collector goes to approximately ground potential and Q02 cuts off. The base potential of Q03 and Q04 is then raised toward +20v so that they are also cut off.

If the collector on the preceding logic card were at -0.5v, its output diode would conduct and hold the input of the P51 card at about -1.0v. This is sufficiently positive to bias the emitter-base junction of Q01 in the reverse direction. Q01 would then cease to conduct and its collector would go negative, causing Q02 to conduct. This places a negative potential on the bases of Q03 and Q04, causing them to conduct, and permitting current to flow from pin 6 to -20v. Pin 12 is grounded when the card is used as a read driver, so that capacitor C03 can supply an initial surge of current.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.

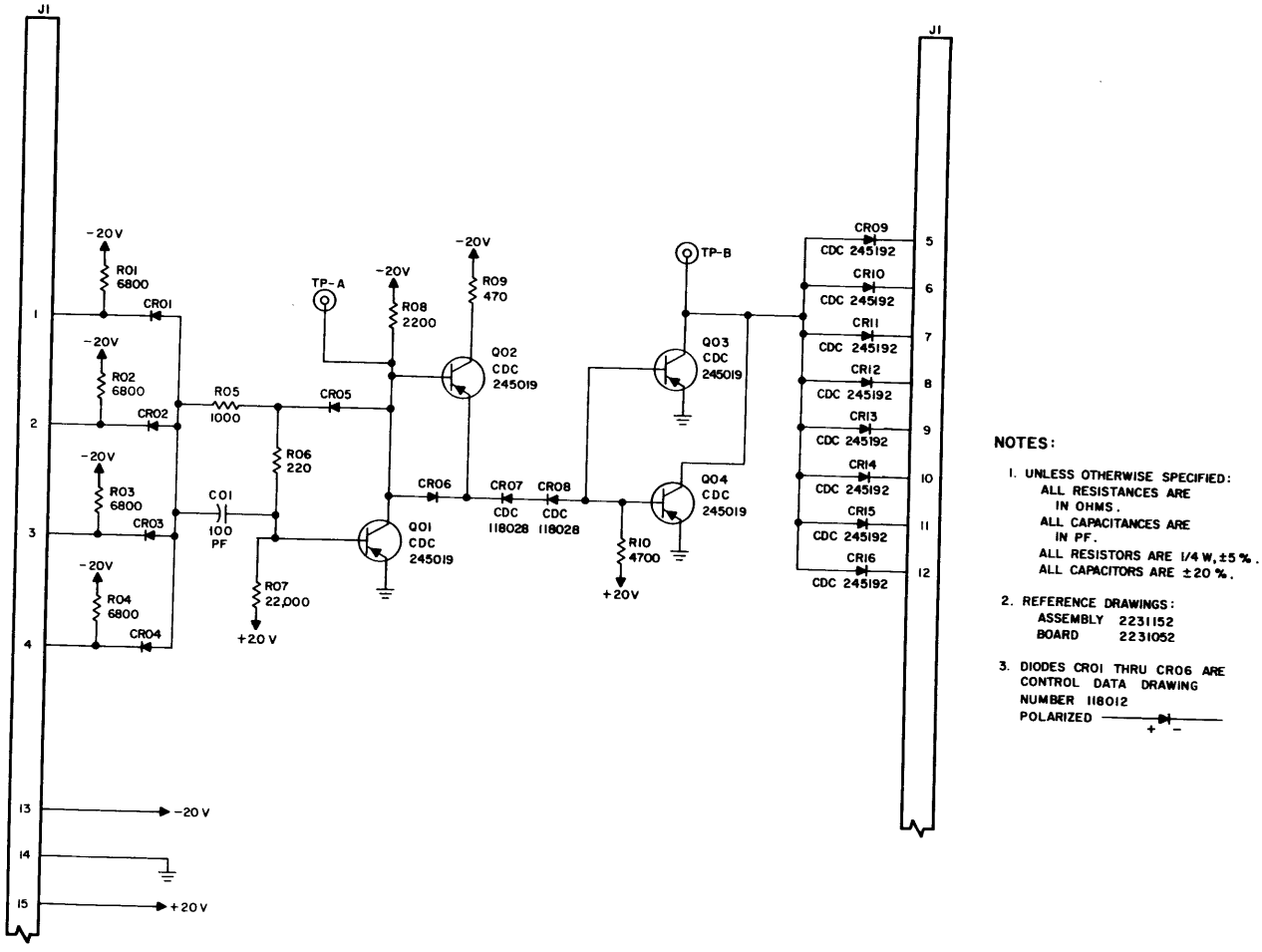
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231151
   BOARD 2231051

3. DIODES CR01 THRU CR06 AND CR09 ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED

Memory Driver P51A

MEMORY DIVERTER
Card Type P52

Card P52 simultaneously grounds eight of the wires threading the magnetic cores in the memory unit to provide complete circuit paths for the read and half-write current. Transistors Q03 and Q04 conduct when all inputs are "0".



NOTES:

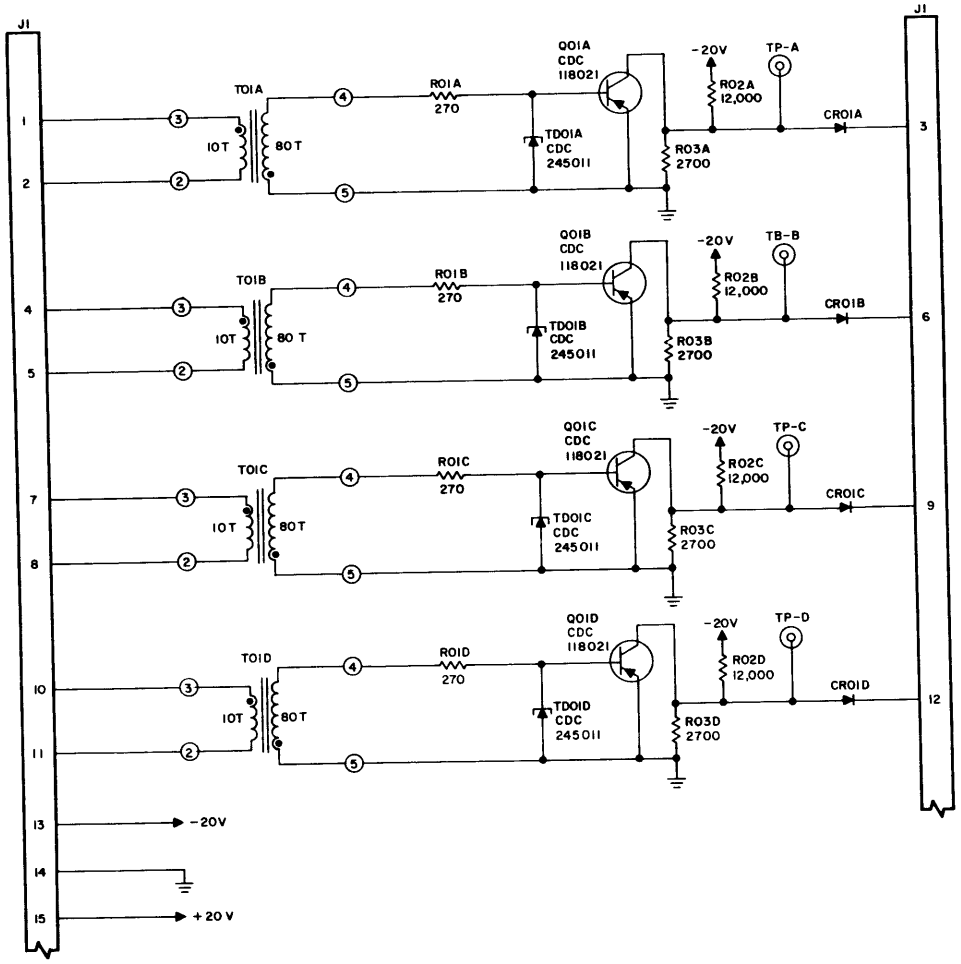
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5 %.
   ALL CAPACITORS ARE ±20 %.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231152
   BOARD 2231052
3. DIODES CR01 THRU CR06 ARE CONTROL DATA DRAWING NUMBER 118012
   POLARIZED

Memory Diverter P52

SENSE AMPLIFIER
Card Type P56

Card P56 detects, amplifies, and shapes the pulses induced in a sense winding when the state of a magnetic core is changed by a read current pulse. The card contains four identical amplifiers, A, B, C, and D. Each amplifier consists of a grounded emitter PNP transistor with a tunnel diode connected from the base to ground, to reject noise below a predetermined threshold and square the pulse. The base of the transistor is driven by a 1 : 8 step-up transformer in which the primary winding is connected in series with the sense wire threading one of the rows of magnetic memory cores.

Example: Assume that an input is being received and terminal 4 of the transformer is starting to go negative. This causes current to flow through the 270 ohm resistor R01 and through the tunnel diode TD01 to ground. Initially the card has a -3v output, since the tunnel diode in its low voltage state does not permit transistor Q01 to conduct. When tunnel diode current has increased to 1 ma, it switches to its high voltage state. Q01 conducts and the card output goes to -0.5v, where it remains as long as TD01 is in its high voltage state. When the input current decreases to 0.1 ma, the tunnel diode switches back to its low voltage state, Q01 is cut off, and the card output returns to -3v. In this manner, a square wave output is produced and noise signals insufficient to switch the tunnel diode are rejected.



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCES ARE IN OHMS.
   ALL CAPACITANCES ARE IN PF.
   ALL RESISTORS ARE 1/4 W, ±5%.
   ALL CAPACITORS ARE ±20%.
2. REFERENCE DRAWINGS:
   ASSEMBLY 2231156
   BOARD 2231056
3. DIODES CR01A THRU CR01D ARE CONTROL DATA DRAWING NUMBER 118012 POLARIZED

Sense Amplifier P56

► ►CUT OUT FOR USE AS LOOSE-LEAF BINDER TITLE TAB

CONTROL DATA
CORPORATION

8100 34th AVE. SO., MINNEAPOLIS, MINN. 55440

PRINTED IN U.S.A.