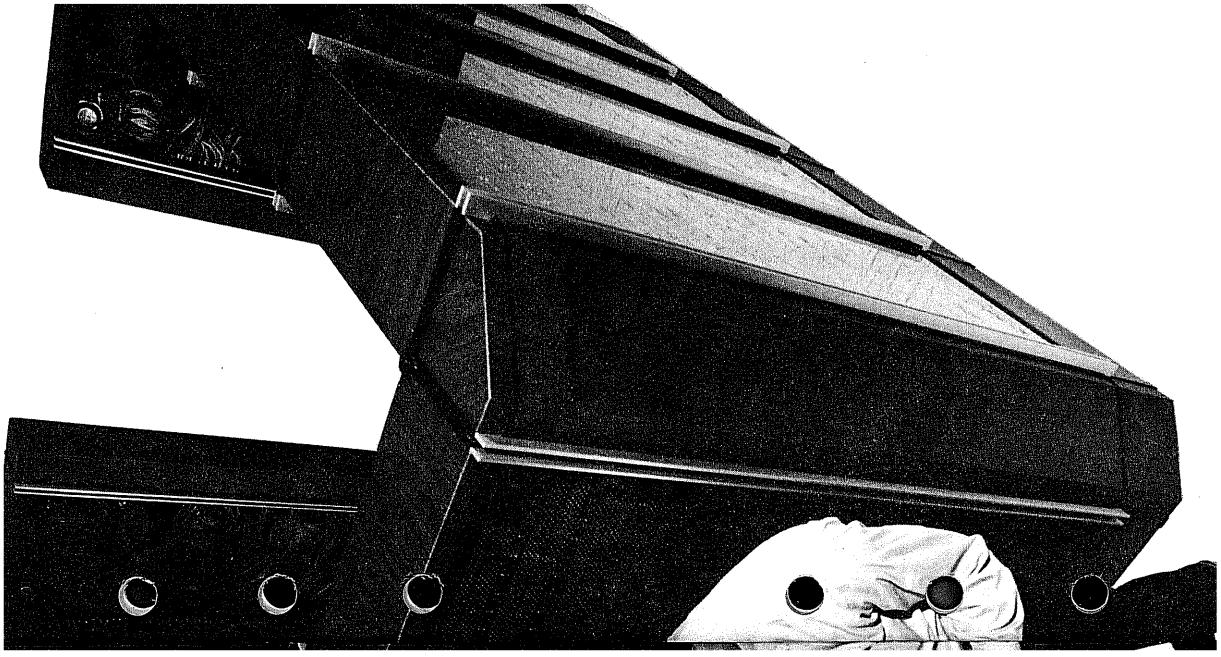
Control Data®
7600 Computer System

Hardware Features

DAVID E. LEE
17.8.70

7600 the system for the 70's



RECORD of REVISIONS

REVISION	NOTES
01	Initial printing.
12-1-68	
02	Manual revised. This edition obsoletes all previous
3-20-69	editions.

FORM CA 230

Pub. No. 60258500

Printed in United States of America

Address comments concerning this manual to:

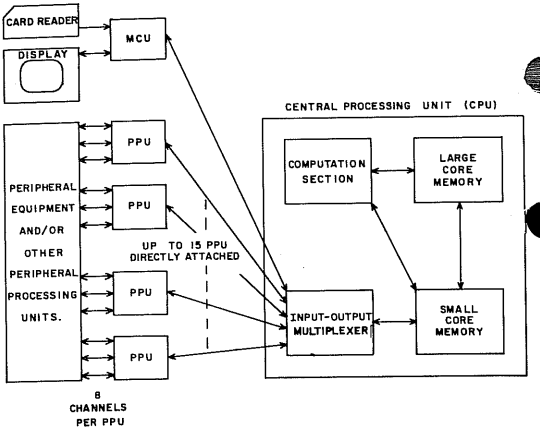
Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
St. Paul, Minnesota 55112

CONTENTS

INTRODUCTION

This booklet presents the salient hardware features of the CONTROL DATA® 7600 Computer System. For complete information on the 7600 Computer System, refer to the Control Data 7600 Computer System Reference Manual, Publication number 60258200.

7600 SYSTEM



CENTRAL PROCESSING UNIT (CPU)

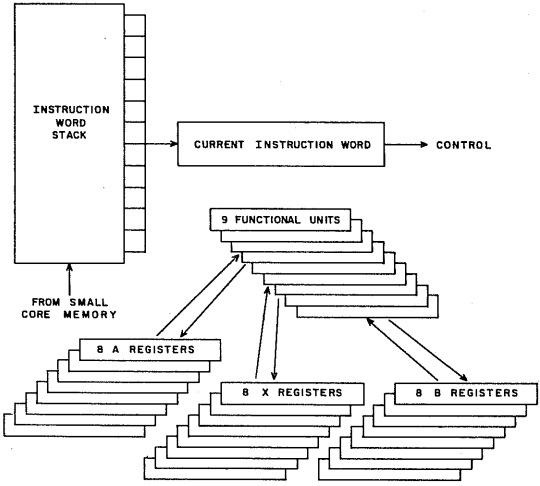
- 60-bit Computation Section
- 60-bit Small Core Memory (65,536 words) plus parity
- 60-bit Large Core Memory (512,000 words) plus parity
- CPU Input/Output Section (15 channels)

PERIPHERAL PROCESSING UNITS (PPU)

- 12-bit computation Section
- 8 fully duplex data channels

CENTRAL PROCESSING UNIT (CPU)

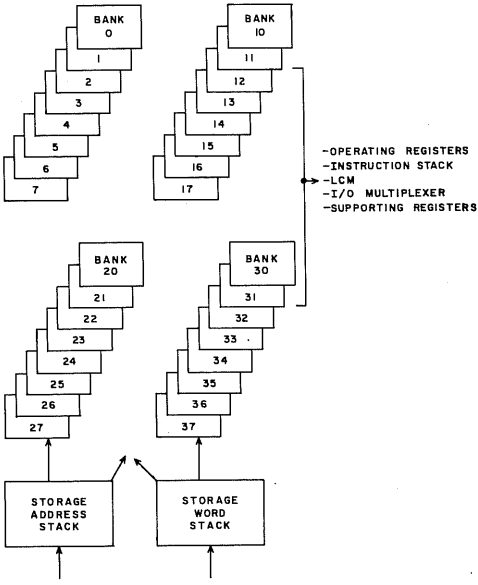
CPU COMPUTATION SECTION



- 60-bit internal word
- binary computation in fixed and floating point format
- 12-word (60 bits) instruction stack
- 24 operating registers
  8 18-bit A registers
  8 18-bit B registers
  8 60-bit X registers
- nine independent functional units

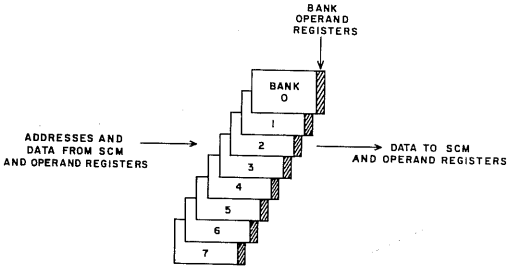
  Long Add
  Floating Add
  Floating Multiply
  Floating Divide
  Boolean
  Shift
  Normalize
  Population Count
  Increment
- Synchronous internal logic with 27.5 nanosecond clock period

CPU SMALL CORE MEMORY (SCM)



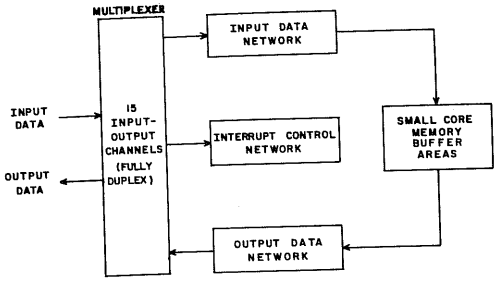
- 65,536 words of coincident current memory (60) bits plus parity)
- 32 independent banks; sequential addresses in separate banks
- 2048 words per bank
- 275 nanosecond read/write cycle time
- 27.5 nanosecond per word maximum transfer rate

CPU LARGE CORE MEMORY (LCM)



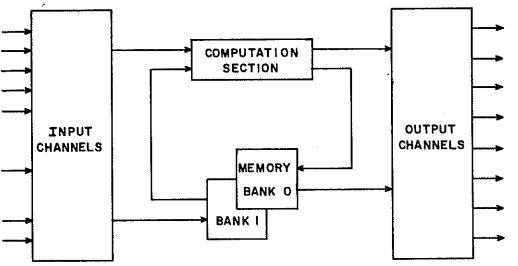
- 512,000 words of linear select memory (60 bits plus parity)
- 8 independent banks, each with an 8-word operand holding register
- 64,000 words per bank
- 1760 nanosecond read/write cycle time
- 8 words read simultaneously into bank operand register each reference; if addressed word is in bank operand register, no memory access is required
- 27.5 nanosecond per word maximum transfer rate
- operands directly accessible by CPU

CPU INPUT/OUTPUT SECTION



- 15 independent channels (asynchronous)
- each channel fully duplex
- buffer areas of 128 words each channel; buffer area sizes can be changed by wiring change
- 55 nanoseconds per 60-bit word maximum transfer rate to SCM

PERIPHERAL PROCESSING UNITS (PPU)



COMPUTATION SECTION

- 12-bit internal word
- binary computation in fixed point
- synchronous internal logic with 27.5 nanosecond clock period

CORE MEMORY

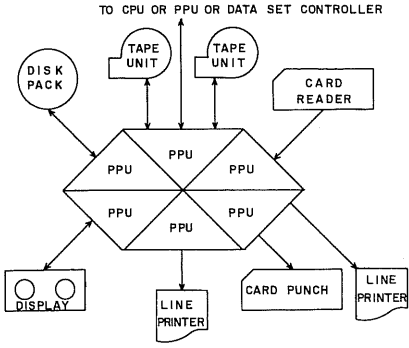
- 4096 words of coincident current memory (12 bits plus parity)
- two independent banks; consecutive addresses to alternate banks
- 2048 words per bank
- 275 nanosecond read/write cycle time

INPUT/OUTPUT SECTION

- 8 independent channels (asynchronous)
- each channel fully duplex (12-bit)
- 247.5 nanoseconds per 12-bit word maximum transfer rate

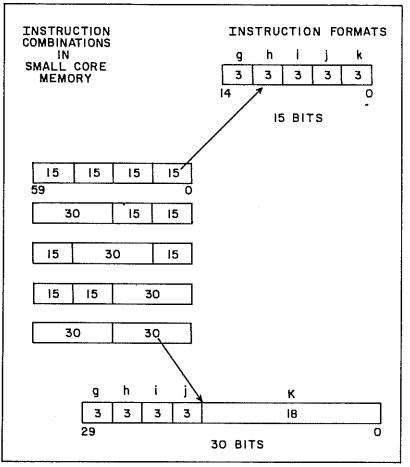
PERIPHERAL EQUIPMENT CONFIGURATIONS

Peripheral equipments are attached to a cluster of interconnected PPU's to form an I/O station. Such a station can communicate with the multiplexer in the CPU directly or via another PPU. A representative configuration is shown below.



This diagram is necessarily simplified to basic data paths.

CENTRAL PROCESSING UNIT INSTRUCTIONS



EXPLANATION OF SYMBOLS USED IN CENTRAL PROCESSOR INSTRUCTION LISTINGS

A One of eight address registers (18 bits)

B One of eight index registers (18 bits)

gh Instruction code (6 bits)

i Specifies which of eight designated registers (3 bits). Is also used in some instructions as part of the operation code.

j Specifies which of eight designated registers (3 bits)

k Specifies which of eight designated registers (3 bits)

K Constant, indicating branch

X One of eight operand registers (60 bits)

CENTRAL PROCESSOR TIMING NOTES

1. Times given include clock periods known to occur before instruction issue, but do not consider register conflict conditions that might delay issue.

Except for the multiply and divide units, all functional units permit new instructions to enter them every clock period. A new instruction may enter the multiply unit in any clock period, provided there was no operation initiated in the preceding clock period. A new instruction can enter the divide unit two clock periods prior to completion of a previous divide operation. Once an instruction issues to a functional unit, it is executed in a fixed amount of time. No delays are possible.

Times given for instructions 01 to 07 and 50 to 57 do not consider memory conflict conditions or SAS back-up conditions caused by bank conflicts.

2. Execution of Block Copy instructions (011 and 012) will be delayed until the following conditions are satisfied:

a. All operating registers are free.

b. No SCM bank conflicts exist.

c. LCM is not busy.

3. A delay will occur during instructions 011, 012, and 013 when an I/O section word request is made. A minimum delay of one clock period is required to enter the I/O word address in the address stream to the SAS. An additional delay will occur if the I/O reference causes a bank conflict in SCM.

4. A delay will occur in the execution of the Exchange Exit instruction (013) until two conditions are satisfied:

a. All operating registers are free.

b. No SCM bank conflicts exist.

5. The Read LCM and Write LCM instructions (014 and 015) will not issue until three conditions are satisfied.

a. LCM is not busy.

b. Xj register is free.

c. Xk register is free.

6. A Read LCM instruction (014) for a word already residing in an LCM bank operand register as a result of a previous instruction will require three clock periods. For a word not currently residing in one of the LCM bank operand registers, the instruction requires 14 clock periods.

7. The Reset Buffer instructions and Read Channel Status instructions (016 and 017) will not issue and begin execution until the required B registers are free.

8. Jump instruction 02i0K will not begin execution until the Bi register is free. Instruction execution will also be delayed if an instruction fetch is in process.

9. The execution of a branch instruction (030 to 037, 04ijk, 05ijk, 06ijk and 07ijk) will be delayed if an instruction fetch is in process.

10. Instructions 10 to 47 and 60 to 77 will not issue until the following conditions are satisfied:

a. The required A, B, and X registers are free.

b. X and B register input paths will be free during the required clock period.

c. No SAS backup condition exists.

d. The multiply unit is free (instructions 40, 41, and 42 only).

e. The divide unit is free (instructions 44 and 45 only).

11. Instructions 50 to 57 will not issue until the following conditions are satisfied:

a. The required A, B, and X registers are free.

b. No SAS backup condition exists.

12. A delay may occur in the execution of the Return Jump instruction (0100K) if the instruction stack control has requested one or more instruction words that have not arrived at the instruction stack (likely to occur in straight line coding).

CENTRAL PROCESSOR INSTRUCTIONS

MNEMONIC CODE	INSTRUCTION CODE	NAME	EXECUTION TIME (Clock Periods)	FUNCTIONAL UNIT
ES	00000	Error exit to EEA	-	-
RJ	0100K	Return jump to K	Min 13*	-
RL	011jK	Block copy K + (Bj) words from LCM to SCM	Min = N + 15**	
WL	012jK	Block copy K + (Bj) words from SCM to LCM	Min = N + 11**	-
MC	01300	Exchange exit to NEA if exit flag clear	Min = 28	-
ME	013jK	Exchange exit to K +(Bj) if exit flag set	Min = 28	-
RX	014jK	Read LCM at (Xk) to Xj	3, 14*	-
WX	015jK	Write (Xj) into LCM at (Xk)	3	-
RI	0160k	Reset channel (Bk) input buffer if j = 0	4	-
IB	016jk	Read channel (Bk) input status to Bj if j ± 0	3	-
TB	016j0	Set Bj to current clock time		
RO	0170k	Reset channel (Bk) output buffer if j = 0	16	-
OB	017jk	Read channel (Bk) output status to Bj if j ± 0	3	-
JP	02i0K	Jump to K + (Bi)	Min 3 (in stack jump) Min 11 (out of stack jump)	
ZR	030jK	Branch to K if (Xj) = 0	Min 2 (branch fall through) Min 3 (branch in stack) Min 11 (branch out of stack)	-
NZ	031jK	Branch to K if (Xj) ±0	Same as above	-
PL	032jK	Branch to K if (Xj) positive		-
NG	033jK	Branch to K if (Xj) negative		-
IR	034jK	Branch to K if (Xj) in range		-

*Refer to Timing Notes

**N = Number of words in the block

MNE MONIC CODE	IN- STRUC- TION CODE	NAME	EXECU- TION TIME (Clock Periods)	FUNC- TIONAL UNIT
OR	035jK	Branch to K if (Xj) not in range	Same as above	-
DF	036jK	Branch to K if (Xj) definite		-
ID	037jK	Branch to K if (Xj) indefinite		-
EQ	04ijK	Branch to K if (Bi) = (Bj)	Min 2 (branch fall through) Min 3 (branch in stack) Min 11 (branch out of stack)	-
NE	05ijK	Branch to K if (Bi) ± (Bj)	Same as above	-
GE	06ijK	Branch to K if (Bi) ≥ (Bj)		-
LT	07ijK	Branch to K if (Bi) < (Bj)		-
BX	10ij0	Copy (Xj) to Xi		Boo- lean
BX	11ijk	Logical product of (Xj) and (Xk) to Xi	2	Boo- lean
BX	12ijk	Logical sum of (Xj) plus (Xk) to Xi	2	Boo- lean
BX	13ijk	Logical difference of (Xj) minus (Xk) to Xi	2	Boo- lean
BX	14i0k	Copy complement of (Xk) to Xi	2	Boo- lean
BX	15ijk	Logical product of (Xj) and comp (Xk) to Xi	2	Boo- lean
BX	16ijk	Logical sum (Xj) plus comp (Xk) to Xi	2	Boo- lean
BX	17ijk	Logical difference of (Xj) minus comp (Xk) to Xi	2	Boo- lean
LX	20ijk	Left shift (Xi) by jk	2	Shift
AX	21ijk	Right shift (Xi) by jk	2	Shift
LX	22ijk	Left shift (Xk) by (Bj) to Xi	2	Shift
AX	23ijk	Right shift (Xk) by (Bj) to Xi	2	Shift
NX	24ijk	Normalize (Xk) to Xi and Bj	3	Nor- malize
ZX	25ijk	Round and normal- ize (Xk) to Xi and Bj	3	Nor- malize
UX	26ijk	Unpack (Xk) to Xi and Bj	2	Boo- lean

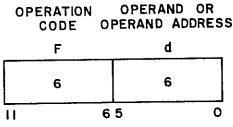
MNE-MONIC CODE	IN-STRUC-TION CODE	NAME	EXECU-TION TIME (Clock Periods)	FUNC-TIONAL UNIT
PX	27ijk	Pack (Xk) and (Bj) to Xi	2	Boo-lean
FX	30ijk	Floating sum of (Xj) plus (Xk) to Xi	4	Float-ing Add
FX	31ijk	Floating difference of (Xj) minus (Xk) to Xi	4	Float-ing Add
DX	32ijk	Floating DP sum of (Xj) plus (Xk) to Xi	4	Float-ing Add
DX	33ijk	Floating DP differ-ence of (Xj) minus (Xk) to Xi	4	Float-ing Add
RX	34ijk	Round floating sum of (Xj) plus (Xk) to Xi	4	Float-ing Add
RX	35ijk	Round floating dif-ference of (Xj) mi-nus (Xk) to Xi	4	Float-ing Add
IX	36ijk	Integer sum of (Xj) plus (Xk) to Xi	2	Long Add
IX	37ijk	Integer difference of (Xj) minus (Xk) to Xi	2	Long Add
FX	40ijk	Floating product of (Xj) times (Xk) to Xi	5	Multiply
RX	41ijk	Round floating product of (Xj) times (Xk) to Xi	5	Multiply
DX	42ijk	Floating DP prod-uct of (Xj) times (Xk) to Xi	5	Multiply
MX	43ijk	Form mask of jk bits to Xi	2	Shift
FX	44ijk	Floating divide (Xj) by (Xk) to Xi	20	Divide
RX	45ijk	Round floating di-vide (Xj) by (Xk) to Xi	20	Divide
NO	46000	Pass	2	-
CX	47i0k	Population count of (Xk) to Xi	2	Popu-lation Count
SA	50ijK	Increment (Aj) plus K to Ai	Min 2 (no storage reference) Min 8 (storage reference)	Incre-ment
SA	51ijK	Increment (Bj) plus K to Ai	Same as above	Incre-ment
SA	52ijK	Increment (Xj) plus K to Ai		Incre-ment
SA	53ijk	Increment (Xj) plus (Bk) to Ai		Incre-ment
SA	54ijk	Increment (Aj) plus (Bk) to Ai	Min 2 (no storage reference) Min 8 (storage reference)	Incre-ment

MNE-MONIC CODE	IN-STRUC-TION CODE	NAME	EXECU-TION TIME (Clock Periods)	FUNC-TIONAL UNIT
SA	55ijk	Increment (Aj) minus (Bk) to Ai	Same as above	Incre-ment
SA	56ijk	Increment (Bj) plus (Bk) to Ai		Incre-ment
SA	57ijk	Increment (Bj) minus (Bk) to Ai		Incre-ment
SB	60ijK	Increment (Aj) plus K to Bi	2	Incre-ment
SB	61ijK	Increment (Bj) plus K to Bi	2	Incre-ment
SB	62ijK	Increment (Xj) plus K to Bi	2	Incre-ment
SB	63ijk	Increment (Xj) plus (Bk) to Bi	2	Incre-ment
SB	64ijk	Increment (Aj) plus (Bk) to Bi	2	Incre-ment
SB	65ijk	Increment (Aj) minus (Bk) to Bi	2	Incre-ment
SB	66ijk	Increment (Bj) plus (Bk) to Bi	2	Incre-ment
SB	67ijk	Increment (Bj) minus (Bk) to Bi	2	Incre-ment
SX	70ijK	Increment (Aj) plus K to Xi	2	Incre-ment
SX	71ijK	Increment (Bj) plus K to Xi	2	Incre-ment
SX	72ijK	Increment (Xj) plus K to Xi	2	Incre-ment
SX	73ijk	Increment (Xj) plus (Bk) to Xi	2	Incre-ment
SX	74ijk	Increment (Aj) plus (Bk) to Xi	2	Incre ment
SX	75ijk	Increment (Aj) minus (Bk) to Xi	2	Incre-ment
SX	76ijk	Increment (Bj) plus (Bk) to Xi	2	Incre-ment
SX	77ijk	Increment (Bj) minus (Bk) to Xi	2	Incre-ment

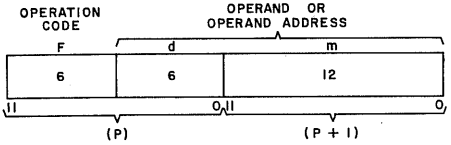
PERIPHERAL PROCESSING UNIT INSTRUCTIONS

EXPLANATION OF PERIPHERAL PROCESSOR INSTRUCTION FORMATS

An instruction may have a 12-bit or a 24-bit format. The 12-bit format has a 6-bit operation code F and a 6-bit operand or operand address d.



The 24-bit format uses the 12-bit quantity m, which is the contents of the next program address (P + 1), with d to form an 18-bit operand or operand address.



EXPLANATION OF SYMBOLS USED IN PERIPHERAL PROCESSOR INSTRUCTION LISTINGS

d	Implies d itself.
(d)	Implies the contents of d.
((d))	Implies the contents of the location specified by d.
m	Implies m itself used as an address.
m + (d)	The contents of d are added to m to form an operand (jump address).
(m + (d))	The contents of d are added to m to form the address of the operand.
dm	Implies an 18-bit quantity with d as the upper 6 bits and m as the lower 12 bits.

PERIPHERAL PROCESSOR INSTRUCTIONS

MNE-MONIC CODE	INSTRUC-TION CODE (Octal)	NAME	EXECUTION TIME (Clock Periods)
EXN	00	Error stop	-
LJM	0100	Long jump to m	10 or 15
LJM	01XX	Long jump to m + (d)	15, 20, 25
RJM	0200	Return jump to m	15 or 20
RJM	02XX	Return jump to m + (d)	20, 25, 30
UJN	03	Unconditional jump d*	8, 10
ZJN	04	Zero jump d	5
NJN	05	Nonzero jump d	5
PJN	06	Positive jump d	5
MJN	07	Negative jump d	5
SHN	10	Shift d	Minimum 6, Maximum 34
LMN	11	Logical difference d	5
LPN	12	Logical product d	5
SCN	13	Selective clear d	5
LDN	14	Load d	5
LCN	15	Load complement d	5
ADN	16	Add d	5
SBN	17	Subtract d	5
LDC	20	Load dm	10
ADC	21	Add dm	10
LPC	22	Logical product dm	10
LMC	23	Logical difference dm	10

NOTES:

1. Where more than one time is given, the shorter time is obtained when full use of bank phasing (back-to-back storage references to alternate banks) is made.

2. Conditional jump instructions list times for the "jump not taken" case. Add 3 or 5 clock periods for the "jump taken" case, depending on the value of d.

3. For the 10 (shift) instruction: Minimum time is required if the shift count<3; for shift counts > 3, add 1 clock period per shift beyond 3 to the minimum time.

PSN	24	Pass	5
PSN	25	Pass	
PSN	26	Pass	
PSN	27	Pass	
LDD	30	Load (d)	15
ADD	31	Add (d)	15
SBD	32	Subtract (d)	15
LMD	33	Logical difference (d)	15
STD	34	Store (d)	15
RAD	35	Replace add (d)	25
AOD	36	Replace add one (d)	25
SOD	37	Replace subtract one (d)	25
LDI	40	Load ((d))	15, 25
ADI	41	Add ((d))	15, 25
SBI	42	Subtract ((d))	15, 25
LMI	43	Logical difference ((d))	15, 25

*d must not be 00 or 77.

MNE-MONIC CODE	INSTRUC-TION CODE (Octal)	NAME	EXECUTION TIME (Clock Periods)
STI	44	Store ((d))	15, 25
RAI	45	Replace add ((d))	25, 35
AOI	46	Replace add one ((d))	25, 35
SOI	47	Replace subtract one ((d))	25, 35
LDM	5000	Load (m)	20
LDM	50XX	Load (m + (d))	20, 30
ADM	5100	Add (m)	20
ADM	51XX	Add (m + (d))	20, 30
SBM	5200	Subtract (m)	20
SBM	52XX	Subtract (m + (d))	20, 30
LMM	5300	Logical difference (m)	20
LMM	53XX	Logical difference (m + (d))	20, 30
STM	5400	Store (m)	20
STM	54XX	Store (m + (d))	20, 30
RAM	5500	Replace add (m)	30
RAM	55XX	Replace add (m + (d))	30, 40
ADM	5600	Replace add one (m)	30
ADM	56XX	Replace add one (m + (d))	30, 40
SOM	5700	Replace subtract one (m)	30
SOM	57XX	Replace subtract one (m + (d))	30, 40
FIM	60	Jump on input word flag	10*
EIM	61	Jump if no input word flag	10
IRM	62	Jump on input record flag	10
NIM	63	Jump if no input record flag	10
FOM	64	Jump on output word flag	10
EOM	65	Jump if no output word flag	10
ORM	66	Jump on output record flag	10
NOM	67	Jump if no output record flag	10
IAN	70	Input to A from channel d	9**

*Jump instruction times are for the "jump not taken" case. The "jump taken" execution time is identical if the jump is to an alternate bank. If the jump is taken to the same bank, add 5 clock periods.

**Assume input channel d word flag is set; if not set, add the time waiting for flag to set.

MNE-MONIC CODE	IN-STRUC-TION CODE	NAME	EXECUTION TIME (Clock Periods)
IAM	71	Input (A) words to m from channel d	+
OAN	72	Output from A on channel d	9++
OAM	73	Output (A) words from m on channel d	+
RFN	74	Output record flag on channel d	5
PSN	75	Pass	5
PSN	76	Pass	5
ESN	77	Error Stop	- (restart only by a Dead Start)

+Timing for these instructions are sample times only for various cases. Assumptions made for each case are stated on the following page.

++Assumes output channel d word flag is clear; if not clear, add the time waiting for flag to clear.

71 INSTRUCTION

Case 1: Assume:

a. a block input terminated by a record flag rather than by decrementing (A) to zero.

b. a 2 clock period response time between the resume and the word flag.

c. a 3-word block followed by a record flag.

d. the channel d input word flag is set at instruction initiation, and

e. the first data reference is to the alternate storage bank.

Execution Time = 42 clock periods.

Case 2: Assume:

a. a block input terminated by reducing (A) to zero.

b. same response as in item b, Case 1.

c. a count of 2 in the A register, and

d. items d and e in Case 1 are true.

Execution Time = 24 clock periods.

Case 3: Assume:

a. a block input initiated with (A) = zero.

Execution Time = 10 clock periods.

73 INSTRUCTION

Case 1: Assume:

a. a count of 3 in the A register.

b. the device has a 2 clock period response time from receipt of word pulse to transmission of resume pulse.

c. the output channel d word flag is clear, and

d. the first word of the block is read from the alternate storage bank.

Execution Time = 34 clock periods.

Case 2: Assume:

a. a block output initiated with (A) = zero.

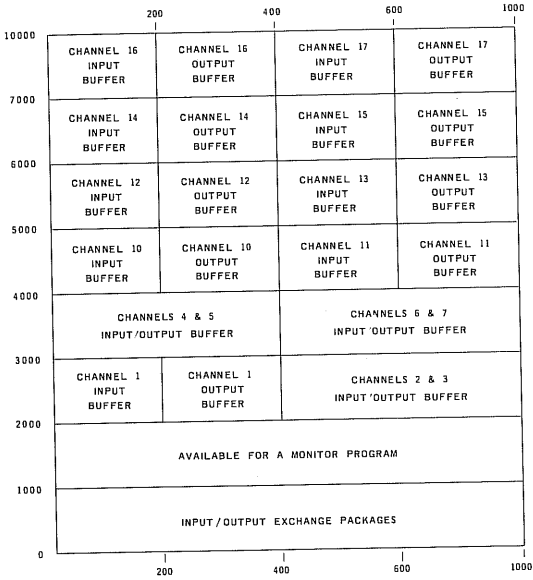
Execution Time = 10 clock periods.

EXCHANGE PACKAGE

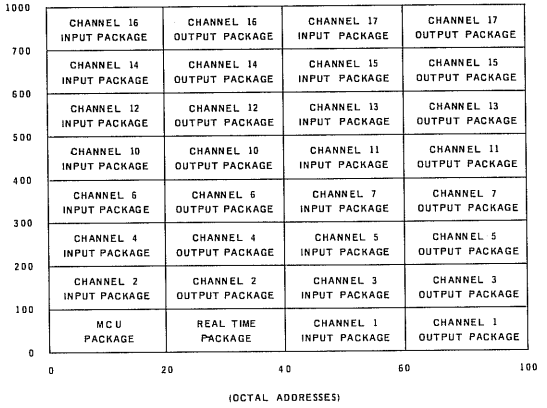
SCM LOCATION			
n +	P	A0	BPA
n + 1	RAS	A1	B1
n + 2	FLS	A2	B2
n + 3	PSD	A3	B3
n + 4	RAL	A4	B4
n + 5	FLL	A5	B5
n + 6	NEA	A6	B6
n + 7	EEA	A7	B7
n + 8	X0		
n + 9	X1		
n + 10	X2		
n + 11	X3		
n + 12	X4		
n + 13	X5		
n + 14	X6		
n + 15	X7		

A0 - A7	A Registers
B1 - B7	B Registers
X0 - X7	X Registers
P	Program Address Register
BPA	Breakpoint Address
RAS	Reference Address – Small Core Memory
FLS	Field Length – Small Core Memory
PSD	Program Status Designations
RAL	Reference Address – Large Core Memory
FLL	Field Length – Large Core Memory
NEA	Normal Exit Address
EEA	Error Exit Address

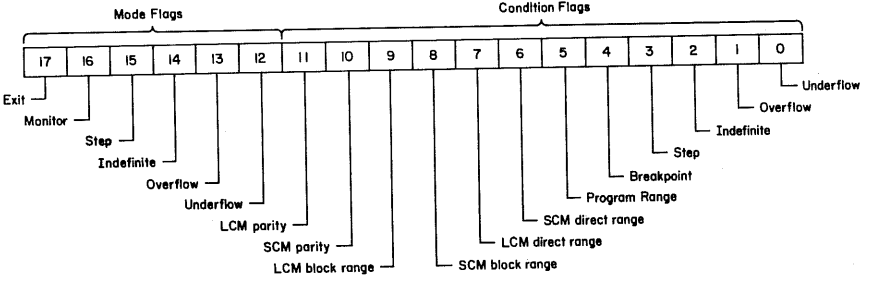
INPUT / OUTPUT BUFFER AREAS IN SCM



INPUT/OUTPUT EXCHANGE AREAS IN SCM

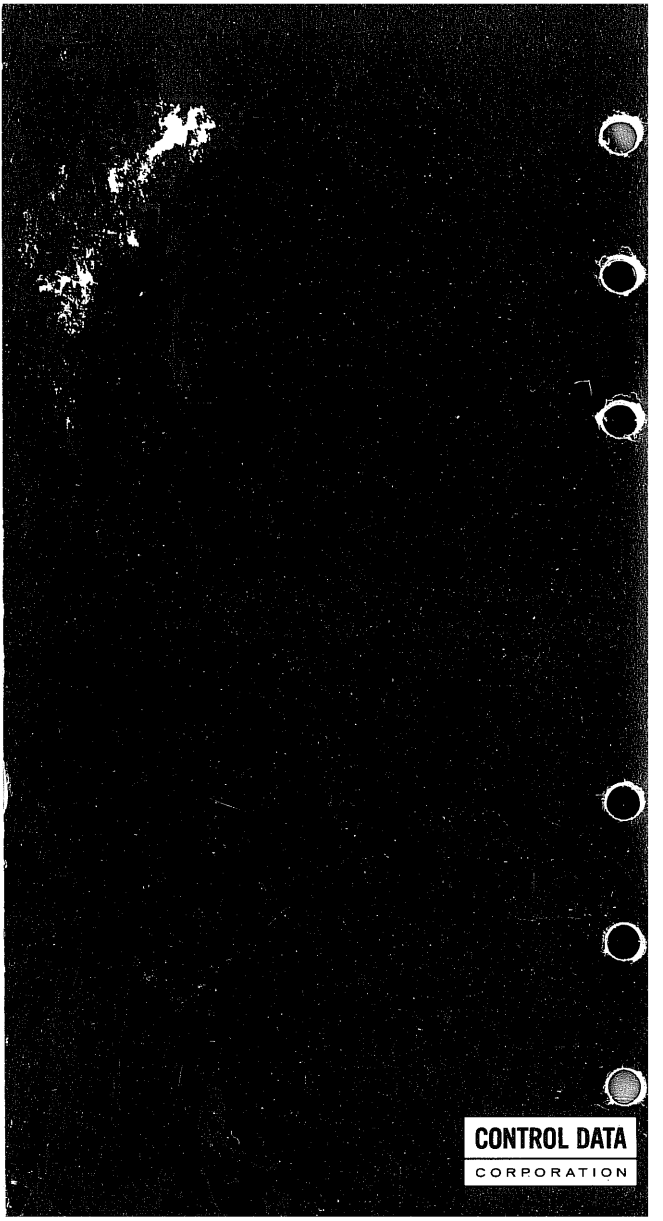


PROGRAM STATUS DESIGNATIONS REGISTER



GLOSSARY

BPA	Breakpoint Address
Clock Period	27.5 nanoseconds
CPU	Central Processing Unit
EEA	Error Exit Address
FLL	Field Length - LCM
FLS	Field Length - SCM
LCM	Large Core Memory
MCU	Maintenance Control Unit
NEA	Normal Exit Address
P	Program Address Register
PPU	Peripheral Processing Units
PSD	Program Status Designations
RAS	Reference Address - SCM
RAL	Reference Address - LCM
SAS	Storage Address Stack
SCM	Small Core Memory
SWS	Storage Word Stack


CONTROL DATA
CORPORATION