3100
3200

Control Data®
3100 AND 3200
COMPUTER SYSTEMS
INSTRUCTION CODES

DAVID E. LEE
9/1/69.

3100
3200

Control Data®
3100 AND 3200
COMPUTER SYSTEMS
INSTRUCTION CODES

60150200	**Record of Revisions**
REVISION	NOTES
A	Publication Change Order 12544 which does not advance
(1-27-66)	the Product Designation. Pages 1, 2, 11, 16 and 25
	revised. This edition obsoletes all previous editions.
B	Publications Change Order 16022 updates manual through
(3-15-67)	MDR45 (3200), MDR35 (3100) and incorporates
	miscellaneous corrections. This edition obsoletes all
	previous editions.

Pub. No. 60150200
March, 1967

Printed in the United States of America

Address comments concerning this manual to:

Control Data Corporation
Technical Publications Department
4201 North Lexington Avenue
St. Paul, Minnesota 55112

CONTENTS

NUMERICAL LISTING

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
00.0	HLT	halt
00.1	SJ1	selective jump; jump if key 1 is set
00.2	SJ2	selective jump; jump if key 2 is set
00.3	SJ3	selective jump; jump if key 3 is set
00.4	SJ4	selective jump; jump if key 4 is set
00.5	SJ5	selective jump; jump if key 5 is set
00.6	SJ6	selective jump; jump if key 6 is set
00.7	RTJ	return jump
01	UJP, I	unconditional jump
02.0	NOP	(no operation)
02.1-3	IJI	index jump, incremental
02.4	NOP	(no operation)
02.5-7	IJD	index jump, decremental
03.0	AZJ, EQ	compare A with zero; jump if (A) = 0
03.1	AZJ, NE	compare A with zero; jump if (A) $\neq$ 0
03.2	AZJ, GE	compare A with zero; jump if (A) $\geq$ 0
03.3	AZJ, LT	compare A with zero; jump if (A) < 0
03.4	AQJ, EQ	compare A with Q; jump if (A) = (Q)
03.5	AQJ, NE	compare A with Q; jump if (A) $\neq$ (Q)
03.6	AQJ, GE	compare A with Q; jump if (A) $\geq$ (Q)
03.7	AQJ, LT	compare A with Q; jump if (A) < (Q)
04.0	ISE	skip next instruction if y = 0

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
04.1-3	ISE	skip next instruction if $(B^b) = y$
04.4	ASE, S	skip next instruction if (A) = y, sign extended
04.5	QSE, S	skip next instruction if (Q) = y, sign extended
04.6	ASE	skip next instruction if $(A)_{15} = y$
04.7	QSE	skip next instruction if $(Q)_{15} = y$
05.0	ISG	skip next instruction if y = 0
05.1-3	ISG	skip next instruction if $(B^b) \geq y$
05.4	ASG, S	skip next instruction if $(A) \geq y$, sign extended
05.5	QSG, S	skip next instruction if $(Q) \geq y$, sign extended
05.6	ASG	skip next instruction if $(A) \geq y$
05.7	QSG	skip next instruction if $(Q) \geq y$
06	MEQ	masked equality search
07	MTH	masked threshold search
10.0	SSH	storage shift
10.1-3	ISI	index skip, incremental
10.4	ISD	skip next instruction if y = 0
10.5-7	ISD	index skip, decremental
11.0-3	ECHA	enter character address into A
11.4-7	ECHA, S	enter character address, sign extended, into A

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
12.0-3	SHA	shift A
12.4-7	SHQ	shift Q
13.0-3	SHAQ	shift AQ
13.4-7	SCAQ	scale AQ
14.0	NOP	(no operation)
14.1-3	ENI	enter index with y
14.4	ENA, S	enter A with y, sign extended
14.5	ENQ, S	enter Q with y, sign extended
14.6	ENA	enter A with y
14.7	ENQ	enter Q with y
15.0	NOP	(no operation)
15.1-3	INI	increase index by y
15.4	INA, S	increase A by y, sign extended
15.5	INQ, S	increase Q by y, sign extended
15.6	INA	increase A by y
15.7	INQ	increase Q by y
16.0	NOP	(no operation)
16.1-3	XOI	exclusive OR of B^b and y
16.4	XOA, S	exclusive OR of A and y, sign extended
16.5	XOQ, S	exclusive OR of Q and y, sign extended
16.6	XOA	exclusive OR of A and y
16.7	XOQ	exclusive OR of Q and y
17.0	NOP	(no operation)
17.1-3	ANI	AND of B^b and y
17.4	ANA, S	AND of A and y, sign extended
17.5	ANQ, S	AND of Q and y, sign extended
17.6	ANA	AND of A and y
17.7	ANQ	AND of Q and y

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
20	LDA,I	load A
21	LDQ,I	load Q
22	LACH	load A, character
23	LQCH	load Q, character
24	LCA,I	load A, complement
25	LDAQ,I	load AQ
26	LCAQ,I	load AQ, complement
27	LDL,I	load A, logical
30	ADA,I	add to A
31	SBA,I	subtract from A
32	ADAQ,I	add to AQ
33	SBAQ,I	subtract from AQ
34	RAD,I	replace add
35	SSA,I	selectively set A
36	SCA,I	selectively complement A
37	LPA,I	logical product A
40	STA,I	store A
41	STQ,I	store Q
42	SACH	store A, character
43	SQCH	store Q, character
44	SWA,I	store word address
45	STAQ,I	store AQ
46	SCHA,I	store character address
47	STI,I	store index
50	MUA,I	multiply A
51	DVA,I	divide A
52	CPR,I	compare (within limits test)
53.00	TIA	clear A
53.(1-3)0	TIA	transfer (B^b) to A
53.40	NOP	(no operation)
53.(5-7)0	TAI	transfer (A) to B^b
53.(0-3)1	TMQ	transfer (Register v) to Q

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
53.(4-7)1	TQM	transfer (Q) to Register v
53.(0-3)2	TMA	transfer (Register v) to A
53.(4-7)2	TAM	transfer (A) to Register v
53.03	NOP	(no operation)
53.(1-3)3	TMI	transfer (Register v) to B^b
53.43	TIM	clear Register v
53.(5-7)3	TIM	transfer (B^b) to Register v
53.04	AQA	transfer (A) + (Q) to A
53.(1-3)4	AIA	transfer (A) + (B^b) to A
53.44	NOP	(no operation)
53.(5-7)4	IAI	transfer (A) + (B^b) to B^b
54	LDI,I	load index
55.0	NOP	(no operation)
55.1*	ELQ	transfer (E_L) to Q
55.2*	EUA	transfer (E_U) to A
55.3*	EAQ	transfer (E) to AQ
55.4	NOP	(no operation)
55.5*	QEL	transfer (Q) to E_L
55.6*	AEU	transfer (A) to E_U
55.7*	AQE	transfer (AQ) to E
56*	MUAQ,I	multiply AQ
57*	DVAQ,I	divide AQ
60*	FAD,I	FP addition to AQ
61*	FSB,I	FP subtraction from AQ
62*	FMU,I	FP multiplication of AQ
63*	FDV,I	FP division of AQ
64**	LDE	load E_D
65**	STE	store E_D

*Trapped instruction if double-precision floating point option is not available.

**Trapped instruction if BCD option is not available.

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
66**	ADE	add to (E_D)
67**	SBE	subtract from (E_D)
70.0-3**	SFE	shift E
70.4**	EZJ, EQ	E zero jump; jump if (E) = 0
70.5**	EZJ, LT	E zero jump; jump if (E) < 0
70.6**	EOJ	E overflow jump
70.7**	SET	set D register
71.0-3	SRCE	search for character equality
	SRCN	search for character inequality
71.4-7	SRCE, INT	search for character equality, interrupt upon completion
	SRCN, INT	search for character inequality, interrupt upon completion
72.0-3	MOVE	move l characters from r to s
72.4-7	MOVE, INT	move l characters from r to s, interrupt upon completion
73.0-3	INPC, INT B, H	character-addressed input to storage
73.4-7	INAC, INT	input character to A
74.0-3	INPW, INT, B, N	word-addressed input to storage
74.4-7	INAW, INT	input word to A
75.0-3	OUTC, INT B, H	character-addressed output from storage
75.4-7	OTAC, INT	output character from A
76.0-3	OUTW, INT B, N	word-addressed output from storage
76.4-7	OTAW, INT	output word from A

**Trapped instruction if BCD option is not available.

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
77.0	CON	connect
77.1	SEL	select function
77.2ch, x; x = 0	COPY	copy external status
77.2ch, x; x ≠ 0	EXS	sense external status
77.3ch, x; x = 0	CINS	copy internal status
77.3ch, x; x ≠ 0	INS	sense internal status
77.4	INTS	sense interrupt
77.50	INCL	clear interrupt
77.51	IOCL	clear I/O, typewriter, and Search/Move
77.511*	CILO	lockout external interrupts during 'ch' busy
77.512	CLCA	clear channel activity
77.52	SSIM	selectively set interrupt mask register
77.53	SCIM	selectively clear interrupt mask register
77.57	IAPR	interrupt associated processor
77.60	PAUS	pause
77.61**	PRP	priority pause
77.70	SLS	selective stop
77.71	SFPF	set floating point fault
77.72	SBCD	set BCD fault
77.73	DINT	disable interrupt control
77.74	EINT	enable interrupt control
77.75	CTI	set control typewriter input
77.76	CTO	set console typewriter output
77.77	UCS	unconditional stop

*Not available on 3104 and 3114-A/B Computers.

**Available on 3200 Computers only.

ALPHABETICAL LISTING

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
ADA, I	30	add to A
ADAQ, I	32	add to AQ
ADE**	66	add to (E_D)
AEU*	55.6	transfer (A) to E_U
AIA	53.(1-3)4	transfer (A) + (B^b) to A
ANA	17.6	AND of A and y
ANA, S	17.4	AND of A and y, sign extended
ANI	17.1-3	AND of B^b and y
ANQ	17.7	AND of Q and y
ANQ, S	17.5	AND of Q and y, sign extended
AQA	53.04	transfer (A) + (Q) to A
AQE	55.7	transfer (AQ) to E
AQJ, EQ	03.4	compare A with Q; jump if (A) = (Q)
AQJ, GE	03.6	compare A with Q; jump if (A) $\geq$ (Q)
AQJ, LT	03.7	compare A with Q; jump if (A) < (Q)
AQJ, NE	03.5	compare A with Q; jump if (A) $\neq$ (Q)
ASE	04.6	skip next instruction if (A) = y
ASE, S	04.4	skip next instruction if (A) = y, sign extended
ASG	05.6	skip next instruction if (A) $\geq$ y
ASG, S	05.4	skip next instruction if (A) $\geq$ y, sign extended

*Trapped instruction if double-precision floating point option is not available.

**Trapped instruction if BCD option is not available.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
AZJ,EQ	03.0	compare A with zero; jump if (A) = 0
AZJ,GE	03.2	compare A with zero; jump if (A) $\geq$ 0
AZJ,LT	03.3	compare A with zero; jump if (A) $<$ 0
AZJ,NE	03.1	compare A with zero; jump if (A) $\neq$ 0
CILO**	77.511	lockout external interrupts during 'ch' busy
CINS	77.3ch,x; x = 0	copy internal status
CLCA	77.512	clear channel activity
CON	77.0	connect
COPY	77.2ch,x; x = 0	copy external status
CPR,I	52	compare (within limits test)
CTI	77.75	set console typewriter input
CTO	77.76	set console typewriter output
DINT	77.73	disable interrupt control
DVA,I	51	divide A
DVAQ,I*	57	divide AQ
EAQ*	55.3	transfer (E) to AQ
ECHA	11.0-3	enter character address into A
ECHA,S	11.4-7	enter A with 17-bit character address, sign extended
EINT	77.74	enable interrupt control
ELQ*	55.1	transfer (E_L) to Q
ENA	14.6	enter A with y
ENA,S	14.4	enter A with y, sign extended

*Trapped instruction if double-precision floating point option is not available.

**Not available on 3104 and 3114-A/B Computers.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
ENI	14.1-3	enter index with y
ENQ	14.7	enter Q with y
ENQ, S	14.5	enter Q with y, sign extended
EOJ**	70.6	E overflow jump
EUA*	55.2	transfer (E_U) to A
EXS	77.2ch, x; $x \neq 0$	sense external status
EZJ, EQ**	70.4	E zero jump; jump if (E) = 0
EZJ, LT**	70.5	E zero jump; jump if (E) < 0
FAD, I*	60	FP addition to AQ
FDV, I*	63	FP division of AQ
FMU, I*	62	FP multiplication of AQ
FSB, I*	61	FP subtraction from AQ
HLT	00.0	halt
IAI	53.(5-7)4	transfer (A) + (B^b) to B^b
IAPR	77.57	interrupt associated processor
IJD	02.5-7	index jump, decremental
IJI	02.1-3	index jump, incremental
INA	15.6	increase (A) by y
INA, S	15.4	increase (A) by y, sign extended
INAC, INT	73.4-7	input character to A
INAW, INT	74.4-7	input word to A
INCL	77.50	clear interrupt
INI	15.1-3	increase index by y

*Trapped instruction if double-precision floating point option is not available.

**Trapped instruction if BCD option is not available.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
INPC, INT, B, H	73.0-3	character-addressed input to storage
INPW, INT, B, N	74.0-3	word-addressed input to storage
INQ	15.7	increase Q by y
INQ, S	15.5	increase Q by y, sign extended
INS	77.3ch, x; x ≠ 0	sense internal status
INTS	77.4	sense interrupt
IOCL	77.51	clear I/O, typewriter, and Search/Move
ISD	10.4	skip next instruction if y = 0
ISD	10.5-7	index skip, decremental
ISE	04.0	skip next instruction if y = 0
ISE	04.1-3	skip next instruction if $(B^b) = y$
ISG	05.0	skip next instruction if y = 0
ISG	05.1-3	skip next instruction if $(B^b) \geq y$
ISI	10.1-3	index skip, incremental
LACH	22	load A, character
LCA, I	24	load A, complement
LCAQ, I	26	load AQ, complement
LDA, I	20	load A
LDAQ, I	25	load AQ
LDE**	64	load E_D
LDI, I	54	load index
LDL, I	27	load A, logical
LDQ, I	21	load Q
LPA, I	37	logical product A
LQCH	23	load Q, character

**Trapped instruction if BCD option is not available.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
MEQ	06	masked equality search
MOVE,INT	72.0-3	move l characters from r to s
MTH	07	masked threshold search
MUA,I	50	multiply A
MUAQ,I*	56	multiply AQ
NOP	14	(no operation)
OTAC,INT	75.4-7	output character from A
OTAW,INT	76.4-7	output word from A
OUTC,INT, B,H	75.0-3	character-addressed output from storage
OUTW,INT, B,N	76.0-3	word-addressed output from storage
PAUS	77.60	pause
PRP**	77.61	priority pause
QEL*	55.5	transfer (Q) to E_L
QSE	04.7	skip next instruction if (Q) = y
QSE,S	04.5	skip next instruction if (Q) = y, sign extended
QSG	05.7	skip next instruction if (Q) $\geq$ y
QSG,S	05.5	skip next instruction if (Q) $\geq$ y, sign extended
RAD,I	34	replace add
RTJ	00.7	return jump
SACH	42	store A, character
SBA,I	31	subtract from A
SBAQ,I	33	subtract from AQ
SBCD	77.72	set BCD fault

*Trapped instruction if double-precision floating point option is not available.

**Available on 3200 Computers only.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
SBE**	67	subtract from (E_D)
SCA,I	36	selectively complement A
SCAQ	13.4-7	scale AQ
SCHA,I	46	store character address
SCIM	77.53	selectively clear interrupt mask register
SEL	77.1	select function
SET**	70.7	set D register
SFE**	70.0-3	shift (E)
SFPF	77.71	set floating point fault
SHA	12.0-3	shift A
SHAQ	13.0-3	shift AQ
SHQ	12.4-7	shift Q
SJ1	00.1	selective jump; jump if key 1 is set
SJ2	00.2	selective jump; jump if key 2 is set
SJ3	00.3	selective jump; jump if key 3 is set
SJ4	00.4	selective jump; jump if key 4 is set
SJ5	00.5	selective jump; jump if key 5 is set
SJ6	00.6	selective jump; jump if key 6 is set
SLS	77.70	selective stop
SQCH	43	store Q character
SRCE, INT	71	search for character equality
SRCH, INT	71	search for character inequality
SSA,I	35	selectively set A

**Trapped instruction if BCD option is not available.

MNEMONIC CODE	NUMERICAL CODE	INSTRUCTION
SSH	10.0	storage shift
SSIM	77.52	selectively set interrupt mask register
STA, I	40	store A
STAQ, I	45	store AQ
STE**	65	store E
STI, I	47	store index
STQ, I	41	store (Q)
SWA, I	44	store word address
TAI	53.(5-7)0	transfer (A) to B^b
TAM	53.(4-7)2	transfer (A) to Register v
TIA	53.(1-3)0	transfer (B^b) to A
TIM	53.(5-7)3	transfer (B^b) to Register v
TMA	53.(0-3)2	transfer (Register v) to A
TMI	53.(1-3)3	transfer (Register v) to B^b
TMQ	53.(0-3)1	transfer (Register v) to Q
TQM	53.(4-7)1	transfer (Q) to Register v
UCS	77.77	unconditional stop
UJP, I	01	unconditional jump
XOA	16.6	exclusive OR of A and y
XOA, S	16.4	exclusive OR of A and y, sign extended
XOI	16.1-3	exclusive OR of B^b and y
XOQ	16.7	exclusive OR of Q and y
XOQ, S	16.5	exclusive OR of Q and y, sign extended

**Trapped instruction if BCD option is not available.

INSTRUCTION GROUPS

1. STOPS AND JUMPS

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
00.0	HLT	halt
00.1	SJ1	selective jump; jump if key 1 is set
00.2	SJ2	selective jump; jump if key 2 is set
00.3	SJ3	selective jump; jump if key 3 is set
00.4	SJ4	selective jump; jump if key 4 is set
00.5	SJ5	selective jump; jump if key 5 is set
00.6	SJ6	selective jump; jump if key 6 is set
00.7	RTJ	return jump
01	UJP, I	unconditional jump
02.1-3	IJI	index jump; incremental
02.5-7	IJD	index jump; decremental
03.0	AZJ, EQ	compare A with zero; jump if (A) = 0
03.1	AZJ, NE	compare A with zero; jump if (A) $\neq$ 0
03.2	AZJ, GE	compare A with zero; jump if (A) $\geq$ 0
03.3	AZJ, LT	compare A with zero; jump if (A) < 0
03.4	AQJ, EQ	compare A with Q; jump if (A) = (Q)
03.5	AQJ, NE	compare A with Q; jump if (A) $\neq$ (Q)
03.6	AQJ, GE	compare A with Q; jump if (A) $\geq$ (Q)
03.7	AQJ, LT	compare A with Q; jump if (A) < (Q)
77.70	SLS	selective stop
77.77	UCS	unconditional stop

2. REGISTER OPERATIONS WITHOUT STORAGE REFERENCE

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
04.0	ISE	skip next instruction if y = 0
04.1-3	ISE	skip next instruction if (B^b) = y
04.4	ASE, S	skip next instruction if (A) = y, sign extended
04.5	QSE, S	skip next instruction if (Q) = y, sign extended
04.6	ASE	skip next instruction if (A) = y
04.7	QSE	skip next instruction if (Q) = y
05.0	ISG	skip next instruction if y = 0
05.1-3	ISG	skip next instruction if (B^b) $\geq$ y
05.4	ASG, S	skip next instruction if (A) $\geq$ y, sign extended
05.5	QSG, S	skip next instruction if (Q) $\geq$ y, sign extended
05.6	ASG	skip next instruction if (A) $\geq$ y
05.7	QSG	skip next instruction if (Q) $\geq$ y
10.1-3	ISI	index skip; incremental
10.4	ISD	skip next instruction if y = 0
10.5-7	ISD	index skip; decremental
11.0-3	ECHA	enter character address into A
11.4-7	ECHA, S	enter character address, sign extended, into A

2. REGISTER OPERATIONS WITHOUT STORAGE REFERENCE (Cont'd)

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
12.0-3	SHA	shift A
12.4-7	SHQ	shift Q
13.0-3	SHAQ	shift AQ
13.4-7	SCAQ	scale AQ
14.1-3	ENI	enter index with y
14.4	ENA, S	enter A with y, sign extended
14.5	ENQ, S	enter Q with y, sign extended
14.6	ENA	enter A with y
14.7	ENQ	enter Q with y
15.1-3	INI	increase index by y
15.4	INA, S	increase A by y, sign extended
15.5	INQ, S	increase Q by y, sign extended
15.6	INA	increase A by y
15.7	INQ	increase Q by y
16.1-3	XOI	exclusive OR of B^b and y
16.4	XOA, S	exclusive OR of A and y, sign extended
16.5	XOQ, S	exclusive OR of Q and y, sign extended
16.6	XOA	exclusive OR of A and y
16.7	XOQ	exclusive OR of Q and y
17.1-3	ANI	AND of B^b and y
17.4	ANA, S	AND of A and y, sign extended
17.5	ANQ, S	AND of Q and y, sign extended
17.6	ANA	AND of A and y
17.7	ANQ	AND of Q and y

3. STORAGE TEST

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
06	MEQ	masked equality search
07	MTH	masked threshold search
10.0	SSH	storage shift
52	CPR, I	compare (within limits test)

4. LOGICAL INSTRUCTIONS WITH STORAGE REFERENCE

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
35	SSA, I	selectively set A
36	SCA, I	selectively complement A
37	LPA, I	logical product A

5. LOAD

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
20	LDA, I	load A
21	LDQ, I	load Q
22	LACH	load A, character
23	LQCH	load Q, character
24	LCA, I	load A, complement
25	LDAQ, I	load AQ
26	LCAQ, I	load AQ, complement
27	LDL, I	load A, logical
54	LDI, I	load index

6. STORE

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
40	STA, I	store A
41	STQ, I	store Q
42	SACH	store A, character
43	SQCH	store Q, character
44	SWA, I	store word address
45	STAQ, I	store AQ
46	SCHA, I	store character address
47	STI, I	store index

7. INTER-REGISTER TRANSFER, 24-BIT PRECISION

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
53.(1-3)0	TIA	transfer (B^b) to A
53.(5-7)0	TAI	transfer (A) to B^b
53.(0-3)1	TMQ	transfer (Register v) to Q
53.(4-7)1	TQM	transfer (Q) to Register v
53.(0-3)2	TMA	transfer (Register v) to A
52.(4-7)2	TAM	transfer (A) to Register v
53.(1-3)3	TMI	transfer (Register v) to B^b
53.(5-7)3	TIM	transfer (B^b) to Register v
53.0	AQA	transfer (A) + (Q) to A
53.(1-3)4	AIA	transfer (A) + (B^b) to A
53.(5-7)4	IAI	transfer (A) + (B^b) to B^b

8. INTER-REGISTER TRANSFER, 48-BIT PRECISION*

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
55.1	ELQ	transfer (E_L) to Q
55.2	EUA	transfer (E_U) to A
55.3	EAQ	transfer (E) to AQ
55.5	QEL	transfer (Q) to E_L
55.6	AEU	transfer (A) to E_U
55.7	AQE	transfer (AQ) to E_D

9. ARITHMETIC, FIXED POINT, 24-BIT PRECISION

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
30	ADA, I	add to A
31	SBA, I	subtract from A
34	RAD, I	replace add
50	MUA, I	multiply A
51	DVA, I	divide A

10. ARITHMETIC, FIXED POINT, 48-BIT PRECISION

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
32	ADAQ, I	add to AQ
33	SBAQ, I	subtract from AQ
56*	MUAQ, I	multiply AQ
57*	DVAQ, I	divide AQ
60*	FAD, I	FP addition to AQ
61*	FSB, I	FP subtraction from AQ
62*	FMU, I	FP multiplication of AQ
63*	FDV, I	FP division of AQ

*Trapped instructions if double-precision floating point option is not available in 3100 or 3200 Computer.

11. BCD**

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
64	LDE	load E_D
65	STE	store E_D
66	ADE	add to (E_D)
67	SBE	subtract from (E_D)
70.0-3	SFE	shift E
70.4	EZJ, EQ	E zero jump; jump if (E) = 0
70.5	EZJ, LT	E zero jump; jump if (E) < 0
70.6	EOJ	E overflow jump
70.7	SET	set D register

12. SEARCH/MOVE

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
71.0-3	SRCE	search for character equality
	SRCN	search for character inequality
71.4-7	SRCE, INT	search for character equality, interrupt upon completion
	SRCN, INT	search for character inequality, interrupt upon completion
72.0-3	MOVE	move l characters from r to s
72.4-7	MOVE, INT	move l characters from r to s, interrupt upon completion

**Trapped instructions if BCD option is not available in 3100 or 3200 Computers.

13. INPUT/OUTPUT

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
73.0-3	INPC, INT, B, H	character-addressed input to storage
73.4-7	INAC, INT	input character to A
74.0-3	INPW, INT, B, N	word-addressed input to storage
74.4-7	INAW, INT	input word to A
75.0-3	OUTC, INT, B, H	character-addressed output from storage
75.4-7	OTAC, INT	output from A character
76.0-3	OUTW, INT, B, N	word-addressed output from storage
76.4-7	OTAW, INT	output word from A

14. SENSING, CONTROL AND INTERRUPT

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
77.0	CON	connect
77.1	SEL	select function
77.2ch,x; x = 0	COPY	copy external status
77.2ch,x; x ≠ 0	EXS	sense external status
77.3ch, x; x = 0	CINS	copy internal status
77.3ch, x; x ≠ 0	INS	sense internal status
77.4	INTS	sense interrupt
77.50	INCL	clear interrupt
77.51	IOCL	clear I/O, typewriter, and Search/Move
77.511*	CILO	lockout external interrupts during 'ch' busy
77.512	CLCA	clear channel activity
77.52	SSIM	selectively set interrupt mask register

*Not available on 3104 and 3114-A/B Computers.

14. SENSING, CONTROL AND INTERRUPT (Cont'd)

NUMERICAL CODE	MNEMONIC CODE	INSTRUCTION
77.53	SCIM	selectively clear interrupt mask register
77.57	IAPR	interrupt associated processor
77.60	PAUS	pause
77.61*	PRP	priority pause
77.71	SFPF	set floating point fault
77.72	SBCD	set BCD fault
77.73	DINT	disable interrupt control
77.74	EINT	enable interrupt control
77.75	CTI	set console typewriter input
77.76	CTO	set console typewriter output

*Available on 3200 Computers only.

SUPPLEMENTARY CODES

1. 3100 COMPUTER SYSTEM

INTERNAL STATUS SENSING MASK CODES

Used with 77.3 (INS) instruction

Mask Bits	Mask Codes	Condition Represented
00	0001	Parity error on channel ch
01	0002	Channel ch busy reading
02	0004	Channel ch busy writing
03	0010	External reject active on channel ch
04	0020	No-response reject active on channel ch
05	0040	Illegal write
06	0100	Channel ch preset by CON or SEL, but no reading or writing in progress
07	0200	Internal I/O channel interrupt on channel ch, upon: 1) completion of read or write operation, or 2) end of record.
08	0400	Exponent overflow/underflow fault (floating point)
09	1000	Arithmetic overflow fault (adder)
10	2000	Divide fault
11	4000	BCD fault

INTERRUPT SENSING MASK CODES

Used with 77.4 (INTS) instruction

Mask Bits	Mask Codes	Interrupt Sensing Mask Bit Assignments
00	0001	External equipment interrupt line 0 active
01	0002	1
02	0004	2

INTERRUPT SENSING MASK CODES (Cont'd)

Used with 77.4 (INTS) instruction

Mask Bits	Mask Codes	Interrupt Sensing Mask Bit Assignments
03	0010	3
04	0020	4
05	0040	5
06	0100	6
07	0200	7
08	0400	Real-time clock
09	1000	Exponent overflow/underflow & BCD faults
10	2000	Arithmetic overflow & divide faults
11	4000	Search/Move completion

INTERRUPT MASK REGISTER CODES

Used with 77.50 (INCL), 77.52 (SSIM), 77.53 (SCIM) instruction

Mask Bits	Mask Codes	Interrupt Conditions Represented
00	0001	I/O Channel 0, internal & equipment
01	0002	1
02	0004	2
03	0010	3
04	0020	(not used)
05	0040	(not used)
06	0100	(not used)
07	0200	(not used)
08	0400	Real-time clock
09	1000	Exponent overflow/underflow & BCD faults
10	2000	Arithmetic overflow & divide faults
11	4000	Search/Move completion

BLOCK CONTROL CLEARING MASK CODES

Used with 77.51 (IOCL) instruction

Mask Bits	Mask Codes	Controls Cleared
00	0001	I/O channel 0
01	0002	1
02	0004	2
03	0010	3
04	0020	(not used)
05	0040	(not used)
06	0100	(not used)
07	0200	(not used)
08	0400	Console typewriter
09	1000	(not used)
10	2000	(not used)
11	4000	Search/Move

PAUSE SENSING MASK CODES

Used with 77.6 (PAUS) instruction

Mask Bits	Mask Codes	Condition
00	0001	I/O channel 0 busy
01	0002	1
02	0004	2
03	0010	3
04	0020	(not used)
05	0040	(not used)
06	0100	(not used)
07	0200	(not used)
08	0400	Typewriter input or output in progress
09	1000	Finish FF at typewriter not set
10	2000	Repeat FF at typewriter not set
11	4000	Search or Move operation in progress

INTERRUPT CODES

Stored in lower 12 bits of address 00005

Codes	Conditions
00LCh*	External interrupt
010Ch	I/O channel interrupt
0110	Real-time clock interrupt
0111	Arithmetic overflow fault
0112	Divide fault
0113	Exponent overflow fault
0114	BCD fault
0115	Search/Move interrupt
0116	Manual interrupt
0117	Associated processor interrupt

*L = line 0-7; Ch = channel designator, 0-3

2. 3200 COMPUTER SYSTEM

INTERNAL STATUS SENSING MASK CODES

Used with 77.3 (INS) instruction

Mask Bits	Mask Codes	Condition Represented
00	0001	Parity error on channel ch
01	0002	Channel ch busy reading
02	0004	Channel ch busy writing
03	0010	External reject active on channel ch
04	0020	No-response reject active on channel ch
05	0040	Illegal write
06	0100	Channel ch preset by CON or SEL, but no reading or writing in progress
07	0200	Internal I/O channel interrupt on channel ch, upon: 1) completion of read or write operation, or 2) end of record

INTERNAL STATUS SENSING MASK CODES (Cont'd)

Used with 77.3 (INS) instruction

Mask Bits	Mask Codes	Condition Represented
08	0400	Exponent overflow fault (floating point)
09	1000	Arithmetic overflow fault (adder)
10	2000	Divide fault
11	4000	BCD fault

INTERRUPT SENSING MASK CODES

Used with 77.4 (INTS) instruction

Mask Bits	Mask Codes	Interrupt Sensing Mask Bit Assignments
00	0001	External equipment interrupt line 0 active
01	0002	1
02	0004	2
03	0010	3
04	0020	4
05	0040	5
06	0100	6
07	0200	7
08	0400	Real-time clock interrupt
09	1000	Exponent overflow or BCD fault
10	2000	Arithmetic overflow or divide fault
11	4000	Search/Move completion interrupt

INTERRUPT MASK REGISTER CODES

Used with 77.50 (INCL), 77.52 (SSIM), 77.53 (SCIM) instruction

Mask Bits	Mask Codes	Interrupt Conditions Represented
00	0001	I/O Channel 0, internal & equipment
01	0002	1
02	0004	2
03	0010	3
04	0020	4
05	0040	5
06	0100	6
07	0200	7
08	0400	Real-time clock
09	1000	Exponent overflow & BCD faults
10	2000	Arithmetic overflow & divide faults
11	4000	Search/Move completion

BLOCK CONTROL CLEARING MASK CODES

Used with 77.51 (IOCL) instruction

Mask Bits	Mask Codes	Controls Cleared
00	0001	I/O channel 0
01	0002	1
02	0004	2
03	0010	3
04	0020	4
05	0040	5
06	0100	6
07	0200	7
08	0400	Console typewriter
09	1000	unused (CILO)
10	2000	unused (CLCA)
11	4000	Search/Move

PAUSE SENSING MASK CODES

Used with 77.60 (PAUS) and 77.61 (PRP) instructions

Mask Bits	Mask Codes	Condition
00	0001	I/O channel 0 busy
01	0002	1
02	0004	2
03	0010	3
04	0020	4
05	0040	5
06	0100	6
07	0200	7
08	0400	Typewriter input or output in progress
09	1000	Finish FF at typewriter not set
10	2000	Repeat FF at typewriter not set
11	4000	Search or Move operation in progress

INTERRUPT CODES

Stored in lower 12 bits of address 00005

Codes	Conditions
00LCh*	External interrupt
010Ch	I/O channel interrupt
0110	Real-time clock interrupt
0111	Arithmetic overflow fault
0112	Divide fault
0113	Exponent overflow fault
0114	BCD fault
0115	Search/Move interrupt
0116	Manual interrupt
0117	Associated processor interrupt

*L = line 0-7; Ch = channel designator, 0-7

3. 3100/3200 CONSOLE TYPEWRITER CODES

Print-out	Case	Internal BCD Code
0	L	00
1	L	01
2	L	02
3	L	03
4	L	04
5	L	05
6	L	06
7	L	07
8	L	10
9	L	11
±	U	12
=	L	13
"	U	14
:	U	15
;	L	16
?	U	17
+	U	20
A	U or L	21
B	U or L	22
C	U or L	23
D	U or L	24
E	U or L	25
F	U or L	26
G	U or L	27
H	U or L	30
I	U or L	31
(shift to LC)		32
. (period)	U and L	33
)	U	34
' (apostrophe)	L	35
@	U	36
!	L	37

3. 3100/3200 CONSOLE TYPEWRITER CODES (Cont'd)

Print-out	Case	Internal BCD Code
- (minus)	L	40
J	U or L	41
K	U or L	42
L	U or L	43
M	U or L	44
N	U or L	45
O	U or L	46
P	U or L	47
Q	U or L	50
R	U or L	51
o (degree)	U	52
$	U	53
*	U	54
#	U	55
%	U	56
(shift to UC)		57
(space)		60
/	L	61
S	U or L	62
T	U or L	63
U	U or L	64
V	U or L	65
W	U or L	66
X	U or L	67
Y	U or L	70
Z	U or L	71
&	U	72
, (comma)	U and L	73
(	U	74
(tab)		75
(backspace)		76
(carriage return)		77

CONTROL DATA
CORPORATION
DEVELOPMENT DIVISION
4201 North Lexington Avenue St. Paul, Minnesota