2019 south ritchey street · santa ana, california 92705 · (714) 558-8211

CAL DATA
ASYNCHRONOUS CONTROLLER
(P/N C81080660)

TECHNICAL MANUAL
C21518079-X1

DOCUMENT C21518079
Revision X1
September 1975

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REVISIONS

Revision	Date	Approval	Description
X1	9/75		Preliminary edition

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SECTION 1
INTRODUCTION

1.1 SCOPE

This manual provides the information needed to understand and maintain the Cal Data Asynchronous Controller (part number C81080660) when used with the drawing package provided. The information in this manual is for the use of a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques. A basic knowledge of design principals and circuits used in small computers is assumed, hence no tutorial material of this kind is included. An understanding of the Cal Data MACROBUS is also assumed.

As a stand-alone publication, this manual has a good functional and physical description of the Asynchronous Controller, providing the information needed to understand its capabilities and features. The maintenance coverage of this manual is commensurate with the prerequisite skills and knowledge of the defined user, characteristics of the product and maintainability requirements established by Cal Data.

1.2 DOCUMENTATION

The following paragraphs define publications and conventions that support this manual.

1.2.1 Publications

Figure 1-1 illustrates the relationship between Cal Data system elements and technical publications. Controlled copies of publications are provided in accordance with the terms of the purchase contract.

1.2.2 Engineering Drawings

For maintenance purposes, this manual is supported by a drawing package that contains schematic diagrams, assembly drawings and other required engineering drawings. The drawing package is updated with the latest revision of each drawing.

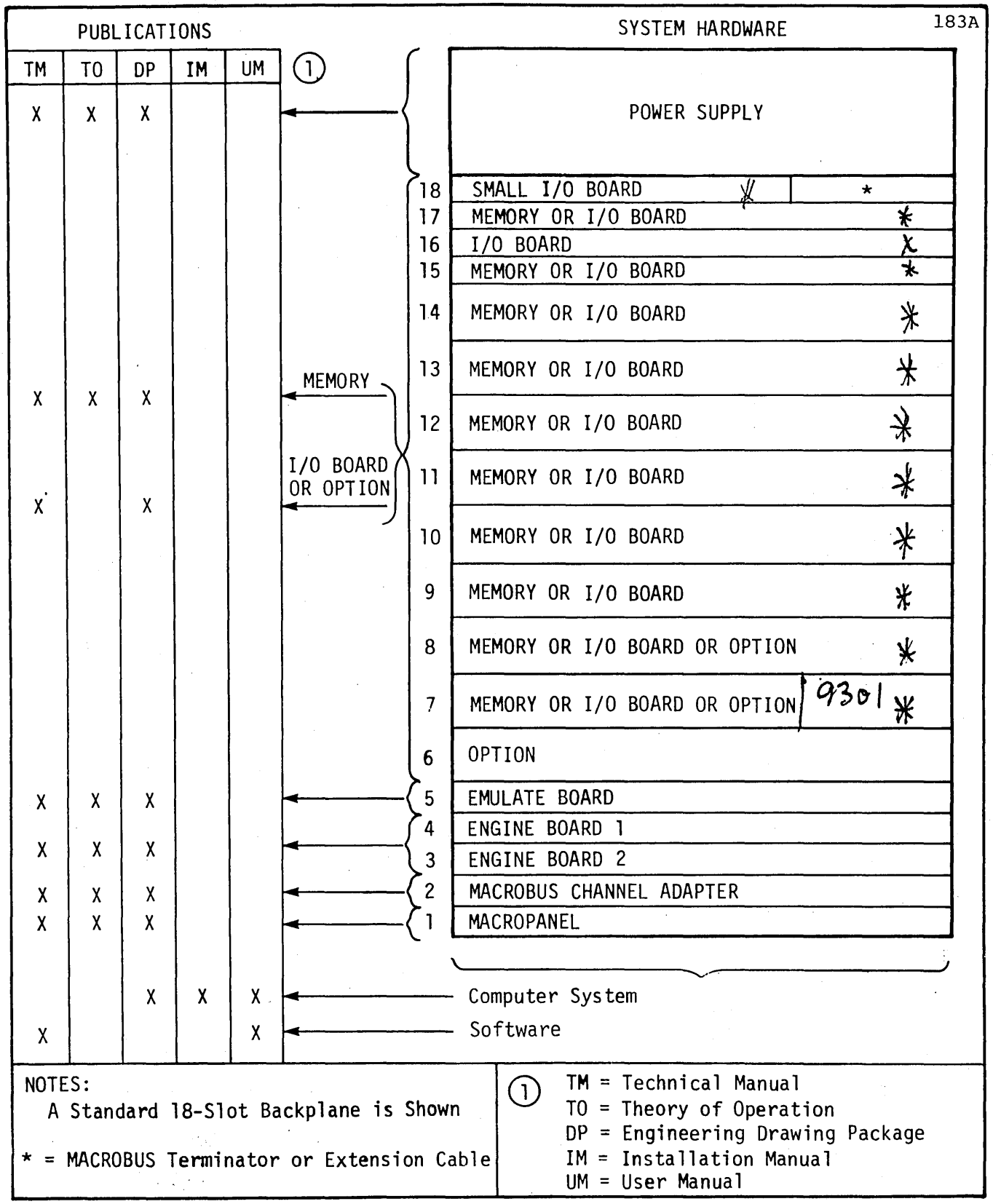


Figure 1-1. Relationship of Publications to Cal Data System Elements

* BG CARDS D Connector jumpers toward rear.

1.2.3 Abbreviations and Conventions

Table 1-1 lists the abbreviations found in this manual. Conventions used in the text of this manual include:

a. The proper names of signals are capitalized.

b. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.

c. Octal numbers are followed by a subscript eight for easy identification.

d. A colon is used to indicate a range of bits. For example, the range of Address bits A12 to A03 is written A12:A03.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data	California Data Processors
CPU	central processing unit (Engine)
I/O	input/output
modem	modulator/demodulator
cm	centimeter
°C	degrees, Celsius
cfm	cubic feet per minute
lps	liters per second
psi	pounds per square inch
mA	milliampere
µA	microampere
V	volt
Vdc	volts, direct current
I	current
kg	kilogram

SECTION 2
FUNCTIONAL DESCRIPTION

2.1 GENERAL

The Asynchronous Controller provides the interface needed to attach terminal devices to the MACROBUS (Figure 2-1). The controller is designed to transmit and receive serial, asynchronous data. The controller is capable of full-duplex or half-duplex operation. The interface with the selected device can be either current loop or EIA interface standard RS-232C.

The rest of this section is written primarily with reference to the use of a Teletype model ASR teleprinter terminal that includes a paper tape reader/punch.

The transfer of control information, data and status information between the CPU and Asynchronous Controller is by programmed instructions. The data transfers are either on a word or byte basis.

2.1.1 Data Transfer Characteristics

Data transmission between the controller and a peripheral device is in serial form, utilizing the asynchronous start/stop transmission technique. The transmission of information is in the form of start bit, data, stop bit(s). The start bit is a logical ZERO (SPACE) added to the front, while the stop element is a logic ONE (MARK) added to the end.

To allow the controller the ability to communicate with a wide variety of peripherals, options to vary the data character length, number of stop bits, parity over the data character and transmission rates have been included. Selectable transmission rates are as follows:

9600	600
4800	300
2400	150
1800	134.5
1200	~~110~~ 110

These rates are switch selectable (Section 3) with the transmit and receive rates being equal. The number of stop bits is determined by baud-rate selection:

110 baud = two stop bits
All other rates = one stop bit

Word length can be varied from five to eight bits, with parity (if selected) added after the last data bit.

Parity selection and error flags are strap selectable.

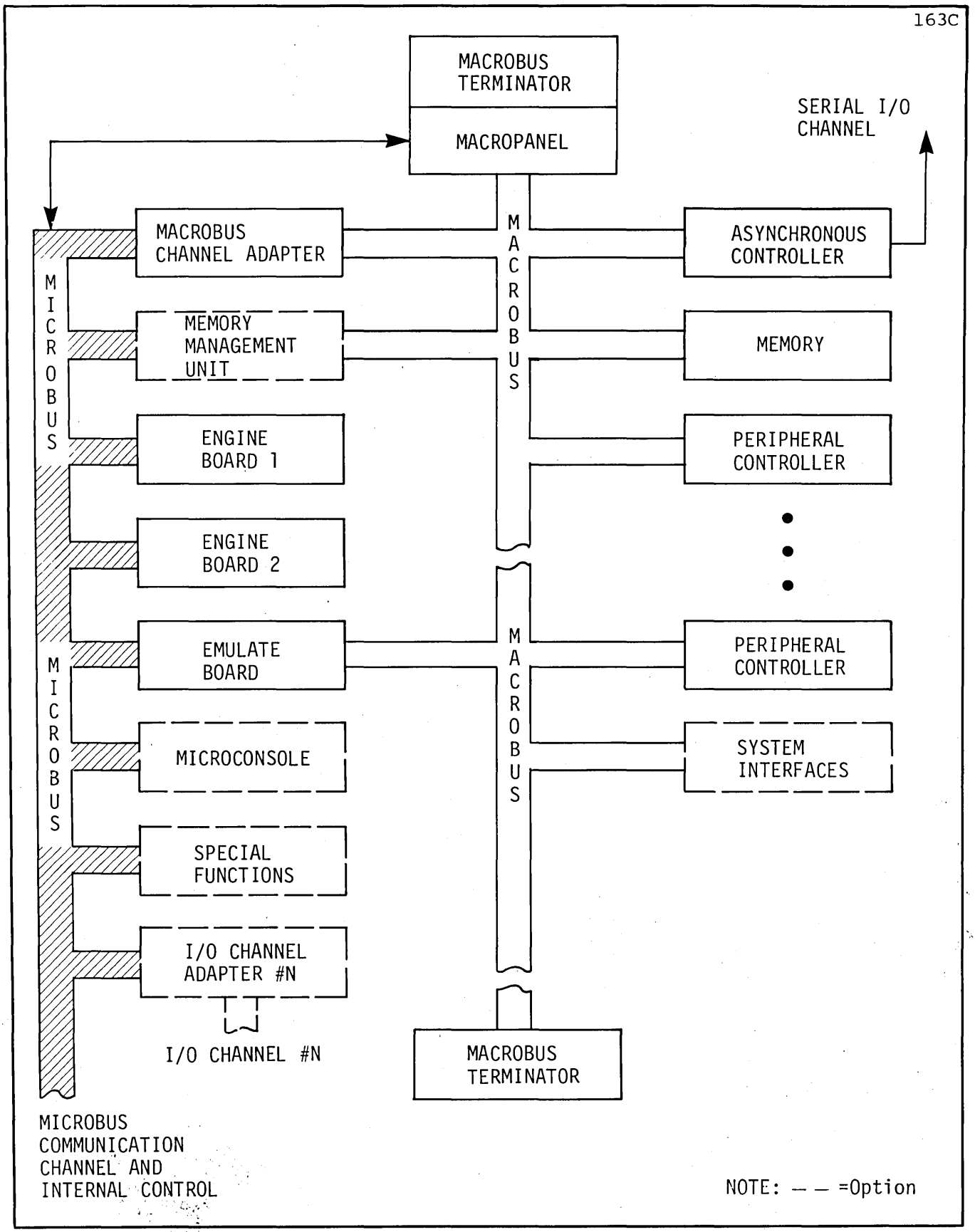


Figure 2-1. Cal Data Computer System Organization

2.2 PROGRAMMING

The Asynchronous Controller has four addressable registers that can be modified or read using any memory-reference instruction with the appropriate MACROBUS address. The MACROBUS address and name of each register are given below:

777560_8	Keyboard/reader control and status register
777562_8	Keyboard/reader data buffer
777564_8	Printer/punch control and status register
777566_8	Printer/punch data buffer

Unused "word" data transferred to the serial device are ignored. (undefined input data should be masked out by the controller drive program.)

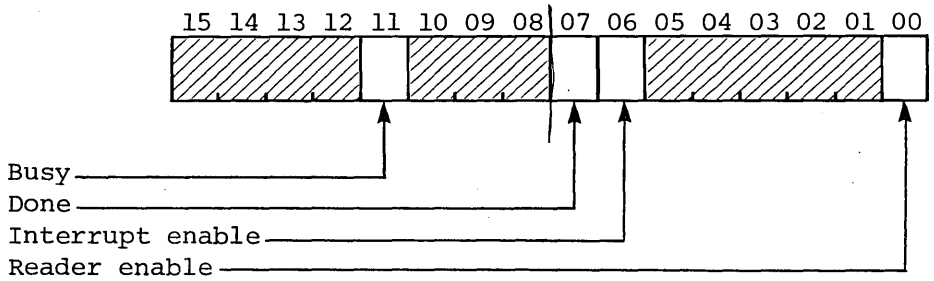
Interrupt characteristics of the controller are:

Priority level	BR4 (with the keyboard/reader wired in series above the printer/punch)
Interrupt vector:	
keyboard/reader	60_8
printer/punch	64_8

A priority header is provided for BR4.

2.2.1 Keyboard/Reader Control and Status Register

The basic keyboard/reader register (MACROBUS address 777560_8) bit structure is shown below (see 2.2.5 for data-set option):



The following paragraphs define the functions and limitations of each significant register bit. All other bits are unused in the basic configuration.

BIT 11, Busy

Bit 11 indicates that a START bit or information bits are being received by the controller. The bit is set by a MARK-to-SPACE change (start bit) on character input. Bit 11 remains set until the first stop bit (MARK) is detected.

Bit 11 is reset by INIT or the first MARK of a stop sequence.

Bit 11 can be read by the program.

Bit 07, Done

Bit 07 is set when a character is available in the reader data buffer. With bit 06 set, setting bit 07 activates the controller interrupt logic.

Bit 07 is reset by executing an instruction referencing the keyboard/reader data buffer, executing a read command (setting bit 00) or by INIT.

Bit 07 can be read by the program.

Bit 06, Interrupt Enable

Bit 06 is set to enable the controller interrupt logic.

Bit 06 is reset by INIT.

Bit 06 can be read by the program.

Bit 00, Reader Enable

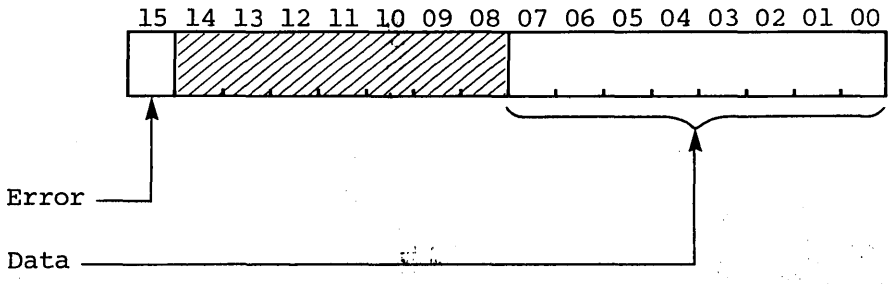
Bit 00 causes the reader to read and advance one character. The bit is not used to communicate with the keyboard.

Bit 00 is reset by INIT or by the start bit of an input bit stream.

Bit 00 cannot be read by the program.

2.2.2 Keyboard/Reader Data Buffer

The keyboard/reader buffer (MACROBUS address 777562_8) bit structure is shown below:



The following paragraphs define the functions and limitations of each significant buffer bit. All other bits are unused.

Bit 15, Error

Bit 15 is set when the deserializer detects that a data byte has not been captured by the CPU before a new byte has been assembled in the receiver register. The bit is set when the first stop bit is a SPACE

after assembly of a character. Bit 15 is also set if received parity is incorrect, if parity is enabled.

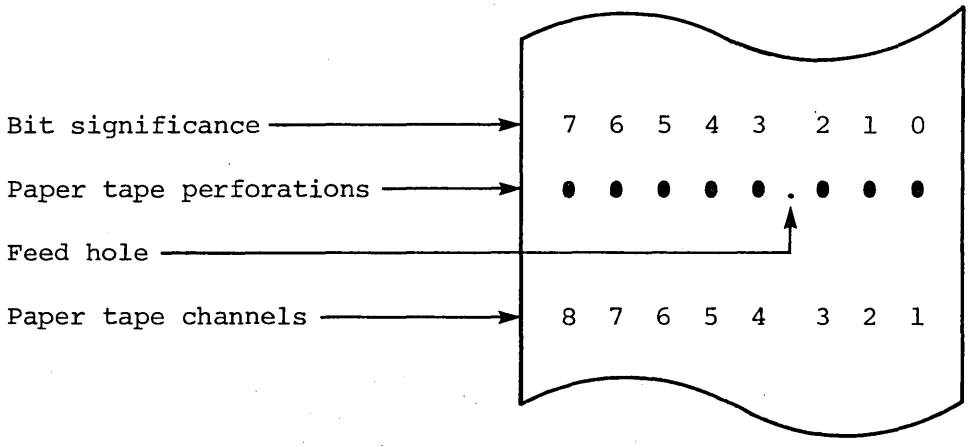
Bit 15 is reset when the buffer is read by the program.

Bit 15 can be read by the program.

Bits 07 to 00, Data

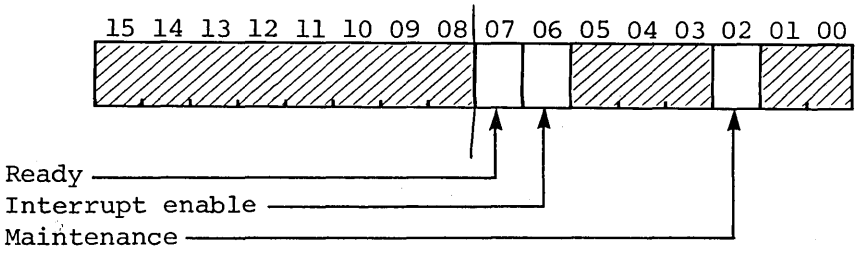
The buffer holds a data character received from the keyboard or reader to be read by the program. It is reset on receipt of a start bit for a new character.

The relationship of paper tape channels to data bits is shown below:



2.2.3 Printer/Punch Control and Status Register

The printer/punch register (MACROBUS address 777564_8) bit structure is shown below:



The following paragraphs define the functions and limitations of each significant register bit.

Bit 07, Ready

Bit 07 indicates that the printer/punch buffer is empty (printer/punch available). The bit is set whenever the buffer is reset or by INIT.

Loading the buffer resets bit 07.

Bit 07 can be read by the program.

Bit 06, Interrupt Enable

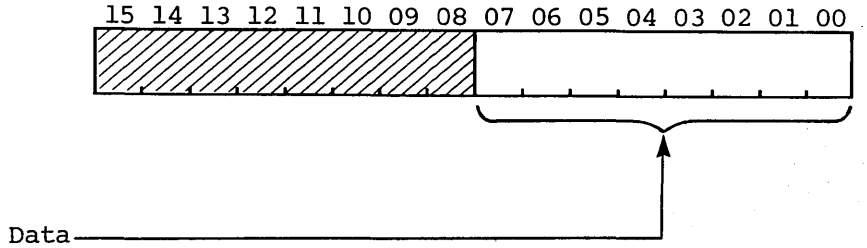
Bit 06 allows bit 07 to activate the controller interrupt logic. Bit 06 can be set, reset or read by the program or reset by INIT.

Bit 02, Maintenance

When bit 02 is enabled, the external serial input line is disabled and the serial output of the printer/punch buffer is utilized in its place. Bit 02 can be set, reset or read by the program.

2.2.4 Printer/Punch Data Buffer

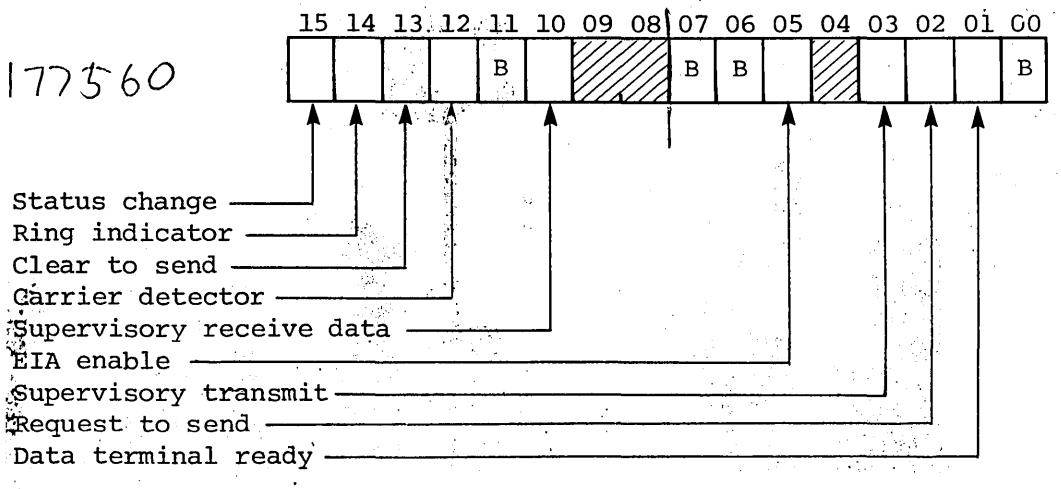
The printer/punch buffer (MACROBUS address 777566_8) bit structure is shown below:



The buffer holds a data character to be punched or printed. The buffer is loaded (but cannot be read) by the program.

2.2.5 Data-Set Option

When the controller is wired for EIA data-set operation (requiring modem control), additional bits of the keyboard/reader control and status register are used, as shown below



The following paragraphs define the functions and limitations of each optional register bit. Paragraph 2.2.1 defines the basic register bits (labeled B in the diagram above).

Bit 15, Status Change

Bit 15 is set by a MARK-to-SPACE change in the data-set control status. Status bits are:

Ring indicator
Clear to send
Carrier detect
Supervisory receive data

Setting bit 15 conditions the data-set interrupt to occur if bit 05 is set.

Bit 15 is reset by the reading of this register or by INIT.

Bit 15 can be read by the program.

Bit 14, Ring Indicator

Bit 14 is set by a MARK-to-SPACE change in the Ring Indicator signal from the data set. The RING IND signal indicates that the local data set is being "called" by a distant data set. Setting bit 14 causes bit 15 to set.

Bit 14 is reset by a SPACE-to-MARK change in RING IND.

Bit 14 can be read by the program.

Bit 13, Clear to Send

Bit 13 is set by a MARK-to-SPACE change in the Clear to Send signal from the data set. The CLR TO SND signal indicates the readiness of the data set to transmit to a distant station. Setting bit 13 causes bit 15 to be set.

Bit 13 is reset by a SPACE-to-MARK change in CLR TO SND.

Bit 13 can be read by the program.

Bit 12, Carrier Detector

Bit 12 is set by a MARK-to-SPACE change in the Carrier Detect signal from the data set. The CAR DET signal indicates the establishment of an incoming line. Setting bit 12 causes bit 15 to be set.

Bit 12 is reset by a SPACE-to-MARK change in CAR DET.

Bit 12 can be read by the program and should be sampled while data are being transmitted or received to detect loss of carrier.

Bit 10, Supervisory Receive Data

Bit 10 is set by a MARK-to-SPACE change in the Supervisory Receive Data signal from the data set. The SPRV REC DATA signal indicates reception of "reverse channel" data by the data set. Setting bit 10 causes bit 15 to be set.

Bit 10 is reset by a SPACE-to-MARK change in SPRV REC DATA.

Bit 10 can be read by the program and should be sampled when using a Bell 202 data set to reconstruct low-baud-rate serial data sent by a distant station.

Bit 05, EIA Enable

Bit 05 is set by the program to arm the EIA interrupt system. When bit 05 is set, setting bit 15 causes an interrupt request to be sent to the CPU.

Bit 05 can be set, reset or read by the program, or reset by INIT.

Bit 03, Supervisory Transmit

Bit 03 is set by the program to serialize low-baud-rate data sent to a distant station. When bit 03 is set, the Supervisory Transmit signal to the data set is placed in the SPACE state.

Bit 03 can be set, reset or read by the program, or reset by INIT.

Bit 02, Request to Send

Bit 02 is set by the program to indicate readiness of the program to transmit data on the Request to Send line. When bit 02 is set, the REQ TO SEND signal to the data set is placed in the SPACE state.

Bit 02 can be set, reset or read by the program, or reset by INIT.

Bit 01, Data Terminal Ready

Bit 01 is set by the program to enable operation of the local data set. When bit 01 is set the Data Terminal Ready signal to the data set is placed in the SPACE state. Bit 01 must always be set to send or receive data.

Bit 01 can be set, reset or read by the program, or reset by INIT.

2.3 SPECIFICATIONS

General specifications for the controller are given in Table 2-1.

Table 2-1. Cal Data Asynchronous Controller Specifications

Characteristic	Specification
FUNCTIONAL	
Transmission Rates	110, 134.5, 150, 300, 600, 1200, 1800 2400, 4800 and 9600 baud, switch selectable
Stop Bits	110 baud = two stop bits All other rates = one stop bit
Word Length	Five to eight bits, plus parity (if selected), strap selectable
MACROBUS Addresses	Keyboard/reader control and status register = 777560_8 Keyboard/reader data buffer = 777562_8 Printer/punch control and status register = 777564_8 Printer/punch data buffer = 777566_8
Priority Level	BR4
Interrupt Vector	Keyboard/reader = 60_8 Printer/punch = 64_8
ELECTRICAL	
Interface	Connectors A and B interface with the standard Cal Data MACROBUS. Connectors P1 and P2 interface with the external terminal. Power and ground connections are made at connectors C to F.
Power:	Operating Amperes / Voltage Tolerance
+5 Vdc	1.7 ± 10% / ± 5%
-15 Vdc	0.035 ± 10% / ± 20%
MECHANICAL	
Configuration	Hex-width printed-circuit board
Dimensions	15.7 by 8.9 inches (39.9 by 22.6 cm)
Mounting Centers	0.75 inch (1.9 cm) recommended minimum
ENVIRONMENTAL	
Operating Temperature	0 to +50°C
Airflow	115 cfm (54 lps), minimum
Humidity	10 to 90% relative, with condensation

SECTION 3
PHYSICAL DESCRIPTION

3.1 GENERAL

The controller (Figure 3-1) is a hex-width board 15.7 by 8.9 inches (39.9 by 22.6 cm) that normally plugs into any "hex-width I/O" slot of the Cal Data computer chassis. The right-hand edge of the board has a 1.0 by 5.5 inch (2.5 by 14.0 cm) cutout as clearance for the side-mounted cooling fans in the chassis.

3.2 CONNECTORS

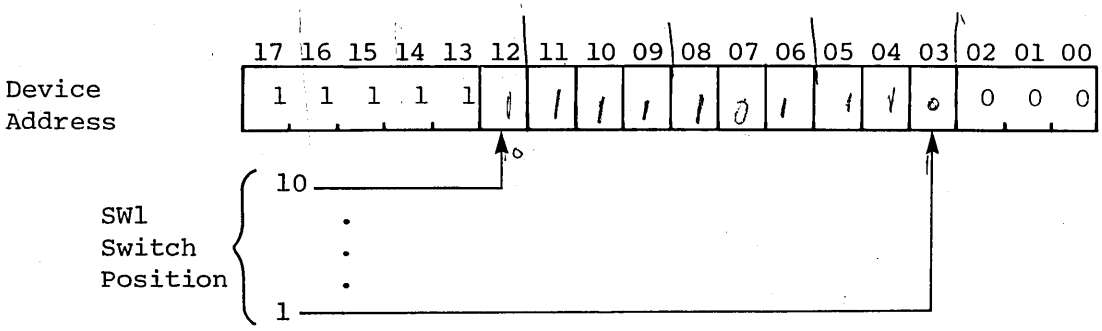
There are six integral printed-circuit connectors (A to F) on the bottom edge of the board and two discrete connectors (P1 and P2) on the top edge. Interface pin assignments are defined in Appendix A.

Connectors A and B interface with the MACROBUS. Connectors C to F provide power and additional bus signals. Connectors P1 and P2 interface via cable with the serial I/O device being controlled.

3.3 ADJUSTABLE ELEMENTS

3.3.1 Device Address

Switch element SW1 is used to select a portion of the MACROBUS Address (lines A12:A03) to which the controller address decode logic responds. Each of the 10 switch positions can be set to allow a ZERO (switch closed) or ONE on the corresponding Address line to be recognized as part of the controller address:



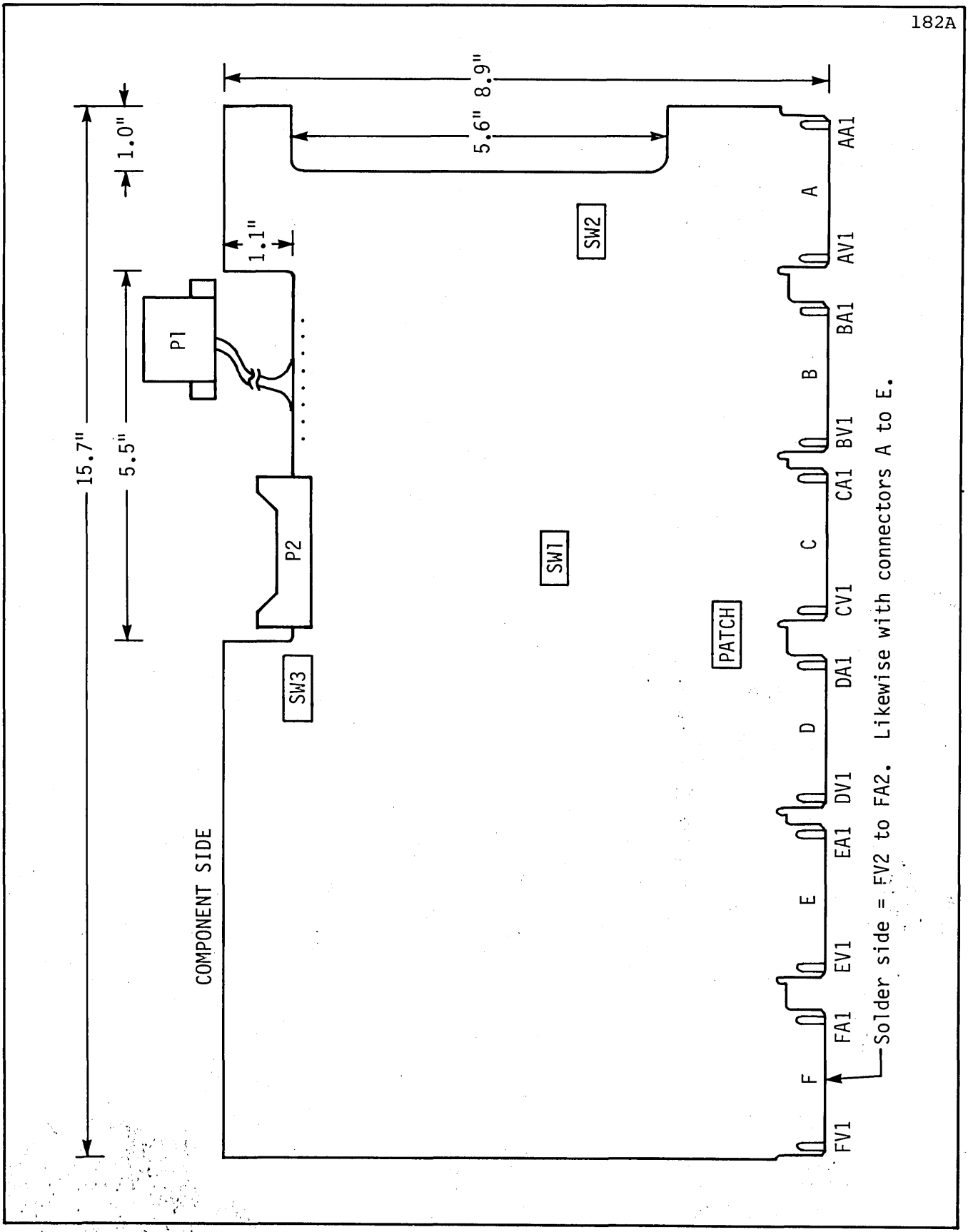
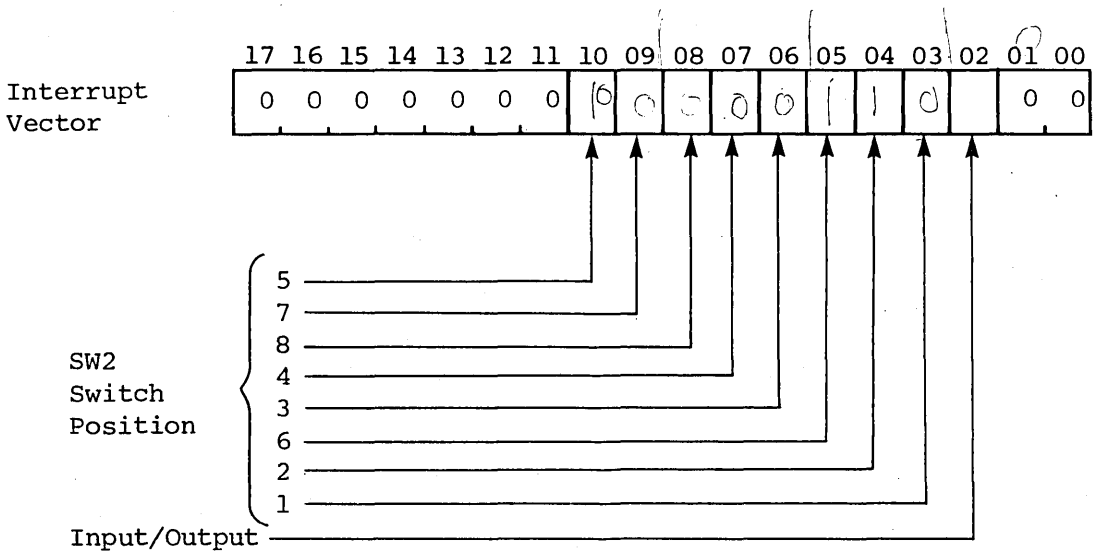


Figure 3-1. Asynchronous Controller Board Configuration

3.3.2 Interrupt Address

Switch element SW2 is used to select a portion of the interrupt address (MACROBUS lines D10:D03) output by the controller when an interrupt request is acknowledged by the CPU. Each of the eight switch positions can be set to allow a ZERO (switch closed) or ONE to be transmitted on the corresponding Data line:

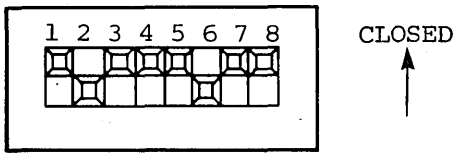


Bit 02 is set by the controller interrupt logic.

Example

Set addresses 60_8 (input from keyboard/reader) and 64_8 (output to printer/punch).

This is done by opening switches 2 and 6, and closing switches 1, 3, 4, 5, 7 and 8:



3.3.3 Baud Rate

Switch element SW3 is used to select the serial transmission rate of the controller. Each of the 10 switch positions selects one baud rate, as follows:

SW3 Position	Baud Rate	SW3 Position	Baud Rate
1	9600	6 5	600
2	4800	~~7~~ 6	300
3	2400	8	150
4	1800	9	134.5
5	1200	10	110

A closed switch position enables the corresponding baud rate.

3.3.4 Interrupt Request Level

Patch 1 is used to select the level at which the controller requests CPU interrupt service on the MACROBUS. The patch provided selects Bus Request BR4 and jumpers Bus Grant lines BG5, BG6 and BG7 unchanged. BG4 is patched into the controller logic.

3.3.5 Parity

Strapping between "E" points on the board is used to select parity.

Strapping E7 to E8 enables the parity generation and checking circuits. E1 and E2 determine the parity selected:

a. E1 strapped to E2 selects odd parity.

b. E1 and E2 open selects even parity.

E7 and E8 open inhibits the parity function.

3.3.6 Character Length

The strapping between E3 to E6 determines the character length:

Character Length	Straps
8 bits	No straps
7 bits	E3 to E4
6 bits	E5 to E6
5 bits	E3 to E4, E5 to E6

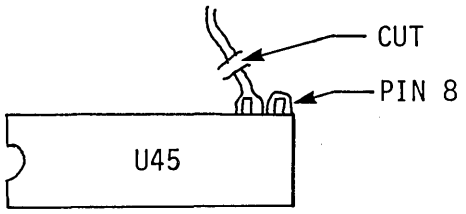
3.3.7 Special Option Control Register

Strapping E9 to E10 disables the special option control register, inhibiting character length selection, parity selection and stop-bit selection functions.

3.3.8 Buffering

Single buffering, or the occurrence of Output Data Ready at the end of the output shift cycle, is enabled by strapping E19 to E20.

Double buffering is possible by cutting the etch at U45 pin 9 and strapping E19 to E20 and E21:



This strapping arrangement causes Output Data Ready to occur on the loading of the output shift register from the transmit data register and indicates that the transmitter receiver circuit is ready to receive another character. The output shift register must be allowed enough time to transmit two full characters, including stop bits, before another two are transferred from the CPU.

3.3.9 Request to Send

The Request to Send signal to the data set can be set to a SPACE condition whenever computer power is on by removing the strap between E17 and E18.

The Data Terminal Ready signal to the data set should be moved from J2 pin DD to join with the Request to Send signal at J2 pin V.

3.3.10 EIA Modem Status

Data-set status bits 15, 14, 13, 12 and 10 of the keyboard/reader control and status register can be disabled by cutting the etch between E22 and E23.

SECTION 4
INTERFACE

4.1 GENERAL

The controller interfaces with the other computer boards via the chassis backplane, which includes the MACROBUS. The interface with the MACROBUS (connectors A and B) conforms to the standard interfacing rules for I/O compatibility described in the MACROBUS Channel Adapter Technical Manual, C21518013.

The controller interfaces with terminal devices via connectors P1 and P2 at the top of the board. Different cable and plug arrangements are provided, depending on the specific terminal device used.

Pin assignments for all interface connectors are listed in Appendix A.

4.2 CIRCUITS

Because the controller is attached to the MACROBUS along with other peripheral devices and memory, the MACROBUS loading introduced by the board is an important system consideration for configurations with a large amount of memory or numerous peripheral devices. The controller minimizes the loading of receivers and the leakage current of drivers in the high state (these being the critical bus-loading parameters). This is accomplished in two ways:

a. The driver leakage load is limited to that of one gate instead of two (as is common in some logic designs).

b. A Cal Data proprietary MACROBUS receiver circuit improves speed and reduces drive requirements.

4.2.1 Line Driver

The line driver is a TTL buffer. The critical MACROBUS specifications for the device are:

Output low voltage at 50 mA sink (V_{OL})	+0.5 V max
Output high leakage current at 2.5 V (I_{OH})	+60 µA max

4.2.2 Line Receiver

The controller uses a Cal Data line receiver. The critical MACROBUS specifications for this device are:

Input high threshold (V_{IH})	+2.5 V min
Input low threshold (V_{IL})	+1.4 V max
Input current at +2.5 V (I_{IH})	+60 µA max
Input current at 0.0 V (I_{IL})	±25 µA max

4.2.3 MACROBUS Loading

The limiting MACROBUS loading occurs on the bidirectional Data lines that have one receiver and one driver for each I/O module. Worst-case MACROBUS load specifications are:

V_{IH}	+2.5 V min
V_{IL}	+1.4 V max
I_{IH}	±120 µA max at +2.5 V
I_{IL}	±25 µA max at 0.0 V

SECTION 5
MAINTENANCE

5.1 GENERAL

This section describes preventive and corrective maintenance procedures. In general, corrective maintenance is limited to isolation of a system fault to a specific board, followed by replacement of the board. Troubleshooting may then be used to verify that the suspected board is malfunctioning and to help diagnose the specific problem. Repair should be conducted at the factory or by an authorized Cal Data representative.

5.2 PREVENTIVE MAINTENANCE

All Cal Data circuit boards are reliable solid-state devices designed to perform continuously for many years without degradation. Preventive maintenance consists of performing the following tasks every six months:

a. Inspect each board for damaged wires or components, or other obvious defects.

b. Using a low-pressure source of air (75 psi one foot from the board or 5 kg/cm^2 30 cm from the board), blow off accumulated dust and foreign matter.

c. Check the +5 Vdc input from the backplane. It should be within ±5 percent.

Another aspect of preventive maintenance is proper handling. The following points should be observed:

a. Always be sure that system power is OFF before installing or removing any board.

b. Install each board with the component side toward the front of the chassis. Check each board for proper orientation before attempting to install it. Because the connectors are keyed, excessive force applied to a reversed board can result in connector damage. Make sure that the board is completely and evenly seated.

c. Insert and remove each board slowly and carefully so that it does not make contact with adjacent boards.

d. Never use components as finger grips; use the grip areas at the corners of the board.

e. To prevent oxides from forming on the gold plating, do not touch connectors.

5.3 CORRECTIVE MAINTENANCE

Repair of a board in the field is not recommended. If a malfunction is detected, replace the board with a spare known to be operating properly and return the malfunctioning board for repair to California Data Processors or an authorized representative.

APPENDIX A
CONNECTOR PIN ASSIGNMENTS

Table A-1. Connector A Pin Assignments, MACROBUS

Name		Signal	Pin	Pin		Signal	Name
Initialize		BUS INIT-L	A1	A2		+5V	+5 Vdc
Interrupt		BUS INTR-L	B1	B2		GND	Ground
Data 00		BUS D00-L	C1	C2		GND	Ground
Data 02		BUS D02-L	D1	D2		BUS D01-L	Data 01
Data 04		BUS D04-L	E1	E2		BUS D03-L	Data 03
Data 06		BUS D06-L	F1	F2		BUS D05-L	Data 05
Data 08		BUS D08-L	H1	H2		BUS D07-L	Data 07
Data 10		BUS D10-L	J1	J2		BUS D09-L	Data 09
Data 12		BUS D12-L	K1	K2		BUS D11-L	Data 11
Data 14		BUS D14-L	L1	L2		BUS D13-L	Data 13
Parity Bit Low	*	BUS PA-L	M1	M2		BUS D15-L	Data 15
Ground		GND	N1	N2	*	BUS PB-L	Parity Bit High
Ground		GND	P1	P2		BUS BBSY-L	Bus Busy
Ground		GND	R1	R2		BUS SACK-L	Selection Acknowledgement
Ground		GND	S1	S2	*	BUS NPR-L	Nonprocessor Request
Ground		GND	T1	T2		BUS BR7-L	Bus Request 7
Nonprocessor Grant	*	BUS NPG-H	U1	U2		BUS BR6-L	Bus Request 6
Bus Grant 7	*	BUS BG7-H	V1	V2		GND	Ground

* These signals are assigned on the backplane but are not used on this assembly.

Table A-2. Connector B Pin Assignments, MACROBUS

Name	Signal	Pin	Pin	Signal	Name
Bus Grant 6	* BUS BG6-H	A1	A2	+5V	+5 Vdc
Bus Grant 5	* BUS BG5-H	B1	B2	GND	Ground
Bus Request 5	BUS BR5-L	C1	C2	GND	Ground
Ground	GND	D1	D2	BUS BR4-L	Bus Request 4
Ground	GND	E1	E2	* BUS BG4-H	Bus Grant 4
AC Low	* BUS ACLO-L	F1	F2	* BUS DCLO-L	DC Low
Address 01	BUS A01-L	H1	H2	BUS A00-L	Address 00
Address 03	BUS A03-L	J1	J2	BUS A02-L	Address 02
Address 05	BUS A05-L	K1	K2	BUS A04-L	Address 04
Address 07	BUS A07-L	L1	L2	BUS A06-L	Address 06
Address 09	BUS A09-L	M1	M2	BUS A08-L	Address 08
Address 11	BUS A11-L	N1	N2	BUS A10-L	Address 10
Address 13	BUS A13-L	P1	P2	BUS A12-L	Address 12
Address 15	BUS A15-L	R1	R2	BUS A14-L	Address 14
Address 17	BUS A17-L	S1	S2	BUS A16-L	Address 16
Ground	GND	T1	T2	BUS C1-L	Control 1
Slave Synchronization	BUS SSYN-L	U1	U2	BUS C0-L	Control 0
Master Synchronization	BUS MSYN-L	V1	V2	GND	Ground

* These signals are assigned on the backplane but are not used on this assembly.

Table A-3. Connector C Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
M Bus 00	* MB000-L	A1	A2	+5V	+5 Vdc
M Bus 01	* MB001-L	B1	B2	-15V	-15 Vdc
M Bus 02	* MB002-L	C1	C2	GND	Ground
M Bus 03	* MB003-L	D1	D2	* MB004-L	M Bus 04
M Bus 05	* MB005-L	E1	E2	* MB006-L	M Bus 06
M Bus 07	* MB007-L	F1	F2	* MB008-L	M Bus 08
M Bus 09	* MB009-L	H1	H2	* MB010-L	M Bus 10
M Bus 11	* MB011-L	J1	J2	* MB012-L	M Bus 12
M Bus 13	* MB013-L	K1	K2	* MB014-L	M Bus 14
M Bus 15	* MB015-L	L1	L2	* AB000-H	A Bus 00
A Bus 01	* AB001-H	M1	M2	* AB002-H	A Bus 02
A Bus 03	* AB003-H	N1	N2	* AB004-H	A Bus 04
A Bus 05	* AB005-H	P1	P2	* AB006-H	A Bus 06
A Bus 07	* AB007-H	R1	R2	* AB008-H	A Bus 08
A Bus 09	* AB009-H	S1	S2	* AB010-H	A Bus 10
Ground	GND	T1	T2	* AB011-H	A Bus 11
A Bus 13	* AB013-H	U1	U2	* AB012-H	A Bus 12
A Bus 15	* AB015-H	V1	V2	* AB014-H	A Bus 14

* These signals are assigned on the backplane but are not used on this assembly.

Table A-4. Connector D Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Power Failure Interrupt	* PFINT-H	A1	A2	+5V	+5 Vdc
Halt Interrupt	* HLINT-H	B1	B2	-15V	-15 Vdc
Data Switch 16	* DS16-H	C1	C2	GND	Ground
Data Switch 17	* DS17-H	D1	D2	* LTCL-L	Line-Frequency Clock
Virtual Address	* VIRTAD-H	E1	E2	* PBBSY-L	Processor Bus Busy
Control Count 00	* CC000-L	F1	F2	* HALTP-L	Panel Halt
Control Count 01	* CC001-L	H1	H2	* MSR15-L	Microstatus Register 15
Control Count 02	* CC002-L	J1	J2	* RESET-L	Reset
Control Count 03	* CC003-L	K1	K2	BUS BG7-IN	Bus Grant 7 In
Control Count 04	* CC004-L	L1	L2	BUS BG7-OUT	Bus Grant 7 Out
Control Count 05	* CC005-L	M1	M2	BUS BG6-IN	Bus Grant 6 In
Control Count 06	* CC006-L	N1	N2	BUS BG6-OUT	Bus Grant 6 Out
Control Count 07	* CC007-L	P1	P2	BUS BG5-IN	Bus Grant 5 In
Control Count 08	* CC008-L	R1	R2	BUS BG5-OUT	Bus Grant 5 Out
Control Count 09	* CC009-L	S1	S2	BUS BG4-IN	Bus Grant 4 In
Ground	GND	T1	T2	BUS BG4-OUT	Bus Grant 4 Out
Control Count 10	* CC010-L	U1	U2	* BUS NPG-IN	Nonprocessor Grant In
Control Count 11	* CC011-L	V1	V2	* BUS NPG-OUT	Nonprocessor Grant Out

* These signals are assigned on the backplane but are not used on this assembly.

Table A-5. Connector E Pin Assignments

Name	Signal	Pin	Pin	Signal	Name
Control Memory 00	* CM000-H	A1	A2	+5V	+5 Vdc
Control Memory 01	* CM001-H	B1	B2	-15V	-15 Vdc
Control Memory 02	* CM002-H	C1	C2	GND	Ground
Control Memory 03	* CM003-H	D1	D2	* CM004-H	Control Memory 04
Control Memory 05	* CM005-H	E1	E2	* CM006-H	Control Memory 06
Control Memory 07	* CM007-H	F1	F2	* EMINH-L	Emulate Inhibit
Control Memory 09	* CM009-H	H1	H2	* CM008-H	Control Memory 08
Control Memory 11	* CM011-H	J1	J2	* CM010-H	Control Memory 10
Decode Address 00	* DAD00-H	K1	K2	* CM012-H	Control Memory 12
Control Memory 13	* CM013-H	L1	L2	* CM014-H	Control Memory 14
Control Memory 15	* CM015-H	M1	M2	* DAD01-H	Decode Address 01
Control Memory 17	* CM017-H	N1	N2	* CM016-H	Control Memory 16
Control Memory 19	* CM019-H	P1	P2	* CM018-H	Control Memory 18
Switch Register 0	* SRO-L	R1	R2	* CM020-H	Control Memory 20
Control Memory 21	* CM021-H	S1	S2	* CM022-H	Control Memory 22
Ground	GND	T1	T2	* CM024-H	Control Memory 24
Control Memory 23	* CM023-H	U1	U2	* CM026-H	Control Memory 26
Control Memory 25	* CM025-H	V1	V2	* CM027-H	Control Memory 27

* These signals are assigned on the backplane but are not used on this assembly.

Table A-6. Connector F Pin Assignments

Name		Signal	Pin	Pin		Signal	Name
Control Memory 28	*	CM028-H	A1	A2		+5V	+5 Vdc
Control Memory 29	*	CM029-H	B1	B2		-15V	-15 Vdc
Control Memory 31	*	CM031-H	C1	C2		GND	Ground
Control Memory 31	*	CM030-H	D1	D2	*	CM032-H	Control Memory 32
Control Memory 33	*	CM033-H	E1	E2	*	CM034-H	Control Memory 34
Control Memory 35	*	CM035-H	F1	F2	*	DAD02-H	Decode Address 02
Control Memory 37	*	CM037-H	H1	H2	*	CM036-H	Control Memory 36
Control Memory 39	*	CM039-H	J1	J2	*	CM038-H	Control Memory 38
Instruction Repeat	*	IRPTE-L	K1	K2	*	CM040-H	Control Memory 40
Control Memory 41	*	CM041-H	L1	L2	*	CM042-H	Control Memory 42
Control Memory 43	*	CM043-H	M1	M2	*	CPEN-L	Control Panel Enable
Control Memory 45	*	CM045-H	N1	N2	*	CM044-H	Control Memory 44
Control Memory 47	*	CM047-H	P1	P2	*	CM046-H	Control Memory 46
Decode Address 03	*	DAD03-H	R1	R2	*	ACMSL-L	Alterable Control Memory Select
		Reserved	S1	S2	*	AUXRM-L	Auxiliary ROM Select
Ground		GND	T1	T2	*	IRINH-L	Instruction Inhibit
		Reserved	U1	U2	*	IWAIT-L	Instruction Wait
System Clock	*	SYSCK-L	V1	V2		GND	Ground

*These signals are assigned on the backplane but are not used on this assembly

Table A-7. Connector P1 Pin Assignments

Pin	Signal	Name
2	XMIT	Transmit
3	20 MIL	20 Milliamperes
4	RDR SOL RET	Reader Solenoid Return
5	XMIT RET	Transmit Return
6	RDR SOL	Reader Solenoid

Table A-8. Connector P2 Pin Assignments

Pin	Signal	Name
A	GND	Ground
B	GND	Ground
F	XMIT EIA	Transmit EIA
J	EIA BB	EIA Receive Data
K	20 MIL	20 Milliamperes
T	CLR TO SND	Clear to Send
V	REQ TO SEND	Request to Send
X	RING IND	Ring Indicator
AA	XMIT RET	Transmit Return
BB	CAR DET	Carrier Detector
DD	DT RDY	Data Terminal Ready
EE	RDR SOL RET	Reader Solenoid Return
FF	SUPRV XMIT	Supervisory Transmit
JJ	SPRV REC DATA	Supervisory Receive Data
KK	XMIT	Transmit
PP	RDR SOL	Reader Solenoid
RR	EIA SEL	EIA Select
UU	GND	Ground
VV	GND	Ground

LIST OF MATERIALS

FOR REFERENCE ONLY

ITEM NO.	QTY. REQD.	REFERENCE DESIGNATION	PART NUMBER	DESCRIPTION	NOTES	VENDOR	VENDOR PART NUMBER
1	2	P1,P2	C56150744	CONNECTOR 44 PIN SKT HSNG		BERG	65043-015
2	AR		C37831200	CABLE COMMUNICATIONS-COLOR CODED, UL STYLE 2576, 24 AWG		BLAKE & WIRE CABLE	BC4270
3	1		C56763100	TIE WRAP, I.D. 5/16 X 1 IN		THOMAS &BETTS	TY 51M
4	13		C56150745	CONTACT,SKT		BERG	47743
5	AR		C37611110	WIRE, BUS 20 AWG		ALPHA	297

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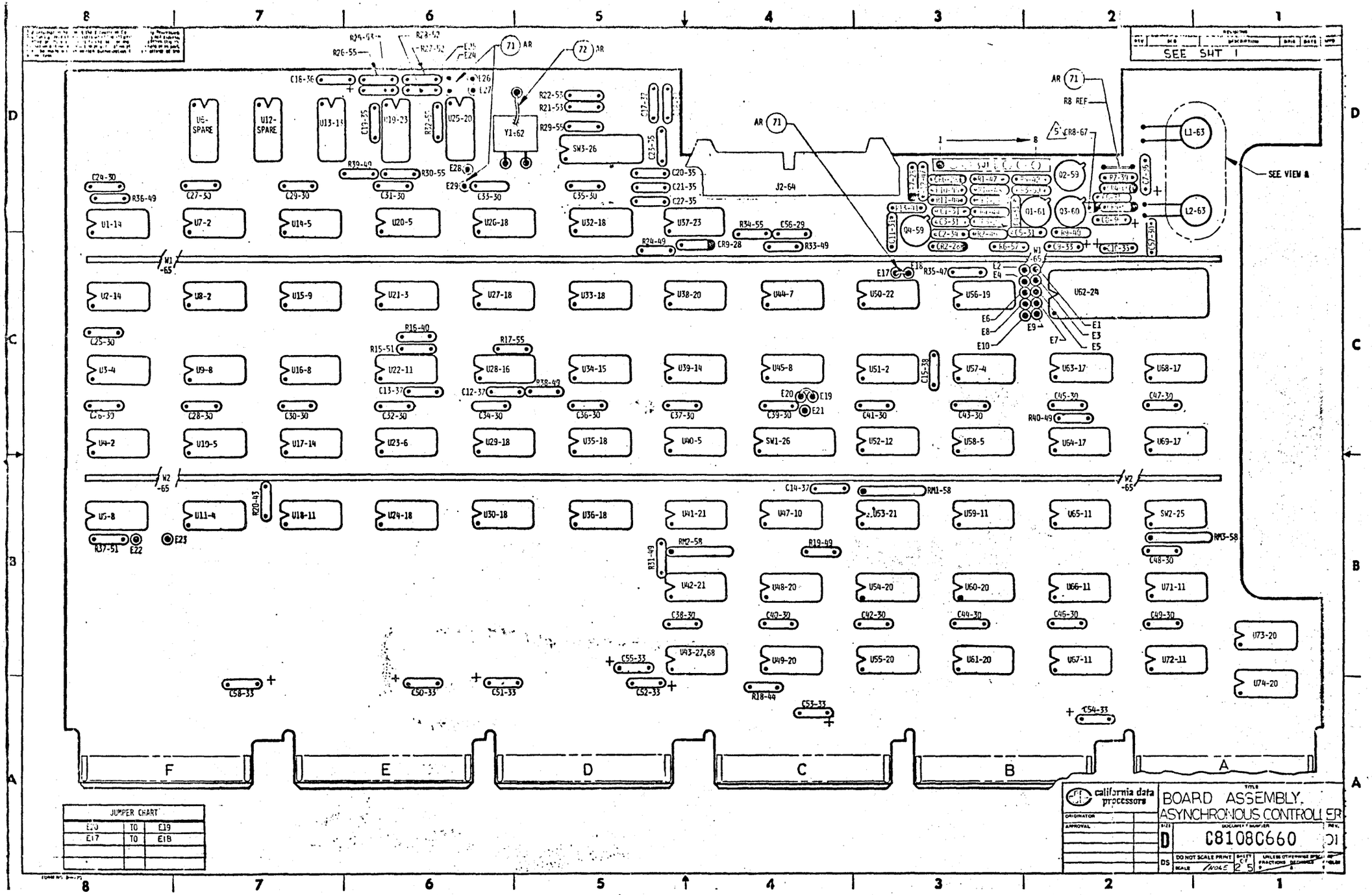
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E
D
C
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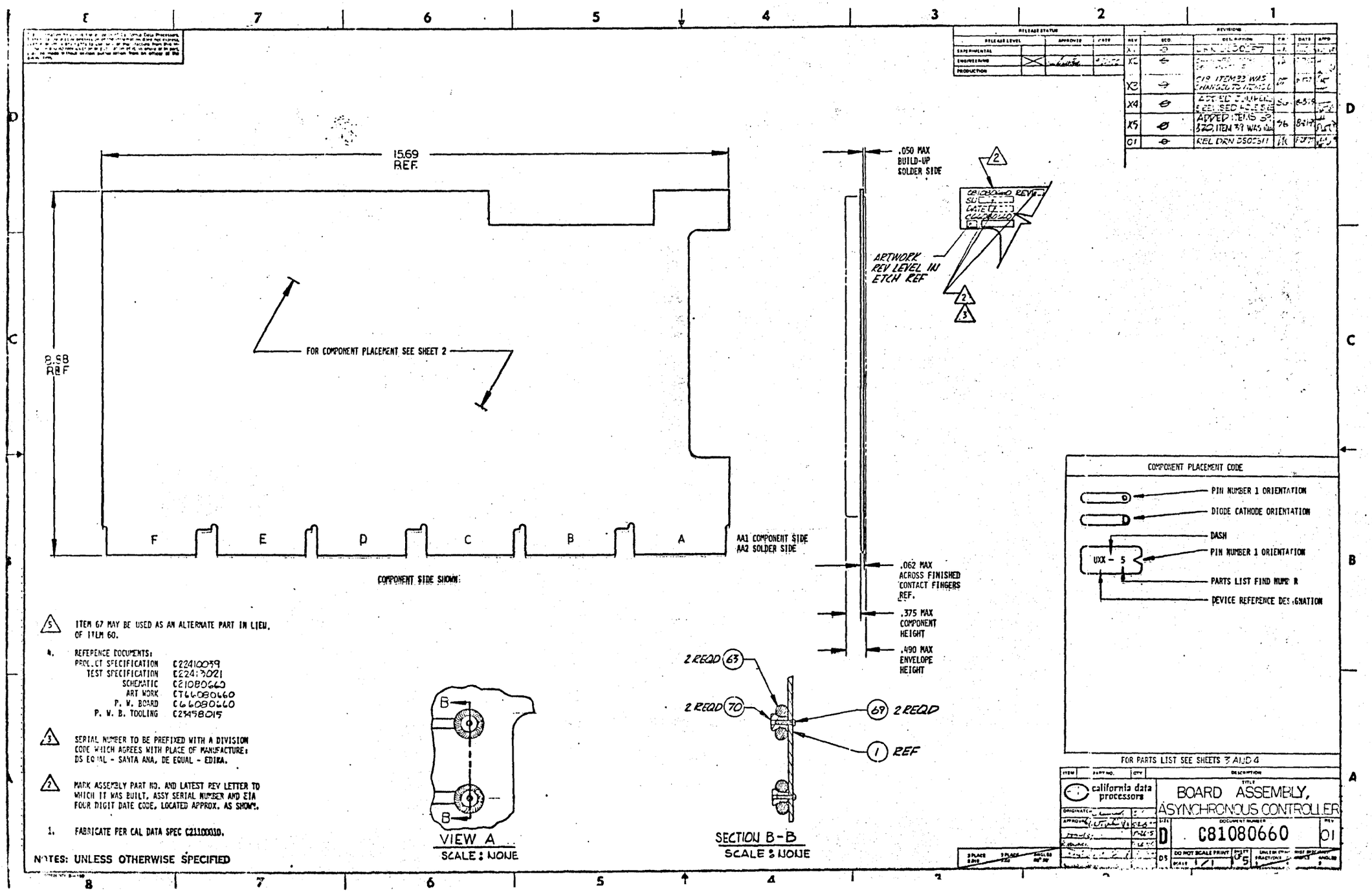


5. ITEM 67 MAY BE USED AS AN ALTERNATE PART IN LIEU OF ITEM 60.

4. REFERENCE DOCUMENTS:

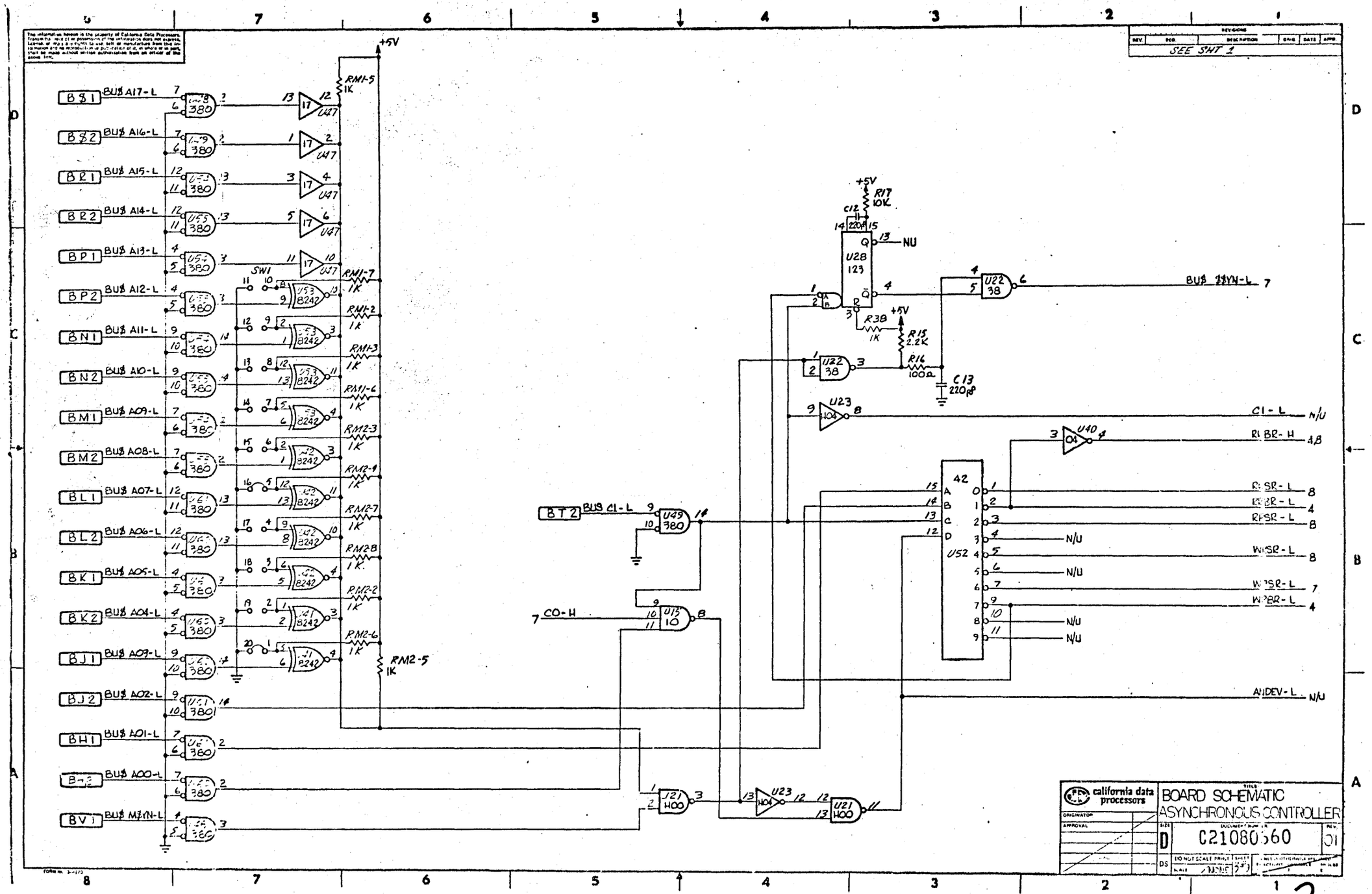
PRODUCT SPECIFICATION	C22410039
TEST SPECIFICATION	C22413021
SCHEMATIC	C21080660
ART WORK	CT66080660
P. W. BOARD	C66080660
P. W. B. TOOLING	C23458015

3. SERIAL NUMBER TO BE PREFIXED WITH A DIVISION CODE WHICH AGREES WITH PLACE OF MANUFACTURE: DS EQUAL - SANTA ANA, DE EQUAL - EDINA.

2. MARK ASSEMBLY PART NO. AND LATEST REV LETTER TO WHICH IT WAS BUILT, ASSY SERIAL NUMBER AND EIA FOUR DIGIT DATE CODE, LOCATED APPROX. AS SHOWN.

1. FABRICATE PER CAL DATA SPEC C21100010.

NOTES: UNLESS OTHERWISE SPECIFIED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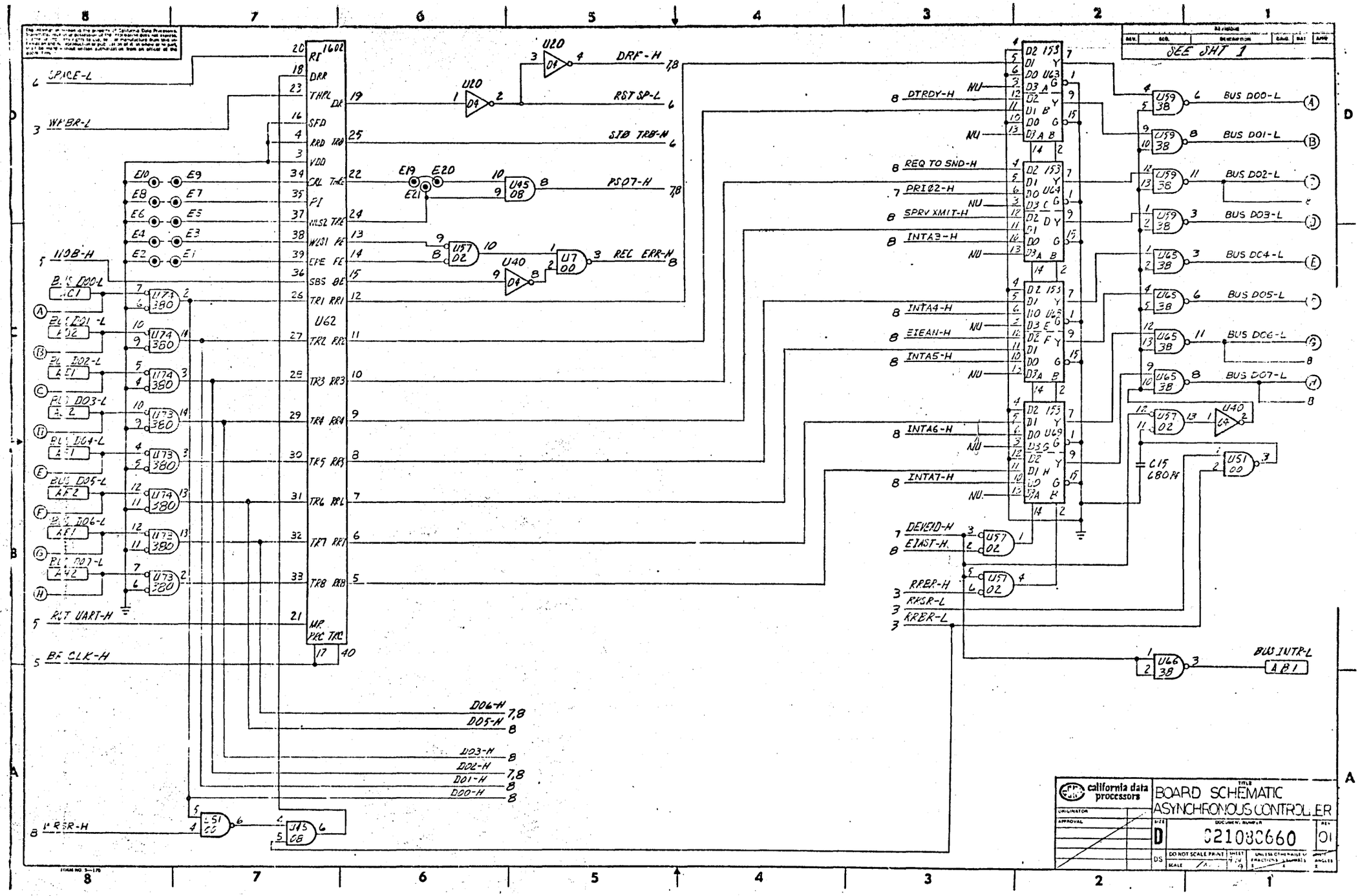
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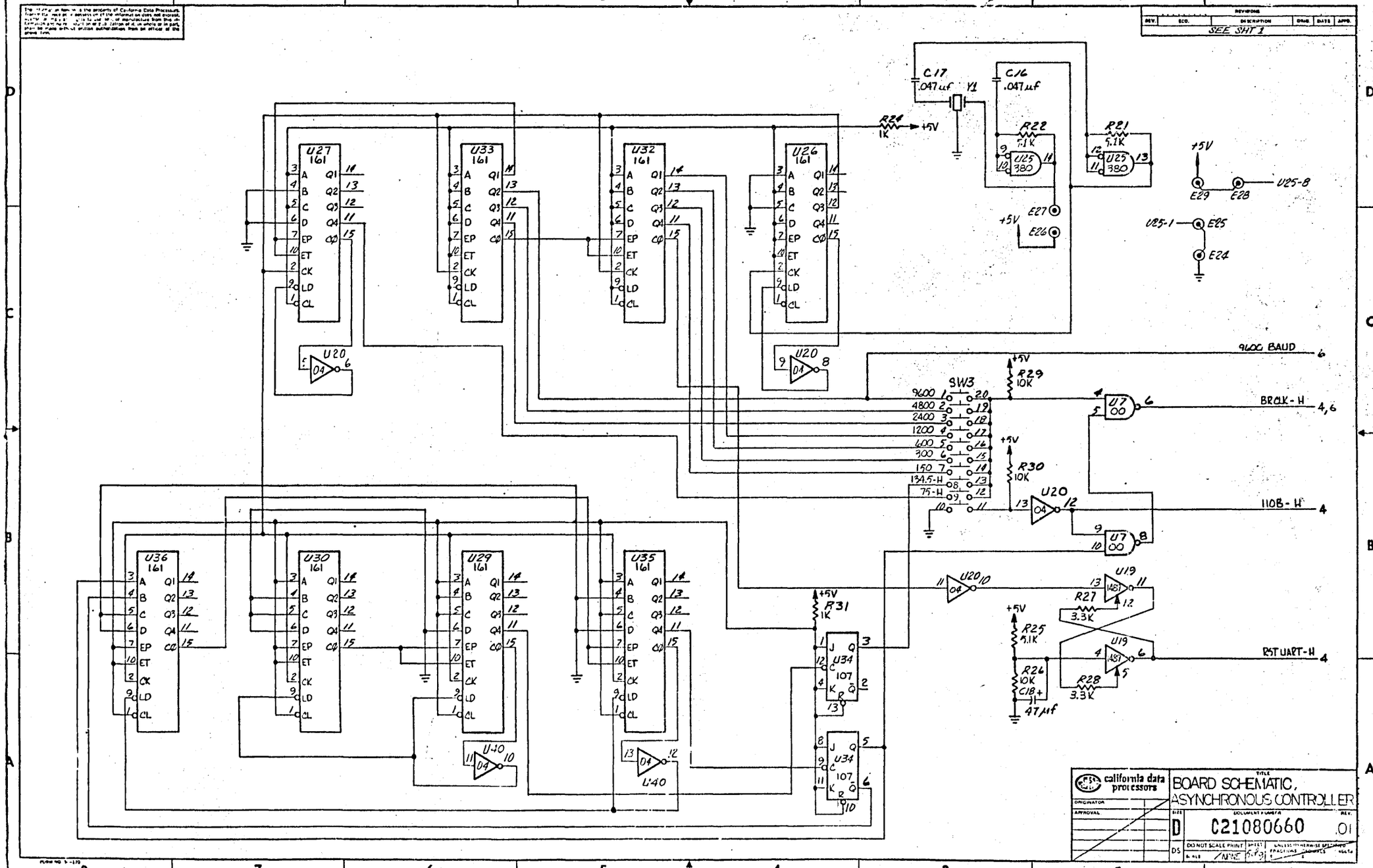

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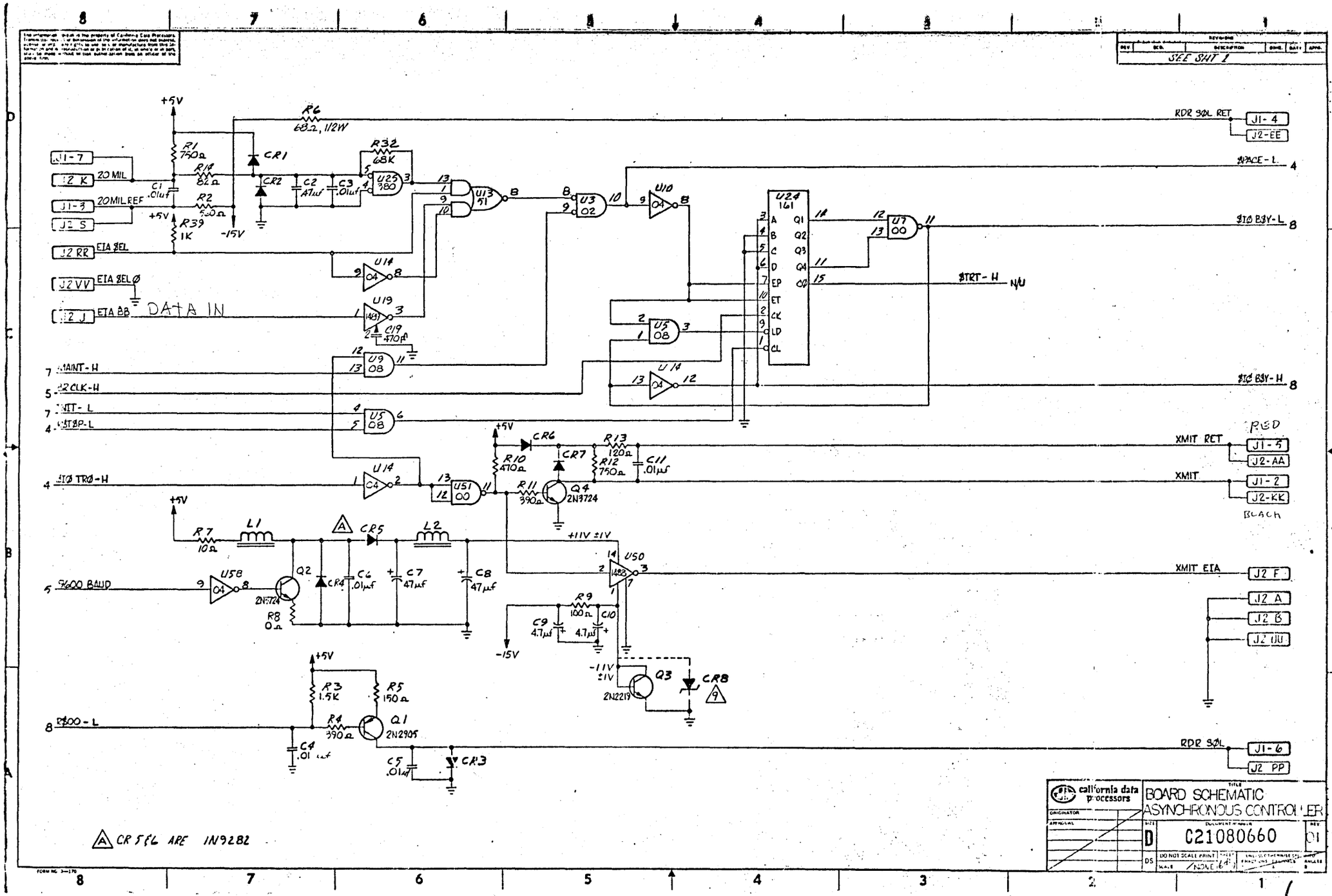
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R2 500Ω
R39 1K
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CR2
R32 68K
C2 47uf
C3 .01uf
U23 380
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U3 02
U10 04
U24 161
U7 00
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STØ B3Y-L
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STRT-H
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XMIT
J1-2
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CR6
CR7
R13 120Ω
R12 750Ω
C11 .01μf
R11 390Ω
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R7 10Ω
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L2
CR5
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C8 47μf
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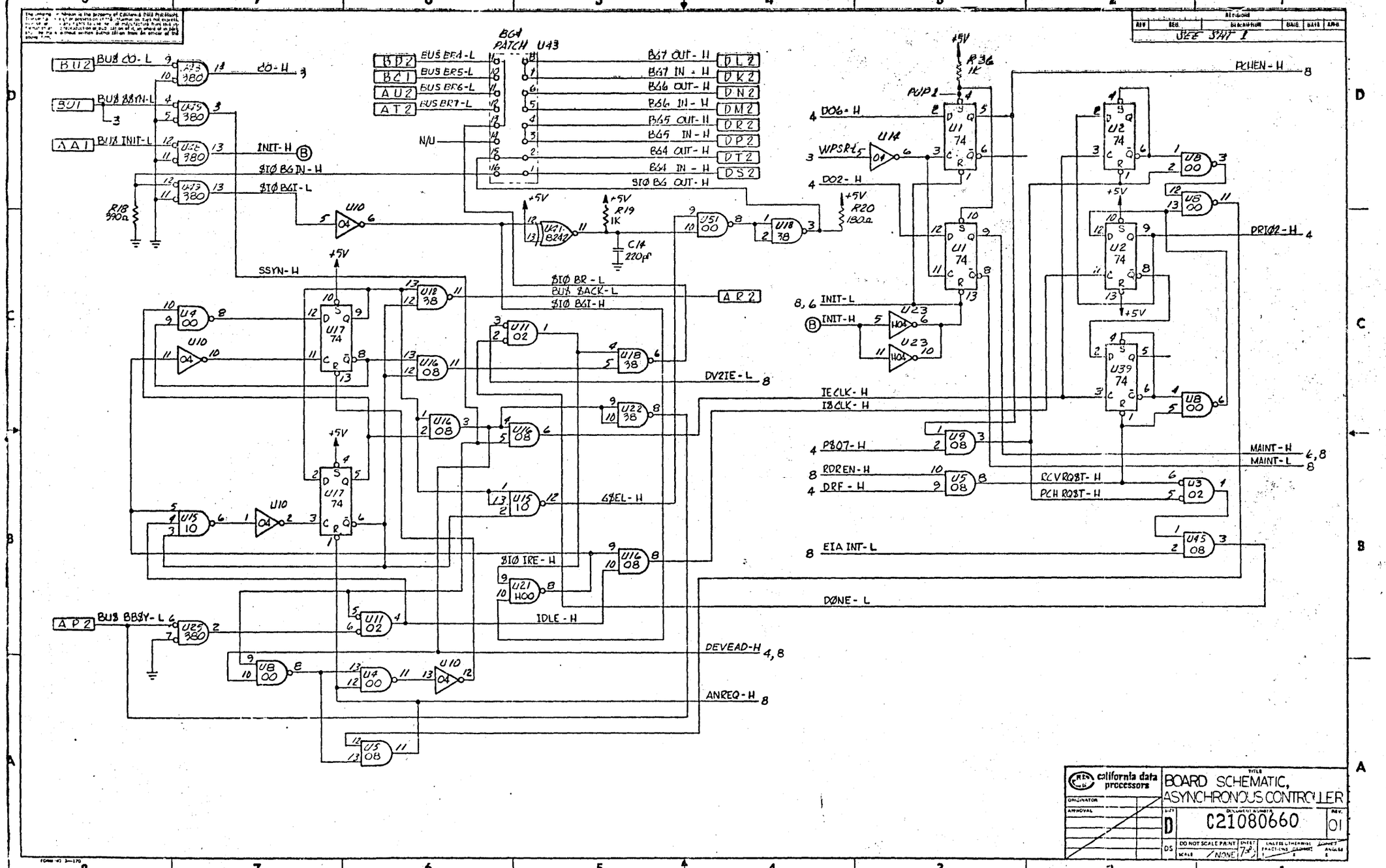

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N/U
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BG6 OUT-H
BG6 IN-H
BG5 OUT-H
BG5 IN-H
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SIO BG OUT-H
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DK2
DN2
DM2
DR2
DP2
DT2
DS2
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BUS SACK-L
SIO BGI-H
AR2
DV2IE-L
GSEL-H
SIO IRE-H
IDLE-H
AP2 BUS BBSY-L
DEVEAD-H
ANREQ-H
DO6-H
WPSR-L
DO2-H
INIT-L
INIT-H
PUP1
R36 1K
PCHEN-H
PRIO2-H
IECLK-H
ISCLK-H
PSO7-H
RDREN-H
DRF-H
MAINT-H
MAINT-L
RCVRQST-H
PCH RQST-H
EIA INT-L
DONE-L
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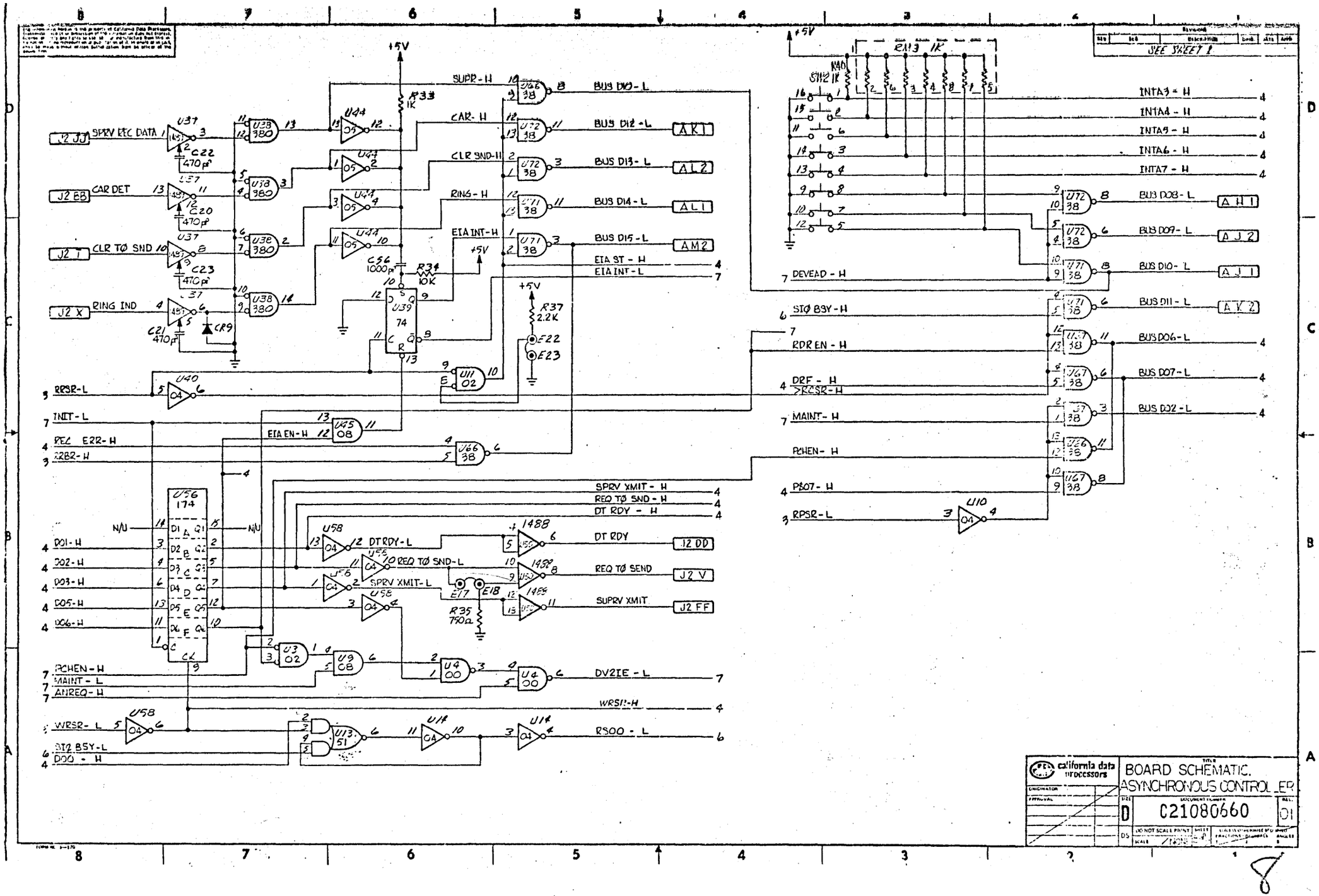
7


SEE SHEET 1
+5V
SUPR-H
CAR-H
CLR SND-H
RING-H
EIA INT-H
BUS D10-L
BUS D12-L
BUS D13-L
BUS D14-L
BUS D15-L
EIA ST-H
EIA INT-L
J2 JJ
SPRV REC DATA
J2 BB
CAR DET
J2 T
CLR TØ SND
J2 X
RING IND
RRSR-L
INIT-L
REC ERR-H
RRBR-H
EIA EN-H
SPRV XMIT-H
REQ TØ SND-H
DT RDY-H
DT RDY-L
REQ TØ SND-L
SPRV XMIT-L
DT RDY
REQ TØ SEND
SUPRV XMIT
J2 DD
J2 V
J2 FF
DV2IE-L
WRSR-H
RSOO-L
PCHEN-H
MAINT-L
ANREQ-H
WRSR-L
SIØ BSY-L
DOO-H
DO1-H
DO2-H
DO3-H
DO5-H
DO6-H
INTA3-H
INTA4-H
INTA5-H
INTA6-H
INTA7-H
BUS DO8-L
BUS DO9-L
BUS D10-L
BUS D11-L
BUS DO6-L
BUS DO7-L
BUS DO2-L
DEVEAD-H
SIØ BSY-H
RDR EN-H
DRF-H
>RCSR-H
MAINT-H
PCHEN-H
PSO7-H
RPSR-L
RM3 1K
R33 1K
R34 10K
R37 2.2K
R35 750Ω
C56 1000pf
C22 470pf
C20 470pf
C23 470pf
C21 470pf
CR9
E22
E23
E17
E18
U39 74
U56 174
U10
U58
U14
U13 51
U3 02
U9 08
U4 00
U11 02
U40 04
U45 08
U66 38
U72 38
U71 38
U67 38
U38 380
U44 05
U37
U46 38
U47 38
U57 38
U26 38
U67 38
U58 04
U14 04
U13 51
U4 00
U9 08
U3 02
U11 02
U40 04
U45 08
U66 38
U72 38
U71 38
U67 38
U38 380
U44 05
U37
U46 38
U47 38
U57 38
U26 38
U67 38
U10 04
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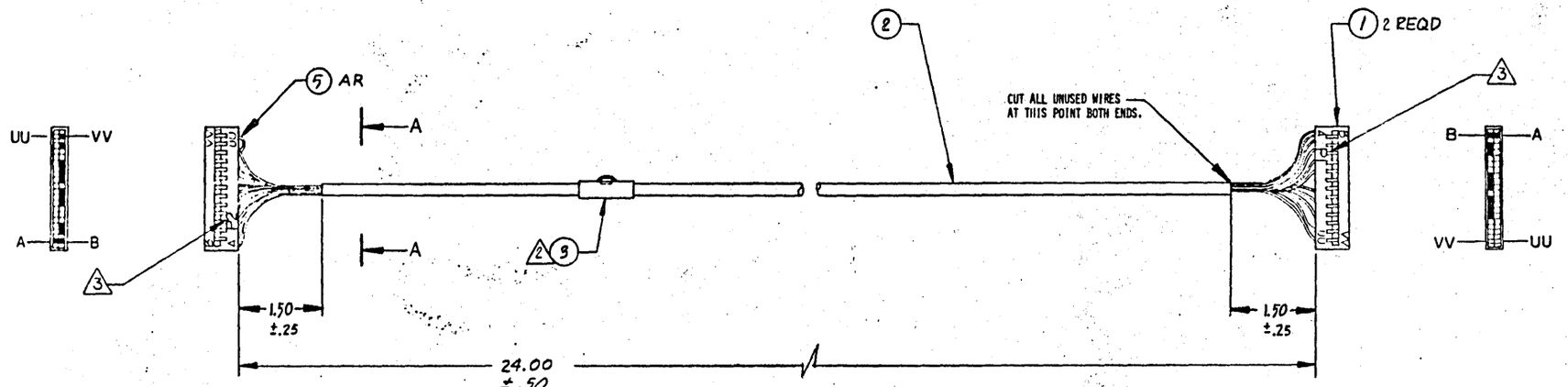
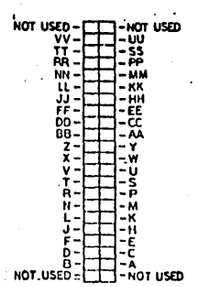
RELEASE STATUS				REVISIONS					
RELEASE LEVEL		APPROVED	DATE	REV	ECO	DESCRIPTION	ORIG	DATE	APPD
EXPERIMENTAL				X1		PRELIMINARY			
ENGINEERING	X		9-30-75	X2	74	ADDED P/N 2270100			
PRODUCTION				01		REL PER D300311			





VIEW A
SCALE: NONE

WIRE TAB LISTING

NOTES	BERG (P1) WIRE GAUGE	WIRE COLOR	TERM. METHOD	ORIGIN	BERG (P2) DESTINATION	TERM. METHOD	FUNCTION
TO CHS		SHIELD & DRAIN		A	A		GROUND
	24	GRN		B	B		GROUND
	24	RED		F	F		EIA XMIT
	24	ORG		J	J		EIA BB
	24	YEL		T	T		CLR TO SND
	24	BLK		V	V		REQ TO SEND
	24	GREY		X	X		RING IND
	24	BLU		BB	BB		CAR DET
	24	VIO		DD	DD		DTA RDY
	24	BRN		FF	FF		SPRV XMIT DATA
	24	WHT		JJ	JJ		SPRV REC DATA
JUMPER					RR		EIA SEL
JUMPER					VV		GROUND

3. PERMANENTLY MARK REFERENCE DESIGNATIONS ON CONNECTORS.
2. PERMANENTLY MARK PART NO. ON ITEM 3.
1. FABRICATE PER CAL DATA SPEC C22270100.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	PART NO.	QTY.	DESCRIPTION

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TITLE
CABLE ASSEMBLY, ASYNCHRONOUS CONTROLLER LOCAL TERM-2 FT

ORIGINATOR DATE 1-4-76
APPROVED DATE 1-7-76

SIZE D | DOCUMENT NUMBER C85300238 | REV 01

DS | DO NOT SCALE PRINT | UNLESS OTHERWISE SPECIFIED: FRACTIONS ±, DECIMALS ±, ANGLES ±

3 PLACE ±.010 | 2 PLACE ±.03 | ANGLES ±0° 30'

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