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CAL DATA 1 MACROPANEL

THEORY OF OPERATION
C21518029-X0

DOCUMENT C21518029
Revision X0
May 1975

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$4.95

REVISIONS

Revision	Date	Approval	Description
X0	5/75		Preliminary edition

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SECTION 1
INTRODUCTION

1.1 SCOPE

This document describes, functionally and in detail, the operation of the Cal Data 1 Macropanel. This document specifically refers to the Macropanel schematic drawing, C21080310. The reader is assumed to have a working knowledge of the Cal Data 1 computer system and to be familiar with the material in the Cal Data 1 Macropanel Technical Manual, C21518028.

1.2 ABBREVIATIONS AND CONVENTIONS

Table 1-1 lists the abbreviations found in this document. Conventions used in the text include:

a. The proper names of signals and microcommands are capitalized.

b. Equipment panel nomenclature is reproduced in all upper-case characters.

c. ZERO and ONE are used to express binary logic "0" and "1" states, respectively.

d. A colon is used to indicate a range of bits. For example, the range of Address bits A12 to A03 is written A12:A03.

e. Octal numbers are followed by a subscript eight for easy identification.

Table 1-1. Abbreviations

Abbreviation	Meaning
Cal Data	California Data Processors
CPU	central processing unit (Engine)
MCA	MACROBUS Channel Adapter
MMU	Memory Management Unit
MUX	multiplexer
LFC	Line-Frequency Clock
LED	light-emitting diode
cm	centimeter
Vdc	volts, direct current
Hz	hertz

1.3 PHYSICAL DESCRIPTION

The Macropanel contains the indicators and switches for operating the CPU and associated logic and it contains the Line-Frequency Clock, an independent function. The Macropanel circuitry is mounted on a printed-circuit board that normally plugs into the first slot of the computer chassis. A plastic cover (Figure 1-1) is imprinted with the designations of the indicators and switches.

The Macropanel board is a hex-width printed-circuit board 15.7 by 8.9 inches (39.9 by 22.7 cm).

There are six printed-circuit connectors (A to F) on the bottom edge of the board. These connectors plug into the standard backplane connectors. Connectors A and B interface with the MACROBUS. Connectors C to F interface with the main computer Microbus.

The controls and indicators are mounted on the component side of the board so that they fit the openings in the Macropanel cover. The cover is held in place with a bezel.

There are two small connectors on the component side of the Macropanel board. J1 at the upper right of the board is for a user-designed remote-control cable. J2 near the PWR switch is for the control extension cable to the power supply.

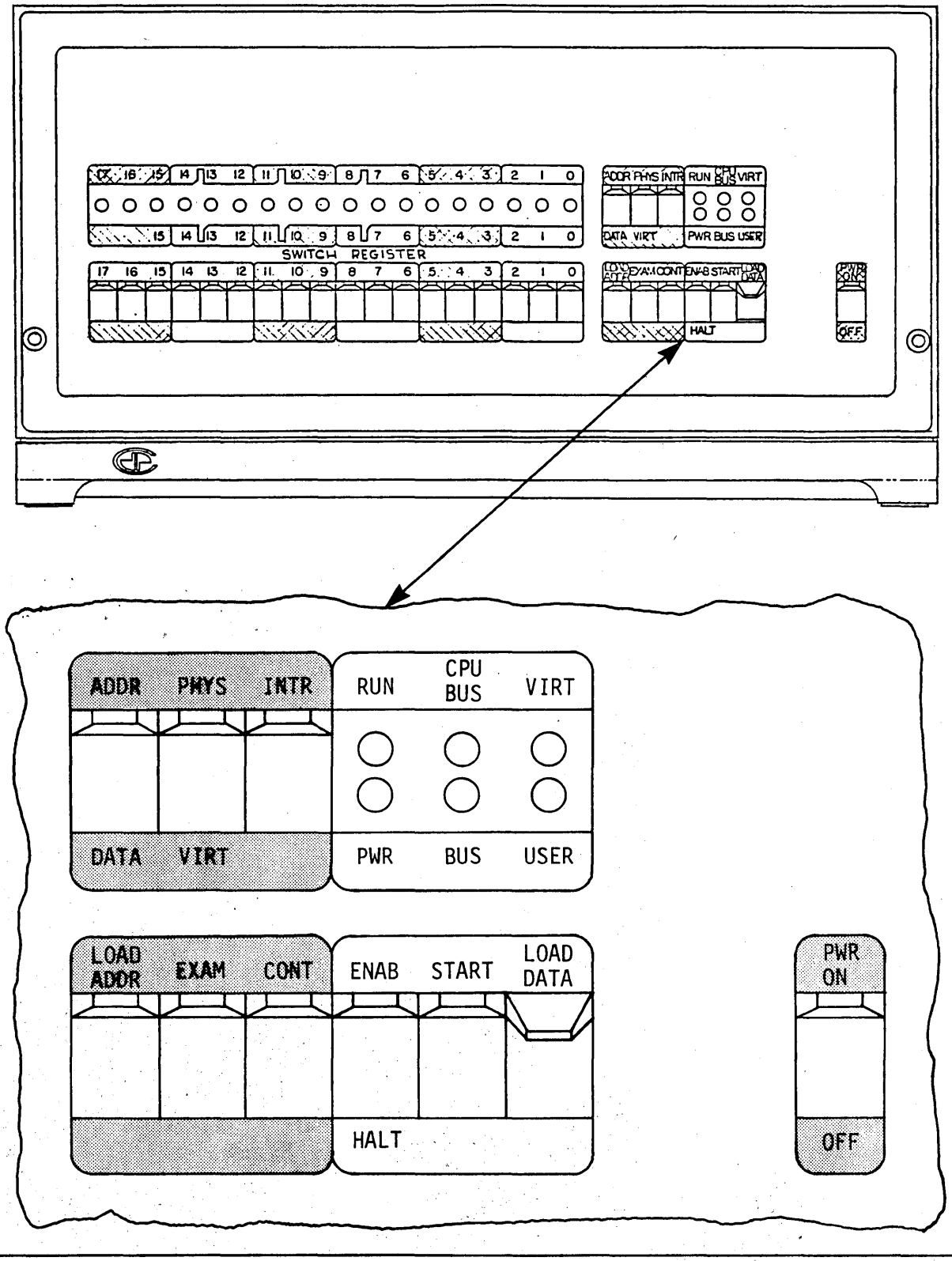

Figure 1-1. Cal Data 135 Macropanel Cover (Typical)

SECTION 2
OPERATION

2.1 GENERAL

The explanation of the operation of the Macropanel in this section is based on the block diagram in Figure 2-1. Each operation that the Macropanel is capable of performing is fully described. Wherever possible, the following information about a particular operation is provided:

a. When it takes place

b. Under what conditions it takes place

c. How it is initiated and by what unit

d. What happens on the Macropanel board

e. What the result is

For troubleshooting, Section 3 describes the logic with reference to the schematic diagram.

2.2 MACROBUS CONTROL

The Macropanel operates as a MACROBUS device. Interpretive microprogram routines become operational and service the Macropanel when the CPU halts. These routines provide the basic system displays and controls, as well as additional convenience functions, and are completely transparent to to the user. The Macropanel can operate the CPU in the run and manual modes.

The only active control switches in the program run mode are Macropanel interrupt (INTR) and enable/halt (ENAB/HALT). In addition, the Macropanel switch register can be read or tested by CPU microcommands. Although it is not a control switch, the power (PWR) switch on the Macropanel can connect and disconnect power to the computer in all operating modes, and must therefore be used with care.

2.2.1 MACROBUS Addresses

An address decoder detects Macropanel addresses on the MACROBUS Address lines, decodes them and asserts enabling signals to the appropriate Macropanel logic sections. The detected addresses are:

a. Line-Frequency Clock address 777546_8

b. Control-switch/display-indicator address 777540_8

c. Switch-register address 777570_8

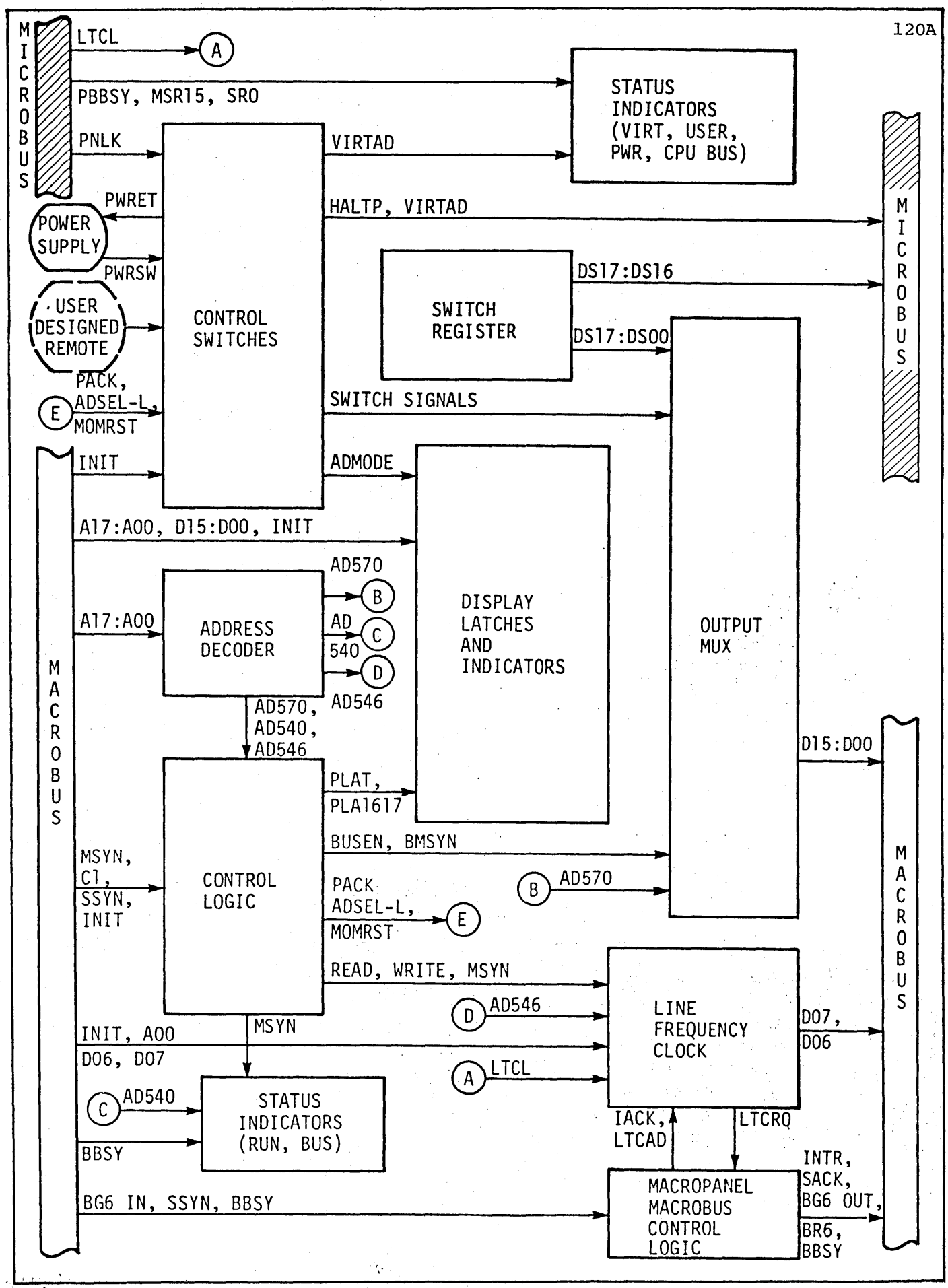

Figure 2-1. Cal Data 1 Macropanel Simplified Block Diagram

2.3 OPERATOR CONTROL

2.3.1 Control Switches and SWITCH REGISTER Switches

The switches on the Macropanel permit manual control of the system with the aid of controlling firmware.

The state of either the control switches or SWITCH REGISTER switches can be read by the CPU. This is done by executing a data input operation addressing the Macropanel, since the Macropanel is a MACROBUS device. A separate address is used for each set of switches to be read, as described in paragraph 2.2.1.

2.3.2 Status and Display Indicators

The indicators on the Macropanel inform the user of the status of the system. The display indicators and some of the status indicators monitor the state of signals on the MACROBUS. Status indicators VIRT, USER, PWR and CPU BUS are set internally by the Macropanel logic and the state of signals on the Microbus.

2.4 LINE-FREQUENCY CLOCK

The Line-Frequency Clock (LFC) generates a CPU interrupt 50 or 60 times per second, depending on the ac power source. The interrupt is the result of a sequence of signals beginning with a Line-Transition Clock (LTCL) originating in the power supply (described in a separate manual). If the LFC interrupt is enabled, an LFC interrupt request (LTCRQ) is transmitted to the MACROBUS priority logic, which generates a MACROBUS request on priority level 6 (BR6). If no higher-priority Bus Request is pending and if the CPU priority level is 5 or lower, a Bus-Grant signal (BG6) is asserted and the Macropanel takes control of the MACROBUS. The priority logic and LFC generate an interrupt request (INTR) along with the Macropanel interrupt address (100_8; that is, D06 asserted). When acknowledged by the CPU, the interrupt request is removed and control of the MACROBUS is given up by the Macropanel. The CPU then executes the LFC interrupt routine. Macropanel MACROBUS priority logic is provided solely to service LFC interrupts.

Interrupt requests from the LFC can be enabled or disabled by the CPU. This is done by addressing the LFC (777546_8) with an output word of data. When set to ONE, bit 06 of the data word (D06) enables the generation of interrupt requests from the LFC and resets any interrupt request already generated. This control of the LFC is permitted only for a correct word-mode Macropanel address. If the byte mode is detected and A00 is set to ONE, LFC control is inhibited. If the byte mode is detected and A00 is reset to ZERO, the Macropanel responds as described above.

The status of the LFC can be read by the CPU by executing a data input operation addressing the LFC. The LFC responds by transmitting two MACROBUS data bits:

Bit	Meaning
D07	State of LFC interrupt request
D06	State of LFC interrupt enable logic

SECTION 3
CIRCUIT DESCRIPTIONS

3.1 GENERAL

The following paragrpahs present detailed descriptions of the major functional areas outlined in Figure 2-1. The signals described are shown as found on the schematic diagram and are defined in Appendix A.

In the detailed presentation, neither every signal nor every logic grouping is described. Those described are considered of basic importance to an understanding of the hardware circuitry. The reader is presumed to be knowledgeable in the reading of schematics and comprehension of common logic configurations.

3.1.1 Diagram Symbols

The meaning of symbols used on the diagrams in this section is defined below:

a. The MACROBUS or Microbus bar or a rounded terminator indicates entry to or exit from the Macropanel.

b. The pointed, pentagonal, off-page connector indicates entry from or exit to another functional area of the Macropanel.

c. Rectangular boxes are groups of logic elements labled as to function.

d. Where applicable, standard logic symbols are used to represent gates, flip-flops, etc.

3.2 ADDRESS DECODER AND CONTROL LOGIC

The address decoder (Figure 3-1) detects Macropanel addresses on MACROBUS Address lines A17 to A00, and provides enabling signals used to generate control signals for all areas of the Macropanel. The detected addresses are:

a. LFC address 777546_8

b. Control-switch/display-indicator address 777540_8

c. Switch-register address 777570_8

These addresses are decoded to produce representative signals AD546, AD540 and AD570. Furthermore, either switch-address signal, AD540 or AD570, asserts Address Select (ADSEL), also used as a control enabling signal.

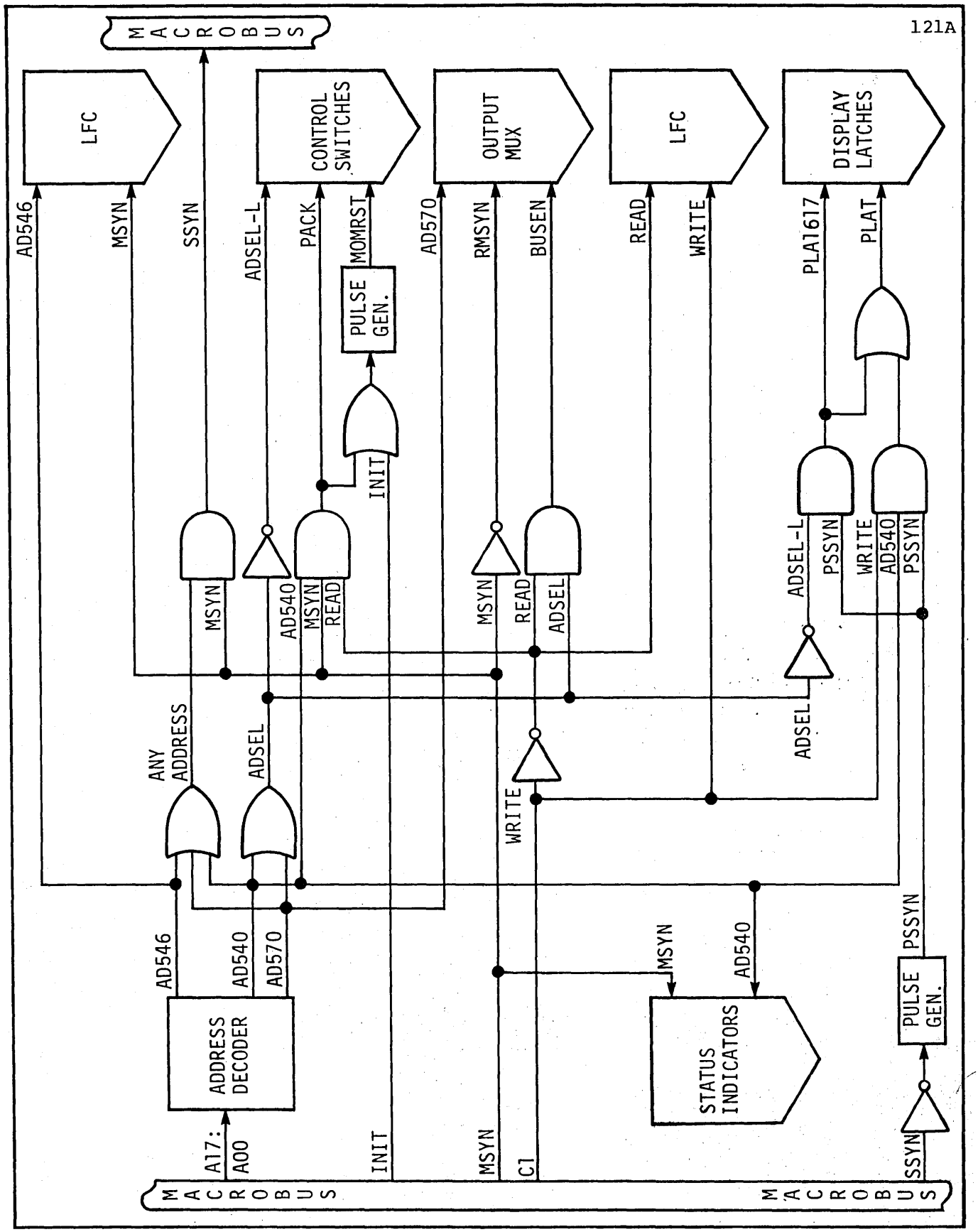

Figure 3-1. Address Decoder and Control Logic

3.2.1 Macropanel Operation

Interaction of the Macropanel with the CPU begins when Master Synchronization (MSYN) is received on the MACROBUS along with any Macropanel address. When this occurs, Slave Synchronization (SSYN) is transmitted to the MACROBUS to signify acceptance of the command. Mode Control signal C1 from the MACROBUS specifies to the Macropanel whether the operation to be performed is data in (READ) or data out (WRITE).

AD540 or AD570 generates ADSEL, used to control functions associated with any non-LFC Macropanel operation. During a read operation, ADSEL generates Bus Enable (BUSEN), which enables data selected by the output multiplexer (MUX) to be placed on the MACROBUS. The data selected are determined by AD570.

AD540, as the control-switch address, enables READ and MSYN to inhibit the Macropanel control switches by generating Panel Clock (PACK). This prevents stored switch settings (refer to subsection 3.3) from being changed while the information is being read. To clear the stored switch settings after a read operation, the termination of PACK generates a Momentary Reset signal (MOMRST). MOMRST is also generated by INIT during a MACROBUS initialization operation.

AD540, as the display indicator address, enables WRITE to load Macropanel display latches 15 to 00 from the MACROBUS data lines when SSYN ends (established by a PSSYN pulse). This is done by generating Panel Latch (PLAT). Only 16 latches are enabled during a write operation, since only 16 data bits can be transferred at one time on the MACROBUS.

PLAT and PLA1617 (Panel Latches 16 and 17) are both generated momentarily by PSSYN when SSYN ends and no switch or indicator operation is taking place (ADSEL off). This enables the Macropanel to continuously monitor MACROBUS data or address values. PLA1617 allows bits 16 and 17 to be loaded. These are utilized to display addresses.

AD546, the LFC address, is transmitted to the LFC (subsection 3.8) along with MSYN, READ and WRITE.

The Macropanel can be disabled while system power is on. This is done with the PANEL LCK switch setting on the back of the power supply, which asserts the Panel Lock signal (PNLK) to the Macropanel.

3.3 CONTROL SWITCHES

Control switches on the Macropanel permit manual control of the system with the aid of the controlling firmware. In addition to the 18-switch-register switches (subsection 3.4), the Macropanel has the following control switches (Figure 3-2) readable at address 777540_8:

a. Power (PWR ON/OFF)

b. Load address (LOAD ADDR)

c. Start (START)

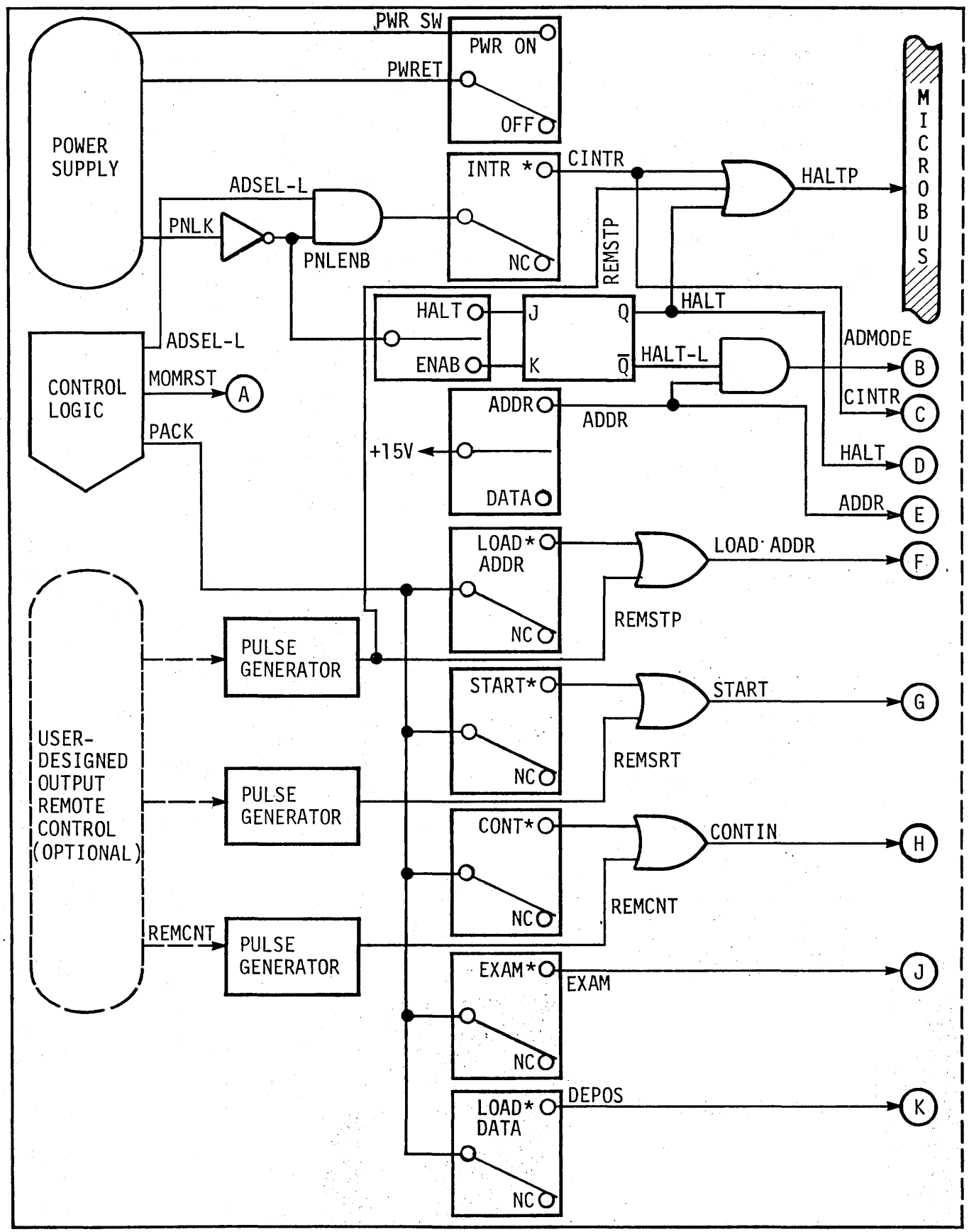

Figure 3-2. Control Switches (continued)

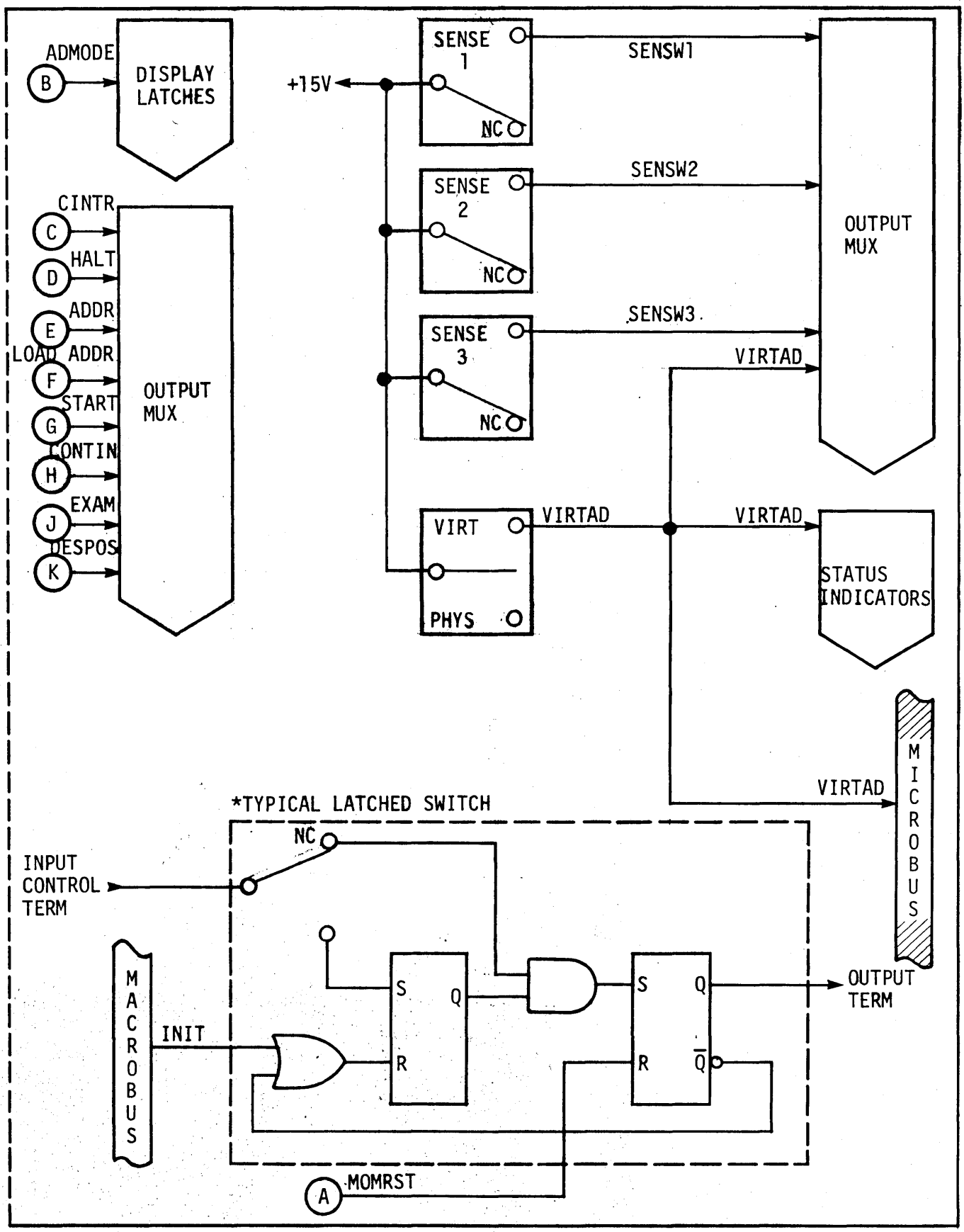

Figure 3-2. Control Switches (continued)

d. Continue (CONT)

e. Examine (EXAM)

f. Load data (LOAD DATA)

g. Macropanel interrupt (INTR)

h. Enable/halt (ENAB/HALT)

i. Address/data (ADDR/DATA)

j. Sense (SENSE 1, 2, 3)

k. Physical/virtual (PHYS/VIRT)

3.3.1 PWR

The PWR switch connects and disconnects the Power Return (PWRET) loop from the power supply. PWRET affects the power relay in the power supply in such a way that PWR must be set to ON for the relay to turn on the power supply (provided that the power supply MAIN PWR switch is also ON).

When PWR is set to OFF, the power supply goes off and cannot turn on.

3.3.2 LOAD ADDR, START, CONT, EXAM and LOAD DATA

The LOAD ADDR, START, CONT, EXAM and LOAD DATA switches are five of six that have latched outputs. Each switch and two latches interact in such a way that the switch must be pressed and released when the switch is enabled (PACK OFF) before an output is generated. Pressing the switch sets the first latch, enabling the second latch to be set when the switch is released. The second latch provides the output of the switch circuitry, which is sent to a particular bit of the output MUX (subsection 3.6).

Provision is made for interfacing the Macropanel with a user-designed remote control for the halt, start and continue functions. Outputs of the LOAD ADDR, START and CONT switches are ORed with remote signals REMSTP, REMSRT and REMCNT (Remote Stop, Start and Continue, respectively). REMSTP also generates Panel Halt (HALTP, refer to paragraph 3.3.3) transmitted to the CPU via the Microbus. In this way, REMSTP initiates a CPU firmware interrupt routine that leads to reading of the Load Address indication, also produced by REMSTP. The latches are reset by INIT from the MACROBUS and MOMRST from the control logic. MOMRST is generated after a switch read operation to prepare the latches for new switch data. MOMRST resets the second latch, which resets the first latch. INIT also generates MOMRST and directly resets the first latch.

3.3.3 INTR

The INTR switch has a latched output (CINTR), as described for other switches in paragraph 3.3.2. CINTR is sent to bit 07 of the output MUX (subsection 3.6). The control term enabling generation of CINTR is

Macropanel Enable (PNLENB) from the power supply panel lock switch (signal PNLK) when ADSEL is off, signifying that no Macropanel switch or indicator operation is taking place.

CINTR is one of three signals that generates Panel Halt (HALTP) to the CPU. The CPU responds by executing a firmware interrupt routine that reads the Macropanel switches and performs other operations as required. Other signals that generate HALTP for CPU processing are HALT and Remote Stop (REMSTP).

3.3.4 HALT/ENAB

The HALT/ENAB switch uses a single output latch to store a HALT indication. HALT is sent to bit 15 of the output MUX (subsection 3.6). The control term enabling generation of HALT is PNLENB from the power supply panel lock switch (signal PNLK).

HALT is one of three signals that generates HALTP to the CPU. This results in a firmware routine that reads the Macropanel switches and performs other operations, as required.

When the HALT/ENAB switch is set to ENAB, HALT-L is provided by the output latch. HALT-L and ADDR from the ADDR/DATA switch (paragraph 3.3.5) generate ADMODE, selecting address or data to be displayed or transmitted.

3.3.5 ADDR/DATA

The ADDR/DATA switch is always enabled and produces Address signal ADDR when set to ADDR. When ADDR is off, the switch is assumed to be set to DATA.

ADDR is sent to bit 08 of the output MUX (subsection 3.6) and is enabled by HALT-L (when the Macropanel is enabled) to generate Address Mode (ADMODE), which determines whether data or addresses (ADMODE true) are displayed.

3.3.6 SENSE 1, 2 and 3

The SENSE switches are always enabled and, when set, provide outputs to particular bits of the output MUX (subsection 3.6).

Not all systems use SENSE switches. In such cases, the switches are removed from the Macropanel, although the internal circuitry remains in place.

3.3.7 PHYS/VIRT

The PHYS/VIRT switch is always enabled and, when set to VIRT, provides a Virtual Address signal (VIRTAD) to bit 06 of the output MUX (subsection 3.6). VIRTAD also turns on a status indicator and is transmitted to the optional Memory Management Unit (MMU) via the Microbus. In the MMU, VIRTAD enables address relocation. When VIRTAD is off (PHYS/VIRT set to PHYS), addresses handled by the MMU are considered to be physical addresses and are not relocated.

Not all systems use PHYS/VIRT (no MMU present). In such cases, the switch may be removed from the Macropanel, although the internal circuitry remains in place.

3.4 SWITCH REGISTER

The 18 SWITCH REGISTER switches (Figure 3-3) are used to set up a data word or address to be transferred to the MACROBUS via the output MUX (refer to subsection 3.6). The MACROBUS Data lines are used even when the switch information is an address. For an address, bits 16 and 17 are read separately as status bits, since only a 16-bit word can be transferred on the MACROBUS data lines. DS17 and DS16 are also placed on the Microbus for use by the MMU, described in a separate publication.

Since the switch register is read by the CPU by accessing address 777570_8, the switches can be used for sense-switch type control of an operating software system.

3.5 DISPLAY LATCHES AND INDICATORS

Eighteen indicators (Figure 3-4) display either a data or address word read from the MACROBUS. The information displayed is selected by the ADDR/DATA switch. Set to ADDR, the switch generates ADMODE, which selects an address display. Otherwise, data are displayed.

The selected display information is stored in latches that drive the light-emitting diode (LED) indicators. During a display indicator write operation, PLAT is generated to load latches 15 to 00. Only these latches are loaded since only 16 bits can be transferred at one time on the MACROBUS. At all other times, PLAT and PLA1617 are generated immediately after each MACROBUS transaction, loading all display latches to continuously monitor MACROBUS data or address values.

3.6 OUTPUT MULTIPLEXER

The output MUX (Figure 3-5) selects a 16-bit word of data or status bits to be placed on the MACROBUS. The word to be selected is determined by AD570 and BUSEN from the address decode and control logic. BUSEN enables the selected word to be transferred through the MUX, but is generated only during a read operation when either AD540 or AD570 (switch addresses) is on. AD570 on selects switch-register data (DS15 to DS00). AD570 off (with BUSEN on) indicates that AD540 is on and selects status data from both the switch register and control switches. Table 3-1 explicitly defines the meaning of each status bit.

The word output from the MUX is placed on the MACROBUS at the proper time by MSYN (buffered as BMSYN).

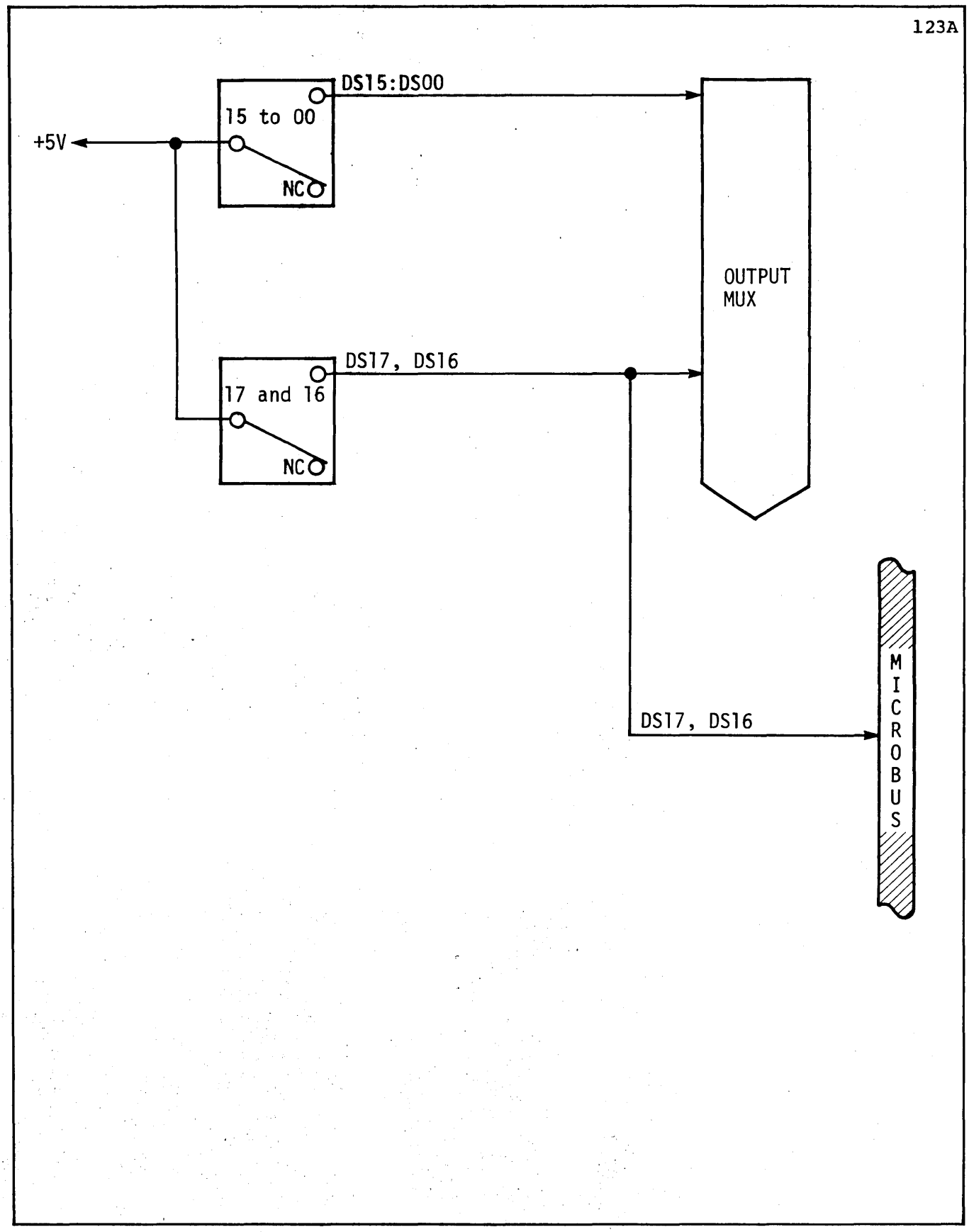

Figure 3-3. Switch Register

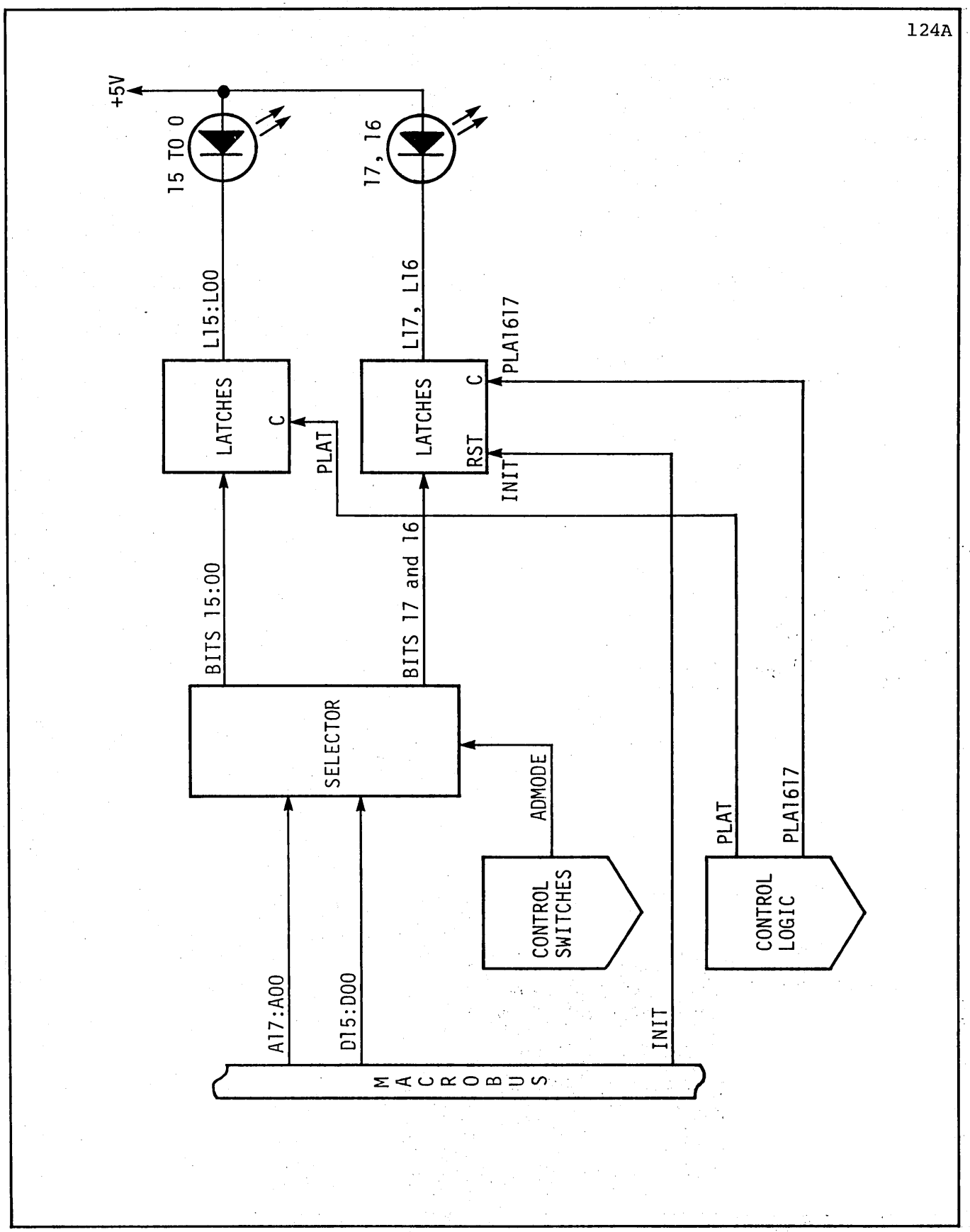

Figure 3-4. Display Latches and Indicators

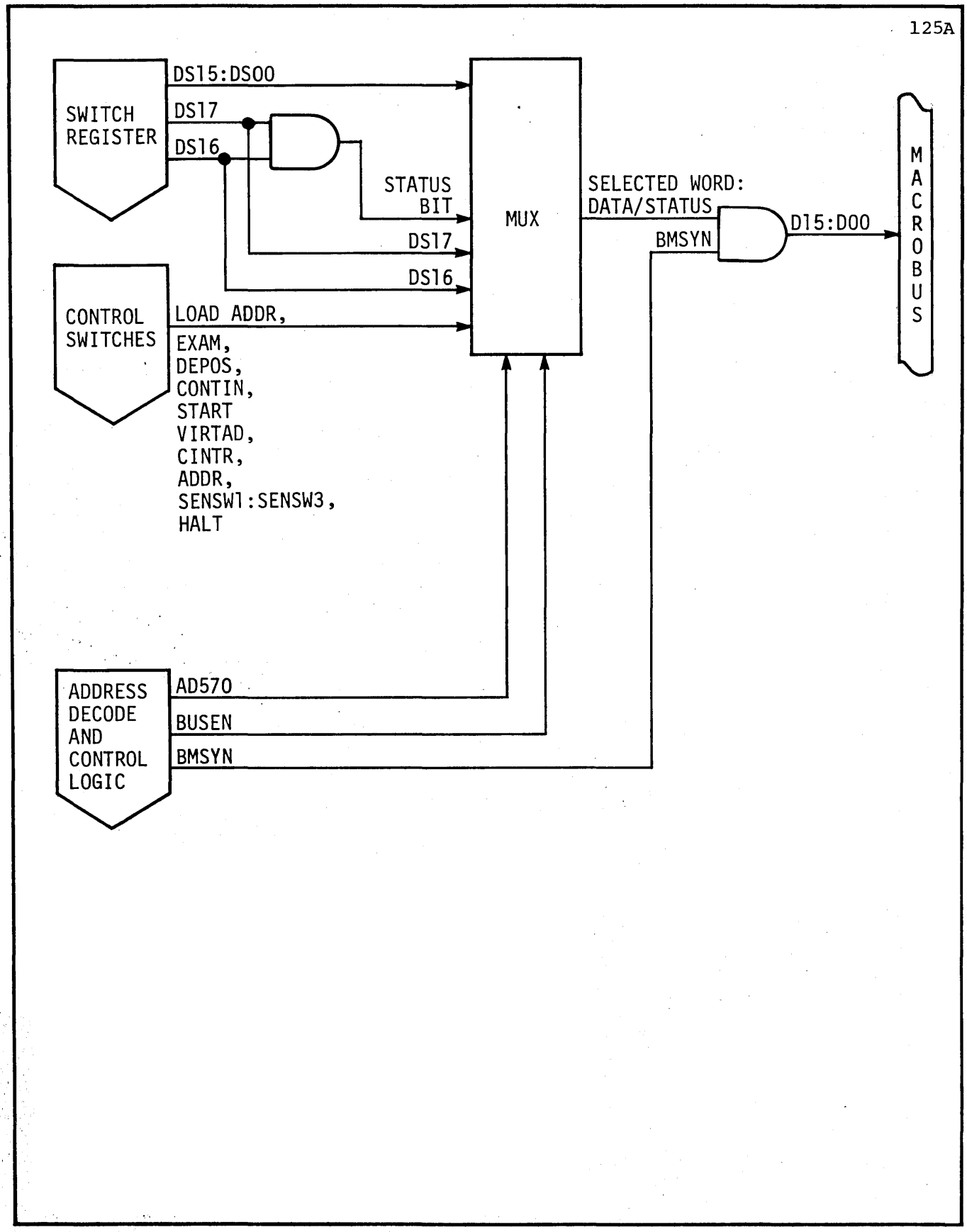

Figure 3-5. Output Multiplexer

Table 3-1. Data Read From MACROBUS Address 777540_8

Data Bit Read	Information	Switch Setting
D15	Setting of enable/halt switch	1 = ENAB 0 = HALT
D14	Setting of switch-register bit 17 (DS17)	1 = up 0 = down
D13	Setting of switch-register bit 16 (DS16)	1 = up 0 = down
D12	DS17 ANDed with DS16	
D11	Setting of sense switch 3, if any	1 = up 0 = down
D10	Setting of sense switch 2, if any	1 = up 0 = down
D09	Setting of sense switch 1, if any	1 = up 0 = down
D08	Setting of address/data switch	1 = ADDR 0 = DATA
D07	Setting of Macropanel interrupt switch	1 = down 0 = INTR
D06	Setting of physical/virtual switch	1 = PHYS 0 = VIRT
D05	Not used	
D04	Setting of start switch	1 = down 0 = START
D03	Setting of continue switch	1 = down 0 = CONT
D02	Setting of load-data switch	1 = LOAD DATA 0 = down
D01	Setting of examine switch	1 = down 0 = EXAM
D00	Setting of load-address switch	1 = down 0 = LOAD ADDR

3.7 STATUS INDICATORS

There are six status indicators (Figure 3-6): PWR, RUN, CPU BUS, BUS, VIRT and USER. These are LED indicators powered by +5 V and turned on by a low condition (nominally ground) at the cathode.

The PWR indicator is on when ac power is applied to the system and is off otherwise. It is connected from +5 V directly to ground.

The RUN indicator is off when the program is halted by a HALT instruction or the HALT/ENAB switch. Such a halt condition causes continuous addressing of the Macropanel (generating AD540) and transfer of Macropanel information, accompanied by MSYN. AD540 and MSYN inhibit the RUN indicator and prevent if from lighting. The RUN indicator is on when the CPU is not halted.

The CPU BUS indicator is on when the CPU has control of the MACROBUS and is off otherwise. It is turned on by the Processor Bus Busy signal (PBBSY) from the CPU.

The BUS indicator is on when any device, including the CPU, has control of the bus and is off otherwise. It is turned on by the MACROBUS Bus Busy signal (BBSY).

The VIRT indicator is on when the PHYS/VIRT switch is in the VIRT position (generating VIRTAD) and the optional MMU is installed and enabled (i.e., when the MMU is relocating virtual addresses), indicated by SR0 from the MMU.

The USER indicator applies only when the MMU is installed and the system is operating in the user mode. It is enabled by the MSR15 signal from the MMU. This indicates that bit 15 of the extended processor status word is set, specifying user mode.

3.8 LINE-FREQUENCY CLOCK

The LFC (Figure 3-7) generates a line-frequency interrupt at MACROBUS priority level 6 (BR6) to the CPU 60 (or 50) times per second. The MACROBUS address of the LFC is 777546_8.

The 60 (or 50) Hz Line-Transistion Clock signal (LTCL) from the power supply is shapped by a pulse generator to produce LCLK. LCLK (or the CPU Initialization signal, INIT sets the LFC clock flip-flop. When both this flip-flop and the LFC interrupt-enable flip-flop are set, an LFC Interrupt Request signal (LTCRQ) is asserted to the Macropanel MACROBUS control logic (subsection 3.9).

Program control of both LFC flip-flops is provided by data output MACROBUS operations from the CPU. A data output operation is signified in the LFC by DATO, developed from the LFC address (AD546), WRITE and MSYN from the control logic. DATO is inhibited during byte-mode operations with A00 set to ONE. DATO clocks in the dc inputs of the LFC flip-flops, resetting the LFC clock interrupt, and setting the LFC interrupt-enable flip-flop if data bit D06 is ONE. Thus, to write into the LFC, the CPU asserts the LFC address, a write command (C1 reset to ZERO), MSYN and D06 (ONE or ZERO) to either set or reset the interrupt-enable flip-flop. The clock flip-flop is unconditionally reset.

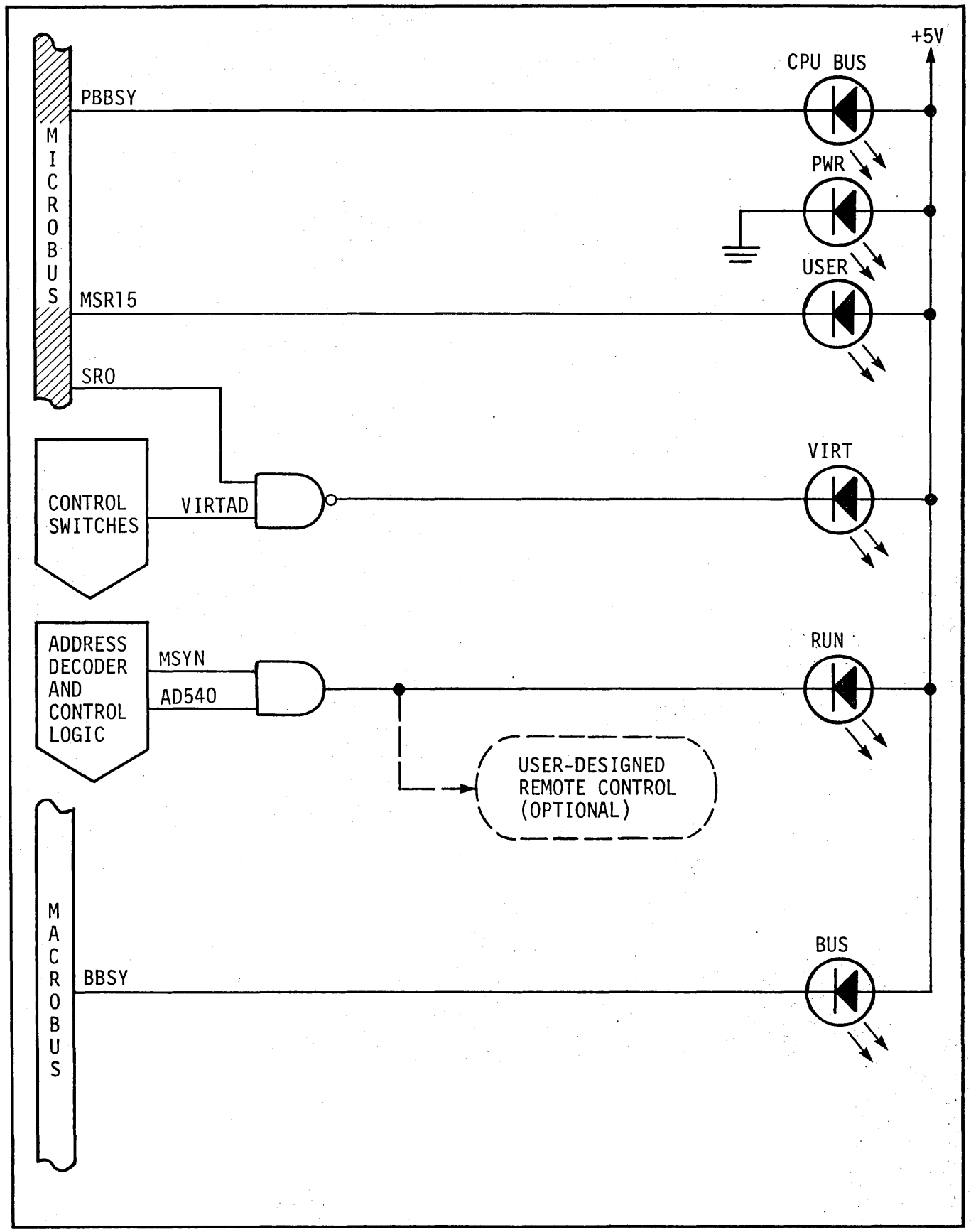

Figure 3-6. Status Indicators

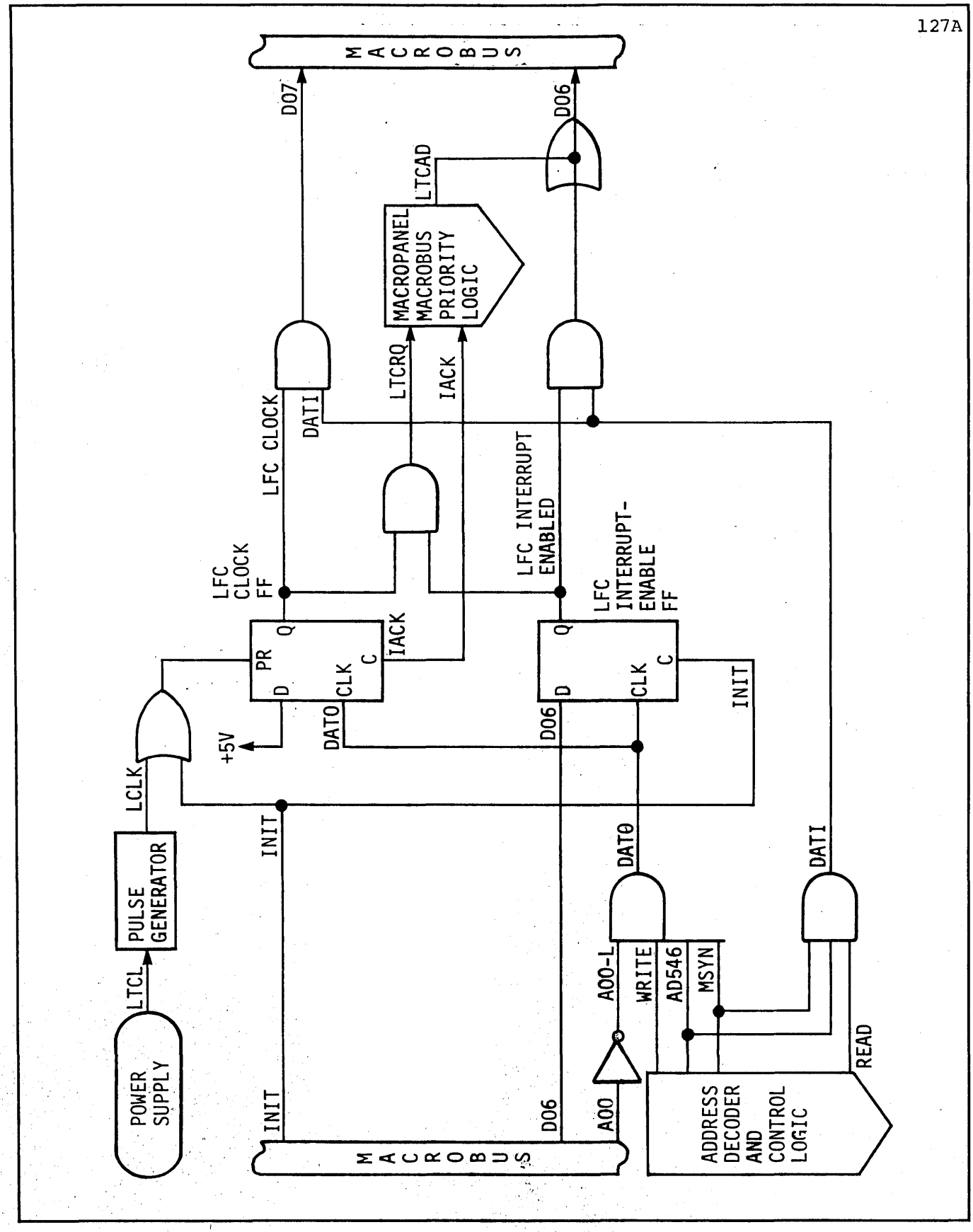

Figure 3-7. Line-Frequency Clock

The status of the LFC flip-flops are read by data input MACROBUS operations from the CPU. A data input operation is signified in the LFC by DATI, developed from AD546, READ and MSYN. DATI gates the true output of the clock flip-flop to D07 and of the interrupt-enable flip-flop to D06.

During interrupt requests (INTR), D06 is asserted on the MACROBUS to provide the Macropanel interrupt address (100_8). For this purpose, D06 is generated from the LFC Address signal (LTCAD) from the Macropanel MACROBUS control logic.

The Macropanel Interrupt Acknowledge signal (IACK) returns from the Macropanel MACROBUS control logic to reset the LFC clock flip-flop, turning off LTCRQ at the end of an LFC interrupt cycle.

The timing diagram in Figure 3-8 shows the relationship of selected signals described in this and in the next subsection.

The LFC is initialized by INIT to the following conditions:

a. LFC clock flip-flop set

b. LFC interrupt-enable flip-flop reset (disable)

3.9 MACROPANEL MACROBUS CONTROL LOGIC

The Macropanel MACROBUS control logic (Figure 3-9) provides the correct sequencing of signals for MACROBUS access during an LFC interrupt operation. This logic works closely with the LFC logic described in subsection 3.8.

The control logic comprises two interrupt-sequencer flip-flops (IS1 and IS2) and associated gating. The inactive state of the sequencer is with both IS flip-flops reset. This condition enables LFC Interrupt Request signal LTCRQ to assert BR6 to the MACROBUS Channel Adapter (MCA). BR6 is the first step in the MACROBUS sequence associated with a CPU interrupt, as shown in Figure 3-8.

Under control of the MCA, the Macropanel Bus Request is held until the CPU has no higher-priority requests pending. The MCA then asserts a Bus Grant (BG6) to the Macropanel, which sets IS1. IS1 set with IS2 reset turns off BR6 and asserts Selection Acknowledge (SACK) on the MACROBUS.

Within the Macropanel MACROBUS control logic, SACK is used to inhibit the propogation of BG6. So that SACK has ample time to be generated, BG6 is delayed in the MACROBUS control logic.

In response to SACK, BG6 and Bus Busy (BBSY) are removed by the MCA. This MACROBUS condition, along with SSYN remaining off and IS2 being reset, sets IS2. With IS1 and IS2 set, the sequencer removes SACK, asserts BBSY and generates an Interrupt Request (INTR) to the MCA.

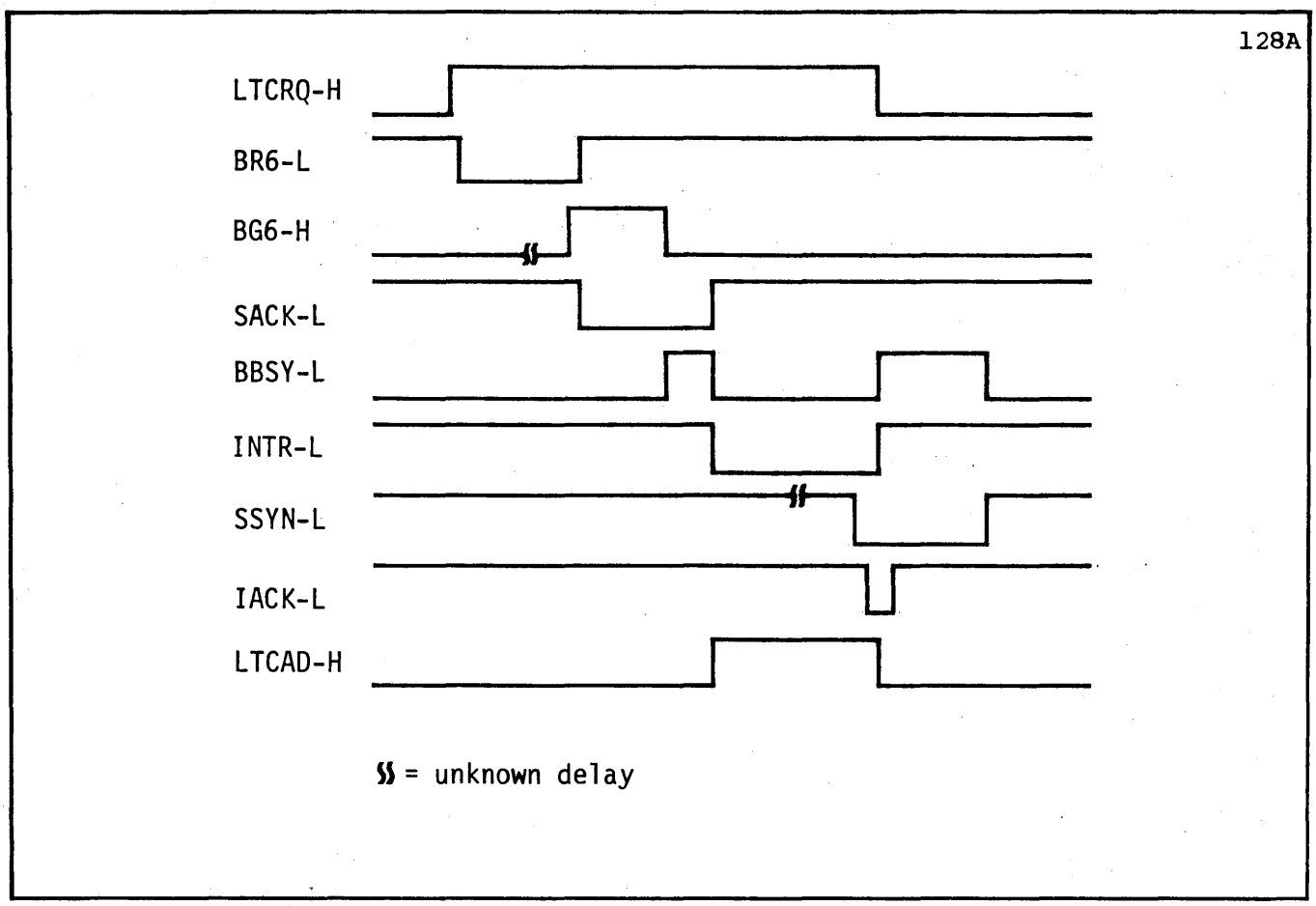

Figure 3-8. LFC MACROBUS Timing

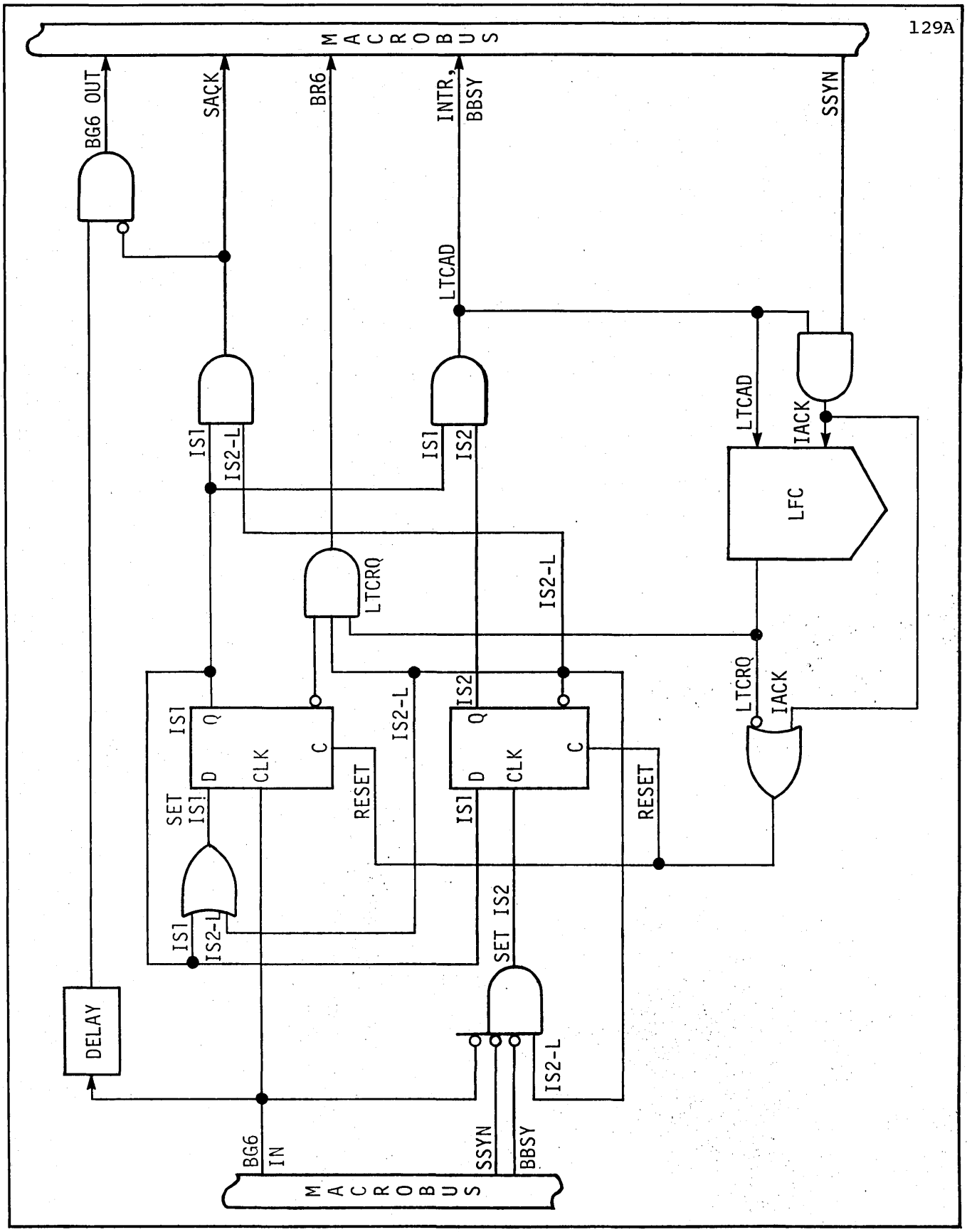

Figure 3-9. Macropanel MACROBUS Control logic

The LFC address signal (LTCAD) is also applied to the LFC logic to generate the LFC interrupt address (D06).

On completion of the interrupt routine, the CPU asserts Slave Synchronization (SSYN), which is enabled by LTCAD to generate an Interrupt Acknowledge signal (IACK). IACK resets both sequencer flip-flops and is applied to the LFC to reset the clock flip-flop, which turns off LTCRQ and all MACROBUS signals from the Macropanel. LTCRQ off maintains the sequencer flip-flops in the reset state.

If BR6 is asserted other than from the LFC, LTCRQ remains off, holding IS1 and IS2 in the reset state. When BG6 is received, it cannot set IS1 to generate SACK, but it is nevertheless delayed for a short period in the Macropanel MACROBUS control logic. Since SACK is not generated, BG6 OUT is propogated to the next MACROBUS device.

APPENDIX A
SIGNAL GLOSSARY

Table A-1 is a glossary of signal names used on the Macropanel schematic. On the schematic, the suffix "-L" on a mnemonic indicates that the signal is asserted (true) when in the low state. This suffix is omitted in Table A-1 and in text.

Table A-1. Cal Data 1 Macropanel Signal Glossary

Mnemonic	Name
A15:A00	Address, bits 15 to 00
A540	MACROBUS Address 777540_8 (panel switches)
A546	MACROBUS Address 777546_8 (LFC)
A570	MACROBUS Address 777570_8 (switch register)
ACMSL	Alterable Control Memory Select
AD540	MACROBUS Address 777540_8 Decoded (Switches)
AD546	MACROBUS Address 777546_8 Decoded (LFC)
AD570	MACROBUS Address 777570_8 Decoded (switch register)
ADDR	Address
ADMODE	Address Mode
ADSEL	Address Select
AUXRM	Auxiliary ROM
BBSY	Bus Busy
BG7 IN:BG4 IN	Bus Grant In, lines 7 to 4
BG7 OUT:BG4 OUT	Bus Grant Out, lines 7 to 4
BMSYN	Bus Master Synchronization
BUS A17:BUS A00	(MACROBUS) Address, bits 17 to 00
BUS ACLO	(MACROBUS) AC Low
BUS BBSY	(MACROBUS) Bus Busy
BUS BG7:BUS BG4	(MACROBUS) Bus Grant, bits 7 to 4
BUS BR7:BUS BR4	(MACROBUS) Bus Request, lines 7 to 4
BUS C1 amd BUS C0	(MACROBUS) Control, bits 1 and 0
BUS D15:BUS D00	(MACROBUS) Data, bits 15 to 00
BUS DCLO	(MACROBUS) DC Low
BUSEN	Bus Enable
BUS INIT	(MACROBUS) Initialize
BUS INTR	(MACROBUS) Interrupt Request
BUS MSYN	(MACROBUS) Master Synchronization
BUS NPG	(MACROBUS) Nonprocessor Grant
BUS NPR	(MACROBUS) Nonprocessor Request
BUS SACK	(MACROBUS) Slave Acknowledge
BUS SSYN	(MACROBUS) Slave Synchronization
CC11:CC00	Microcommand Counter, bits 11 to 00
CINENB	Macropanel Interrupt Enable
CINTR	Macropanel Interrupt
CM47:CM00	Control Memory, bits 47 to 00
CONTIN	Continue

Table A-1. (continued)

Mnemonic	Name
CPEN	cropanel Enable
D15:D00	Data, bits 15 to 00
DAD03:DAD00	Decode Address, bits 03 to 00
DATI	(LFC) Data-In
DATISP	Address/Data Switch
DATO	(LFC) Data-Out
DEPOS	Deposit (load data)
DMSYN	Device Master Synchronization
DS17:DS00	Display Switch, bits 17 to 00
EMINH	Emulate Inhibit
EXAM	Examine
FPHALT	Front Panel Halt
GND	Ground
HALT	Halt
HALTP	Panel Halt
HLINT	Halt Interrupt
IACK	Interrupt Acknowledge
INIT	Initialize
IRINH	Instruction Run Inhibit
IRPTE	Instruction Repeat
IWAIT	Instruction Wait
LCLK	Line Clock
LD ADDR	Load Address Switch
LOAD ADDR	Load Address
LTCAD	LFC Address
LTCL	Line-Transition Clock
LTCRQ	LFC Interrupt Request
MB15:MB00	M Bus, bits 15 to 00
MOMRST	Momentary Reset
MSR15	MMU Status, bit 15
MSYN	Master Synchronization
PACK	Panel Clock
PBBSY	Processor Bus Busy
PFINT	Power Failure Interrupt
PLA1617	Panel Latch 16 and 17
PLAT	Panel Latch
PNLENB	Panel Enable
PNLK	Panel Lock
PSSYN	Panel Slave Synchronization (momentary)
PWRET	Power Return
READ	Read
REMCNT	Remote Continue
REMSRT	Remote Start
REMSTP	Remote Stop
SACK	Selection Acknowledge
SENSW3:SENSW1	Sense Switch 3 to 1
SR0	Status Register, bit 0
SR17:SR00	Switch Register, bits 17 to 00
SSYN	Slave Synchronization

Table A-1. (continued)

Mnemonic	Name
START	Start
STRT	Start Switch
SYSCK	System Clock
VIRTAD	Virtual Address
WRITE	Write
+5V	+5 Vdc
-15V	-15 Vdc