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Am96/1000 Series Dynamic Random-Access Memory Boards

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Address comments concerning this manual to:

ADVANCED MICRO COMPUTERS
Publications Department
3340 Scott Boulevard
Santa Clara, CA 95051

PREFACE

This manual provides general information, an installation and interface guide, principles of operation, and service information for the Advanced Micro Computers Am96/1000 Series Dynamic RAM Boards. Reference Am96/4016B manual when memory board is used in conjunction with 4016B. Additional information is available from the Intel Multibus† Interfacing Application Note AP-28A.

In this manual both active-high (positive true) and active-low (negative true) signals appear in the text. To eliminate confusion and simplify presentation, the following convention is adhered to: whenever a signal is active-low (negative true), its mnemonic is followed by an asterisk (*) (i.e., MEMR* denotes an active-low signal). For a signal that is active-high the asterisk is omitted (i.e., IORW denotes an active-high signal).

The information in this manual is believed to be accurate and complete at the time it was printed. However, AMC reserves the right to change specifications without notice. No responsibility is assumed for errors that might appear in this manual. No part of this manual may be copied or reproduced in any form without prior written permission from AMC.

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CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The Am96/1000 Series RAM Boards are single board dynamic random access memory systems of from 32 to 128K bytes; designed to support Multibus compatible 8 or 16-bit microcomputers, the AmSYS8/8, and AMC MonoBoard Computers. In addition to accommodating up to 128K bytes of storage, the Am96/1000 Series provides dual-port memory accessing, optional byte parity, and an interrupt capability via the Multibus and the P2 Bus. Table 1-1 is the four models of the Am96/1000 produced.

TABLE 1-1. Am96/1000 SERIES RAM MODELS

Model No.	Memory Size
Am96/1032	32K bytes
1064	64K bytes
1096	96K bytes
1128	128K bytes

On-board jumpers enable placement on any 4K-byte address boundary within the 1-megabyte address space of the Multibus and any 64K-byte address boundary within the 16-megabyte address space of the P2 Bus. In addition, on-board control and refresh logic maintain the integrity of the stored data. Refresh occurs automatically and is user transparent.

Features of an Am96/1000 are:

- 32K, 64K, 96K, and 128K byte storage options.
- High-speed operation up to 4 MHz with high performance CPUs (AmZ8000) using the P2 bus with synchronous operation.
- 8-bit/16-bit data bus compatibility for most 8 bit or 16-bit microcomputers.
- Jumper options for advanced acknowledge (AACK) signal to improve response time and throughput.
- Optional parity in both byte and word mode with interrupt capability.

- Dual Bus accesses provide a global RAM link between P1 Multimaster connector and P2 auxiliary connector.
- Address space on 4K byte boundary.
- Multibus and iSBC-80 compatible.

1-2. PHYSICAL DESCRIPTION

Circuit components are mounted on a single four layer printed circuit board as shown in Figure 1-1. Two edge connectors, P1 and P2 provide bus interface. P1 is a standard Multibus† connector described in the manufacturer's literature. P2 is a general purpose configuration that provides a synchronous bus for single processor applications where high performance is desired. Signal descriptions for the P2 bus are listed in tables 2-11, 2-12, and 2-13. This bus can be jumper-selected to support two configurations. A 4 MHz Z8000 can be supported on the general purpose bus with no wait states. When used along with the Multibus connector, the Am96/1000 series RAM board can function as a global link between two systems; a Multibus based system communicates on P1 and a high performance system communicates on P2. The second P2 configuration is used exclusively to interface the Am96/4016B Evaluation Board to the Am96/1000 Series RAM Board.

Maximum memory storage capacity of an Am96/1000 Series RAM Board, 64Kx18 or 128Kx9, is provided by sixty-four 16Kx1 dynamic RAM chips plus eight RAM chips for byte parity. Memory array is organized as four 32K-byte blocks, each contains two 16K-byte pages of high and low data bytes including parity. Nine RAM chips make up the 16K bytes of data plus parity of one page.

Address boundaries, interrupt levels, memory size configurations, and bus configurations are jumpers described in Chapter 2. Control and refresh logic maintain integrity of stored data without CPU supervision. Contention between refresh cycles and read or write cyles is resolved by the control logic.

1-3. FUNCTIONAL DESCRIPTION

The Am96/1000 Series RAM Boards are single board memory systems used in support of Multibus compatible 8-bit or 16-bit microcomputers, the Am96/4016B AmZ8000 Evaluation Board, [either internal or external to System 8 (AmSYS8/8)], the AmZ8000 Real-Time Emulator (RTE-16), and AMC MonoBoard computers. Two specific functions that enhance a microcomputer system using an Am96/1000 series RAM are dual-port memory accessing and optional byte parity.

A functional block diagram of an Am96/1000 Series RAM Board is shown in Figure 1-2. The board stores or transmits words (16 bits) or bytes (8 bits) in two functional configurations:

† Multibus is a registered trademark of Intel Inc.

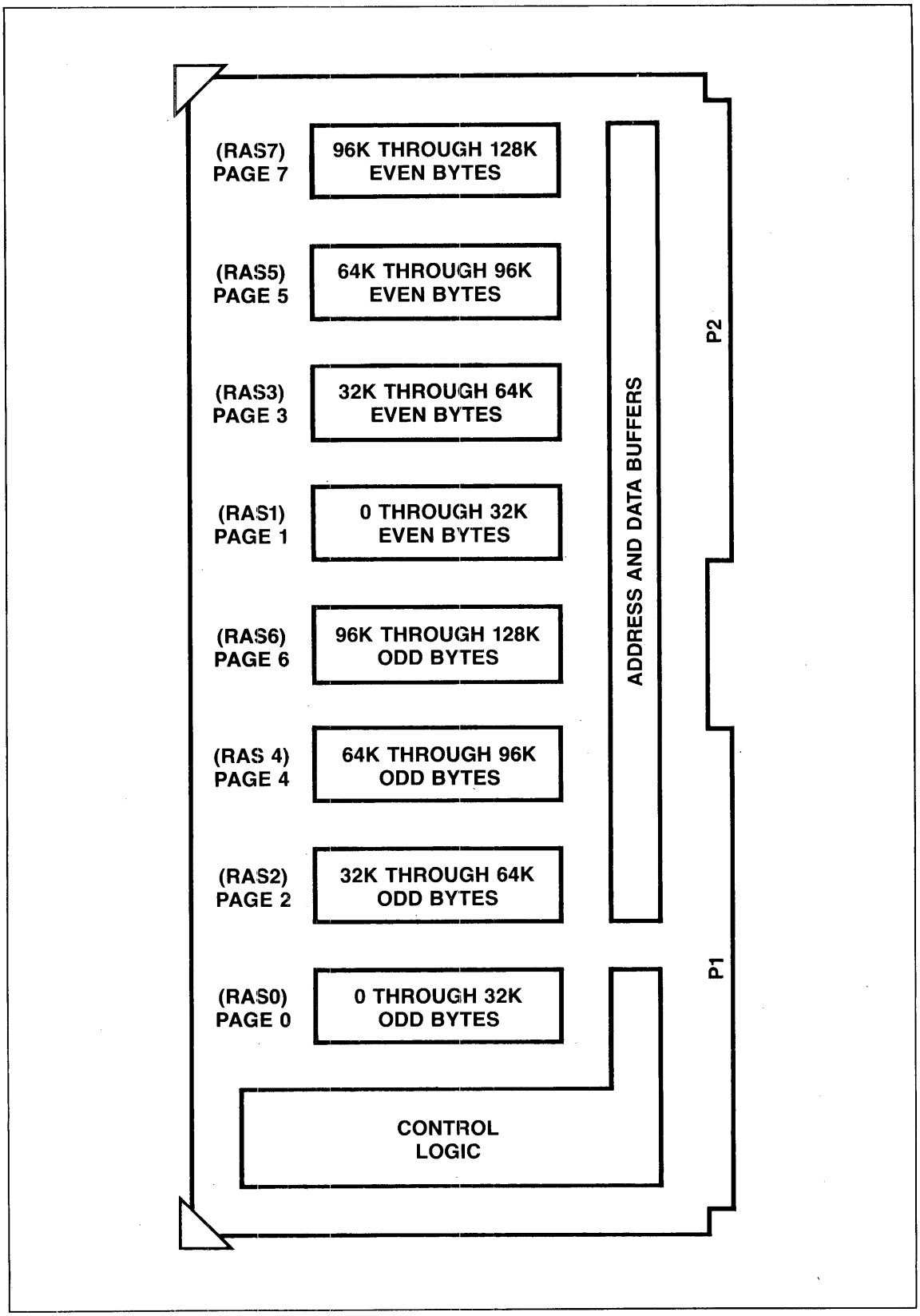


Figure 1-1. 96/1000 Circuit Components Diagram

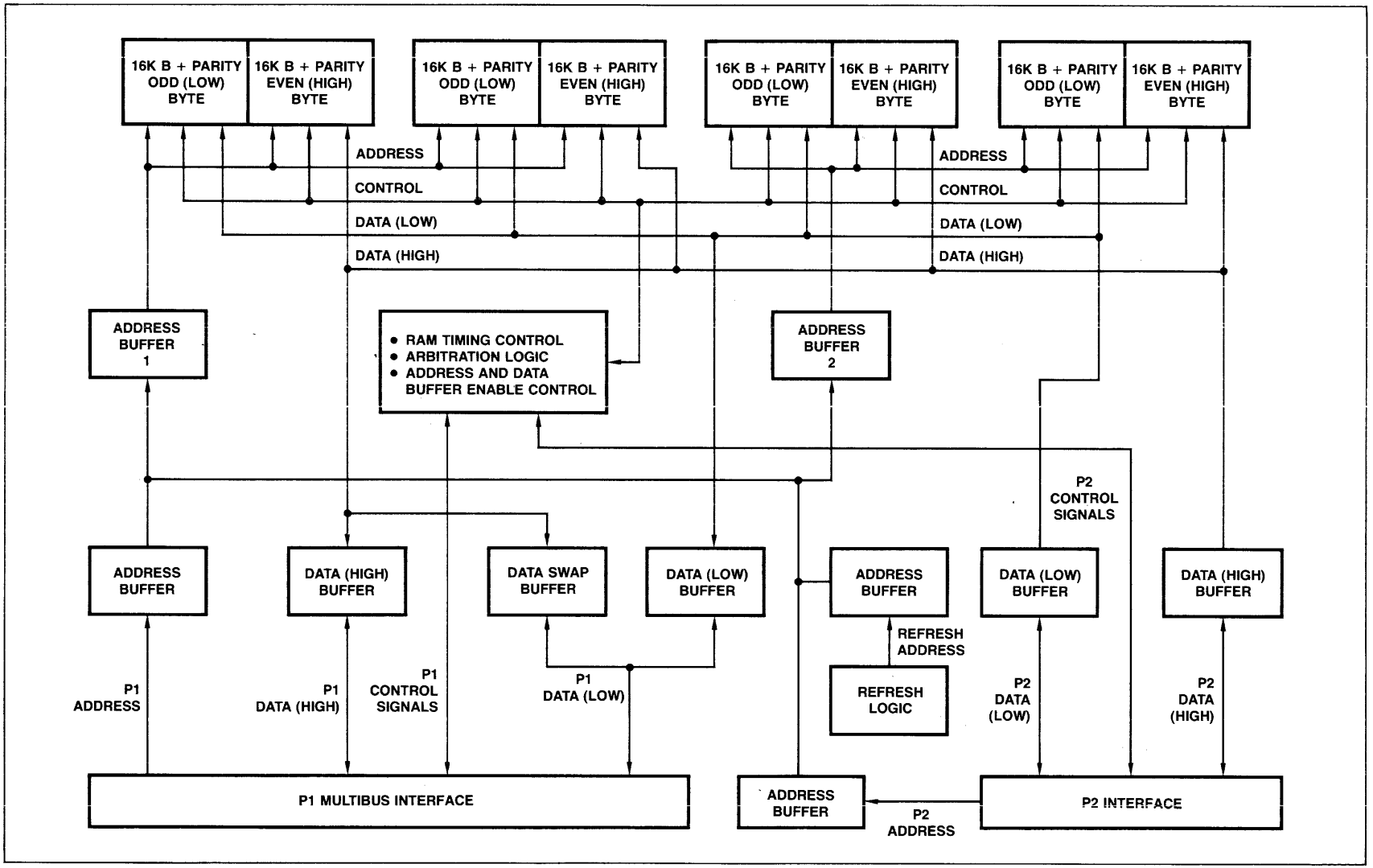


Figure 1-2. Am96/1000 Functional Block Diagram

1. Multibus Configuration (P1)

   - 32K bytes with or without parity
   - 64K bytes with or without parity
   - 96K bytes with or without parity
   - 128K bytes with or without parity

2. General Purpose Configuration (P2)

   - 64K bytes with or without parity
   - 128K bytes with or without parity

Byte High Enable (BHEN*) and Byte/Word* (B/W*) signals from P1 Multibus and P2 Bus respectively, determine byte or word mode of operation. During byte operations, the least significant address bit (AD0) from either bus is used to select which half of the internal data bus to be transferred to the external data bus or which half of the external data bus to be stored in memory.

The board compares hexadecimal address bits ADRC* through ADR13* from the Multibus and address bits AD10 through AD17 from the general purpose Bus with jumper settings to determine if it is being addressed. If these address bits match the jumpers, address bits AD1 through ADE are decoded as shown in figure 1-3.

Memory access originates from 3 sources; the Multibus, the P2 bus, and refresh requests. The refresh request has highest priority. A pending refresh request is processed as soon as the memory access logic completes an operation. A memory access request from the Multibus or the general purpose P2 bus is delayed when another memory operation is in progress or a refresh request is pending. On the Multibus, this is accomplished by delaying transfer acknowledge (XACK*). On the general purpose P2 bus, the hold-off is accomplished by asserting device busy (DBSY*). For simultaneous access requests from the Multibus and the general purpose P2 bus, one is given a higher priority and allowed to start its access first. Priority is alternated to assure proper interleaving of requests from the two buses. When only one bus is used, memory access arbitration is between the bus in use, and the on-board refresh request.

Once the access decision is made, address and data buffer control logic enables the address and data buffers for a selected source onto memory address and data buses. RAM timing control logic then starts a memory access cycle, generating all necessary RAM control signals and indicating that RAM is busy until completion of the access cycle. If another request is pending, the arbitration logic will decide which

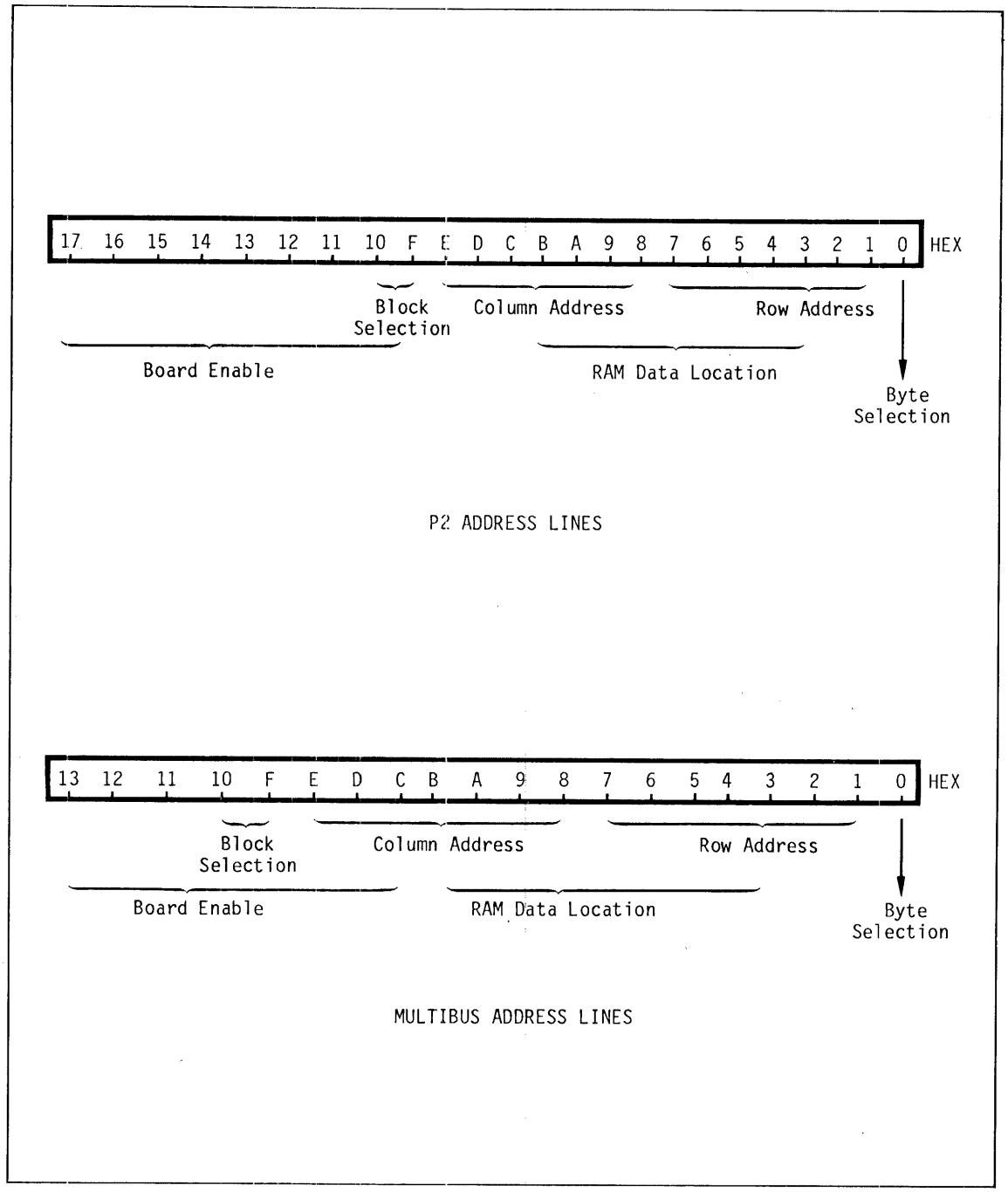


Figure 1-3. Multibus and P2 Bus Address Bit Assignments

source starts the next cycle. If not, the arbitration logic will wait for the next request.

Word data accesses from the Multibus to even addresses transfer RAM high data (bits 8 through F) to/from Multibus high bits (bits 8 through F) through the Data High buffer and RAM low data (bits 0 through 7) to/from Multibus low bits (bits 0 through 7) through the Data Low buffer. To assure this the low address bit (AD0) is ignored during word accesses.

Byte accesses from the Multibus to even addresses transfer RAM low data (bits 0 through 7) to/from Multibus low data (bits 0 through 7) through the Data Low buffers. Byte accesses from the Multibus to odd addresses transfer RAM high data (bits 8 through F) to/from Multibus low data (bits 0 through 7) through the Data Swap buffer. Reference the documents listed in the preface for more Multibus data transfer information.

All read data accesses for the general purpose P2 bus transfer RAM high data (bits 8 through F) to P2 high bits (bits 8 through F) through the Data High buffer and RAM low data (bits 0 through 7) to P2 low bits (bits 0 through 7) through the Data Low buffer. It is up to the user to pick off the correct half of the P2 data bus during a byte read. The AmZ8000 16-bit CPU does this internally for byte reads.

Word write access via the general purpose P2 bus, transfers the P2 high bits (bits 8 through F) to RAM high data (bits 8 through F) through the Data High buffer and the P2 low bits (bits 0 through 7) to RAM low data (bits 0 through 7) through the Data Low buffer.

Byte writes to even addresses via the general purpose P2 bus transfer data from P2 high bits (bits 8 through F) to RAM high data (bits 8 through F) through the Data High buffer. The P2 low bits (bits 0 through 7) are ignored and do not cause any change to RAM low data (bits 0 through 7). Byte writes to odd addresses via the general purpose P2 bus transfer data from P2 low bits (bits 0 through 7) to RAM low data (bits 0 through 7) through the Data Low buffer. The P2 high bits (bits 8 through F) are ignored and do not cause any change to RAM high data (bits 8 through F).

The Am96/1000 Series RAM board can be accessed from the Multibus and the general purpose P2 bus without further consideration when both buses are using independent sections of the RAM. Data is not passed from one bus to the other through memory. There are special considerations, however, when an Am96/1000 Series RAM board is used as a common RAM area for passing data between the Multibus and the general purpose P2 bus. When word data is exchanged between the two buses, there is no problem; data is written as a word from one bus and read as a word from the other bus. When byte operations are performed, either from the Multibus or the general purpose P2 bus, data is stored in memory as illustrated in table 1-2. When a byte is written into a location using an even address from the general purpose P2 bus it is placed in RAM high data. If data from that same location were read from the Multibus RAM low data would be read. Exercise care when

performing data byte operations to pass data between the Multibus and the general purpose P2 bus. This is necessary because the general purpose P2 bus was designed primarly for AmZ8000 support. The AmZ8000 CPU interprets the significance of a data word being high byte then low byte. The 8080 and other typical 8-bit processors that support the Multibus interpret the significance of a data word as low byte then high byte.

TABLE 1-2. RAM DATA USED FOR BYTE OPERATIONS

BUS	ADDRESS	
	EVEN	ODD
Multibus	RAM Low Data (bits 0 through 7)	RAM High Data (bits 8 through F)
General Purpose P2 Bus	RAM High Data (bits 8 through F)	RAM Low Data (bits 0 through 7)

All versions of the Am96/1000 Series RAM Boards can be fitted with a byte parity option to monitor the reliability of the data. When parity is used, the required parity bit is calculated for each write operation and written into memory along with the data. During read operations, both data and parity are read. Parity is again determined from the data and compared to the stored parity. An interrupt can be generated to the CPU on either the Multibus or P2 Bus if there is a parity error.

The Refresh Logic refreshes one row of memory cells every 14 microseconds. Refresh-cycles are never delayed more than one read or write-cycle.

1-4. SPECIFICATIONS

Specifications for the Am96/1000 Series RAM Boards are listed in table 1-3.

TABLE 1-3. Am96/1000 SERIES RAM BOARDS

PHYSICAL:

Board Dimensions:

Width:	30.48 cm (12.00 inches)
Depth:	17.15 cm (6.75 inches)
Thickness:	1.27 cm (0.50 inches)

ENVIRONMENTAL REQUIREMENTS:

Operating Temperature:	0°C to 55°C
Relative Humidity:	Up to 90% without condensation
Storage Temperature:	-40°C to 75°C

POWER REQUIREMENTS:

CONFIGURATION:	+5VDC±10%		+12VDC±10%		-12VDC±10%		-5VDC±10%	
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX
32K	3 Amp	3.9 Amp	54 mA	70 mA	2.3 mA	3 mA	32 µA	42 µA
64K	3 Amp	3.9 Amp	97 mA	126 mA	2.3 mA	3 mA	70 µA	91 µA
96K	3 Amp	3.9 Amp	115 mA	150 mA	2.3 mA	3 mA	97 µA	126 µA
128K	3 Amp	3.9 Amp	156 mA	203 mA	2.3 mA	3 mA	130 µA	169 µA

TECHNICAL:

Word Size:	8-bit and 16-bit
Memory Size:	32K Bytes, 64K Bytes, 96K Bytes, and 128K Bytes
Access Time: (Command to XACK*)	390ns typ., 415ns max.
Access Time: (Command to AACK*)	80ns typ., 315ns max. (Adjustable, See Table 2-9)
Access Time: (AACK* to Memory Access Complete)	130ns to 310ns (Adjustable, see Table 2-9)
Cycle Time:	
Read:	490ns typ., 515ns max.
Write:	490ns typ., 515ns max.
Addressing:	P1 (Multibus); on any 4K boundary in a 1 megabyte address space (all versions) P2 Bus; on 64K boundaries in a 16 megabyte space
Options:	parity bit (byte mode)
Refresh:	Every 14 microseconds and may last for 475 nanoseconds (worst case)

CHAPTER 2
INSTALLATION AND INTERFACE

2-1. INTRODUCTION

This section provides information for installing and interfacing an Am96/1000 Series RAM Board. These instructions include unpacking and inspection, power requirements, cooling requirements, user selectable options, bus interface characteristics, and connector pin assignments.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request the carrier's agent to be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing material for the agent's inspection. Shipping damages should be reported immediately to the carrier.

NOTE

Do not attempt to service the board yourself as this will void the warranty.

2-3. POWER REQUIREMENTS

An Am96/1000 Series RAM Board requires +5 VDC, -5 VDC, +12 VDC, and -12 VDC power supply inputs. If -5 VDC is not available on the bus, connect a jumper between 2 and 3 to obtain the voltage from the on-board -5 VDC Regulator. When -5 VDC is available on the bus, connect jumpers 1 and 2. The currents required for these supplies are listed in table 1-2. It is necessary to ensure that the system power supply has sufficient current margins to accomodate the board requirements. Power is always drawn from P1, even if the P1 interface is never used.

2-4. COOLING REQUIREMENTS

An Am96/1000 Series RAM Board can be operated as a 32K, 64K, 96K, or 128K-Byte memory system. Adequate air circulation must be provided to prevent an ambient temperature above 55°C (131°F).

2-5. USER-SELECTABLE OPTIONS

The Am96/1000 Series RAM board comes from the factory jumpered as required for the option ordered. The address is set at 0000H. No interrupts (for parity errors) are connected to the bus. If this is satisfactory, no additional jumper options need be set-up by the user. Jumpers on board an Am96/1000 Series RAM Board may be used to select Multibus and/or P2 Bus Operations, address boundaries, system interrupt levels, transfer acknowledge (XACK*), Advanced Acknowledge (AACK*), and memory configurations with or without byte parity. Instructions for installing jumpers for these functions are described in the following paragraphs. If a change from one configuration to another is required, remove all jumpers before installing the new configuration.

2-6. BUS SELECTION

An Am96/1000 Series RAM Board is shipped from the factory with jumpers installed for Multibus and General Purpose P2 operation. By changing jumpers, the board can be configured for four additional operating modes. Jumper placement for the five operating modes is shown in the following tables. Multibus and general purpose P2 Bus operation is shown in Table 2-1; Multibus operation only, Table 2-2; General purpose P2 bus operation only, Table 2-3; Am96/4016 P2 bus operation only, Table 2-4; Multibus and Am96/4016B P2 bus operation only, Table 2-5.

TABLE 2-1. MULTIBUS AND GENERAL PURPOSE P2 BUS OPERATION

FROM	TO
2	3
5	7
12	13
17	18
21	22
24	25
26	133
28	29
30	31
33	34
37	38
43	44
46	48
69	70
88	94

TABLE 2-1. MULTIBUS AND GENERAL PURPOSE (Cont.)

FROM	TO
92	93
110	111
111	112
112	134
134	142
96	97
97	136
131	132
139	140
148	149

NOTE

Refer to table 2-6 for address jumper assignments.

TABLE 2-2. P1 MULTIBUS OPERATION ONLY

FROM	TO
2	3
5	7
17	18
31	32
34	35
38	39
43	44
46	47
100	95
42	135
139	140

NOTE

Refer to table 2-6 for address jumper assignments.

TABLE 2-3. GENERAL PURPOSE P2 BUS OPERATION ONLY

FROM	TO
2	3
12	13
21	22
24	25
28	29
33	34
37	38
44	45
69	70
88	94
92	93
96	97
97	136
110	111
111	112
112	134
134	142
131	132
133	141
139	140
148	149
NOTE	
Refer to table 2-6 for address jumper assignments.	

TABLE 2-4. Am96/4016B P2 BUS OPERATION ONLY

FROM	TO
2	3
20	21
23	24
27	28
33	34
37	38
44	45
70	71
100	89
90	93
96	97
130	131
133	141
138	139
NOTE	
Refer to Table 2-6 for address jumper assignments.	

TABLE 2-5. MULTIBUS AND Am96/4016B P2 BUS OPERATION

FROM	TO
2	3
5	7
17	18
20	21
23	24
26	133
27	28
30	31
33	34
37	38
43	44
46	48
70	71
100	89
90	93
96	97
130	131
138	139

NOTE

Refer to table 2-6 for address jumper assignments.

2-7. ADDRESS BOUNDARY SELECTION

An Am96/1000 Series RAM Board can be placed on any 4K-byte boundary in the 1-megabyte address space of the Multibus and on any 64K-byte boundary within the address space of the general purpose P2 bus. Address boundary selection is accomplished by placing jumpers on the address select pins. A jumper present represents a bit value of zero and no jumper present represents a bit value of one. The user can change boundary selection to 128K-byte boundaries on the general purpose P2 bus by removing the connector between jumpers 97 and 136, and installing it on jumpers 99 and 136. In this configuration, there must be a jumper between 127 and 128. When a 64K RAM board is to be used in the upper 64K of a 128K address space, remove jumpers 96 to 97 and 127 to 128; install jumpers from 97 to 136 and 96 to 99. The Am96/1000 RAM boards are shipped from the factory with jumpers installed for address zero on both the Multibus and the general purpose P2 bus. To assign another address boundary, remove the jumpers shown in Table 2-6 that correspond to the address bits used to select that address boundary.

TABLE 2-6. ADDRESS JUMPER ASSIGNMENTS

MULTIBUS		GENERAL PURPOSE P2	
Address Bit	Jumper Pin	Address Bit	Jumper Pin
AD13	64 - 63*	AD17	125 - 126*
AD12	56 - 55*	AD16	119 - 120*
AD11	60 - 59*	AD15	115 - 116*
AD10	66 - 65*	AD14	113 - 114*
ADF	68 - 67*	AD13	117 - 118*
ADE	54 - 53*	AD12	121 - 122*
ADD	58 - 57*	AD11	123 - 124*
ADC	62 - 61*	AD10	127 - 128*
*As shipped = 00000H			

2-8. SYSTEM INTERRUPT SELECTION

An Am96/1000 Series RAM Board has two sets of jumper pads for connecting a memory error to the eight Multibus interrupt lines (INT0 through INT7), the 4016B-P2 bus interrupt lines (NMI) and the general purpose P2 bus interrupt lines (INT0 through INT3). To assign the system-interrupt request level to a memory error interrupt connect a jumper between any two points on the Multibus interrupt pad (table 2-7) and/or the general purpose P2 bus interrupt pad (table 2-8). The interrupt to either P1 or P2 is a 400 nsec. pulse, not a level.

TABLE 2-7. MULTIBUS INTERRUPT CONNECTIONS

FROM	TO	CONNECTION
72	85	INT0*
74	87	INT1*
76	81	INT2*
78	83	INT3*
80	77	INT4*
82	79	INT5*
84	73	INT6*
86	75	INT7*

TABLE 2-8. P2 BUS INTERRUPT CONNECTIONS

FROM	TO	CONNECTION
106	109	NMI* (4016-P2 Bus Only)
104	108	INT0* (General P2 Bus Only)
104	105	INT1* (General P2 Bus Only)
106	109	INT2* (General P2 Bus Only)
106	107	INT3* (General P2 Bus Only)

2-9. ADVANCED ACKNOWLEDGE (AACK*)

The advanced acknowledge signal (AACK*) is user selected to occur 130 to 310 nanoseconds (in increments of 60 nanoseconds) before the transfer acknowledge signal (XACK*). Table 2-9 lists the jumpers and the time at which the AACK* signal is generated with relation to issuance of the CPU command and the time that the memory access is complete with relation to AACK*.

TABLE 2-9. ADVANCED ACKNOWLEDGE (AACK*) DELAY JUMPERS

JUMPER CONNECTION FROM	TO	COMMAND TO AACK DELAY (NSEC)	AACK TO MEMORY ACCESS COMPLETE DELAY (NSEC)
7	5	80 min. -150 max.	310
91	10	140 min. -215 max.	250
8	4	200 min. -275 max.	190
6	9	260 min. -335 max.	130

2-10. DEVICE BUSY (DBSY*)

Device Busy will be driven low should the memory board receive an access request before a current access on P1, or a refresh cycle, has been completed. Device Busy will go inactive following the completion of the current task.

Using the delay jumpers shown in Table 2-10 the DBSY* signal can be held active to induce additional wait states, thus matching the speed of the memory access to the speed of the processor.

TABLE 2-10. DEVICE BUSY (DBSY*) DELAY JUMPERS

Jumper Connection		COMMAND TO DBSY* INACTIVE
FROM	TO	
12	13	20 ns. (minimum)
12	11	120 ns. (minimum)
15	14	220 ns. (minimum)
15	16	320 ns. (minimun)

2-11. MEMORY CONFIGURATIONS

Jumpers 49 through 52 are used to designate 32K, 64K, 96K, or 128K-byte memory. The board is shipped from the factory with jumpers installed for the memory ordered. Assign a different memory configuration as follows:

a. To select the 32K-byte configuration, install a jumper-strap from point 49 to 50 and from point 51 to 52.

b. To select the 64K-byte configuration, install a jumper-strap from point 49 to 50 only.

c. To select the 96K or 128K-byte configuration, no jumper-straps are necessary. When the 96K-byte configuration is selected, the upper 32K-bytes will still respond even though no memory exists in this address space. Therefore, data received from these addresses will be invalid.

2-12. BUS INTERFACE CHARACTERISTICS

Edge connector P2 is an auxiliary bus interface that provides an alternate data transfer path. A comparision of the general purpose and 4016 bus pin assignments are shown in table 2-11. P2 pin assignments are listed in table 2-12 and a description of the signal functions are given in table 2-13. P2 Bus Timing are listed in table 2-14. The P2 command timing for read, write, and interrupt operations are shown in figures 2-1 and 2-2.

TABLE 2-11. GENERAL PURPOSE AND 4016 P2 BUS PIN ASSIGNMENTS AND COMPARISON

PIN	4016 P2	GENERAL PURPOSE P2	PIN	4016 P2	GENERAL PURPOSE P2	PIN	4016 P2	GENERAL PURPOSE P2
1	ADR10	ADR10	21	PHI (CLK)	CLK*	41	AC	ARC
2	ADR11	ADR11	22	STOP*	INT1*	42	AD	ADRD
3	ADR12	ADR12	23	NMI*	INT2*	43	AE	ADRE
4	ADR13	ADR13	24	VI*	INT3*	44	AF	ADRF
5	ADR14	ADR14	25	ST0	GND	45	D0	DAT0
6	ADR15	ADR15	26	ST1	GND	46	D1	DAT1
7	NVI*	ADR16	27	ST2	GND	47	D2	DAT2
8	INH*	ADR17	28	ST3	GND	48	D3	DAT3
9	AS*	MC*	29	A0	ADR0	49	D4	DAT4
10	DS*	DS*	30	A1	ADR1	50	D5	DAT5
11	R/W*	R/W*	31	A2	ADR2	51	D6	DAT6
12	SEGT*	-------	32	A3	ADR3	52	D7	DAT7
13	N/S*	-------	33	A4	ADR4	53	D8	DAT8
14	B/W*	B/W*	34	A5	ADR5	54	D9	DAT9
15	BUSRQ*	-------	35	A6	ADR6	55	DA	DATA
16	BUSAK*	-------	36	A7	ADR7	56	DB	DATB
17	GND	DACK*	37	A8	ADR8	57	DC	DATC
18	GND	INT0*	38	A9	ADR9	58	DD	DATD
19	RST*	PFIN*	39	AA	ADRA	59	DE	DATE
20	WAIT*	DBSY*	40	AB	ADRB	60	DF	DATF

TABLE 2-12. GENERAL PURPOSE P2 BUS PIN ASSIGNMENTS

PIN	SIGNAL	FUNCTION	PIN	SIGNAL	FUNCTION
1	ADR10		31	ADR2	
2	ADR11		32	ADR3	
3	ADR12		33	ADR4	
4	ADR13	Address Bus	34	ADR5	Address Bus
5	ADR14		35	ADR6	
6	ADR15		36	ADR7	
7	ADR16		37	ADR8	
8	ADR17		38	ADR9	
9	MC*	Memory Command	39	ADRA	
10	DS*	Data Strobe	40	ADRB	
11	R/W*	Read/Write	41	ADRC	
12	Unassigned		42	ADRD	
13	Unassigned		43	ADRE	
14	B/W*	Byte/Word	44	ADRF	
15	Unassigned		45	DAT0	
16	Unassigned		46	DAT1	
17	DACK*	Device Acknowledge	47	DAT2	
18	INT0*	System Interrupt	48	DAT3	
19	PFIN*	Power-Fail IN	49	DAT4	
20	DBSY*	Device Busy	50	DAT5	
21	CLK*	Clock	51	DAT6	
22	INT1*		52	DAT7	Data Bus
23	INT2*		53	DAT8	
24	INT3*	System Interrupt	54	DAT9	
25	GND		55	DATA	
26	GND		56	DATB	
27	GND		57	DATC	
28	GND		58	DATD	
29	ADR0		59	DATE	
30	ADR1	Address Bus	60	DATF	

TABLE 2-13. GENERAL PURPOSE P2 BUS (P2) SIGNAL FUNCTIONS

SIGNAL	FUNCTIONAL DESCRIPTION
ADR0-ADR17	Address
DAT0-DATF	Data -- These 16 bidirectional lines transmit/ receive data to and from the specific RAM locations.
DS*	Data Strobe -- Indicates data is valid on bus during a read or write access cycle. This is necessary because a bus command may be issued before data is valid.
R/W*	Read/Write -- Indicates read/write for bus commands. Active low for writes.
B/W*	Byte/Word -- Indicates byte or word bus access, active low for word.
MC*	Memory Command -- Indicates a memory read or write access is being performed.
DBSY*	Device Busy -- Indicates that the memory wants the CPU to wait.
INT0*-INT3*	System Interrupts -- These interrupt inputs can be used to indicate a parity error.
DACK*	Device Acknowledge -- Not a transfer acknowledge. It indicates that there is a memory board present at the address sent out.

TABLE 2-14. GENERAL PURPOSE P2 BUS TIMING

NAME	DESCRIPTION	(200ns. RAMs) MIN.	MAX.
t_{AS}	ADDRESS SETUP TO COMMAND ↓	50	---
t_{AH}	COMMAND ↓ TO ADDRESS INVALID	50	---
t_{acc}	DS* ↓ TO VALID DATA	---	285
t_{RS}	R/W SETUP TO COMMAND ↓	0	---
t_{RH}	COMMAND ↓ TO R/W HOLD TIME	10	---
t_{CB}[3]	COMMAND ↓ TO DBSY ↓	---	22
t_{BW}[3]	DEVICE BUSY PULSE WIDTH	---	50
t_{CDS}	COMMAND ↓ TO DS ↓	105	---
t_{OFF}	COMMAND ↑ TO COMMAND ↓	195	---
t_{DDH}	DS ↓ TO DATA HOLD TIME	180	---
t_{DSH}	COMMAND ↑ TO DS ↑	0	---
t_{DSD}[1]	DS ↓ TO DATA IN STABLE	---	50
t_{DSC}[1]	DS ↓ TO COMMAND ↑	200	---
t_{BDH}[2]	DBSY ↑ TO DATA HOLD TIME	230	---
t_{BDI}[2]	DBSY ↑ TO DATA IN STABLE	---	105
t_{BC}[2]	DBSY ↑ TO COMMAND ↑	265	---
t_{DH}	COMMAND ↑ TO DATA INVALID	60	---
t_{CRD}[1]	COMMAND ↓ TO DATA OUT VALID	---	390
t_{BRD}[2]	DBSY ↑ TO DATA OUT VALID	---	350
t_{WC}	WRITE CYCLE	500	---
t_{RC}	READ CYCLE	495	---

1. Parameters calculated are based on a NO WAIT cycle access.

2. Parameters calculated are based on a WAIT state incurred as a result of an access request.

3. Device Busy is driven low until the memory board is certain that no waits will be required on the current access. It is removed (driven high) as soon as the determination has been made.

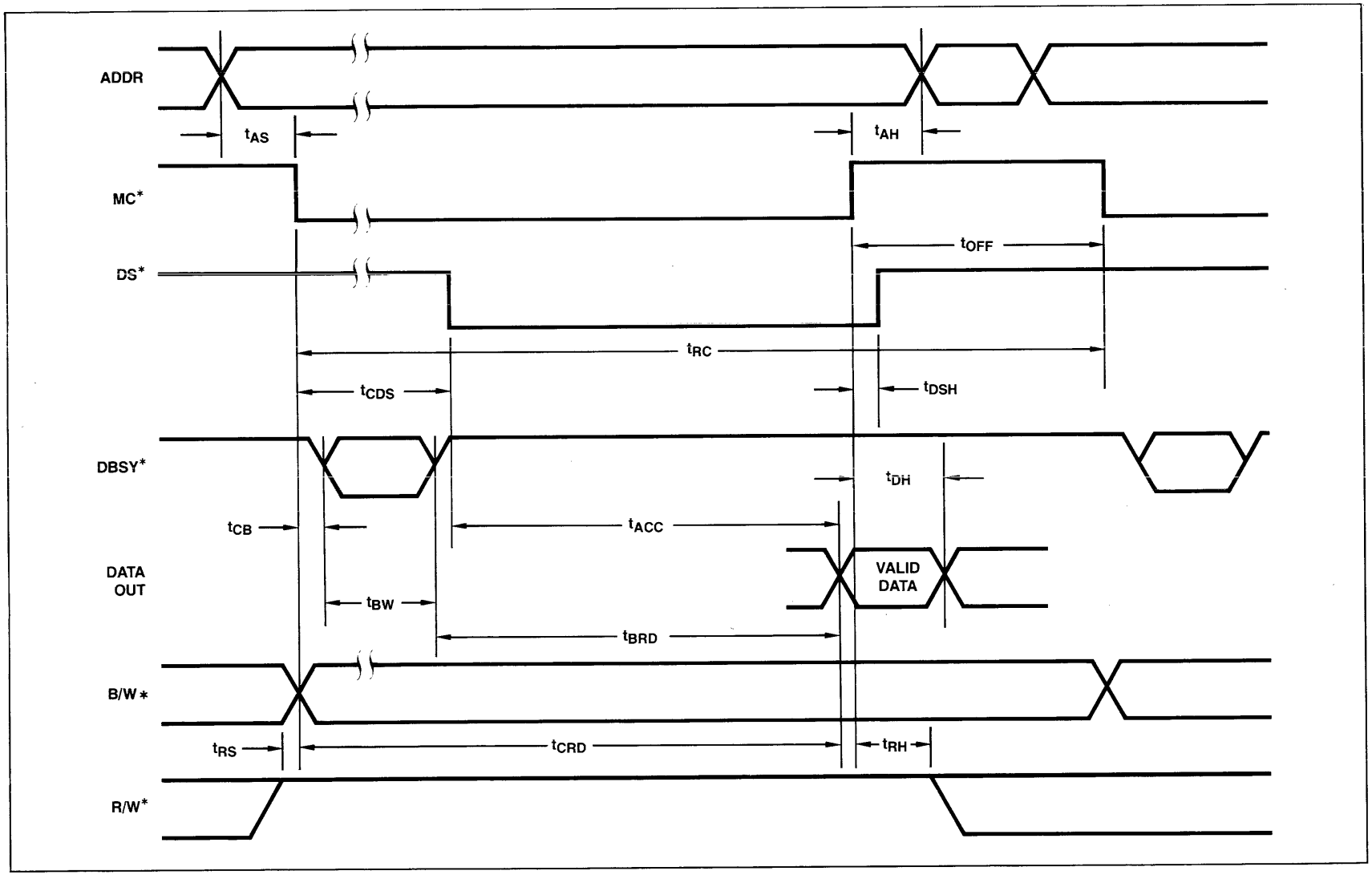


Figure 2-1. General Purpose P2 Bus Read Cycle

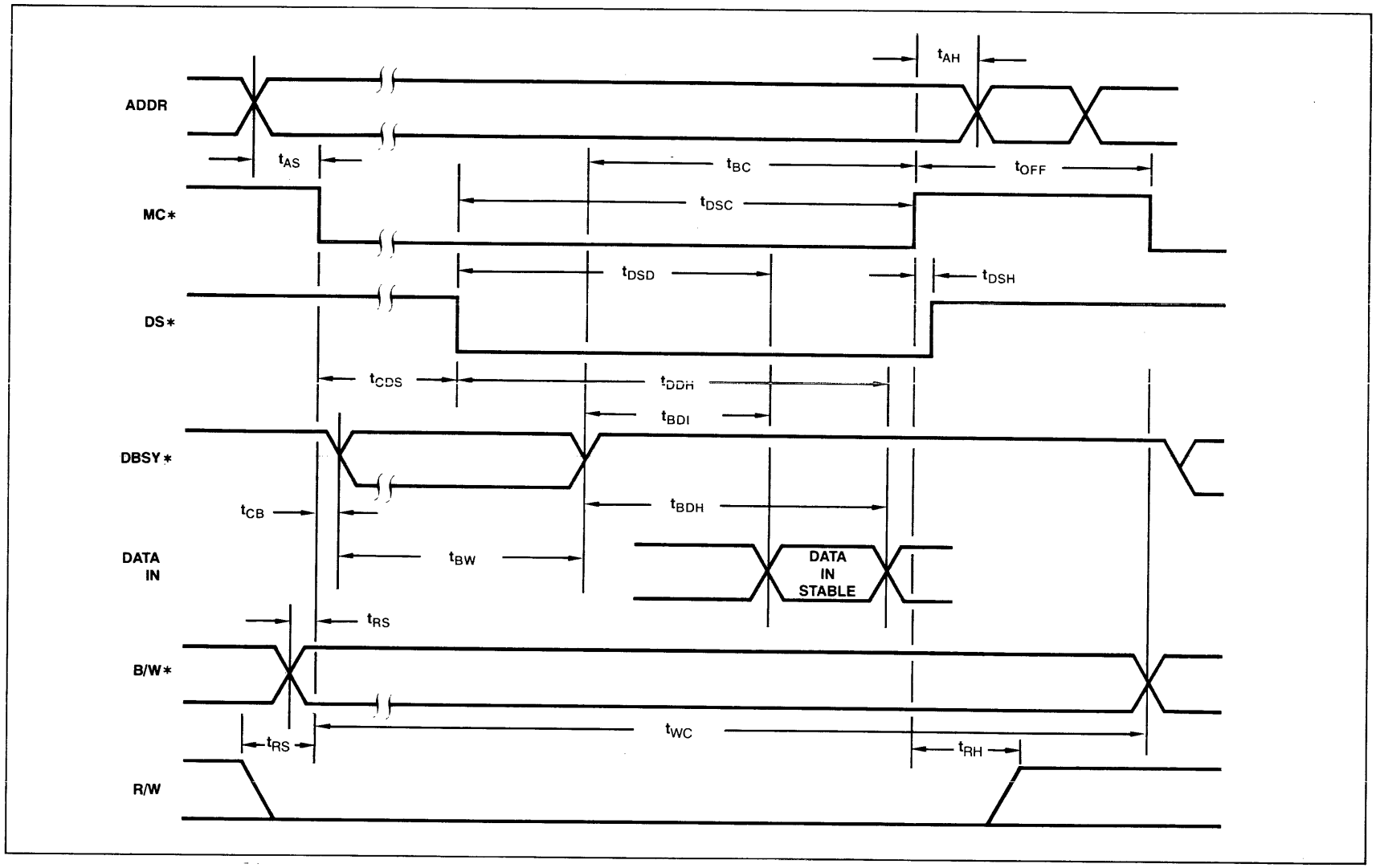


Figure 2-2. General Purpose P2 Bus Write Cycle

CHAPTER 3
THEORY OF OPERATION

3-1. INTRODUCTION

This section provides a block diagram level description of Am96/1000 Series RAM Board hardware implemented functions. Detailed circuit information is contained on Schematic Diagram #109510187-001 provided in chapter 4 and the signal conventions described in the Preface.

3-2. FUNCTIONAL DESCRIPTION

The Am96/1128 128K-Byte Dynamic RAM board, the largest member of the series, is used to describe the theory of operation for a typical Am96/1000 Series RAM Board; Figure 3-1, a functional block diagram of the Am96/1128 illustrates the following.

- Address Control
- Memory Storage
- Timing and Control
- Data Selection

These functional areas decode address outputs from the CPU, store/retrieve and refresh data in memory, regulate on-board control functions and on/off board data transactions.

3-3. ADDRESS BUFFERS

Hexadecimal address lines AD1 through AD10 from the Multibus and general purpose P2 Bus are brought onto the memory board via address buffers U101/U124 and U106/U117. Signals (Z8K CMD and MB EN*) from the memory control logic enable address buffers during read and write cycles. Output from these buffers is 14 internal address bits to the Row and column address multiplexers, U116, U105, U115, and U104. At the multiplexers row addresses are sent to memory devices during RAS* by ROW AD EN*. Timing signal COL AD EN* switches the multiplexers to column addresses that will be accepted by memory devices at CAS* time. Address inputs to RAM logic consist of seven row address bits and seven column address bits time-multiplexed onto internal address bus RAM ADR0 through RAM ADR6. This internal address bus is also timed-shared with the refresh addresses IAD1* though IAD7*.

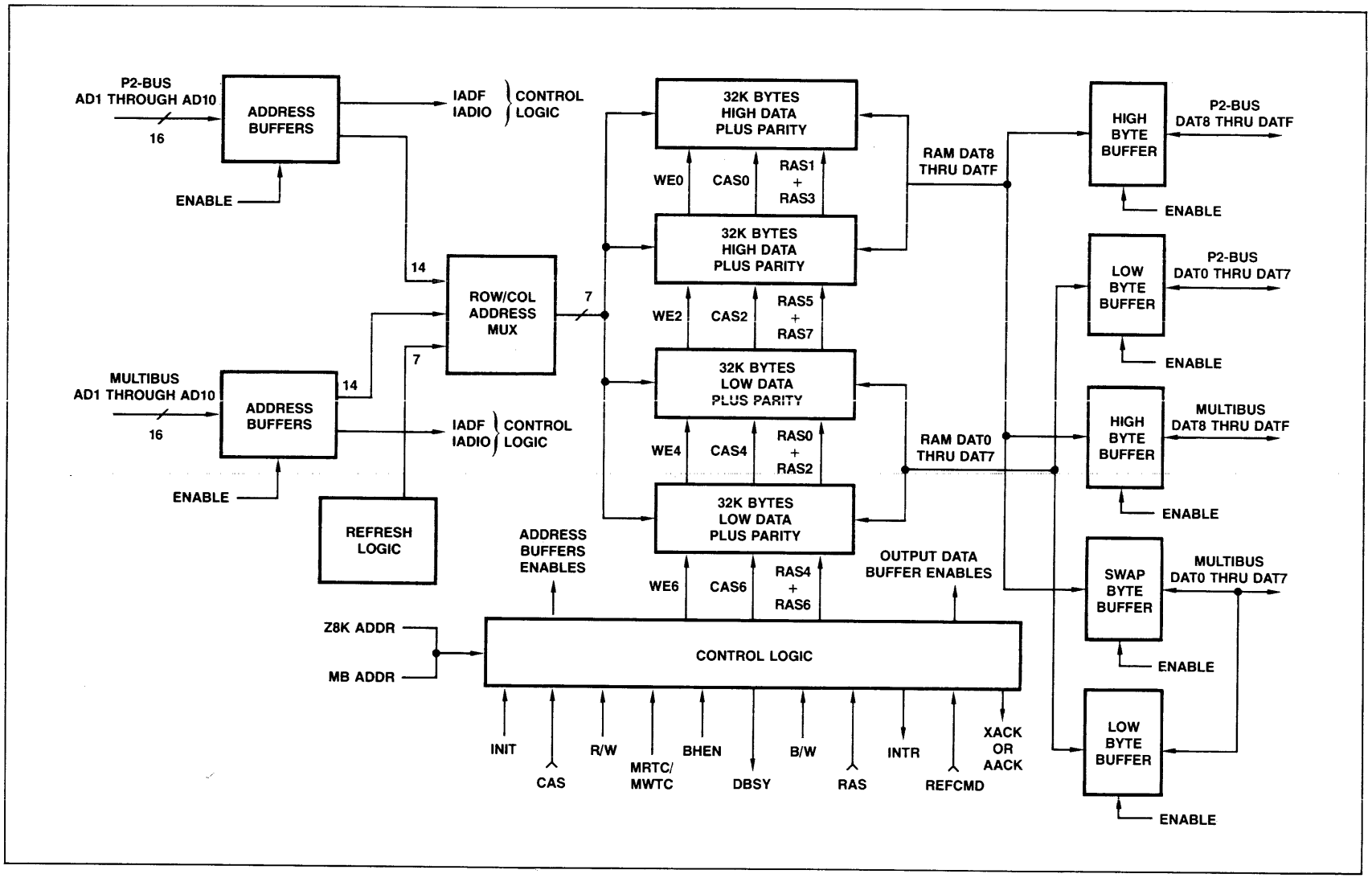


Figure 3-1. Am96/1128 Block Diagram

3-4. ADDRESS DETECTION

Jumpers 113 through 128 assign the Am96/1128 to any 64K-byte boundary in the 16-megabyte address space of the general purpose P2 Bus. Jumpers 53 through 64 assign any 4K-byte boundary in the 1-megabyte address space of the Multibus. Hexadecimal address bits AD10 through AD17 on the general purpose P2 Bus and ADC through AD13 on the Multibus are compared with these jumpers to determine if memory responds to a read or write command. When the memory address is detected, control logic is enabled to receive a read or write command.

3-5. ADDRESS DECODING

Address inputs to the RAM chips consist of row and column addresses time-multiplexed onto the internal address bus. Address bits IADF* and IAD10* are decoded by U67 or U56 to determine which pair out of four pairs of row address strobes (RAS0 and RAS1, RAS2 and RAS3, etc.) to activate. Each row address strobe (RAS0, RAS1, etc.) controls one page of memory addresses. The address of a specific row of RAM chips to be selected is defined by external address bus lines AD1 through AD6. This address is gated to all RAM chips by ROW AD EN* from the control logic. Only RAM banks whose row address strobes are active decode a row address. The control logic activates column address strobes 100 nanoseconds later. These signals cause the RAM chip logic to decode the column address specified by external address lines AD8 through ADF. This address is gated to all RAM chips by COL AD EN* from the control logic. Although a column address is enabled in every RAM chip, an addressed row is enabled only in chips of the bank whose row address strobes are active. The least-significant address bit from either the Multibus or P2 Bus is decoded to determine which data byte gets transferred or replaced.

3-6. MEMORY ARRAY

The memory array consists of 72 16Kx1 dynamic RAM chips, organized into four blocks of 32K-bytes each with byte parity. These blocks are further divided into 16K-byte pages numbered 0 through 7 (two pages per block). Pages 0 and 1 and 2 and 3 operate as pairs. Each page is controlled by a row address strobe (RAS) as illustrated in figure 1-1. Consecutive bytes of a data transfer are not stored in contiguous locations of the same page. Rather, bytes with even addresses (AD0=0) and bytes with odd addresses (AD0=1) are stored in even and odd pages, respectively. The Row Address Strobe Generator performs the function of selecting alternate pages and determining which even and odd page is to be used. When active; RAS0 enables row select circuits in page 0, RAS1 enables row select circuits in page 1, etc. The RAS Generator is controlled by address bits IADF* and IAD10*, byte High Enable (BHEN*), Z8K Byte/Word (B/W*), etc. The manner in which even and odd bytes are

routed between pages and data buses is described in the following paragraphs.

3-7. DATA BUFFERS

Data is routed from the external data buses via transceivers U129, U114, U107, U125, and U118. Timing signals from the control logic enable data buffers to drive data to or from busses during a read or write cycle. When the Am96/1128 is not selected the data buffers are disconnected from the external data busses. U118 (Swap Byte Buffer) provides a data path between Multibus data lines DAT0 through DAT7 and RAM data lines DAT8 through DATF. U118 makes eight bit and sixteen bit transfers possible.

3-8. MULTIBUS DATA TRANSFERS

The Am96/1128 can handle 8-bit bytes or 16-bit words divided into high and low bytes on the P1 connector (Multibus). Byte High Enable (BHEN*) is used to select 8-bit or 16-bit operating mode. BHEN* active (low) indicates a 16-bit word operation on the Multibus.

When BHEN* is inactive (HIGH) and an odd address (AD0=1) is on the Multibus, the high data byte is transferred via data lines DAT0 through DAT7. If an even address (AD0=0) is on the Multibus and BHEN* is HIGH the low data byte is transferred via data lines DAT0 through DAT7.

3-9. GENERAL PURPOSE P2 BUS DATA TRANSFERS

The general purpose P2 Bus memory is word aligned. B/W* active (LOW) indicates 16-bit operations on the general purpose P2 Bus. The least-significant address bit, AD0, determines which byte is transferred. When B/W* is inactive (HIGH) and an odd address (AD0=1) is on the general purpose P2 Bus, the low data byte is transferred over DAT0 through DAT7. When AD0=0 and B/W* is high, the data byte is transferred over DAT8 through DATF. When B/W* is low and AD0=0, the transfer is a 16-bit word with the low byte on DAT0 through DAT7, and the high byte on DAT8 through DATF.

3-10. CONTROL LOGIC

The Control Logic establishes priority for the Multibus, the general purpose P2 Bus, and the on-board refresh. Refresh has the highest priority. The control logic establishes an "alternating priority" scheme when simultaneously accessed via both P1 and P2 busses. This "interleaving" of accesses guarantees no one bus can lock-out the other bus. When a Multibus request is received while the P2 bus is being

serviced, the controller delays the Multibus transfer acknowledge signal and services the request immediately upon completion of the general purpose P2 Bus request. If a request from the general purpose P2 Bus occurs while the Multibus is being serviced, device busy (DBSY*) is driven on the P2 bus until the request can be serviced.

All timing and control signals required for data transfers are generated by the Control Logic. The control sequences that produce these signals are initiated by read and write commands from a CPU. A CPU first addresses the RAM locations to or from which data will be transferred. When the Am96/1128 decodes its address, it enables the control logic to receive the read or write command for Multibus operation. If the command is a read, the controller performs the sequence of operations that reads data from the addressed RAM location and places it on the requesting bus. When the data stabilizes on the bus the controller issues the transfer acknowledge (XACK*) signal. If the command is a write the controller performs the sequence of operations that write the data into the addressed RAM location. When data has been written into RAM, the control logic issues the XACK* signal. The sequence for a write operation is the same as for a read operation except for the direction of data flow.

The same sequence of timing occurs for the general purpose P2 bus as for the Multibus, but no transfer acknowledge is generated. The general purpose P2 bus is a synchronous bus. This means that the memory board must be ready for communication and accept or transmit data within the specified instruction time of the processor.

3-11. REFRESH LOGIC

The refresh function is implemented with hardware and does not require any software supervision. The refresh logic U112, U113, U121, and U122 consists of a timer set to 14 microseconds. When the interval elapses, memory (if not busy) is placed in a refresh-cycle. If memory is busy when the interval elapses, it is placed in a refresh cycle immediately after it is free. In each refresh cycle, one row of every chip in the memory is simultaneously refreshed. During a refresh-cycle memory holds off requests from a CPU.

3-12. ADVANCED ACKNOWLEDGE SIGNAL

In response to a read or write command on the Multibus, a CPU requires Transfer Acknowledge (XACK*) or Advanced Acknowledge (AACK*) from the Am96/1128. The response informs the CPU of completion of a read or write operation. The Am95/1128 returns XACK or the optional AACK to the CPU. AACK is user selected to occur 130 to 310 nanoseconds before XACK, and thus can eliminate the need for a CPU wait state.

3-13. INHIBIT SIGNAL

If the CPU issues an Am96/1128 address on the Multibus, and if there is a ROM device on the Multibus with the same address, the ROM device will issue inhibit (INH1*) to inhibit Am96/1128 memory operation.

3-14. BYTE PARITY

Byte parity is an optional feature on the Am96/1128 board. A parity error can be used to cause an interrupt on the P1 or P2 bus. During a data transfer, byte parity is handled as follows:

- Write data byte is applied to the Parity Generator/Checker (U119 or U102) where the required parity odd bit is generated and stored in memory.

- Read data byte is applied to the Parity Checker portion of U119 or U102 which checks the proper parity. An error is detected if the checked parity is not odd.

The interrupts on P1 and P2 are independent. A parity error caused by a P1 access causes an interrupt pulse of 400 nsec. on P1, but does not cause an interrupt on P2. Similarly, a parity error caused by a P2 access causes a 400 nsec. interrupt pulse on P2, but does not interrupt P1.

3-15. CLOCK SOURCE

The clock source on an Am96/1128 is a 20 MHz oscillator that provides timing for control and refresh functions. The 20 MHz clock signal is divided by two by U13 to produce a 10 MHz clock for use by the refresh logic. All timing and control signals required for data transfers are generated by the control logic.

CHAPTER 4
SERVICE INFORMATION

4-1. INTRODUCTION

This chapter provides service diagrams and information on service and repair assistance for AMC product lines.

4-2. SERVICE AND REPAIR ASSISTANCE

Service and repair assistance can be obtained from Advanced Micro Computers by contacting the AMC Field Service Department in Santa Clara, California at one of the following numbers:

Telephone: (408) 988-7777

Toll Free: (800) 672-3548 California

(800) 538-9791 U.S.A. (except California)

If it is necessary to return a product to Advanced Micro Computers for service or repair, contact the Field Service Department at the previously listed telephone number. A Return Material Authorization number will be provided along with shipping instructions and other important information that will help AMC provide you with fast, efficient service. A purchase order is required for AMC Field Service Department to initiate repair.

Prepare the product for shipment by repackaging it in the original factory packaging material, if available. When the original packaging is not available, wrap the product in a cushioning material (such as AirCap TH-240, manufactured by the Sealed Air Corporation, Hawthorne, New Jersey) and enclose in a heavy-duty corrugated shipping carton. Seal the shipping carton securely, mark it FRAGILE, and ship it to the address specified by the AMC Field Service Department.

Customers outside of the United States can contact an AMC Sales Office or Authorized AMC Distributor for directions on obtaining service or repair assistance.

4-3. SERVICE DIAGRAMS

Figure 4-1 is a component location diagram for the Am96/1128. Schematic diagrams for the Am96/1128 are provided in figures 4-2 through 4-12.

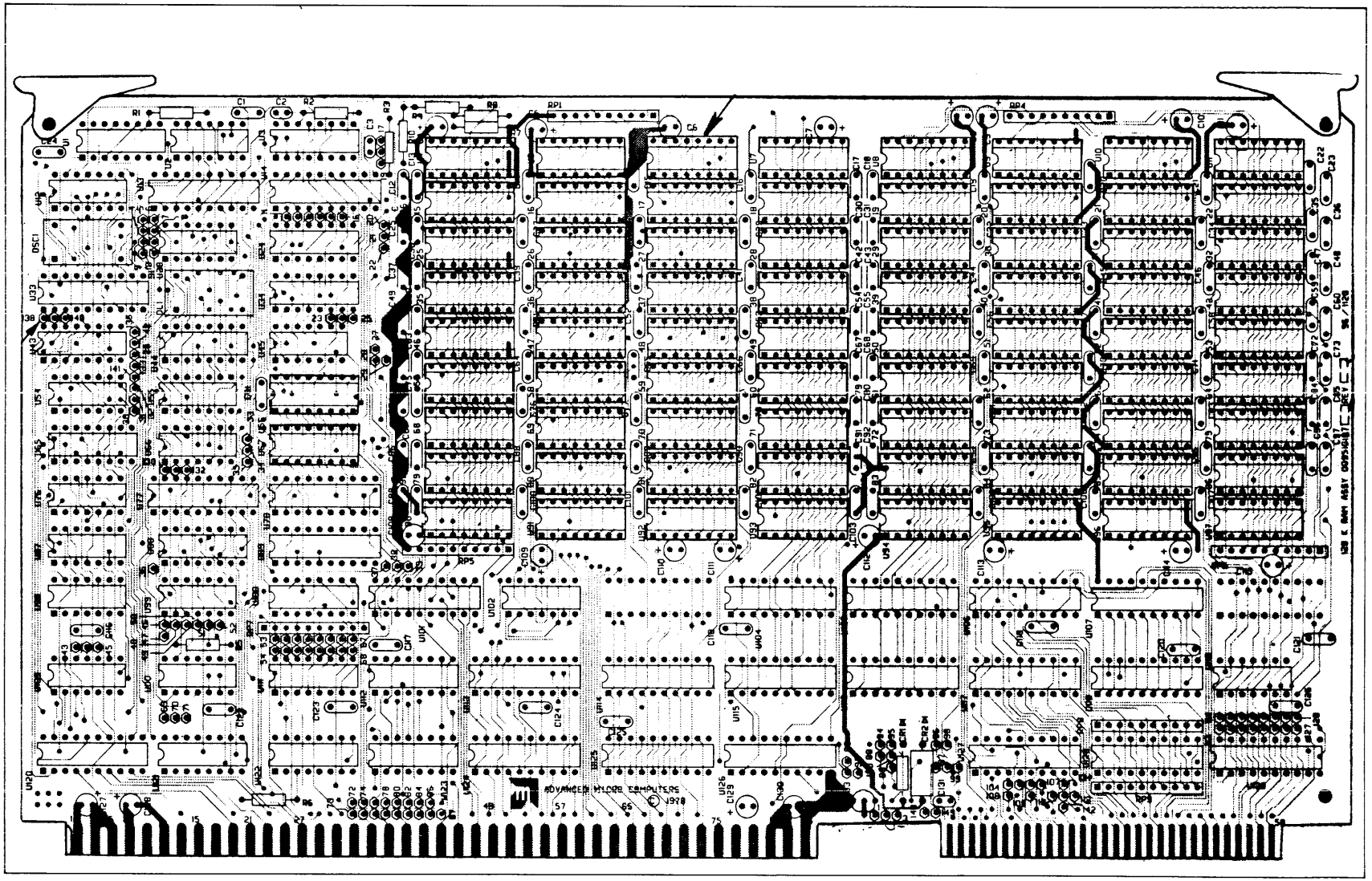
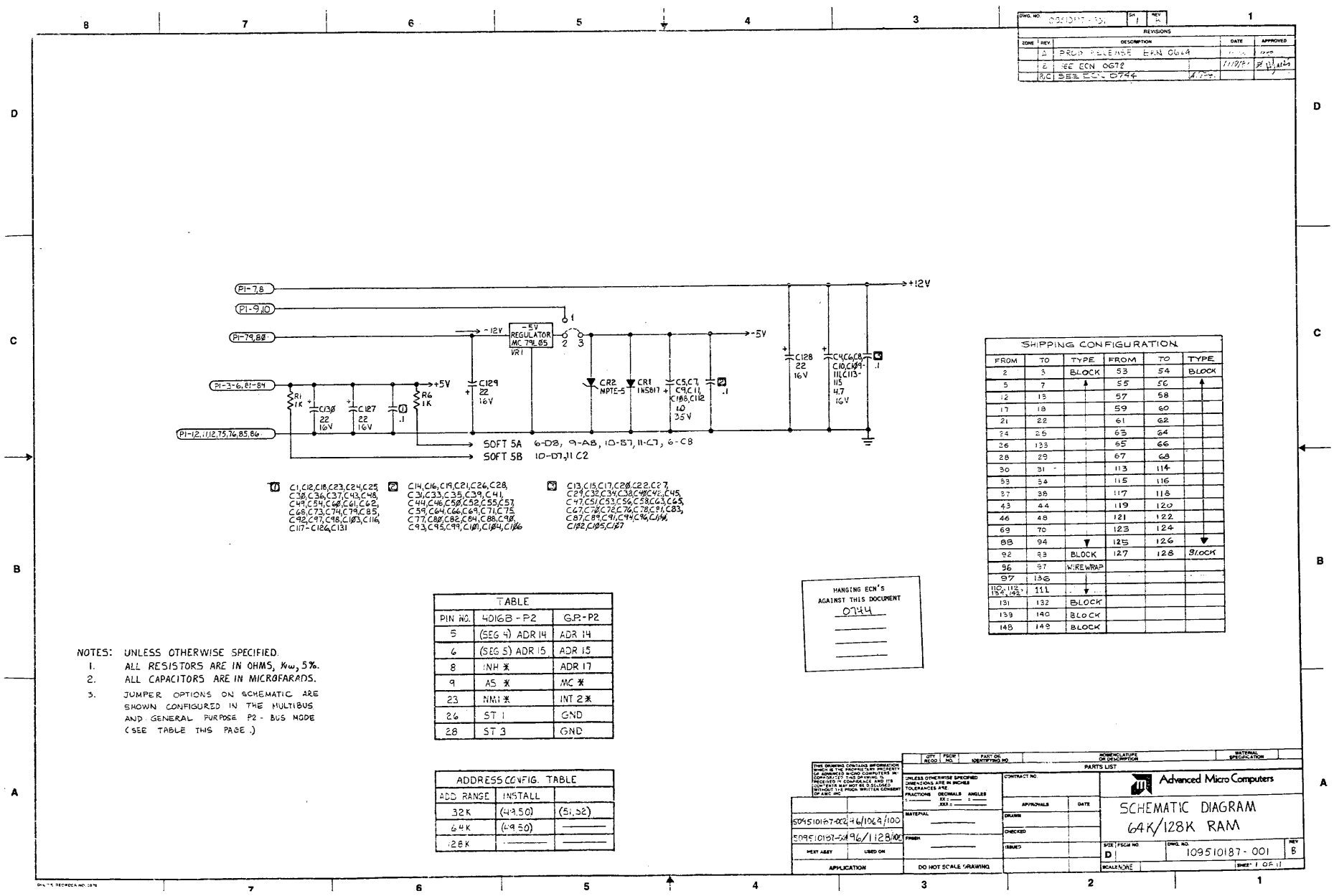


Figure 4-1. Am96/1128 Component Location Diagram



REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A	PROD RELEASE ECN 0624		
	B	SEE ECN 0672	11/19/82	
	C	SEE ECN 0744	4/84	

SHIPPING CONFIGURATION					
FROM	TO	TYPE	FROM	TO	TYPE
2	3	BLOCK	53	54	BLOCK
5	7	↑	55	56	↑
12	13		57	58	
17	18		59	60	
21	22		61	62	
24	25		63	64	
26	133		65	66	
28	29		67	68	
30	31		113	114	
53	54		115	116	
37	38		117	118	
43	44		119	120	
46	48		121	122	
69	70		123	124	
88	94	↓	125	126	↓
92	93	BLOCK	127	128	BLOCK
96	97	WIREWRAP			
97	136	↓			
110, 112, 134, 142	111	↓			
131	132	BLOCK			
139	140	BLOCK			
148	149	BLOCK			

HANGING ECN'S AGAINST THIS DOCUMENT
0744

NOTES: UNLESS OTHERWISE SPECIFIED.
1. ALL RESISTORS ARE IN OHMS, ¼w, 5%.
2. ALL CAPACITORS ARE IN MICROFARADS.
3. JUMPER OPTIONS ON SCHEMATIC ARE SHOWN CONFIGURED IN THE MULTIBUS AND GENERAL PURPOSE P2 - BUS MODE (SEE TABLE THIS PAGE.)

TABLE		
PIN NO.	4016B - P2	G.P.-P2
5	(SEG 4) ADR 14	ADR 14
6	(SEG 5) ADR 15	ADR 15
8	INH *	ADR 17
9	A5 *	MC *
23	NMI *	INT 2 *
26	ST 1	GND
28	ST 3	GND

ADDRESS CONFIG. TABLE		
ADD RANGE	INSTALL	
32K	(49,50)	(51,52)
64K	(49,50)	———
128K	———	———

PARTS LIST				
QTY. REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

509510187-002	96/1064	100	
509510187-001	96/1128	100	
NEXT ASSY	USED ON		
APPLICATION		DO NOT SCALE DRAWING	

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	
ISSUED	

Advanced Micro Computers

SCHEMATIC DIAGRAM
64K/128K RAM

SIZE D | FSCM NO. | DWG. NO. 109510187-001 | REV B

SCALE NONE | SHEET 1 OF 11

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UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
XX = ± XXX = ±

MATERIAL
FINISH

Figure 4-2. Am96/1128 Schematic Sheet 1

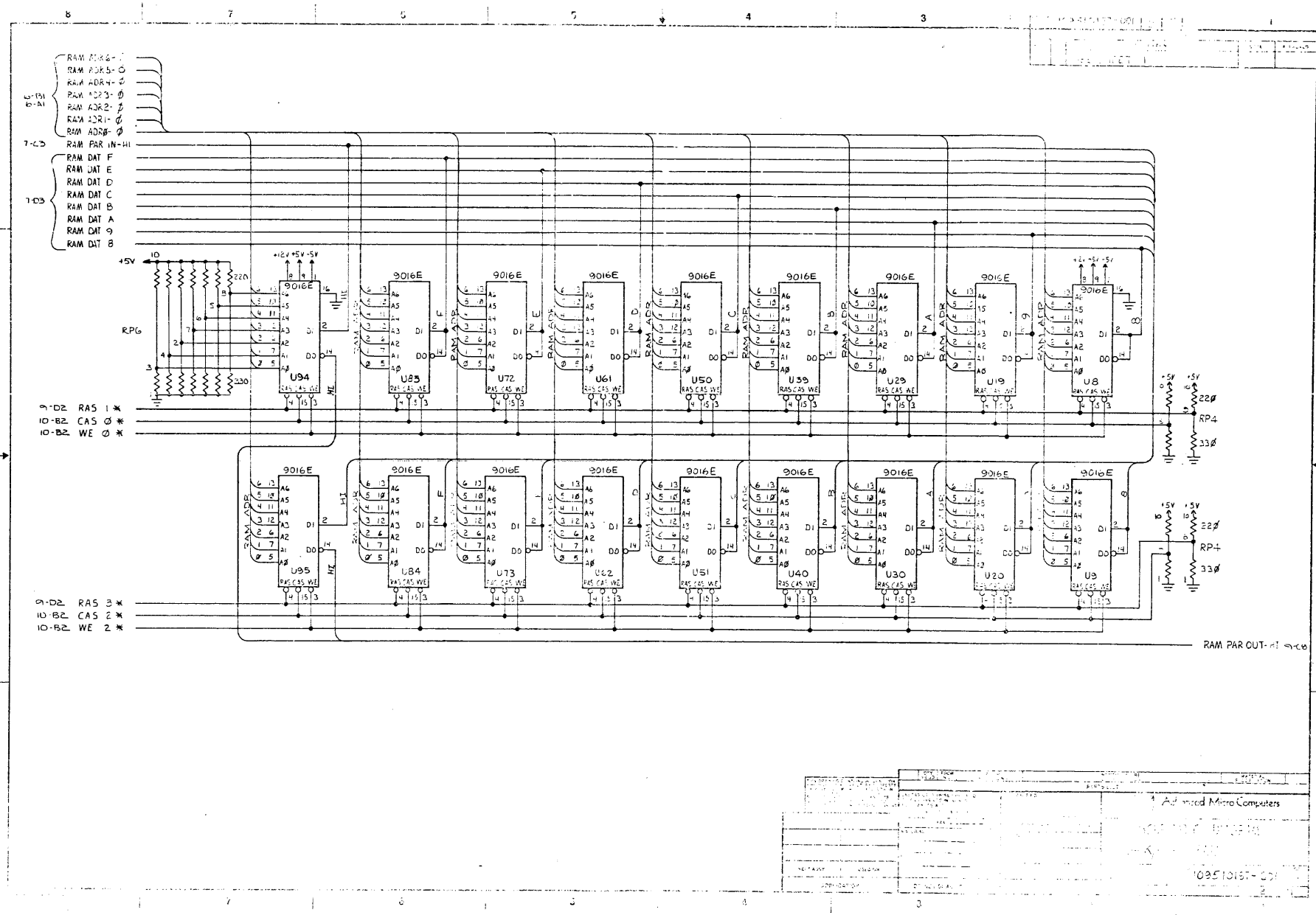


Figure 4-3. Am96/1128 Schematic Sheet 2

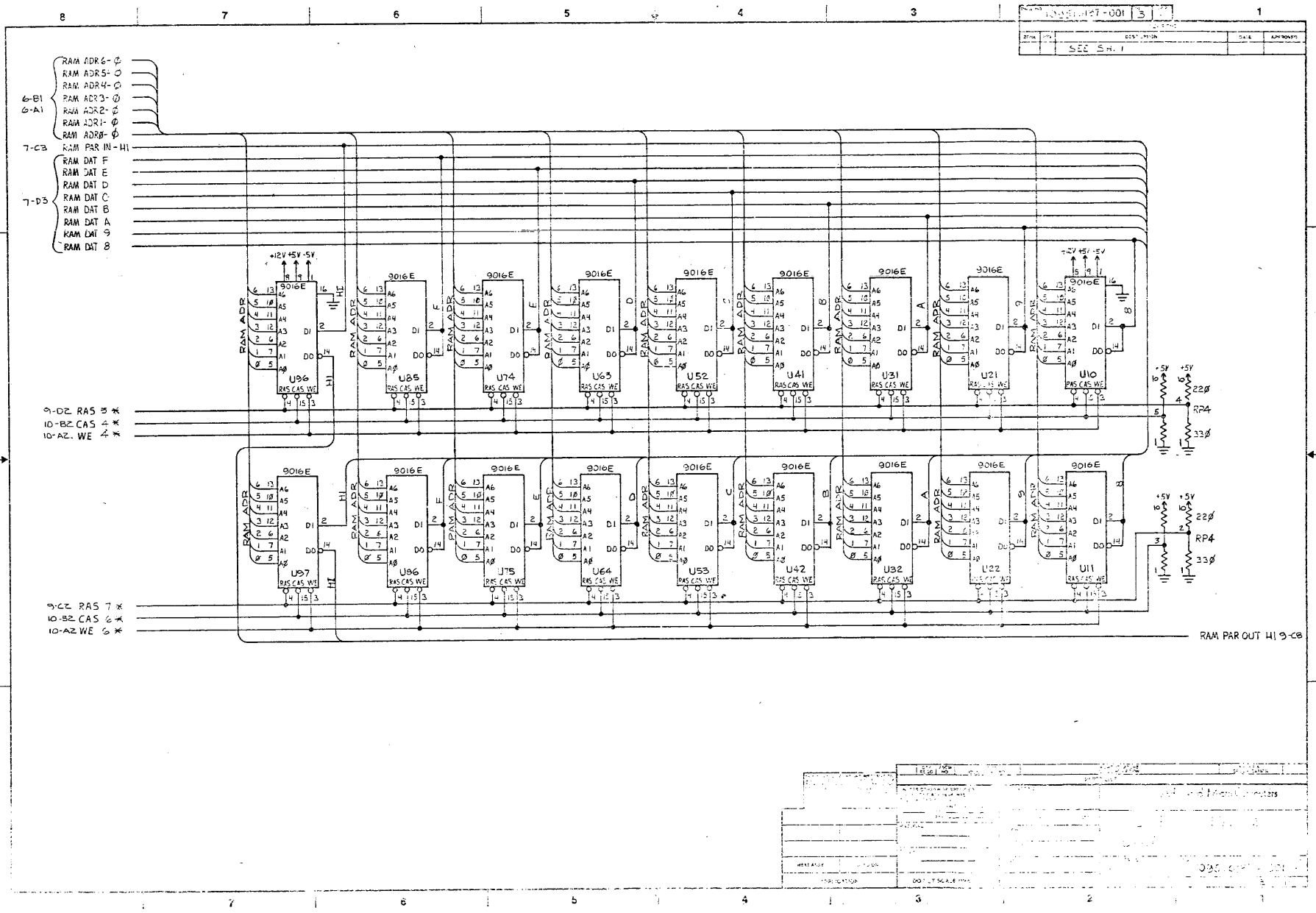


Figure 4-4. Am96/1128 Schematic Sheet 3

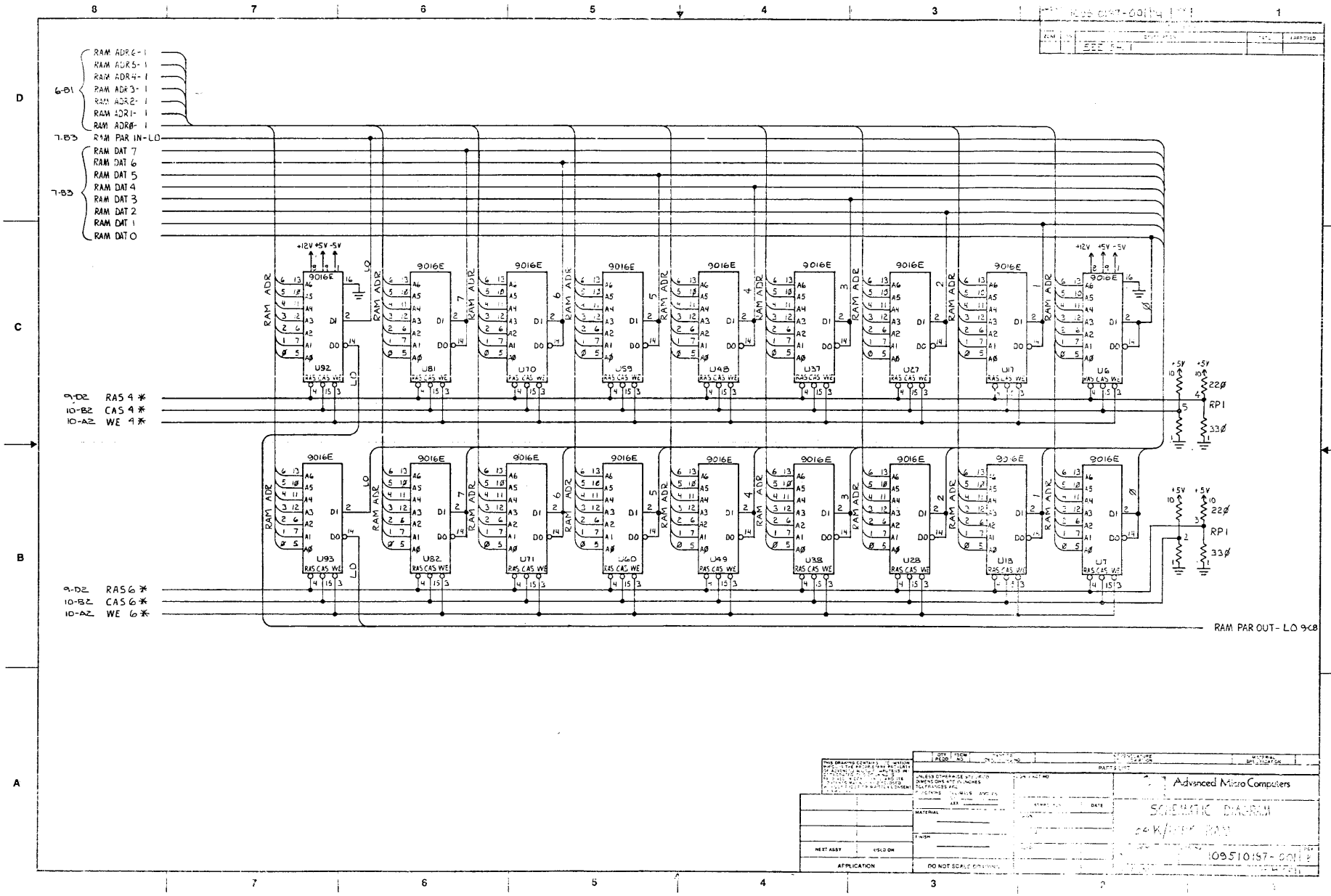


Figure 4-5. Am96/1128 Schematic Sheet 4

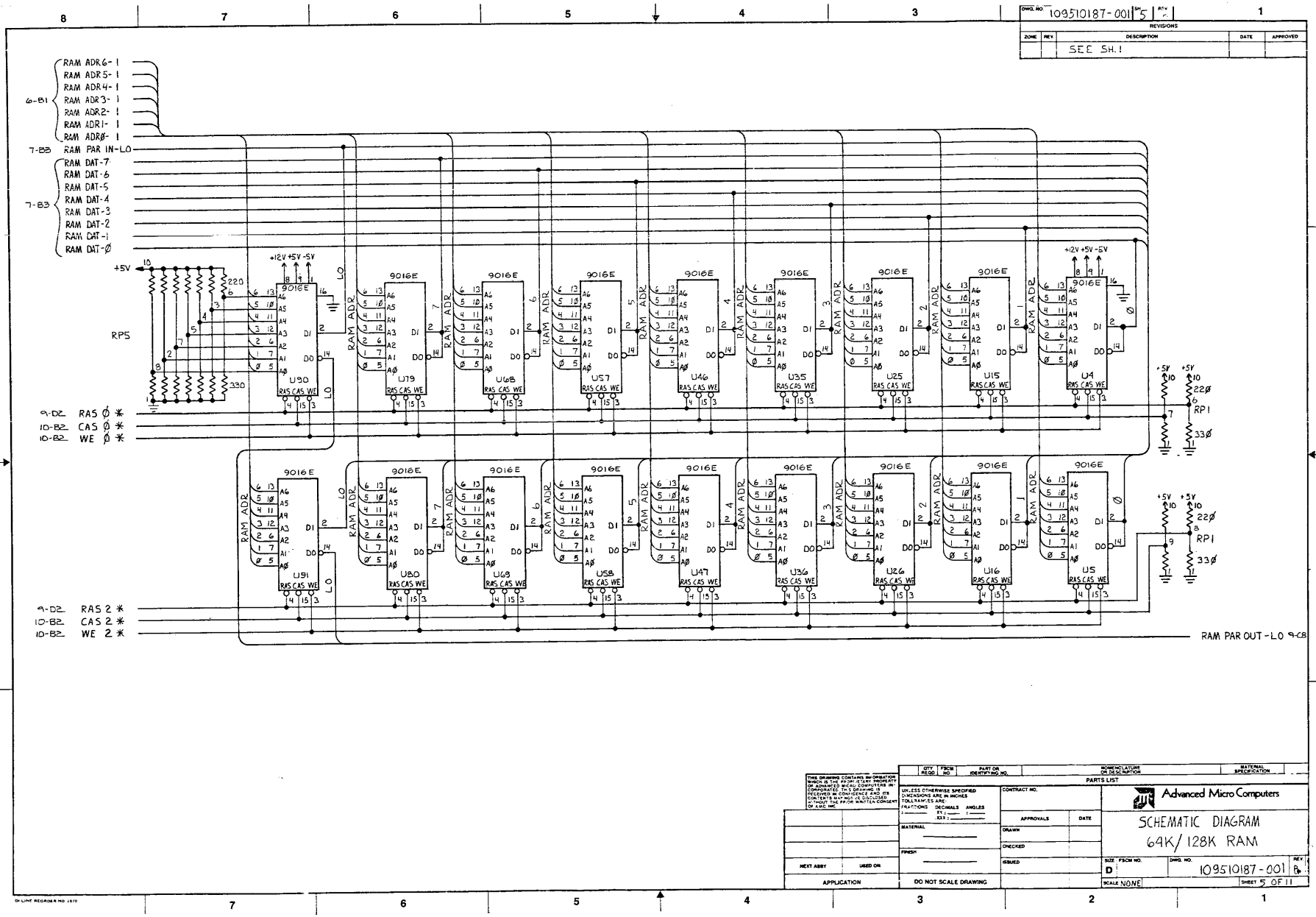


Figure 4-6. Am96/1128 Schematic Sheet 5

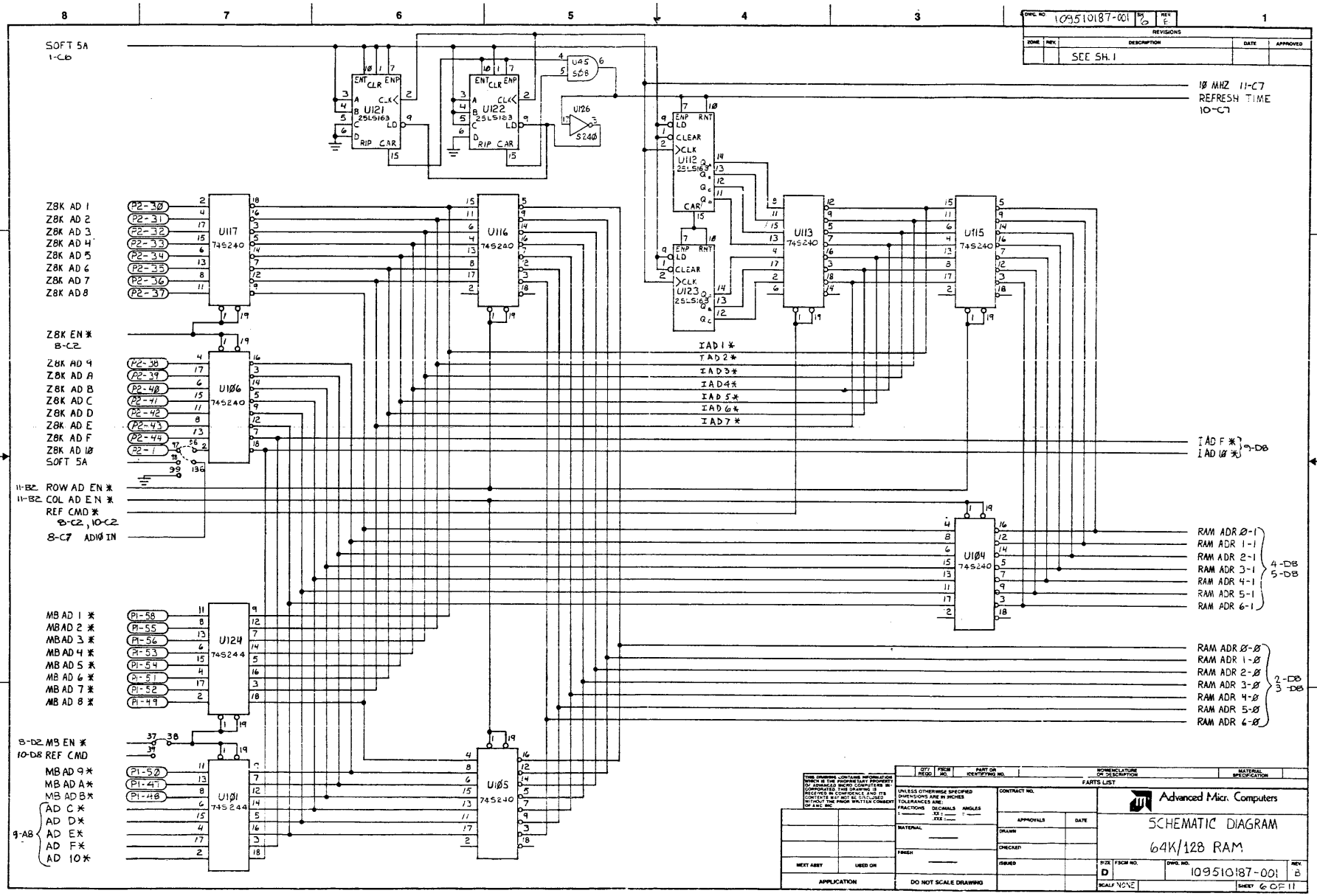


Figure 4-7. Am96/1128 Schematic Sheet 6

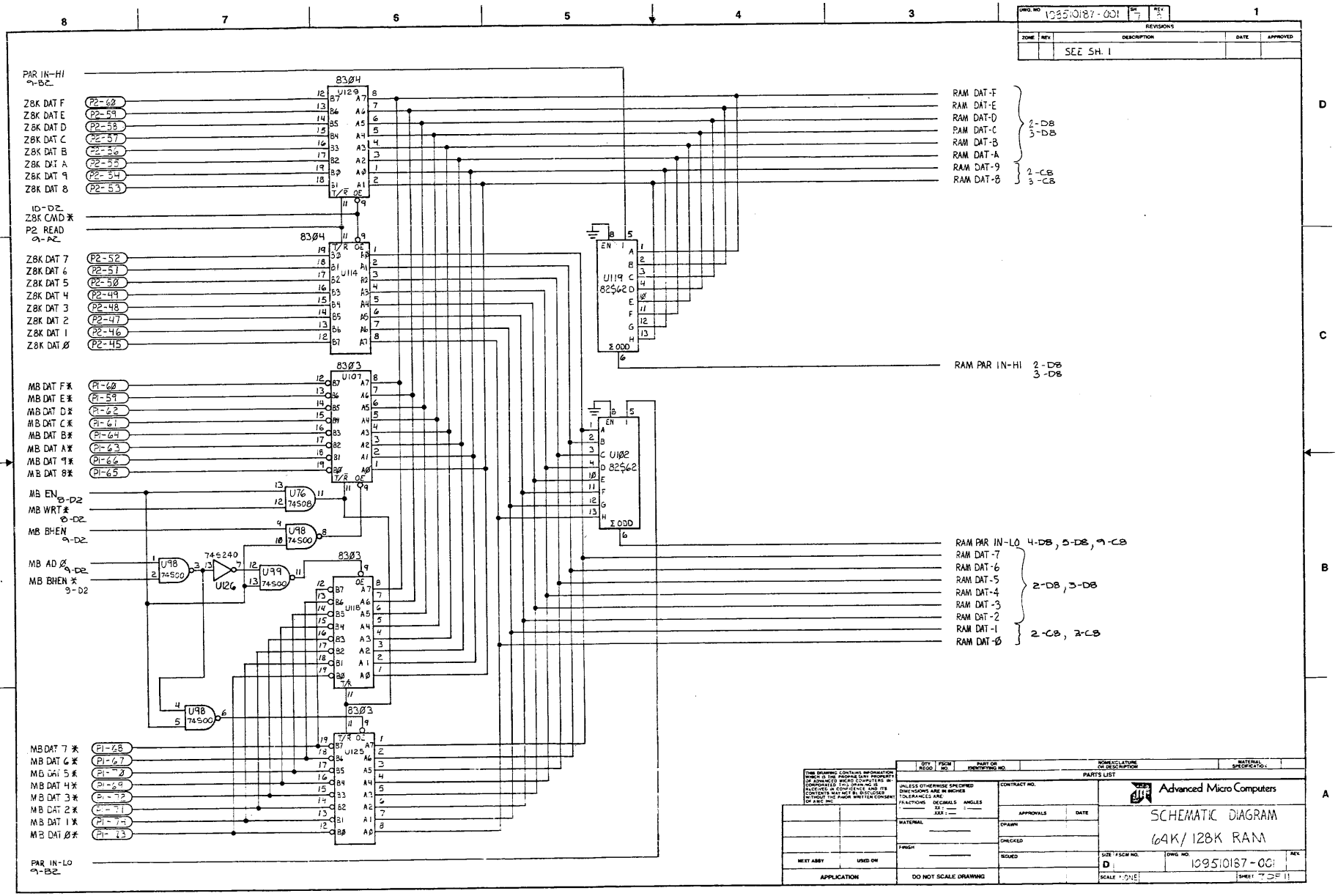


Figure 4-8. Am96/1128 Schematic Sheet 7

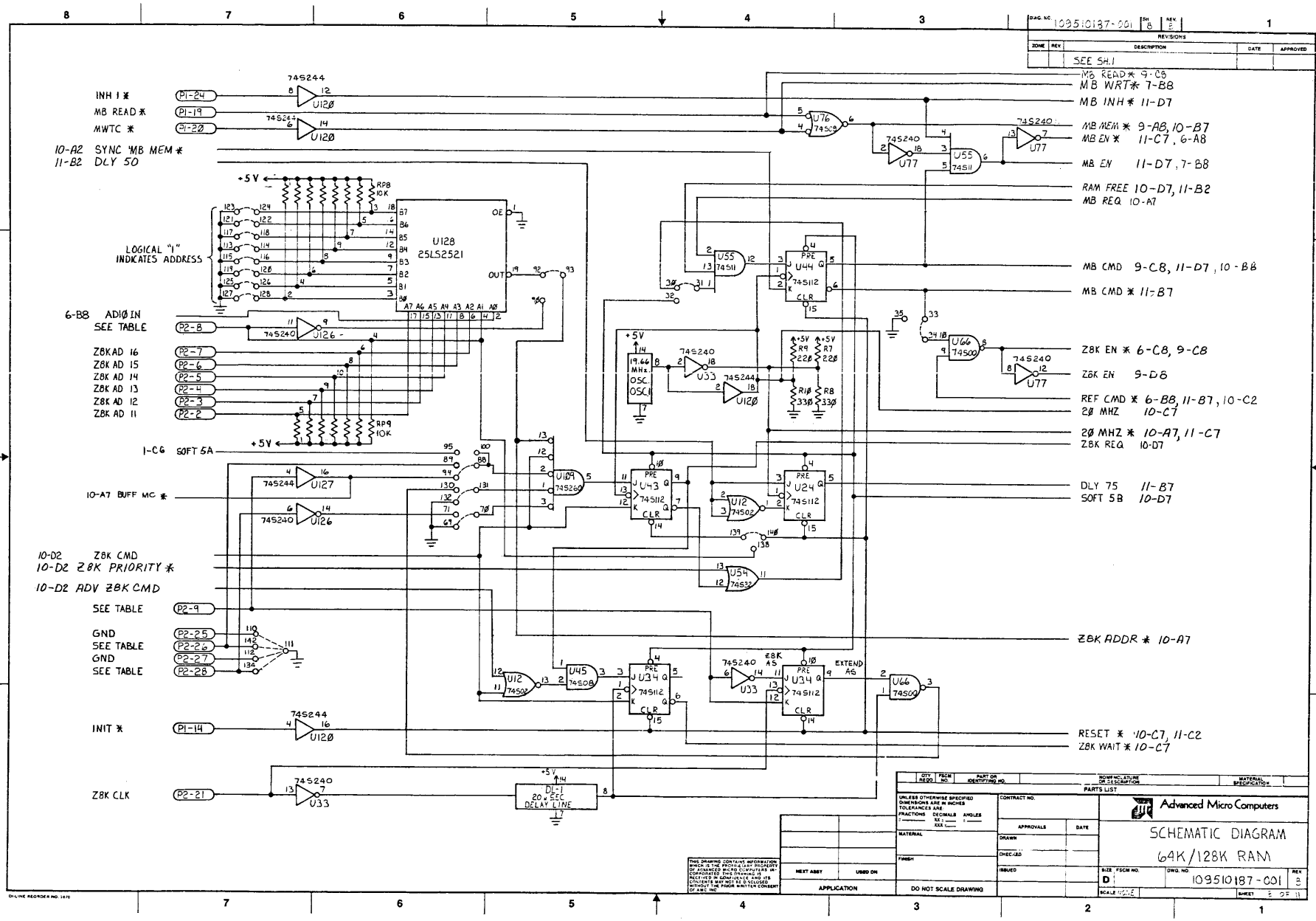


Figure 4-9. Am96/1128 Schematic Sheet 8

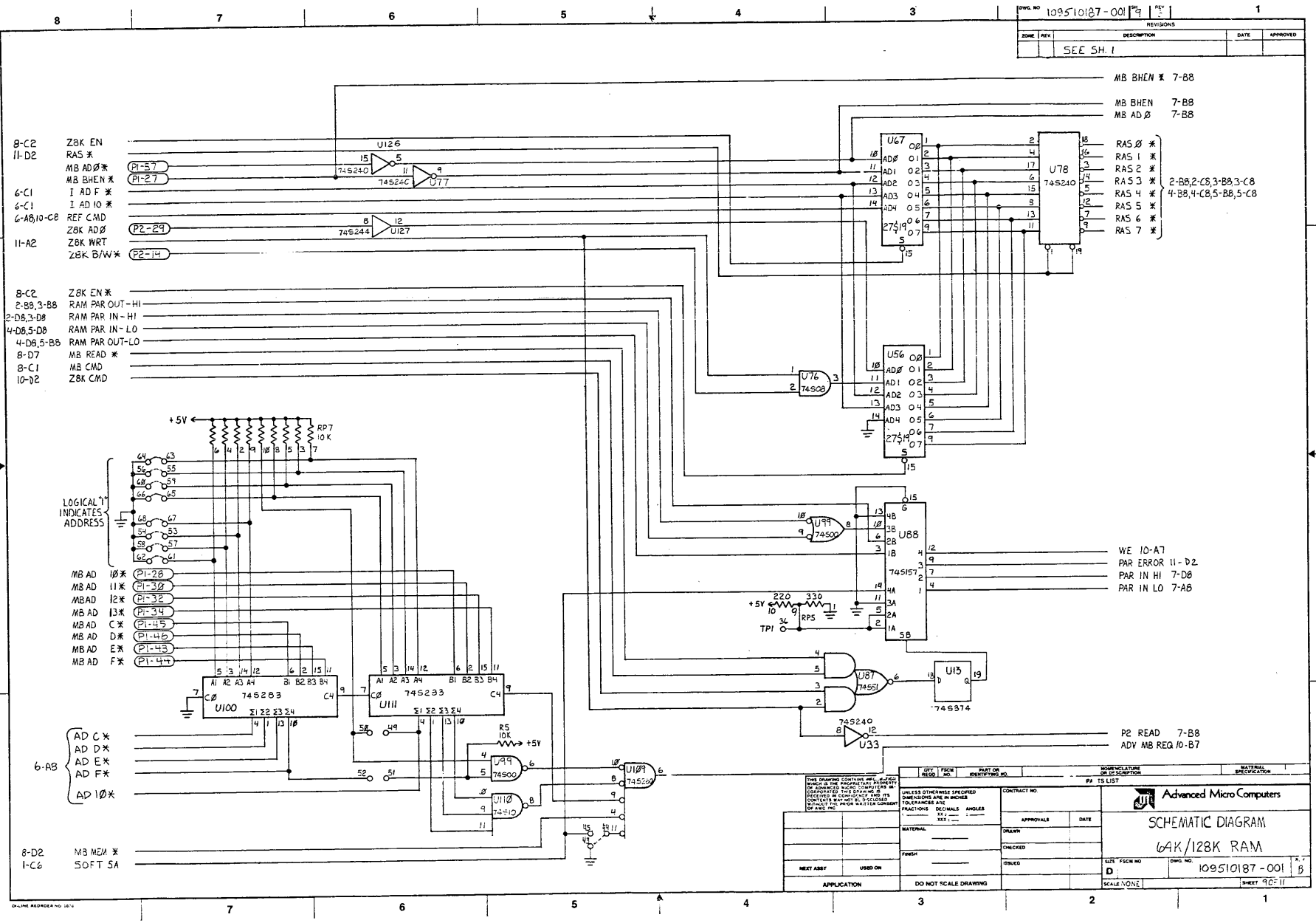


Figure 4-10. Am96/1128 Schematic Sheet 9

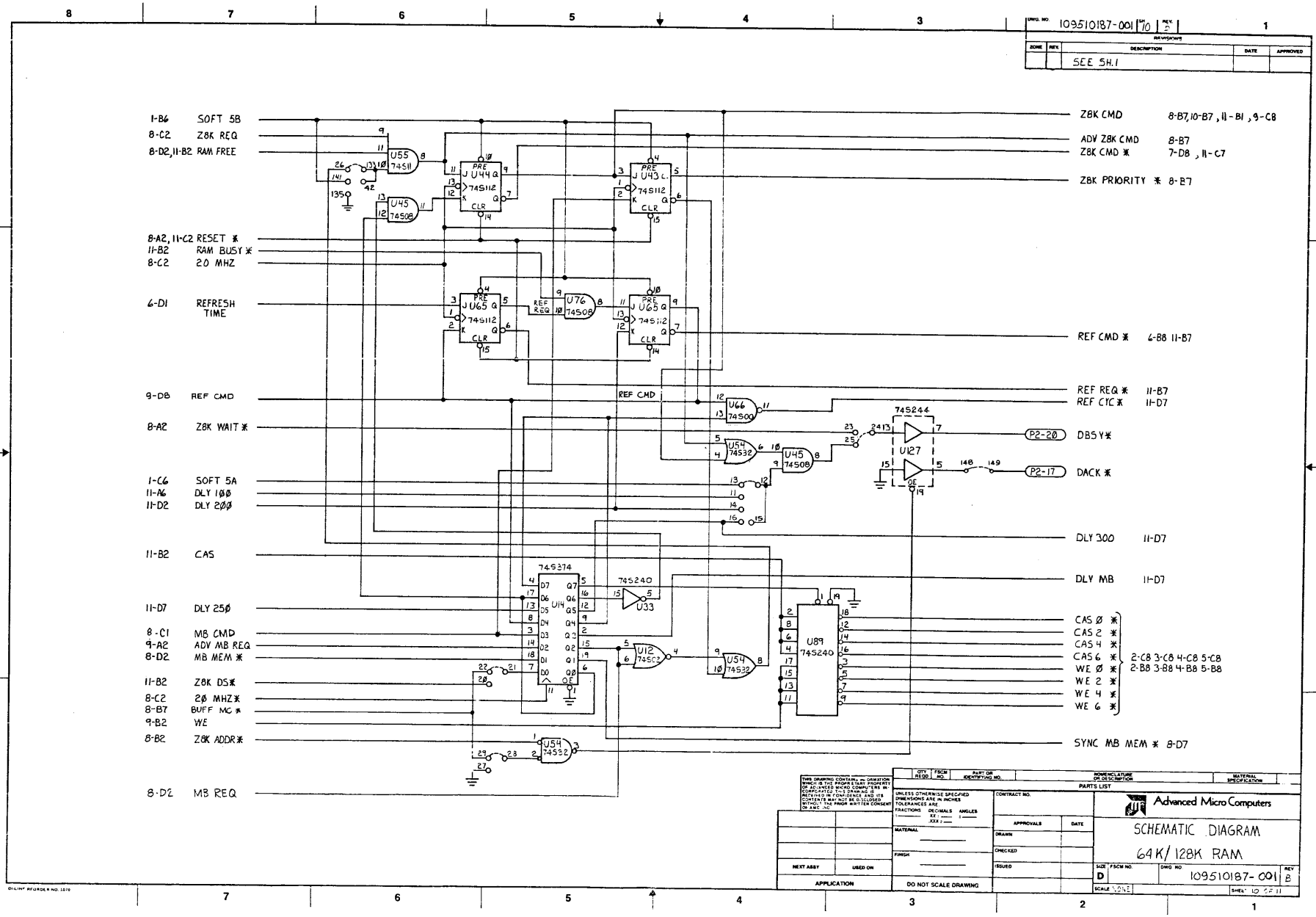


Figure 4-11. Am96/1128 Schematic Sheet 10

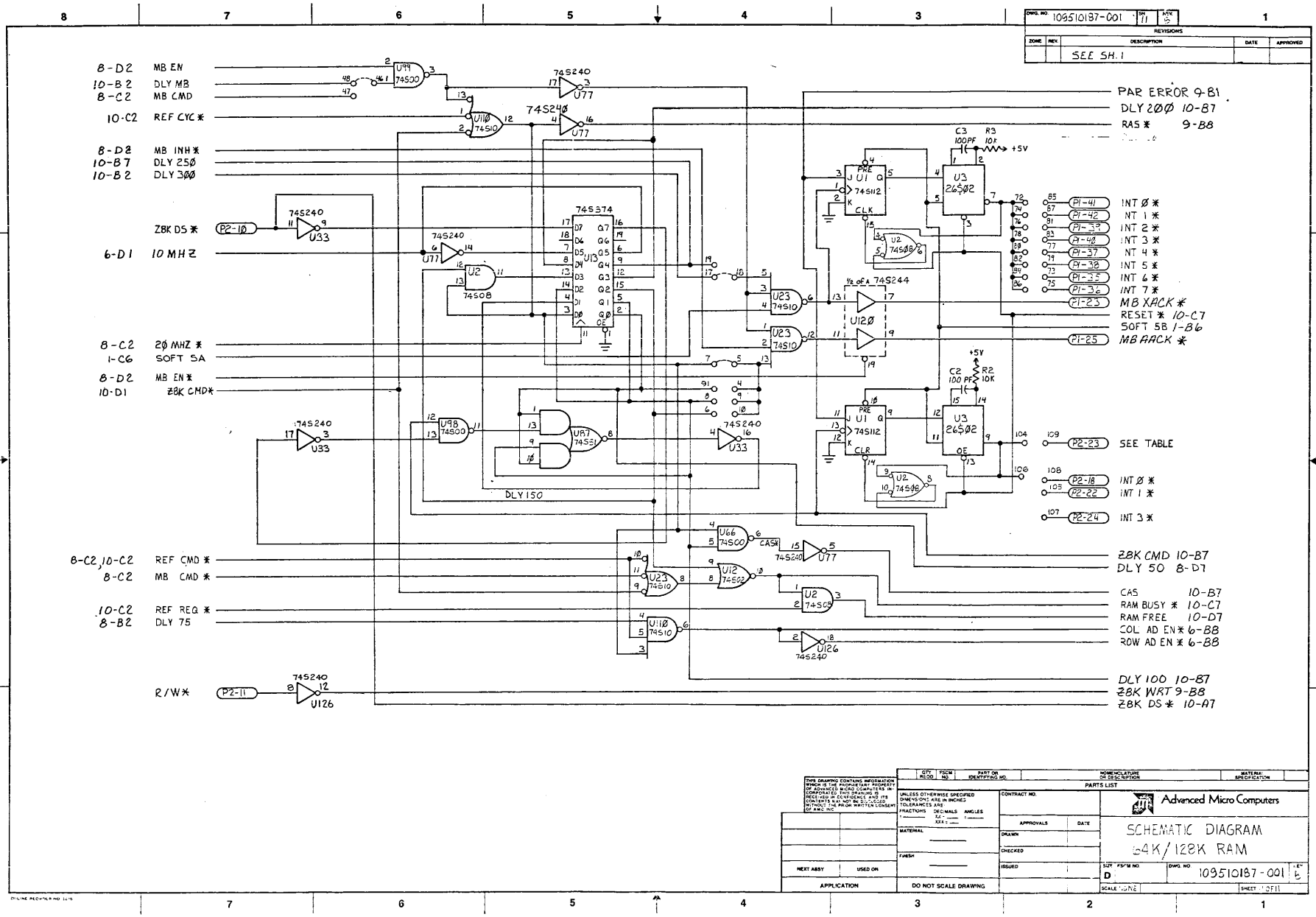


Figure 4-12. Am96/1128 Schematic Sheet 11

Publication Change Notice

Advanced Micro Computers Incorporated
3340 Scott Boulevard
Santa Clara, California 95051
(408) 988-7777

96/1000 SERIES

Date:	September 1, 1981
Title:	Am96/1000 Series, Dynamic RAM Boards
Publication Number:	00680140
Revision Level:	C
Reason for Change:	Correction of table 2-3, Replacement of Schematics in figures 4-11 and 4-12.

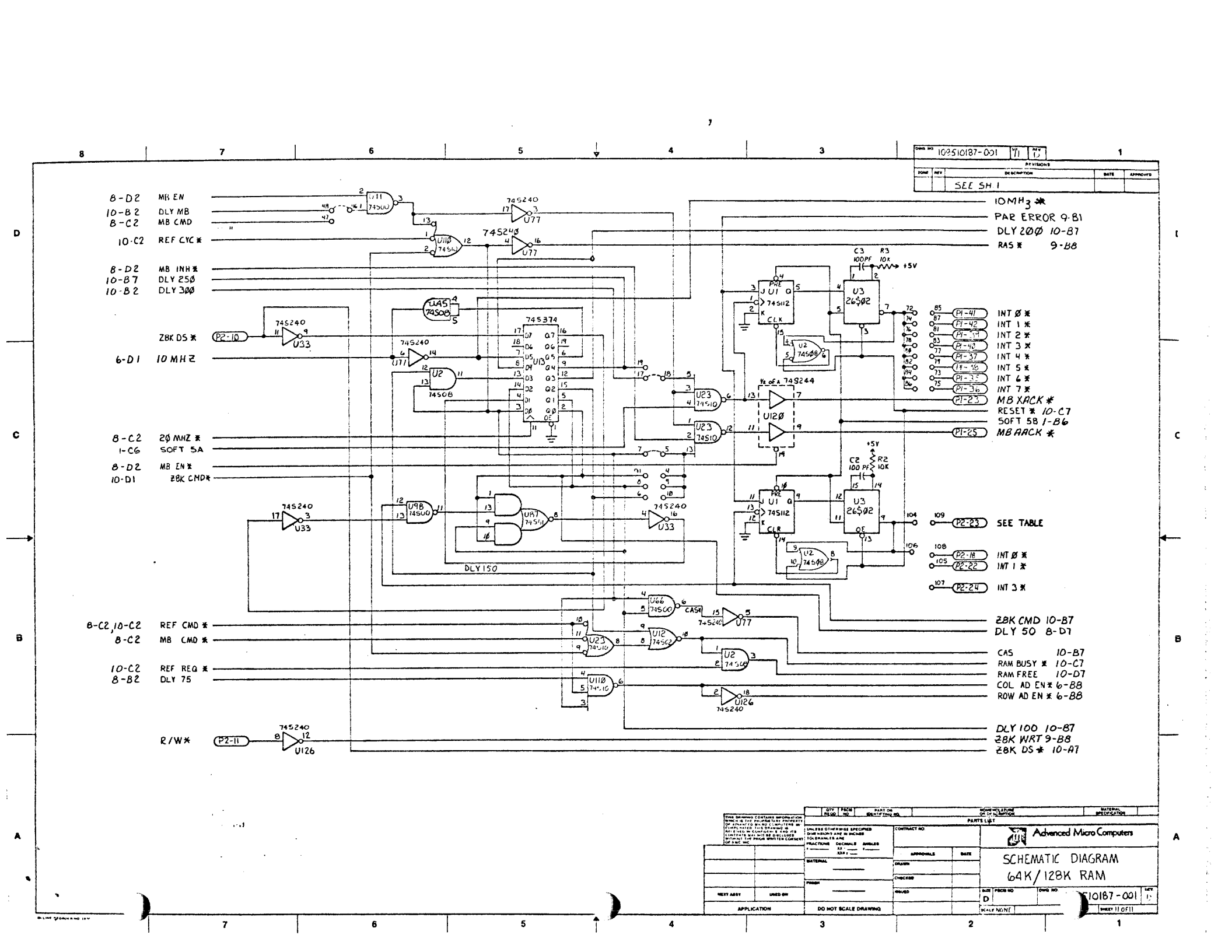
Instructions:

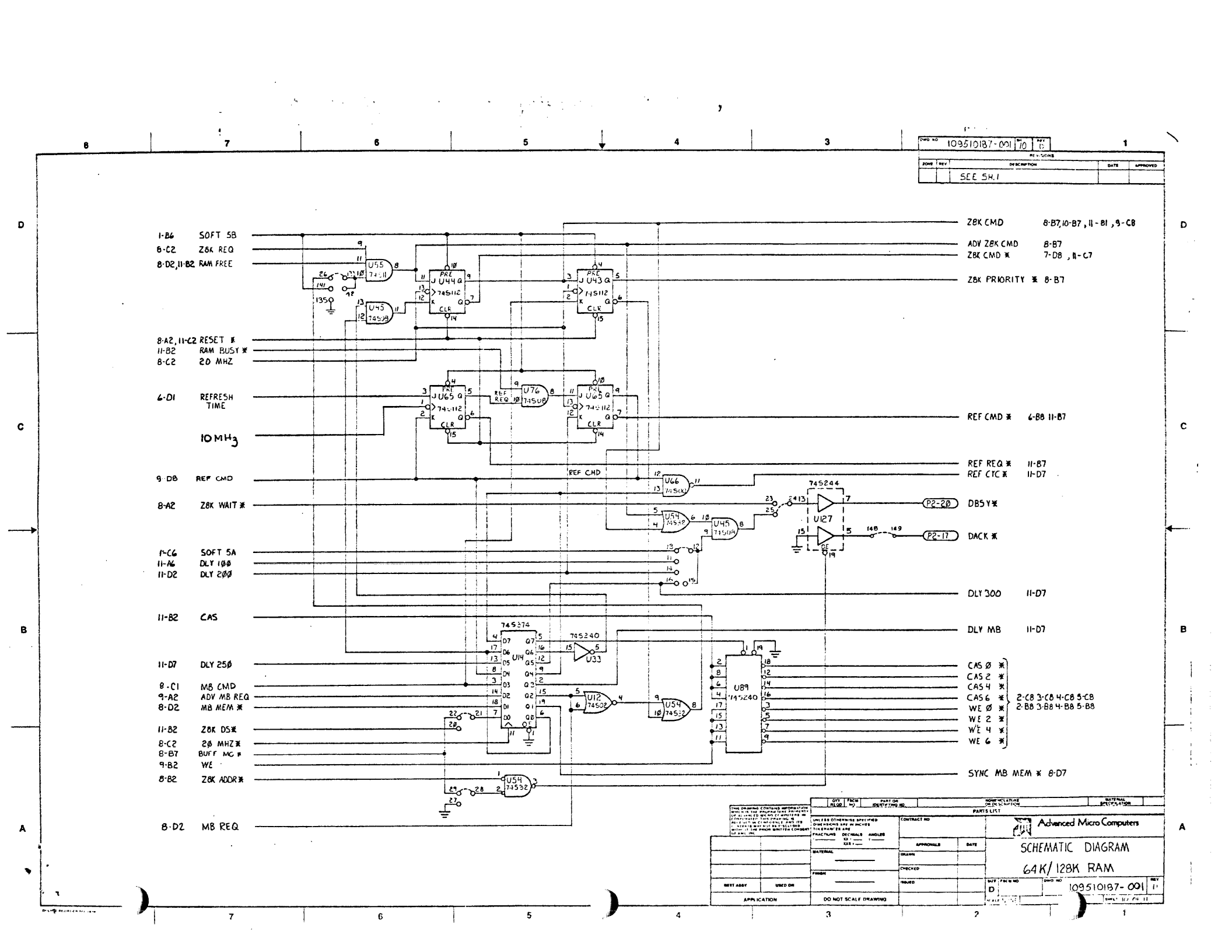
1. On REVISION RECORD Page, Add:

REVISION	DESCRIPTION
C (9/1/81)	Table 2-3 corrected figures 4-11, 4-12, reflect current revision.

2. In table 2-3, delete jumper 97-136
   replace it with 99-136

3. Remove and replace with the attached figures 4-11 and 4-12.


8-D2 MB EN
10-B2 DLY MB
8-C2 MB CMD
10-C2 REF CYC *
8-D2 MB INH *
10-B7 DLY 250
10-B2 DLY 300
Z8K DS *
6-D1 10 MHZ
8-C2 20 MHZ *
1-C6 SOFT 5A
8-D2 MB EN *
10-D1 Z8K CMD *
8-C2,10-C2 REF CMD *
8-C2 MB CMD *
10-C2 REF REQ *
8-B2 DLY 75
R/W *
P2-10
P2-11
10MH3 *
PAR ERROR 9-B1
DLY 200 10-B7
RAS * 9-B8
INT Ø *
INT 1 *
INT 2 *
INT 3 *
INT 4 *
INT 5 *
INT 6 *
INT 7 *
MB XACK *
RESET * 10-C7
SOFT 5B 1-B6
MB AACK *
SEE TABLE
INT Ø *
INT 1 *
INT 3 *
Z8K CMD 10-B7
DLY 50 8-D7
CAS 10-B7
RAM BUSY * 10-C7
RAM FREE 10-D7
COL AD EN * 6-B8
ROW AD EN * 6-B8
DLY 100 10-B7
Z8K WRT 9-B8
Z8K DS * 10-A7
DLY 150
Advanced Micro Computers
SCHEMATIC DIAGRAM
64K/128K RAM
10187-001


DWG NO 109510187-001 SH 10 REV C
REVISIONS
ZONE REV DESCRIPTION DATE APPROVED
SEE SH.1
1-B6 SOFT 5B
6-C2 Z8K REQ
8-D2,11-B2 RAM FREE
8-A2,11-C2 RESET *
11-B2 RAM BUSY *
8-C2 20 MHZ
6-D1 REFRESH TIME
10MH3
9-D8 REF CMD
8-A2 Z8K WAIT *
1-C6 SOFT 5A
11-A6 DLY 100
11-D2 DLY 200
11-B2 CAS
11-D7 DLY 250
8-C1 MB CMD
9-A2 ADV MB REQ
8-D2 MB MEM *
11-B2 Z8K DS *
8-C2 20 MHZ *
8-B7 BUFF MC *
9-B2 WE
8-B2 Z8K ADDR *
8-D2 MB REQ
U55 74S11
U44 J Q 74S112 K CLR
U43 J Q 74S112 K CLR
U45 74S08
U65 J Q 74S112 K CLR
U76 74S08
U66 74S00
U54 74S32
U45 74S08
U127 74S244
P2-20 DB5Y *
P2-17 DACK *
U14 74S374
U33 74S240
U12 74S02
U54 74S32
U89 74S240
Z8K CMD 8-B7,10-B7,11-B1,9-C8
ADV Z8K CMD 8-B7
Z8K CMD * 7-D8,11-C7
Z8K PRIORITY * 8-B7
REF CMD * 6-B8 11-B7
REF REQ * 11-B7
REF CTC * 11-D7
DLY 300 11-D7
DLY MB 11-D7
CAS Ø *
CAS 2 *
CAS 4 *
CAS 6 *
WE Ø *
WE 2 *
WE 4 *
WE 6 *
2-C8 3-C8 4-C8 5-C8
2-B8 3-B8 4-B8 5-B8
SYNC MB MEM * 8-D7
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