Slave Mode

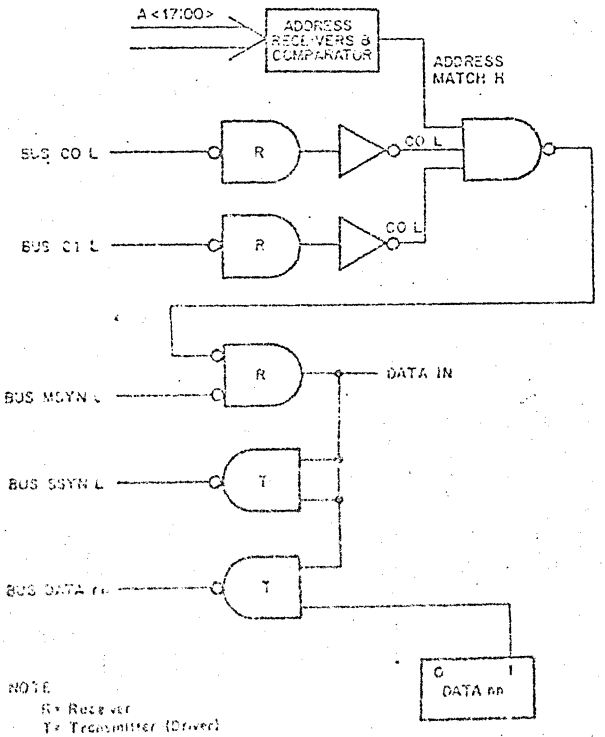
SLAVE MODE OPERATION INCLUDES 2 SEPERATE FUNCTIONS: DATA IN & DATA OUT. THESE MODES WILL BE EXPLAINED SEPERATELY. THESE FUNCTIONS ARE USED FOR LOADING AND READING THE INTERNAL REGISTERS FROM THE UNIBUS. THE REGISTER AND FUNCTIONS AVAILABLE ARE AS FOLLOWS:

Register Description	UNIBUS Address	Comments
Look Ahead Register RCLA	777440	Read Only
Disc Address Register RCDA	777442	Read/Write
Disc Error Status Register RCER	777444	Read Only
Command & Status Register RCCS	777446	Read/Write
Word Count Register RCWC	777450	Read/Write
Current Address Register RCCA	777452	Read/Write
Disc Address Extension Register RCEX	777454	Read/Write

DATA IN MODE USES UNIBUS SIGNALS C0, C1, ADDRESS 0-17, DATA 0-15, MSYN, SSYN IN THE FOLLOWING RELATIONSHIP (Ref. DEC, UNIBUS THEORY OF OPERATION).

1. ADDRESS IS ASSERTED, C0+C1 ARE UNASSERTED
2. 150 ns MIN LATER MSYN IS ASSERTED
3. UPON RECEIVING MSYN THE CONTROLLER ASSERTS SSYN AND DATA 0-15
4. 75 ns MIN LATER MSYN IS REMOVED
5. REMOVAL OF MSYN CAUSES THE CONTROLLER TO REMOVE SSYN AND DATA 0-15
6. 75 ns MIN LATER ADDRESS IS REMOVED WHICH COMPLETES THE CYCLE

THIS SEQUENCE TRANSFERS THE CONTENTS OF A REGISTER SPECIFIED BY ADDRESS 0-17 TO THE UNIBUS WITHOUT DISTURBING THE CONTENTS OF THE REGISTER. A SIMPLIFIED SCHEMATIC AND TIMING DIAGRAM OF THIS OPERATION ARE SHOWN BELOW



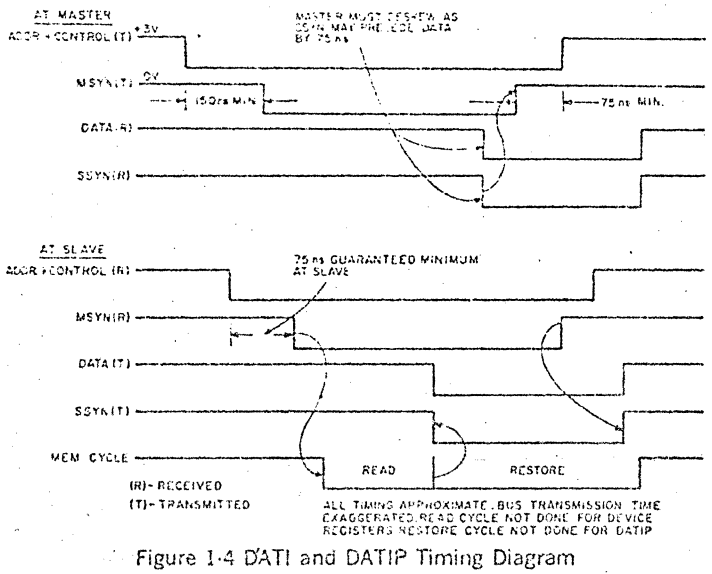


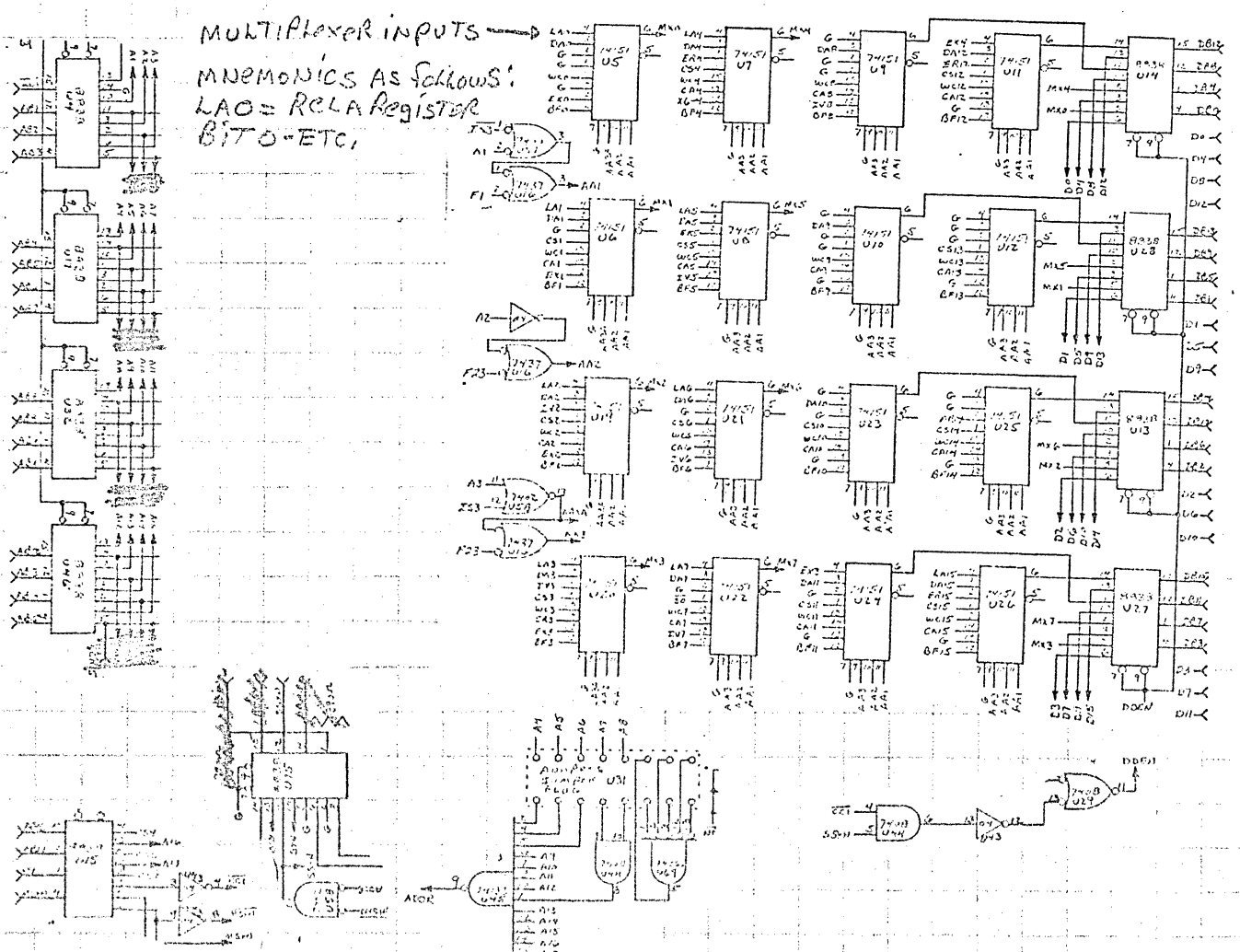
Figure 1-4 DATI and DATIP Timing Diagram

SLAVE MODE - DATA IN (CONTINUED)

THE ACTUAL CIRCUITRY TO PERFORM DATA IN FUNCTION IS DESCRIBED BELOW (REF [redacted] SCHEMATIC) SHEET 5

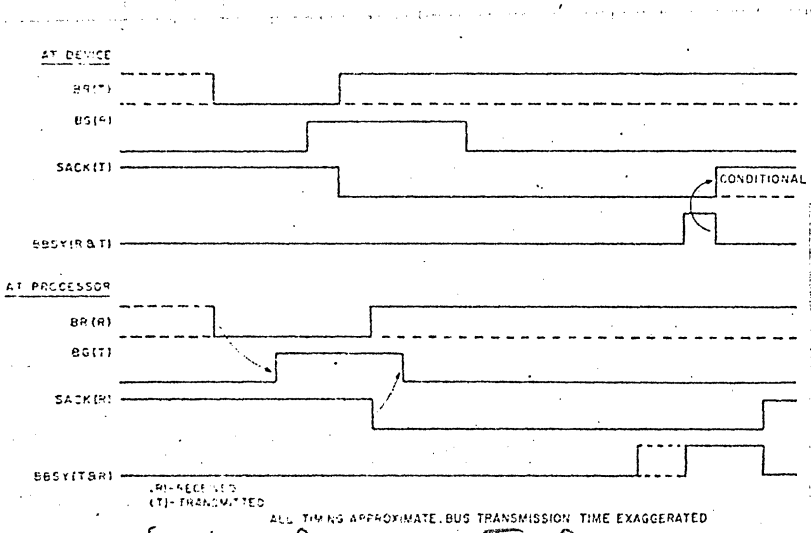
ADDRESS RECEIVERS U4, U17, U32 AND U46 (8838) ARE USED TO TRANSLATE THE UNIBUS ADDRESS LINES TO TTL COMPATABLE SIGNAL LEVELS. A4 - A17 ARE DECODED THROUGH THE ADDRESS JUMPER PLUG* U44 (7408), U69 (74260) AND U45 (74133) TO GENERATE "ADDR". ADDR INDICATES THAT THIS DEVICE IS SELECTED TO PERFORM SOME FUNCTION (0=TRUE). TYPICAL ADDRESSES ALLOWED BY THE JUMPER PLUG ARE 777000 THRU 777760, 777440 - 777454 ARE NORMAL. A1, 2 & 3 ARE CONNECTED THRU ( ) TO THE MULTIPLEXER SELECTOR INPUTS (U5 - U12, U19 - U26) WHICH SELECT THE REGISTER TO BE PRESENTED TO THE INPUTS OF THE BUS DRIVERS (U13, 14, 27 & 28). THIS CONDITION PREVAILS UNTIL MSYN IS RECEIVED FROM THE UNIBUS. MSYN IS RECEIVED BY U15 (8838) AND DECODED BY (U59, 23→1) TO GENERATE SSYN WHICH IS TRANSMITTED BY U75 (8838) AND IS ALSO GATED WITH C1 (7408 - U44) TO FORM SIGNAL DDEN'. DDEN ENABLES THE DATA BUS DRIVERS U13, 14, 27 & 28 TO TRANSMIT DATA TO THE UNIBUS. THIS CONDITION REMAINS UNTIL MSYN IS REMOVED, NEGATING SSYN WHICH NEGATES DDEN. THIS COMPLETES THE DATA IN SYNC - ONCE MSYN IS REMOVED "ADDR" DOES NOTHING

* EXACT WIRING OF JUMPER PLUG IN INSTALLATION SECTION

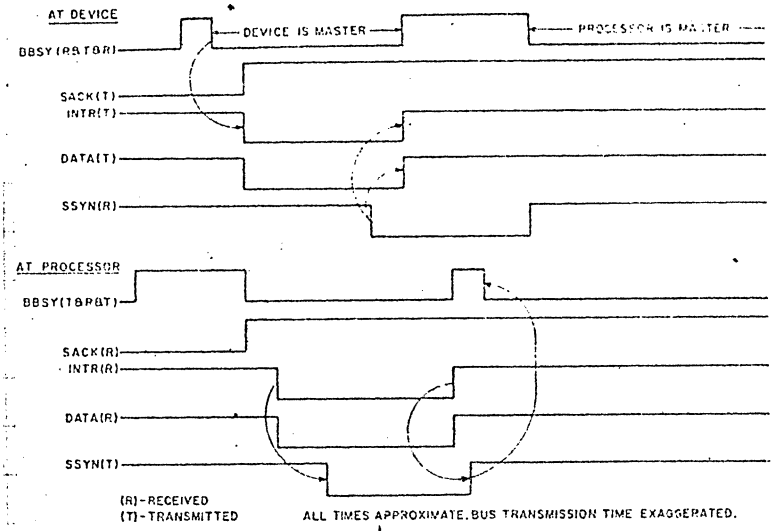


Interrupt Mode

Interrupt mode is used to indicate to the Unibus that a specific function has been completed. This mode is under software control in that bit 6 of the RCCS register permits this function. In order to accomplish an interrupt, bus master must be transferred to the controller which can then place the interrupt vector on the data bus. Below is a timing diagram showing signals and relationships.



Acquiring Bus Master

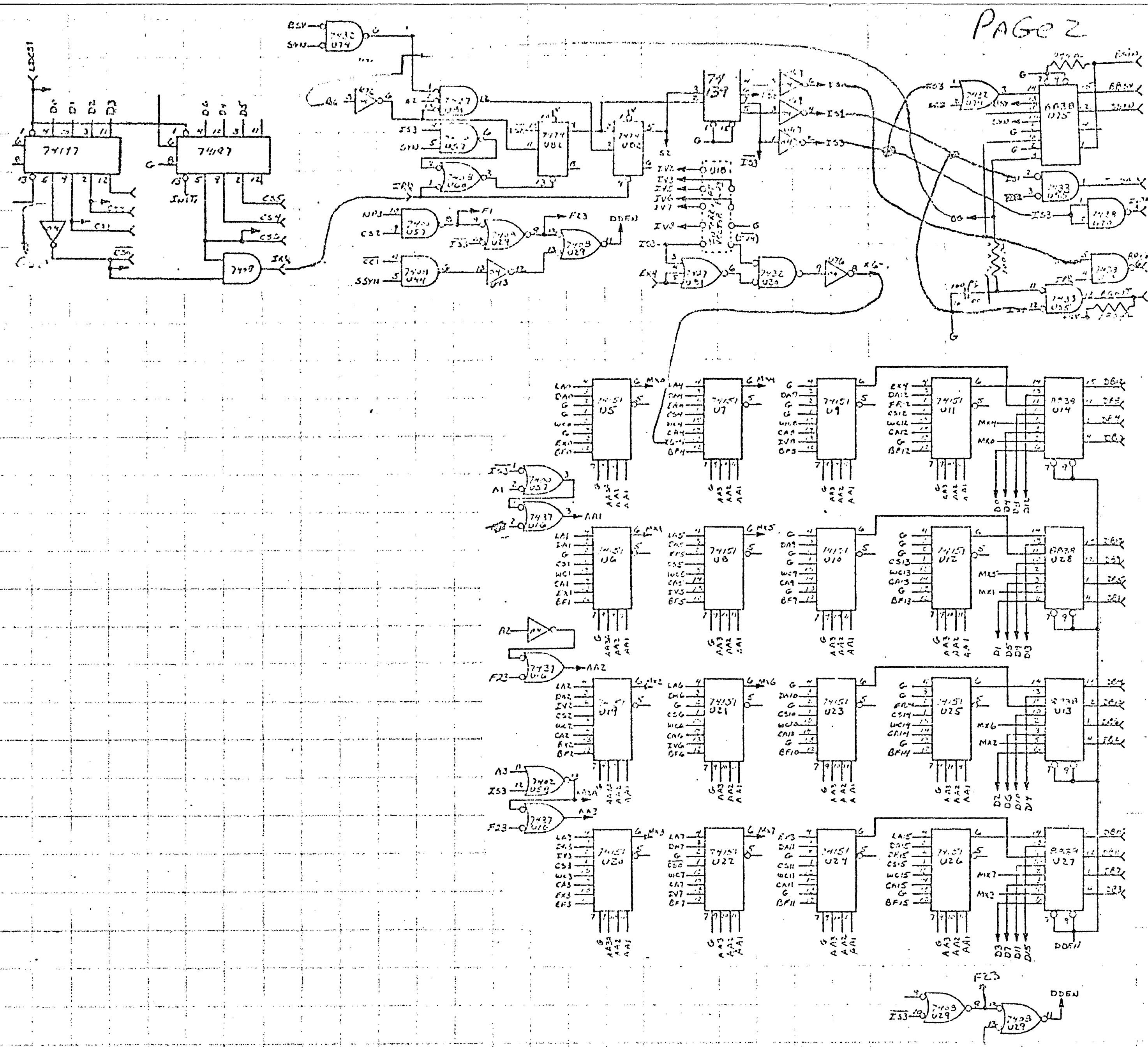


Interrupt Vector Transfer

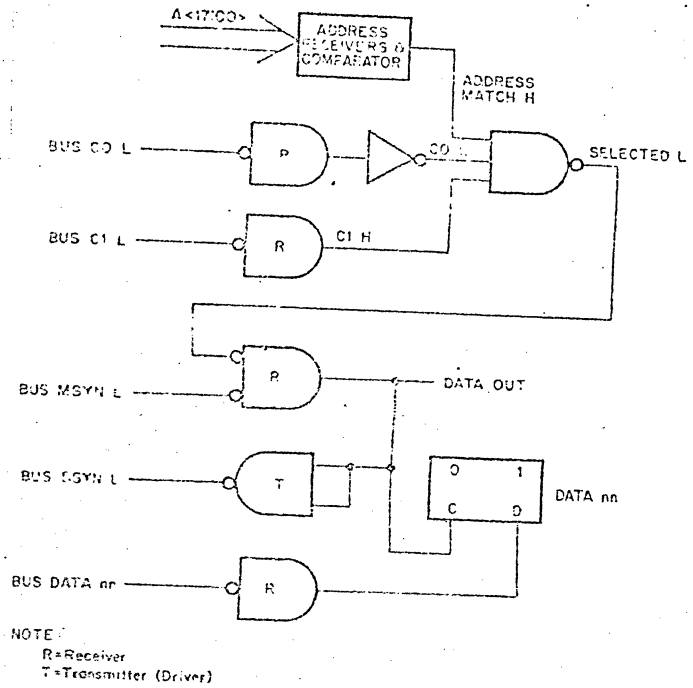
(Ref Schematic Page 2)

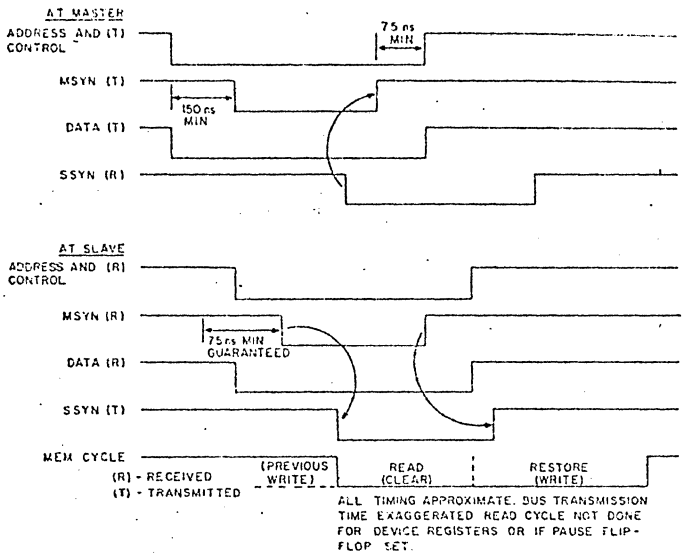
Interrupt is enabled by $\overline{\text{RCCS 0}}$ and RCCS 6 this occurs on completion of a function (Read, write or write clock) or by program control (example clear RCCS 0 & 6 then set RCCS 6). The sequence of operation is as follows: Flops U82 are held reset by IRQ ($\overline{\text{CS0}} \cdot \text{CS6}$). When IRQ becomes true gate U70-6 becomes asserted. When BG in becomes asserted, flop U82-9 becomes set changing the input of the 2-4 line decoder U83 (74139) from IS0 & to IS1. IS1 is used to assert "SACK" (U55-1) and also inhibit BG out (U55-13). When BG, BSY, & SYN become unasserted, gate U81-12 clocks U82-5 which generates IS3. IS3 causes "INTR" (U70-3) and also causes the multiplexer address inputs to become "6" for U7-12 & U21-26 and to become "2" for U5, 6, 19 & 20. It also causes DDEN to transmit data (interrupt vector as defined on the interrupt vector jumper plug). Once SSYN is received U82-9 is reset which removes "INTR" and disables data bus drivers. This locks up the circuitry until IRQ becomes "0", after which the cycle can be repeated if IRQ becomes true ("1").

PAGE 2

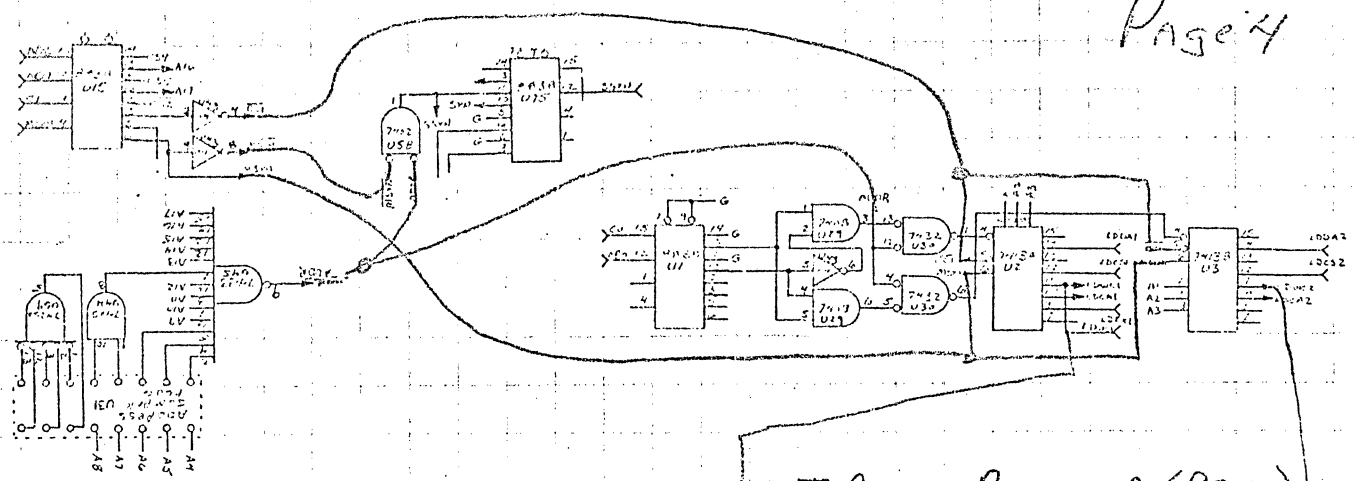


DATA out Mode - DATA OUT mode uses The Same UNIBUS SIGNALS AS DATA IN. The Difference IS That C0 And C1 ARe Different, i.e, C1 IS ASSERTed And C0 DeTERMINES if DATA OUT iSA BYTE oR word TRANSfeR, i.C. C0 ASSERTed iS BYTE TRANSfeR, C0 UNASSeRTed is word TRANSfeR. ADDRess BIT 0 DeTERMINES UPPeR oR Lower BYTE if C0 iS ASSERTed - A0 ASSeRTed TRANSfeRS D8-15, A0 UNASSeRTe TRANSfeRS D0-D7. A SIMPlified SCHeMATIC AND TIMING DIAGRAM iS SHOWN Below FOR WORD TRANSfeRS.

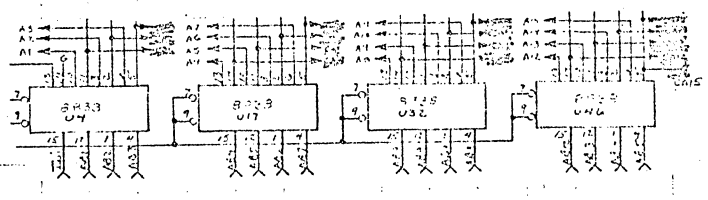


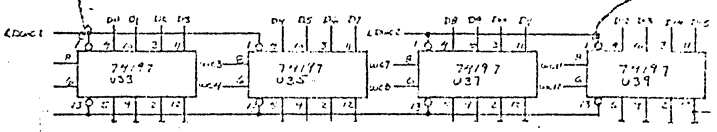


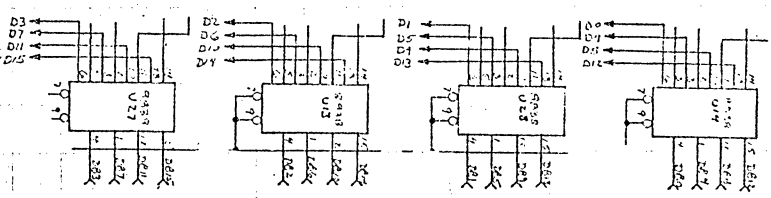
ACTUAL IMPLEMENTATION iS AS follows (Ref SCHEMATIC PAGe 4): AddRESSING IS ACCOMPLISHED The SAME AS DATA IN (U4,17,32,46 with U45,44,69 PROVIDING C1 iS ASSeRTed ENABLING U2 AND U3 AND DISABLING U44 (4,5->6). If C0 iS ASSeRTed, U2 oR U3 ARe SeLected By A0 (A0 ASSeRTed ENABLES U3, A0 UNASSeRTed ENABLES U2). MSYN ASSeRTed COMPLeTES The ENABLING AND U2,3 OUTPUTS GO LOW SETTING The APPROPRIATE REGISTER SELECTED BY A1,2,3. MSYN REMOVED COMPLeTES The TRANSfeR.



TYPICAL REGISTER (RCXX)







DMA (DIRECT MEMORY ACCESS) Mode IS THE NORMAL FUNCTIONAL MODE AND WILL BE DISCUSSED IN THE following FORMAT: 1. COMMON CIRCUITRY 2. SPECIFIC REGISTER FUNCTIONS 3. READ MODE 4. WRITE MODE 5. WRITE CHECK MODE 6. ERROR GENERATION

1. COMMON CIRCUITRY — THE CIRCUITRY COMMON TO ALL DMA FUNCTIONS IS: 1. RCLA REGISTER — U29+30 (BOI) WITH JUMPER PLUG U28 — U29+30 ARE RESET WITH THE ORIGIN MARK FROM THE DISC AND INCREMENTED WITH THE SECTOR MARK. THE U28 JUMPER PLUG IS USED TO DETERMINE THE INTERLACE FACTOR. EXACT WIRING OF THE JUMPER PLUG IS DEFINED IN THE INSTALLATION SECTION. U26+27 ARE COMPARATORS (7485) AND CONNECTED TO RCLA REGISTER VIA THE JUMPER PLUG AND THE RCDA REGISTER TO GENERATE "SCMP" WHEN RCLA = RCDA IF NO ERRORS HAVE OCCURED. SCMP IS A SIGNAL THAT IS TRUE DURING THE SECTOR SELECTED BY RCDA. RCLA BITS 0-7 ARE ALSO CONNECTED TO THE DATA BUS MULTIPLEXER.
2. RCDA REGISTER — U6, 7, 8, +9 (BOI) — THE RCDA REGISTER IS USED TO DETERMINE THE DISC ADDRESS OF A TRANSACTION. RCDA 0 — RCDA 7 ARE CONNECTED TO THE COMPARATORS U26, 27 TO DETERMINE THE SECTOR ADDRESS AND RCDA 8 — RCDA ARE USED TO DETERMINE THE TRACK ADDRESS (LOWER 5 BITS; TA 0-4). RCDA 8 — RCDA 12 ARE CONNECTED TO BUS DRIVERS TO CONTROL TAA 0-4 RESPECTIVELY. RCDA IS LOADED BY THE UNIBUS AT THE START OF A TRANSACTION AND INCREMENTED BY THE END OF A DISC COMMAND (READ, WRITE) "DCMD". RCDA IS CLEARED BY "INIT" WHICH IS A BUS ORIGINATED SIGNAL USED TO INITIALIZE (RESET) PERIPHERAL EQUIPMENTS. RCDA BIT 12 IS USED TO INCREMENT THE RCEX REGISTER. RCDA 0-12 IS ALSO CONNECTED TO THE DATA BUS MULTIPLEXER.
3. RCER REGISTER — THIS REGISTER CONSISTS OF BITS 4, 5, 12, 14, +15 AND ARE USED TO DETERMINE STATUS OF OPERATIONS. THIS REGISTER WILL BE EXPLAINED FURTHER IN READ, WRITE, & WRITE CHECK MODES. THE RCER REGISTER IS AN INTEGRAL PART OF THE CONTROL LOGIC AND IS CLEARED BY THE START OF AN OPERATION.
4. RCCS REGISTER — THE RCCS REGISTER CONSISTS OF BITS 0-8 & 10-15 (NO BIT 9). BITS 0-8 ARE PROGRAM SETTABLE, BITS 10-15 ARE NOT. THIS REGISTER IS AN INTEGRAL PART OF THE CONTROL LOGIC AND WILL BE EXPLAINED FURTHER IN SPECIFIC MODES (READ, WRITE, WRITE CHECK). BITS 4 AND 5 ARE EXTENSION BITS OF THE RCCA REGISTER. RCCA 15 NEGATIVE TRANSITION IS THE CLOCK. BITS 4 & 5 ARE USED TO GENERATE BITS 16 + 17 RESPECTIVELY OF THE ADDRESS BUS DRIVERS.

5. RCWC Register – (U33, 35, 37, 39-B&E) The RCWC Register is used to determine the number of words to be transferred to or from the Disc(s). This Register is cleared by "INIT." and loaded by the UNIBUS. It is incremented by a controller originated UNIBUS transfer (MS). RCWC bit 15 (WC15) is used to set "WCOF" (word count overflow) to indicate end of transfer.

6. RCCA Register – (U34, 36, 38, P40-B&E) The RCCA Register is used to determine the memory address of a data transfer. This Register is cleared by "INIT" and loaded by the UNIBUS. It is incremented by the end of a UNIBUS operation (controller originated). Bit 0 is not implemented allowing only even addressing. RCCA bit 15 (CA15) is used to increment RCCS bits 4 & 5 which make address bits 16 & 17 respectively.

7. RCEX Register – (U5, 24, 23, 25, Jumper Plug U24, Gates U11-1, 4, 10; U33-8, U15-3, & U2) (outputs)
This Register is an extension of the Disc Address Register (RCDA) RCEX bits 0, 1, & 2 are used to generate bits 5, 6 & 7 respectively of the Disc Track Address Bus. EX3 & 4 are used to generate SEL0-3 of the Disc Select Bus. U23, Jumper U24, & U25 are used to determine the number of tracks per disc for each of up to 4 discs in 32 track increments. Gates U11-10, U2-6, & U33-8 are used to clear EX0-2 when changing the Disc Select Bus. If the Disc Select increments past 3, ER5 is generated to stop any further transfers. This Register is cleared by "INIT" and loaded by the UNIBUS. It is incremented by RCDA bit 12.

8. DMA and Bus Interface Circuitry

1. Bus Interface circuitry composes of 3 parts: Data Bus Interface (U13, 14, 27) Address Bus Interface (U4, 17, 32 & 46), and Control Interface (U1, 15 & 25)

The Data Bus Interface translates data in to form DO-D15 and data out as selected by the Data Multiplexer circuitry (U5-12, U19-26). Data out is gated with "DDEN" which is generated in Slave mode by (U44-6), in Interrupt mode by IS3 (U29-8), and in DMA mode by NP3 (U57-8)

The Address Bus Interface translates address in to form A0-A17 which is decoded (U31, 44-8, 45, & 69) to generate "ADDR". This is used in Slave mode only. Address out (RCCA) is gated by NP3. (NP3 will be explained later).

The Control Interface is used to interface control signals (C0, C1, MSYN, SSYN, BUSY, NPR, NPG, BR&BG) to the UNIBUS. The function of these signals will be explained thru out the text.

2. DMA Mode utilized the Bus Interface Circuitry to transfer data to or from the UNIBUS. This is accomplished by acquiring Bus Mastership and then initiating the data transfer. Bus Mastership is acquired by first setting NPR (Non-Processor Request) (U70-8) which in turn asserts NPR on UNIBUS.

The Unibus Replies with NPG (GRANT) (U75-4). This is inverted (U76-8) and Clocks the flop (U84-9) setting it to a "1" which in turn generates NPR (U83-11) which inhibits NPG out (U55-4). This condition prevails until BSY and SSYN are removed. This action clocks the flop PR (U84-5) which releases NPG out and asserts BBSY (U71-3, U75-15). Bus Mastership is now obtained. NP3 (Control Bus) is used to gate address and C1 to the Unibus. It also starts the Master/Slave transfer - This will be discussed later. Data to or from the Unibus is determined by RCCS bit 2 (1=To, 0=From). If RCCS 2 is "1" then DDEN is enabled and the Data Multiplexer is forced to "7" (U57-6, U29-8, U57-3, U16-3, U76-10, U16-8, U58-13, U16-11) This places Buffer Data on the Bus. To receive Data From Bus, Shift Register (U49,50) is enabled by "RD" and clocked by "SRC" which is generated by the Master/Slave transfer circuitry.

The Master/Slave transfer circuitry uses NPR flop (B11-U53-9) and a series of timers (U71-3, 6, 8, 11; U72-2, 4, 6, 12). NP3 places address & control on the Unibus (Data also if transf is to the Bus). The first delay is caused by [U73-3, U72-2] which is 640 ns in duration. When this occurs, MSYN is asserted to the Unibus and Timer [U71-6, U72-4] is enabled. This timer is ~20 us and if it occurs (SNEM), this is interpreted as no response from the Unibus (Non-Existent Memory) and terminates the transaction (SDONE). If SSYN is received from the Unibus, Timer [U71-11, U72-12] is enabled and occurs 640 ns later. This removes MSYN from the Unibus and enables Timer [U71-8, U72-6] which when timed out (SDONE) resets NPR, terminating the transaction. SRC is derived from MSYN and SSYN to clock the Buffer Input Register (U48, 50, 52, 54) for data in transactions.

9. Memory (U61-68) The memory is organized in 16 x 32 bit structure. The input is [U48, 50, 52, 54] which can be in serial or parallel form. The memory outputs to latches (U47, 49, 51, 53) and to shift register (U77, 80). Memory control originates on the control board and will be discussed in Read, Write & Write Check modes of operation.

10. Disc Bus Interface Circuitry - The Disc Bus differs from the Unibus in that all signals are not uni directional. Gates (U10-3, 6, 8, 11, U1-3, 6, 11, U4-6, 8, 11, & U18-8) are used to select track and disc. Disc outputs are buffered by (U20-3, 5, 1, U28-3, 5, U32-3, 11), (U18-3, 6, 11, U4-3) provide the rest of the disc inputs. These signals are all terminated on the control board. All outputs to disc are disabled when the controller is in an idle state.

11. Disc Counter (U43, 44, 45) The Disc Counter is used to keep track of data coming from or going to the disc. "LDC" starts the counter at the "Sector" (selected) and the count steps when the appropriate (S28) number of bits are detected (To/From). Gate (U60-9, U7-4) accomplish this. CS 3 (ABORT) forces the Disc Counter to "0" stopping all disc transactions.

12 DMA COUNTER (U50,52) THE DMA COUNTER IS USED TO KEEP TRACK OF DATA TO & FROM THE UNIBUS. IT IS ENABLED WITH "DMAR" & "DMAW" AND STOPS AT "0" (116) CSR (ABORT) FORCES THE DMA COUNTER TO "0".

13. SECTOR COMPARATOR (U26,27). THE SECTOR COMPARATOR PROVIDES SIGNAL "SCMP" WHEN THE SELECTED SECTOR (CONTENTS OF THE RCDA REGISTER) COMPARES WITH THE ACTUAL SECTOR (CONTENTS OF THE RCLA REGISTER) PROVIDING NO ERROR CONDITIONS EXISTS. "SCMP" IS USED TO INITIATE DISC TRANSACTIONS.

Read, write, write check: These modes utilize common circuitry as explained previously. In order to enter these modes the registers RCCA, RCDA, RCEX, and RCWC must be loaded with appropriate information. Once this is done RCCS is loaded with the proper command (Read, write, write check), which clears the RCER register and RCCS bits 10–15 and initiates the desired function.

The function initiation is controlled by the sequence counter (U41, 43, 44) which uses "SCMP" and various states of the data counter (U57, 59) and disc counter (U45, 44, 45). RCCS bits [illegible] determine the function to be performed.

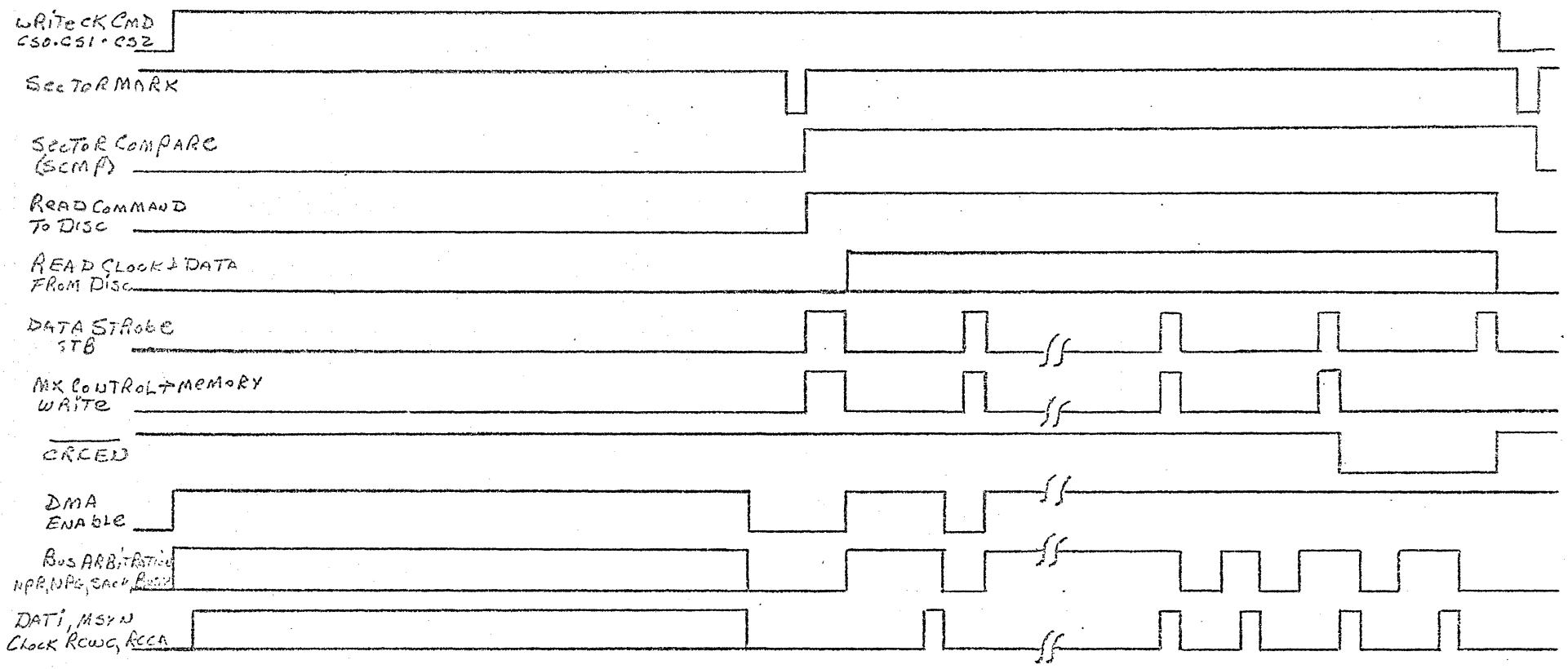
The following explanations assume that RCCA, RCDA, RCEX, and RCWC are properly loaded, no error conditions exist, and the RCCS loading begins the explanation.

1. Write – When the RCCS register is loaded the sequence count [illegible] (one [illegible]), this causes count "0" to jump to "1". In state "1" [illegible] (U[illegible]) is enabled, setting the data counter to 000001 (bits [illegible]), [illegible] gate (U33-3) which in turn enables (U36-6) causing NPR, which causes a data transfer from the Unibus. This transfer process is one word at a time. Transfer continues with N6 going low (32 words). N7 goes hi (1) when N6 goes low which allows the sequence counter to [illegible] "2" (U39) at count "2". The sequence counter waits for SCMP. When SCMP occurs the sequence counter generates "LC" which sets the disc counter to [illegible] which in turn enables "ENA" (U60-9). ENA stays "1" until [illegible] clears [illegible] decodes of the disc counter generate "write" [illegible] (U[illegible]). Data to the disc is generated in the following manner: The [illegible] lines are controlled thru (U42, 55) and (U12-6). During ST0 (T5) the memory is addressed by the disc counter, data is parallel loaded during ST0 time [illegible] and clocked by "CLK" which in write mode is "[illegible]" from the disc. The shift register (U77, 86, [illegible]) is gated with CRC to the disc. The disc counter generates "CRC EN" which shifts out to the disc serially at the end of 32 words transferred.

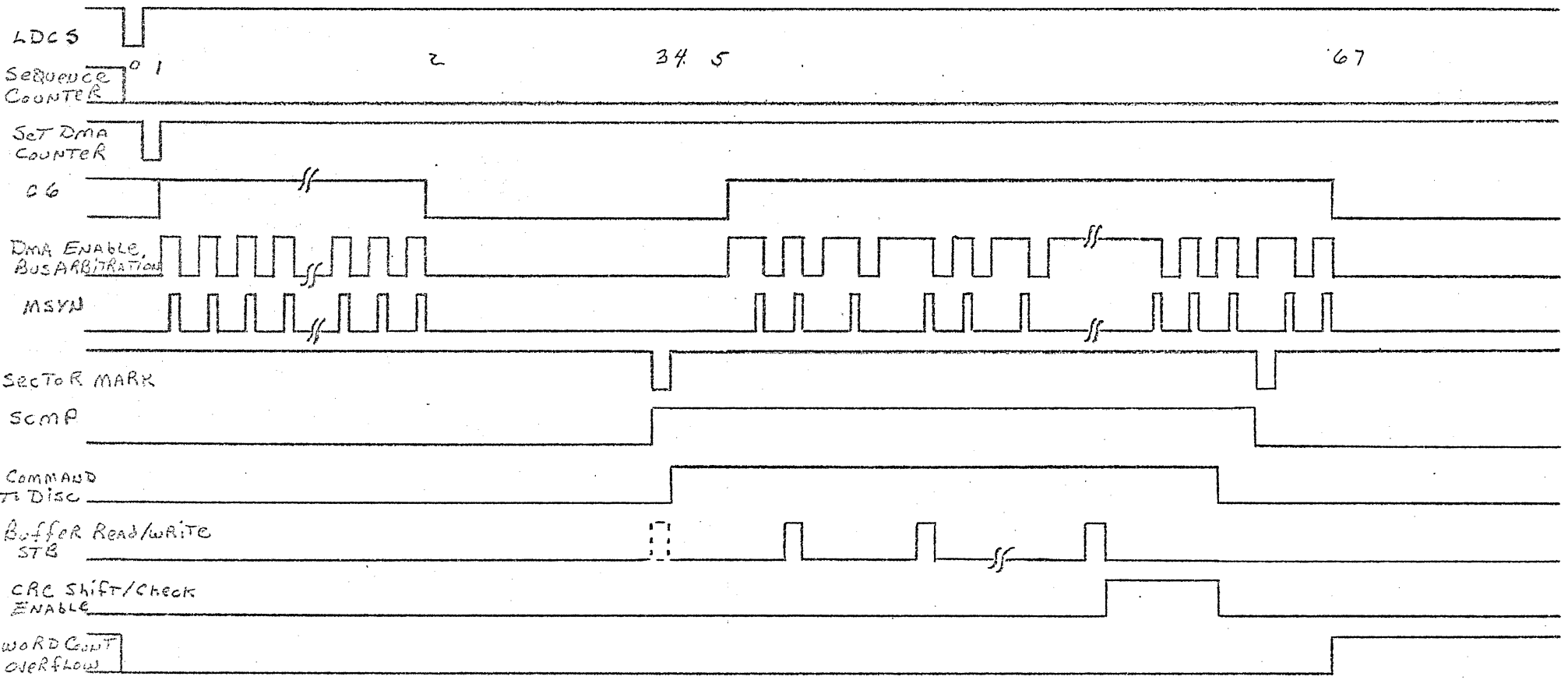
Once a word has been transferred to the disc (01000 H1), the sequence counter loads "SMB" to the data counter (00000100) which allows the [illegible] (U41, U51) to control the data request (NPR). This permits continuous filling of the memory after a word has been written. This process stops after word count overflow (WCOF) becomes true indicating end of transfer. [illegible] flop (U50-9) is used to reset RCCS ∅ at the end of the sector that word count overflow occurred (last sector). Note that if partial sector data is in the buffer, the entire sector will be written. The filling data will be the previous sector data.

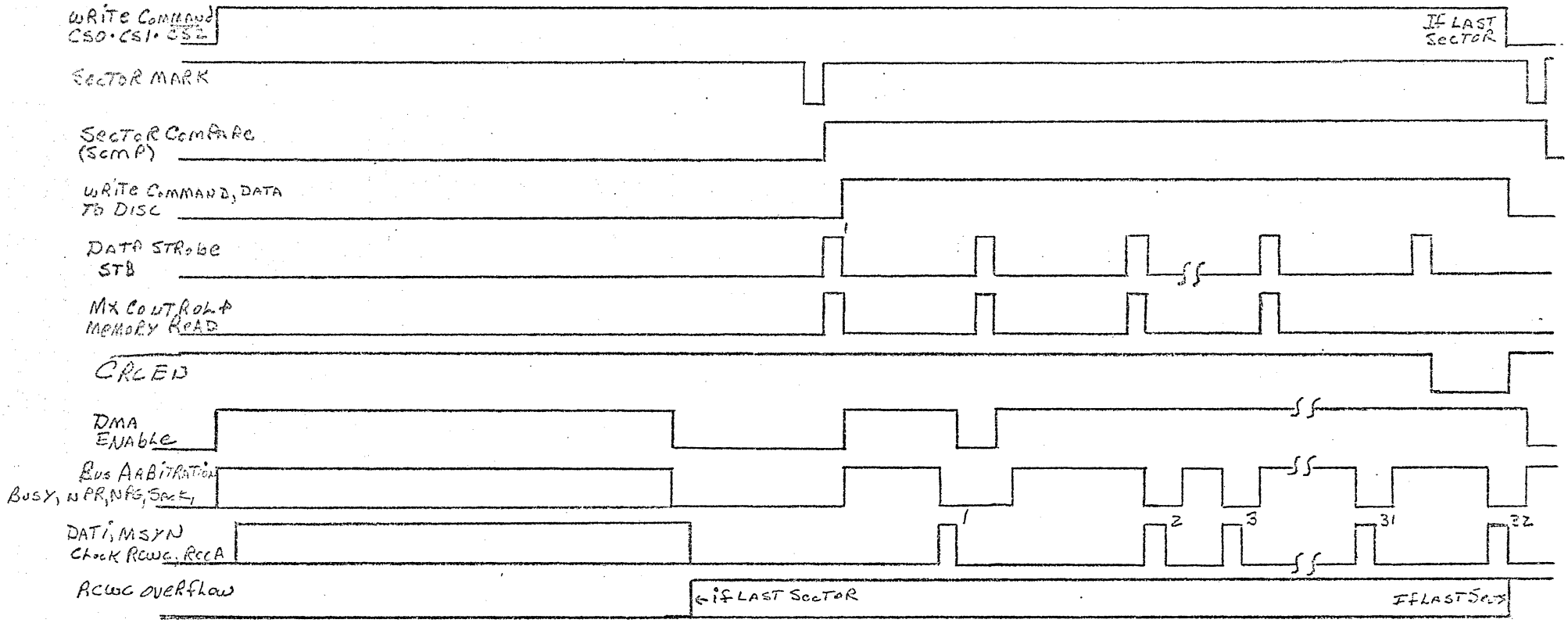
2. READ: The Sequence Counter is Reset By LDCS1 which increments to 2 (CSIF 1) and waits for "SCMP." once "SCMP" is Received "LDC" is Generated which Sets The Disc Counter to 111111100 which Enables "ENA" And Also Enables "RD" which Generates "Read Command" To The Disc And Selects The Read Clock for "CLK" (04?), when The Read Clock is Received from The Disc, The Shift Register (04?, 50, 52, 54 [illegible]) (Also Enabled for [illegible] mode By "RD") Shifts in DATA from The Disc. The Disc Counter increments And The Sequence Counter Generates "SMB" which allows The [illegible] Transfer To occur, This Continues until 32 (16 BIT) words Are Received. Then "CKCE" is Generated And The Read input Data Are [illegible] (U13-11). CRC is Checked By (U3-4-5) And The falling Edge of "ENA" clears The [illegible] Register. This [illegible] [illegible] [illegible] [illegible] Terminated is The same As [illegible].

3. WRITE Check: Sequence Counter Reset, "SMA" Generated By [illegible] [illegible] NT occurs. Sequence Counter waits for "SCMP," SCMP Generates LDC which Generates "RD" And waits for "Read clock". DATA is Loaded from Memory as in write mode And is Compared (U?-?) with incoming Data (U56-9). Process Continues until WCOF which Resets CSO (Same As write).

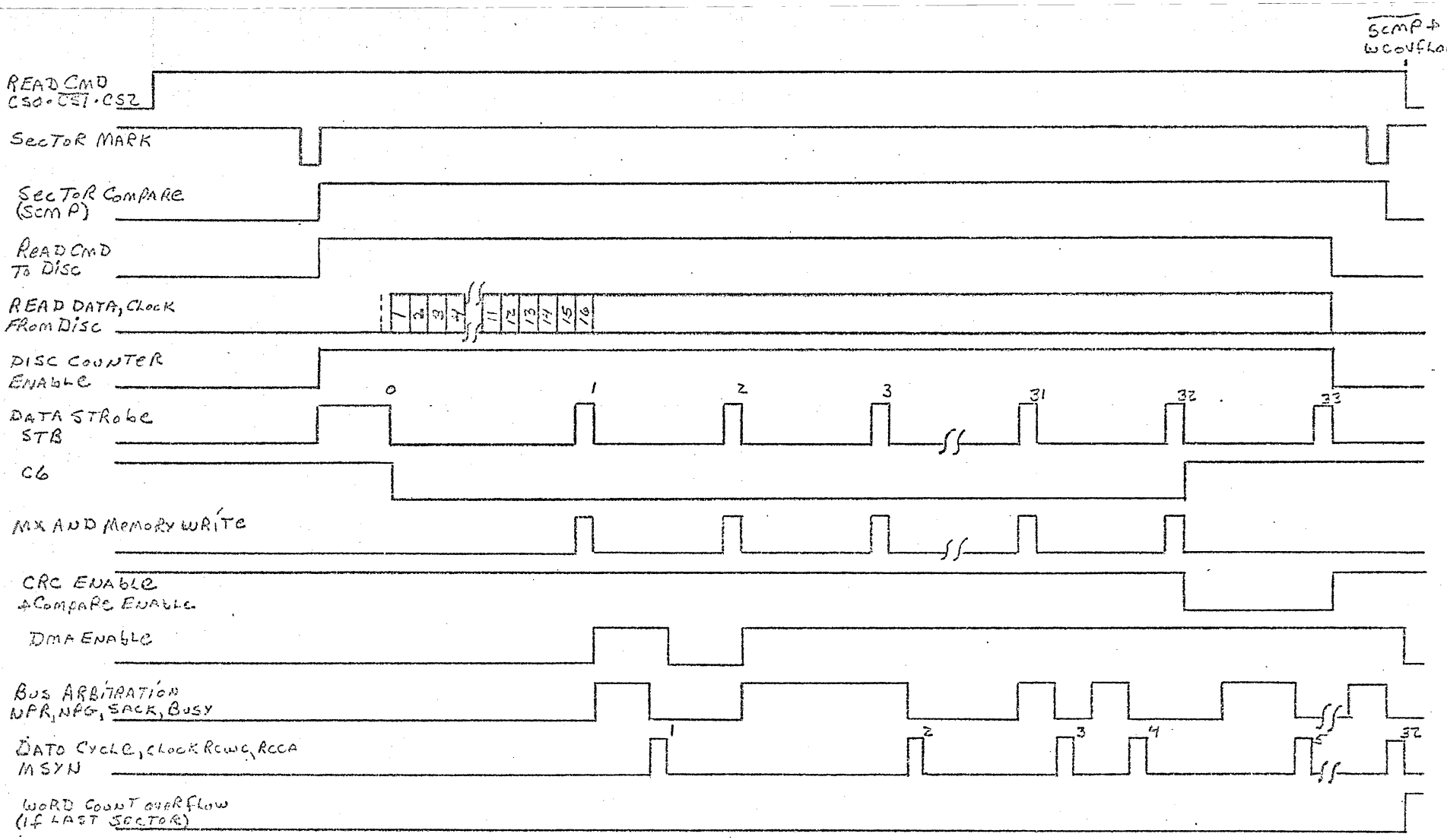


WRITE CHECK MODE TIMING

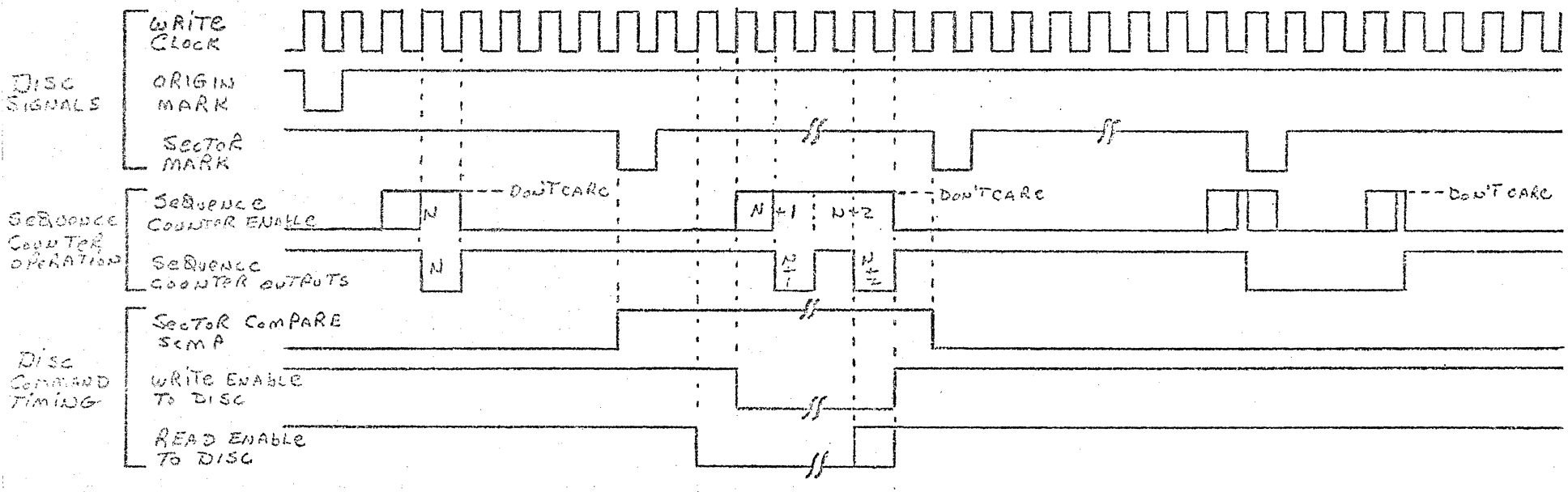

LDCS
SEQUENCE COUNTER
0 1
2
3 4 5
6 7
SET DMA COUNTER
C6
DMA ENABLE, BUS ARBITRATION
MSYN
SECTOR MARK
SCMP
COMMAND TO DISC
BUFFER READ/WRITE STB
CRC SHIFT/CHECK ENABLE
WORD COUNT OVERFLOW

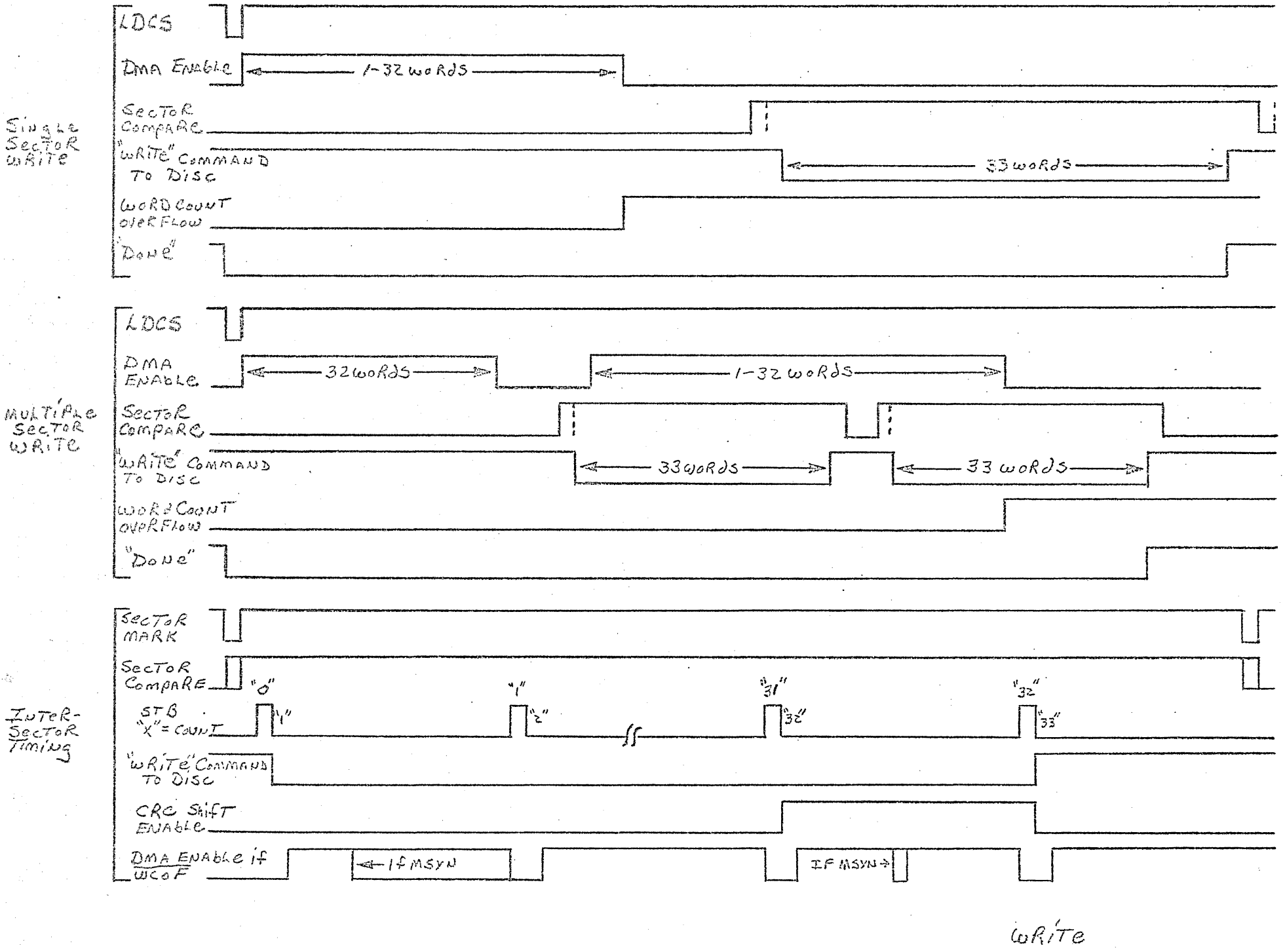


WRITE MODE TIMING

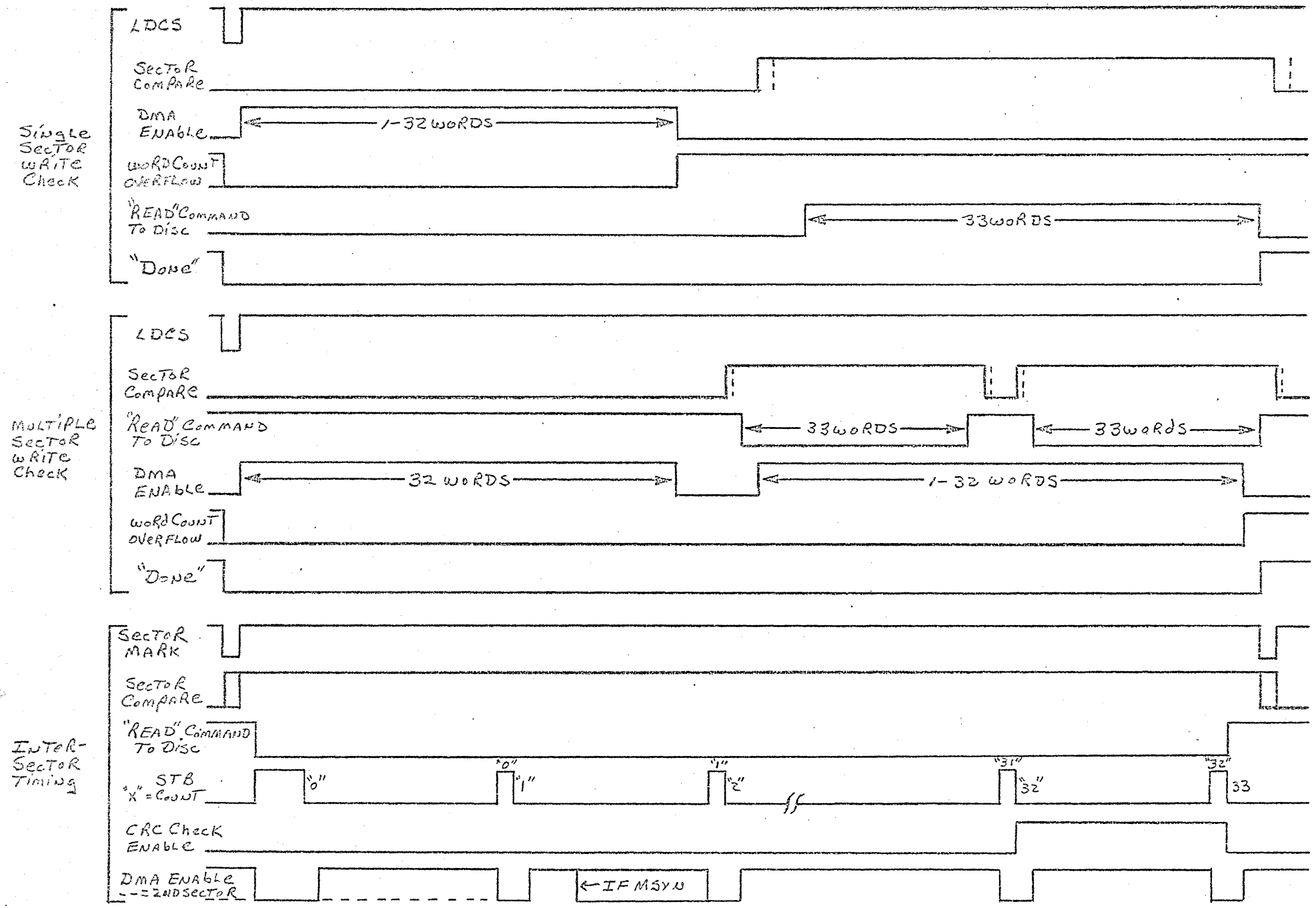


READ MODE Timing

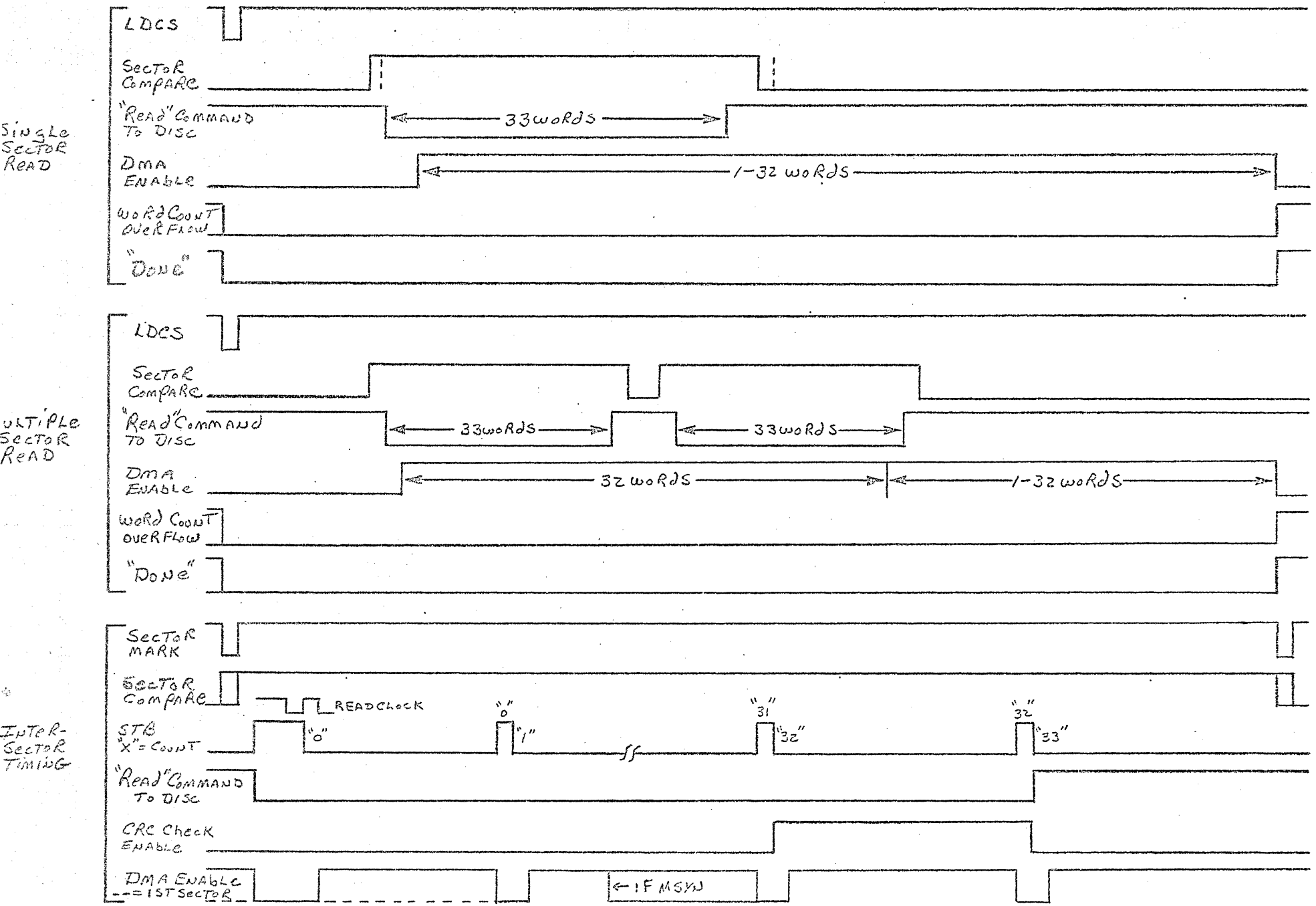

DISC SIGNALS
WRITE CLOCK
ORIGIN MARK
SECTOR MARK
SEQUENCE COUNTER OPERATION
SEQUENCE COUNTER ENABLE
SEQUENCE COUNTER OUTPUTS
DON'T CARE
N
N+1
N+2
DISC COMMAND TIMING
SECTOR COMPARE SCMP
WRITE ENABLE TO DISC
READ ENABLE TO DISC


Single Sector Write
LDCS
DMA Enable
1-32 words
Sector Compare
"Write" Command To Disc
33 words
Word Count Overflow
"Done"
Multiple Sector Write
LDCS
DMA Enable
32 words
1-32 words
Sector Compare
"Write" Command To Disc
33 words
33 words
Word Count Overflow
"Done"
Inter-Sector Timing
Sector Mark
Sector Compare
"0"
"1"
"31"
"32"
STB "X" = Count
"1"
"2"
"32"
"33"
"Write" Command To Disc
CRC Shift Enable
DMA Enable if WCOF
If MSYN
If MSYN

Write


Single Sector Write Check
LDCS
Sector Compare
DMA Enable
1-32 words
Word Count Overflow
"Read" Command To Disc
33 words
"Done"
Multiple Sector Write Check
LDCS
Sector Compare
"Read" Command To Disc
33 words
33 words
DMA Enable
32 words
1-32 words
Word Count Overflow
"Done"
Inter-Sector Timing
Sector Mark
Sector Compare
"Read" Command To Disc
STB
"X" = Count
"0"
"0"
"1"
"1"
"2"
"31"
"32"
"32"
33
CRC Check Enable
DMA Enable
--- = 2nd Sector
← IF MSYN

Write Check


Single Sector Read
LDCS
Sector Compare
"Read" Command To Disc
33 words
DMA Enable
1-32 words
Word Count Overflow
"Done"
Multiple Sector Read
LDCS
Sector Compare
"Read" Command To Disc
33 words
33 words
DMA Enable
32 words
1-32 words
Word Count Overflow
"Done"
Inter-Sector Timing
Sector Mark
Sector Compare
READ Clock
STB "X" = Count
"0"
"0"
"1"
"31"
"32"
"32"
"33"
"Read" Command To Disc
CRC Check Enable
DMA Enable --- 1ST Sector
← 1F MSN

Read