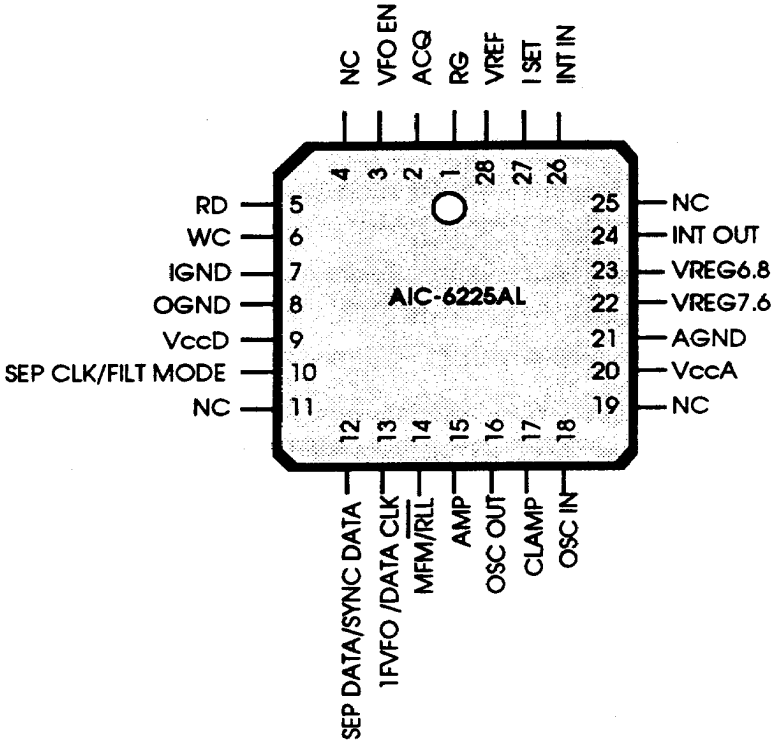
adaptec

AIC-6225A

High-Performance Monolithic Data Separator

PRELIMINARY



QUAD PLCC PACKAGE

- **Advanced Shottky Bipolar Process**
- **Operates At Data Rates Up To 33 Mbits/Sec**
- **Voltage And Temperature Compensated With 100% Tested Margins**
- **Supports Constant Density Recording (CDR)**
- **Winchester, Optical and LAN applications**
- **All Adjustments Eliminated**
- **Precision, High-Q LC Oscillator With External Tank**
- **Ultra Stable VFO "COAST" Capability**
- **Zero-Phase Error Startup Of VFO**
- **Precision, Dual-Gain Charge Pump**
- **User-Defined PLL Performance**
- **Dual-Mode Phase Detector**
- **Filter Mode Pin Available To Change Pole/Zero Location**

OVERVIEW

Function

The AIC-6225A is a complete, monolithic data separator which is unique in bringing both precision and stability to the data separator function. Speeds of 25 Mbits/sec for 2,7 RLL (33 Mbits/sec for 1,7 RLL) are achieved with a window loss guaranteed not to exceed one nanosecond. The AIC-6225A implements a dual-mode phase detector which uses a true, full-frequency, frequency detector to prevent harmonic lock, and a dual-gain charge pump (with high gain for rapid acquisition and low gain for minimum jitter) while tracking data.

Precision

The LC oscillator can be clamped to make possible a zero-phase error startup for consistent and optimum Phase-Locked Loop (PLL) acquisition. The AIC-6225A provides a data synchronizer (data standardizer), and it outputs data clock and synchronized data. If the MFM mode is selected, it outputs NRZ data. To gain increased noise immunity, the device operates from a five-volt supply for the logic and TTL interface, and a 10-volt to 12-volt supply for the analog.

Flexibility

The AIC-6225A is easily designed into any application. This is due to the minimal and versatile TTL interface, and because the user has complete control of every aspect of PLL performance by specification of a minimum number of external components. Designs are stable because every AIC-6225A is shipped with tight tolerances on parameters affecting PLL performance, all of which enable high data rate applications to move swiftly and smoothly from design to production without adjustment and rework.

The oscillator driver has been carefully designed to work with a wide range of external LC components to form a very high-Q, low-phase noise oscillator. While stable frequency generation and low noise (jitter) are very important at lower data rates, they become critical at higher data rates.

All oscillator and filter components are external to the device to provide the designer with the greatest possible degree of flexibility in specifying and controlling the system's performance of the device. For example, by proper selection of external components, the oscillator center frequency may be set from well under one MHz to in excess of 100 MHz; substantially beyond the typical range of application of the device.

Additionally, the oscillator dynamic range may be set from a few percent of center frequency (low VCO gain) to a large percentage of center frequency (high VCO gain), all by proper selection of external oscillator components.

The filter may be varied from a simple lead-lag, which accommodates the gain change (or defeats the gain change, as desired) to a more complex filter, which uses the FILT MODE output to change the pole-zero location by use of the FILT MODE output during the gain change. Accordingly, the overall PLL loop gain and the pole-zero locations may be varied across a wide range.

The AIC-6225A (together with a passive, external filter network and a varactor-tuned LC oscillator network) provides a complete, flexible, high-performance data separator function. All external adjustments and delay lines have been eliminated.

The demanding requirements of the highest-performance rigid disk drives have been accounted for in the circuit design of the AIC-6225A. This allows the AIC-6225A to be used with all disk drives, and it may be located in either the drive (as in SCSI, ESDI, SMD, etc.) or in the controller (ST506).

Package

The AIC-6225A is available in a 28-pin PLCC package. The size of the package and total area required for the hardware for data separation are minimal and, thus, the AIC-6225A is very suitable for all controller designs, including embedded. Figure 1 illustrates a typical embedded target SCSI controller design with Adaptec components. The embedded controller design can be accomplished in about four square inches. Adaptec provides similar solutions for other controller designs with its family of high-performance components.

Test Frequencies and CDR Applications

The Device Test Frequencies (DTF) are: 15, 20, 30, and 50 MHz. These correspond to the speed designator -XX (e.g., AIC-6225A-XX). *For multiple frequency applications (Constant Density Recording-CDR, or Zoned Data Recording-ZDR), the performance of the device is guaranteed over the range 0.5*DTF to 1.1*DTF.* Consult Adaptec for other ranges.

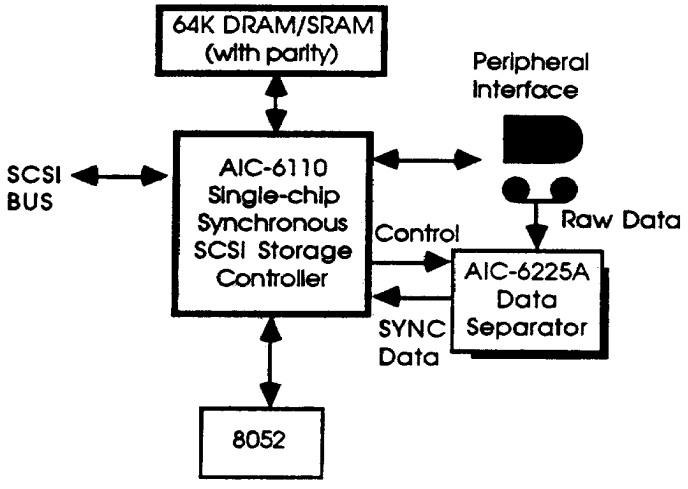


FIGURE 1. EMBEDDED SCSI CONTROLLER

PIN DESCRIPTION

SYMBOL	DIP	PLCC	TYPE	NAME AND FUNCTION
RG	1	1	IN	READ GATE: Controls the phase or frequency mode of AIC-6225A phase detectors. RG may be tied to VFO EN input when VFO EN is used in the level mode. RG should preferably be set at, or prior to, a change in VFO EN. **Logic 1** allows the phase detector to run in the phase mode (data read) or to progress sequentially from the frequency mode to the phase mode. **Logic 0** forces the phase detector to run in the frequency mode.
ACQ	2	2	IN	ACQUIRE: Enables the high gain state of the charge pump for fast PLL acquisition. **Logic 1** allows the charge pump to switch to high gain with a change in VFO EN and to synchronously switch to low gain after approximately 37 pulses at the selected input; i.e., either RD or WC. If the charge pump is in high gain, switching to logic 0 immediately terminates the internal pulse count and causes the charge pump to synchronously switch to low gain. Tying ACQ to RG provides a means for enabling high gain acquisition in the phase mode only. **Logic 0** forces a single or low gain charge pump.
VFO EN	3	3	IN	VFO ENABLE: Used to select input data from RD or WC. The transition from 1 to 0, or 0 to 1, initiates the oscillator clamp, zero-phase error startup sequence, as well as the charge pump gain change sequence (if allowed, via the ACQ input). A positive or negative pulse of width 1 to 3 oscillator periods may be used as the VFO EN input. In this mode, the RD and WC inputs must be tied together with a data selector now external to the AIC-6225A. **Logic 1** selects the RD input. **Logic 0** selects the WC input.
RD	4	5	IN	READ DATA: This is raw encoded data from the disk drive read channel. The AIC-6225A is responsive to the rising edge of the RD input when VFO EN is in the logic 1 state.
WC	5	6	IN	WRITE CLOCK: This is a 50% duty-cycle input which is at the frequency of the oscillator used to write data onto the disk drive or, alternately, an oscillator at the appropriate frequency generated from a clock track on the disk drive. This input is used to allow the AIC-6225A PLL to track the nominal data frequency when RD is not available. The AIC-6225A is responsive to the falling edge of the WC input when VFO EN is in the logic 0 state.
IGND	6	7	GND	INPUT DIGITAL GROUND (common external ground): The two ground pins, IGND and OGND, are to be tied together by the shortest possible lead. Refer to layout suggestions in Appendix 2 for connection to the analog ground, AGND.
OGND	7	8	GND	OUTPUT DIGITAL GROUND (common external ground): See IGND pin, above.
VccD	8	9	PWR	DIGITAL SUPPLY: +5V, ±5%.

SYMBOL	DIP	PLCC	TYPE	NAME AND FUNCTION
SEP CLK/ FILT MODE	9	10	OUT	SEPARATED CLOCK: When MFM/$\overline{RLL}$ pin is in the logic 1 state, the SEP CLK output is made available. This is the decoded clock output from the MFM data stream. FILTER MODE: When MFM/$\overline{RLL}$ pin is in the logic 0 state, the FILT MODE output is made available. The FILT MODE output is logic 1 when the phase detector is in the phase mode and the charge pump is in low gain. Otherwise, it is logic 0. The FILT MODE output may be used to modify the PLL filter when switching from high to low gain at the transition from acquisition to tracking (data read) mode.
SEP DATA/ SYNC DATA	10	12	OUT	SEPARATED DATA: When MFM/$\overline{RLL}$ pin is in the logic 1 state, the SEP DATA output is made available. This is the decoded data (NRZ) from the MFM data stream. SYNCHRONIZED DATA: When MFM/$\overline{RLL}$ pin is in the logic 0 state, the SYNC DATA output is made available. This is the synchronized (standardized) data output and may be supplied to an external RLL or MFM decoder, as appropriate.
1FVFO/ DATA CLK	11	13	OUT	1FVFO: When MFM/$\overline{RLL}$ pin is in the logic 1 state, the 1FVFO output is made available. This output is half the frequency of the VFO and the rising edge clocks SEP DATA, while the falling edge clocks SEP CLK. DATA CLOCK: When MFM/$\overline{RLL}$ pin is in the logic 0 state, DATA CLK is made available. The rising edge of this output clocks SYNC DATA.
MFM/$\overline{RLL}$	12	14	IN	MFM/$\overline{RLL}$ Select: A control input to select, in parallel, one of two possible outputs from each of the three output pins: SEP CLK/FILT MODE, SEP DATA/SYNC DATA, and 1FVFO/DATA CLK. Logic 1 selects the MFM outputs of SEP CLK, SEP DATA, and 1FVFO. Logic 0 selects the RLL outputs of FILT MODE, SYNC DATA, and DATA CLK.
AMP	13	15	ANA	OSCILLATOR AMPLITUDE: Analog pin. Oscillator AGC rate capacitor.
OSC OUT	14	16	ANA	OSCILLATOR OUT: Analog pin. Oscillator current drive.
CLAMP	15	17	ANA	OSCILLATOR CLAMP: Analog pin. Oscillator clamp voltage source.
OSC IN	16	18	ANA	OSCILLATOR IN: Analog pin. Oscillator sense input.
VccA	17	20	PWR	ANALOG SUPPLY: +10V (-5%) to +12V (+5%).
AGND	18	21	GND	ANALOG GROUND (common external ground): All three ground pins are to be tied together. AGND is to be located in an analog ground plane. Refer to Appendix 2 for layout suggestions for connection to digital ground, pins IGND and OGND.
VREG7.6	19	22	ANA	VREG 7.6V: Analog pin. Internally regulated supply, brought out for test only. Attention: No connection is to be made to this pin.

SYMBOL	DIP	PLCC	TYPE	NAME AND FUNCTION
VREG6.8	20	23	ANA	VREG 6.8V: Analog pin. Internally regulated supply, brought out for charge pump bias current only. Attention: No other connection is to be made to this pin.
INT OUT	21	24	ANA	INTEGRATOR OUTPUT: Output of buffer amplifier.
INT IN	22	26	ANA	INTEGRATOR INPUT: Inverting input to buffer amplifier.
I SET	23	27	ANA	CURRENT SET: Charge pump bias current set by external 1%, 100 PPM resistor.
VREF	24	28	ANA	VOLTAGE REFERENCE: Analog pin. Internally generated reference for integrator, brought out for storage capacitor only.

Appendix 1 illustrates possible hardware designs for the AIC-6225A. Figure A1-1 illustrates the AIC-6225A integrated with the AIC-2702,7 RLL ENDEC and the AIC-010 Programmable storage Controller. Figure A1-2 illustrates the AIC-6225A configured with the AIC-6110 Single Chip Synchronous SCSI Controller.

FUNCTIONAL DESCRIPTION

The basic function of the AIC-6225A is to extract the clock (DATA CLK) from a serial, phase-encoded bitstream (RD), and to use that clock to resynchronize the bitstream (SYNC DATA) and clock it into an external receiver. This is accomplished by the PLL (within the AIC-6225A) locking a VCO (Voltage Controlled Oscillator) to the read data, thereby extracting the clock information. The VCO frequency establishes discrete windows of time within the AIC-6225A. An encoded data bit, which is detected within a particular window, is regenerated so as to be synchronous with the VCO clock pulse generating the window. In so doing, the jitter (which existed in the RD due to bit shift, asymmetry, electrical noise, etc.) is eliminated. SYNC DATA from the AIC-6225A may then be clocked into an external decoder, using the AIC-6225A DATA CLK.

If MFM encoding is used, the synchronized data may be internally decoded by the AIC-6225A MFM decoder, with the resulting NRZ data (SEP DATA) being clocked into an external receiver by the AIC-6225A 1FVFO output. The various functional blocks in the AIC-6225A are outlined as follows.

- Input Selector
- Phase Detector
- Charge Pump
- Buffer Amplifier
- Gain Control
- VCO
- VCO Clamp and Restart Sequencer
- Data Synchronizer
- MFM Decoder
- Output Selector
- Voltage Regulator

Figure 2 illustrates a block diagram showing the above functional blocks in relation to each other.

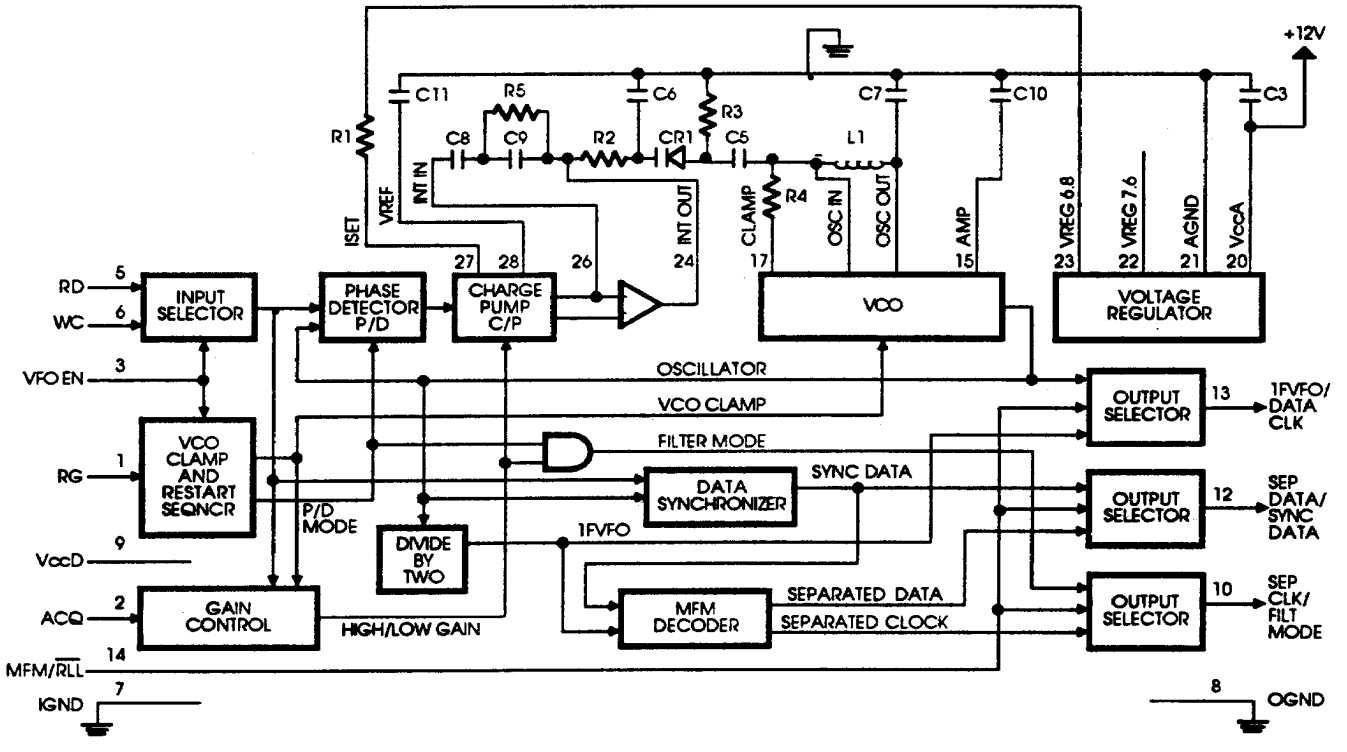


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

INPUT SELECTOR: The input selector selects the WC or RD input to feed the phase detection circuitry of the AIC-6225A. The selection is made based upon the state of VFO EN. When VFO EN is at logic 1, the RD input is selected. When VFO EN is at logic 0, the WC input is selected. The function of the input selector can be bypassed if the designer has external selection circuitry. In this case, the RD and WC inputs must be tied together.

PHASE DETECTOR/PHASE-FREQUENCY DETECTOR: The dual-mode phase detector receives either phase encoded data in the phase mode or a 50% duty-cycle, full-frequency reference clock in the frequency mode. The phase detector controls the charge pump such that the net charge/discharge per cycle is proportional to the phase error between the incoming reference signal and the VFO. In the phase mode, the phase detector provides a window which is set by the oscillator and leads the oscillator by 1/2 period. This establishes a balanced 180 degree phase detection window and eliminates the need for an external delay line.

CHARGE PUMP: The dual gain charge pump sources or sinks current at the INT IN pin, or establishes a high impedance (COAST) condition in the off state.

BUFFER AMPLIFIER: The buffer amplifier is typically connected as an inverting integrator. As an integrator, it acts to sum the charge/discharge currents from the charge pump. When the charge pump is in the hold condition, the INT IN input maintains very high impedance due to the low bias current of the buffer amplifier. The low leakage at the INT IN node prevents phase drift at low frequencies for wideband encoding schemes, or long periods of signal drop out as in the optical application. The passive circuit around the buffer amplifier forms the dominating PLL filter.

GAIN CONTROL: The gain control circuit provides the signal for high gain when the ACQ pin is at logic 1, and a transition occurs on the VFO EN pin. The high gain occurs for about 37 counts of the selected input (RD or WC) and then switches to low gain. The dual gain allows for a quick PLL acquisition in high gain and a stable (low jitter) operation during data tracking.

VCO: The VCO is a varactor-tuned LC-circuit. Selection of the external components sets the center frequency and the range, or VCO gain. The oscillator is a high-Q circuit of low harmonic content, with high noise immunity, all leading to high stability and extremely low jitter.

VCO CLAMP AND RESTART SEQUENCER: The VCO clamp damps the oscillator to DC in approximately one cycle and restarts the oscillator in phase with the incoming reference signal with a full amplitude half cycle. The clamp occurs whenever the VFO EN input changes state and it lasts for three bit periods. At the completion of a data block read, when transitioning from Phase Mode to Frequency Mode, the Zero-Phase Error timing is based on a 50% duty-cycle WC input. Such a signal usually creates a zero-degree start-up phase error, while a 25%/75% duty-cycle signal would create a 90-degree phase error, etc. With the use of a non-50% duty-cycle WC, a larger than normal "bump" will be observed at the VCO control voltage (INT OUT pin), but the time required for phase/frequency lock will not be extended. As this is a noncritical time, performance will not normally be affected.

DATA SYNCHRONIZER: The Data Synchronizer resynchronizes the encoded data to the data clock forming SYNC DATA. For MFM operation, this output serves as the input for the MFM decode logic. For all other encoding schemes, this output must be decoded by an external decoder.

MFM DECODER: The MFM decoder receives the synchronized MFM data from the data synchronizer and decodes it into SEP DATA (NRZ) and SEP CLK.

OUTPUT SELECTOR: The output selector selects either the MFM or the RLL outputs. In the MFM mode, the MFM decoder is enabled. Otherwise, it is disabled and the SYNC DATA and DATA CLK outputs are provided along with the FILT MODE signal. The FILT MODE signal may be used in higher-performance systems to modify the external filter by moving the pole/zero to lower frequencies at the moment the gain is switched from high to low. The purpose is to increase the PLL phase margin at low gain, without compromising the acquisition response at high gain.

VOLTAGE REGULATOR: The internal voltage regulator allows the AIC-6225A to operate over a wide range of analog supply voltages (i.e., 10V/−5% to 12V/+5%) while maintaining the full device specification. This insensitivity to the analog supply voltage provides significant immunity to broadband noise, enabling the robust PLL performance of the device and the low phase noise of the oscillator. The regulator is extremely temperature stable from 0 C to 70 C as a result of the use of an internal bandgap reference. The 6.8V pin supplies bias current to the charge pump via the external 4.99K-1% resistor. Otherwise, the 6.8V and 7.6V pins are brought out for test and should have no other loads or connections.

FUNCTIONAL OPERATION

Figure A1-2 illustrates a possible connection for 2,7 RLL operation using the Adaptec AIC-270. The RG, ACQ, and VFO EN pins are tied together and the AIC-270 provides the selection between RD and WC since these two inputs are tied together. The output relationships between DATA CLK, SYNC DATA, and FILT MODE are shown for an initiation of a block read in Figure 3a, and the completion of a block read in Figure 3b.

Figure A1-1 illustrates a possible connection for MFM operation using the Adaptec AIC-250. The RG initiates and completes the read process. The VFO EN input is a pulse of two or three bit times wide and the AIC-250 provides the selection between RD and WC, as these two inputs are tied together. Finally, the ACQ pin is hard-wired to logic 1 to enable high gain in the charge pump whenever the VFO EN input changes state. The output relationships between 1FVFO, SEP DATA, and SEP CLK are shown for an initiation of a block read in Figure 4a, and the completion of a block read in Figure 4b.

Initiation of a Block Read

(See Figures 3a and 4a.) The sequence of Figure 3a illustrates typical timing of the AIC-6225A configured with the AIC-270. It starts with the AIC-6225A phase and frequency locked to the full frequency, 50% duty cycle signal at the WC input. This signal represents the reference oscillator used for write clock or the reference signal from a clock or servo track on the disk drive. The AIC-6225A is initially in low gain, frequency mode of operation.

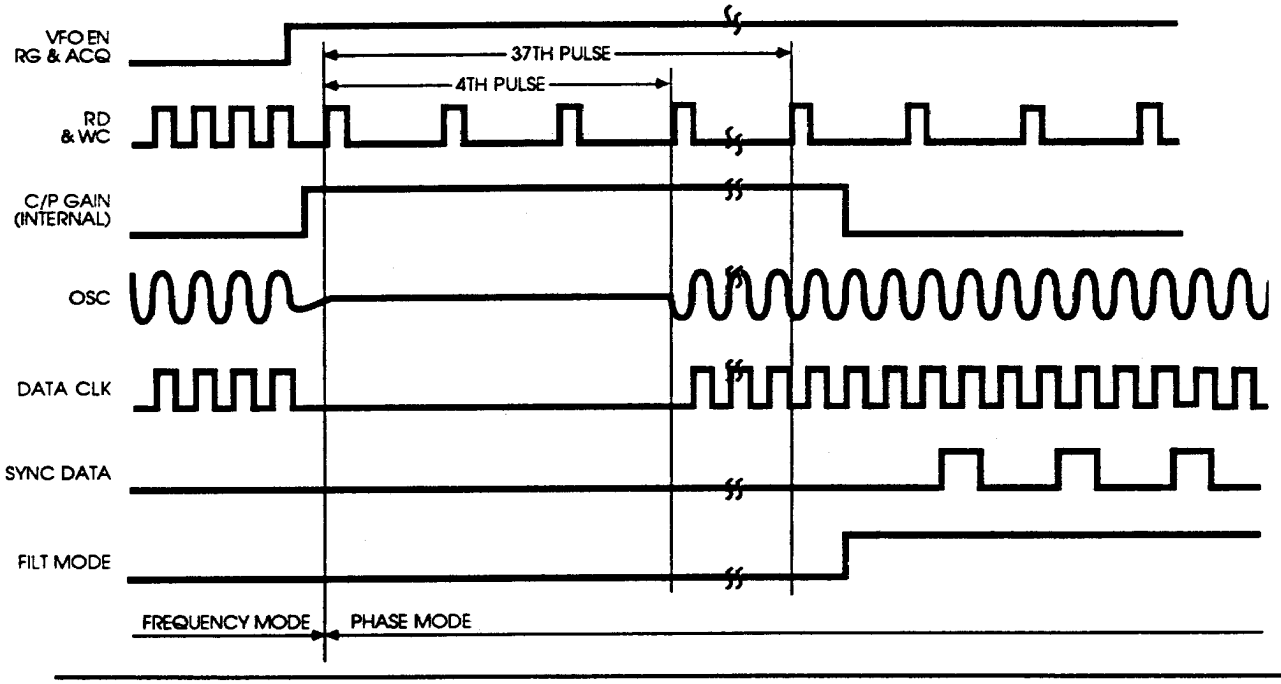


FIGURE 3a. AIC-6225A TIMING DIAGRAM CONFIGURED WITH THE AIC-270 FOR 2,7 RLL: INITIATION OF A BLOCK READ

The block read is initiated when RG, ACQ, and VFO EN go to logic 1. A logic 1 at RG enables the switch to phase mode. A logic 1 at ACQ enables the switch to high gain. A change in the state of VFO EN initiates the clamp sequence and then switches the AIC-6225A to phase mode and to high gain. When the clamp is activated, the external tank circuit goes to DC. The clamp is released on the fourth data bit at which time the external tank restarts with a full amplitude signal in phase with the fourth bit. The PLL is phase locked in the high-gain mode and is making minor adjustments for any residual phase or frequency mismatch. These adjustments may be observed at the INT OUT pin, which is the VFO control voltage. After the 37th bit following the change in VFO EN, the charge pump gain switches to low (acquisition complete), the FILT MODE output goes to logic 1, and the data synchronizer is enabled: the AIC-6225A is ready to read data. It should be noted that the sequence of 37 bits after VFO EN may be truncated by bringing the ACQ input to logic 0, providing for a shorter preamble.

The sequence of Figure 4a illustrates MFM operation, configured with the AIC-250, and is different from Figure 3a in that the RG input occurs early, enabling the switch to phase mode. The switch from frequency to phase mode occurs with the rising edge of VFO EN. VFO EN is now a pulse of two to three data bits times in width. The falling edge of VFO EN retriggers, or restarts, the clamp sequence and gain count of 37 bits. The remainder of the sequence is similar to that of Figure 3a.

The outputs for MFM are the decoded clock output (SEP CLK), decoded NRZ data (SEP DATA), and the 1FVFO signal which is half the frequency of the VFO. Note that the rising edge of 1FVFO clocks SEP DATA and the falling edge clocks SEP CLK.

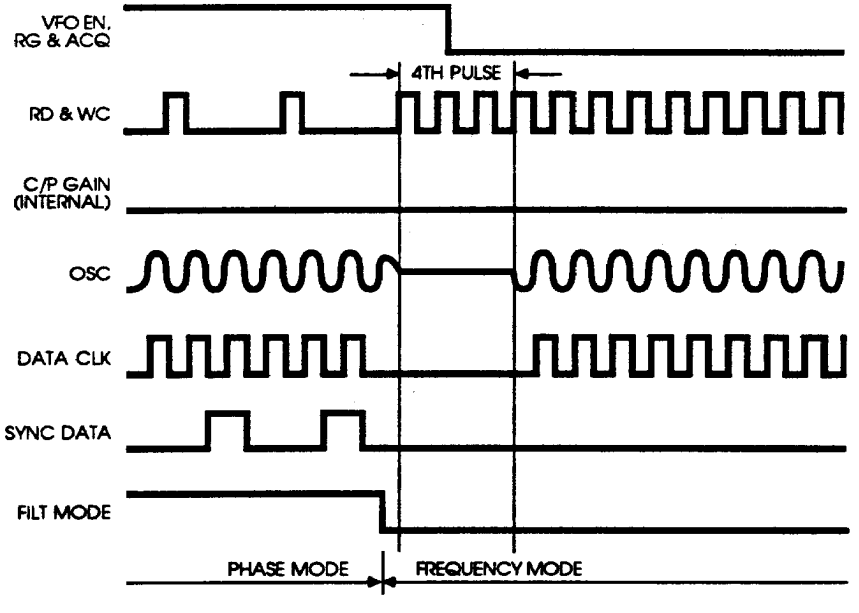


FIGURE 3b. AIC-6225A TIMING DIAGRAM CONFIGURED WITH THE AIC-270 FOR 2,7 RLL: COMPLETION OF A BLOCK READ

Completion of a Block Read

(See Figures 3b and 4b.) The sequence of Figure 3b continues with the timing of the AIC-6225A configured with the AIC-270 and starts with the PLL phase-locked to the data signal at the RD input. At the end of the data block, RG, ACQ, and VFO EN go to logic 0. The phase detector switches to the frequency mode, the charge pump remains in low gain, the clamp is activated, and the FILT MODE output goes to logic 0. With the arrival of the fourth bit, the clamp is released and the oscillator starts in phase with the fourth bit.

The sequence of Figure 4b illustrates MFM operation, configured with the AIC-250, and is different from Figure 3b in that high gain is used in the frequency mode. The switch from phase to frequency mode occurs with the change in state of RG. VFO EN is now a pulse of two to three data bit times in width. The falling edge of VFO EN retriggers, or restarts, the clamp sequence and the gain count of 37 bits. The remainder of the sequence is similar to that of Figure 3b.

The MFM outputs (SEP CLK and SEP DATA) are disabled, while the 1FVFO output is available at half the VFO frequency.

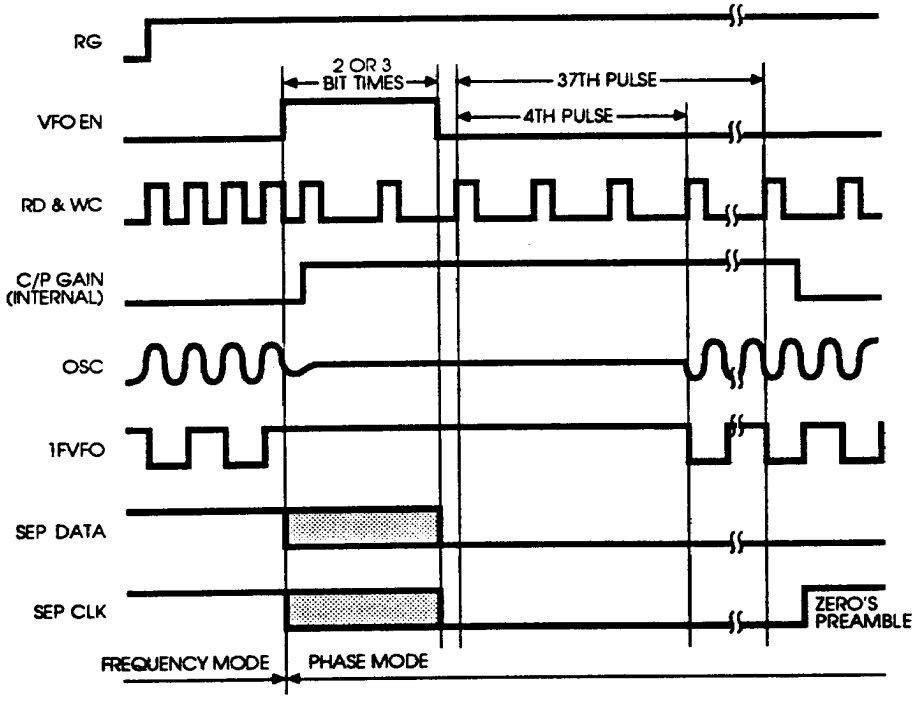


FIGURE 4a. AIC-6225A TIMING DIAGRAM CONFIGURED WITH THE AIC-250 FOR MFM: INITIATION OF A BLOCK READ

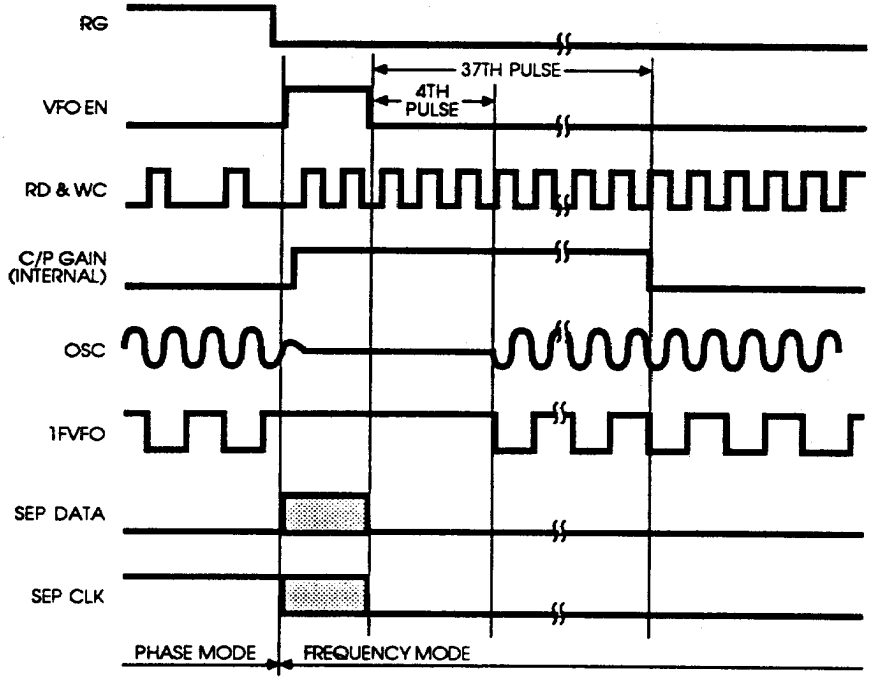


FIGURE 4b. AIC-6225A TIMING DIAGRAM CONFIGURED WITH THE AIC-250 FOR MFM: COMPLETION OF A BLOCK READ

ABSOLUTE MAXIMUM RATINGS AND D.C. CHARACTERISTICS

Absolute Maximum Ratings

Supply Voltage: Analog Vcc (VccA) 14.5V
Supply Voltage: Digital Vcc (VccD) 7.0V
Input Voltage Range ..... IGND –0.2V to VccD +0.2V
Operating Free-Air Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... –25 to 125°C
Lead Temperature Range ..... 60 Sec at 300°C
ESD Potential ..... 2 kV
Continuous Power Dissipation:
28-Pin PLCC ..... TBD

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
VccA	Analog Supply Voltage	9.5	12.0	12.6	V	
IccA	Analog Supply Current			48	mA	VccA = 12.6V
VccD	Digital Supply Voltage	4.75	5.0	5.25	V	
IccD	Digital Supply Current			53	mA	VccD = 5.25V
	Analog to Digital Ground Differential	–0.2		0.2	V	

Electrical Characteristics

(Conditions: At 25°C ambient, VccA = 9.5V to 12.6V, VccD = 4.75V to 5.25V, unless otherwise noted.)

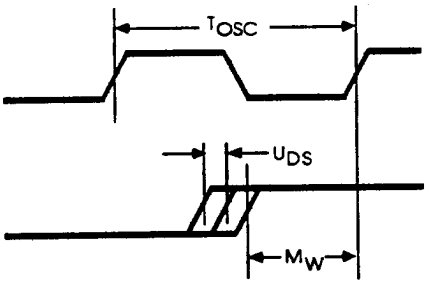
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITION
$F_{OP\,MAX}$	Maximum Operating Frequency	60			MHz	
$F_{OSC\,MAX}$	Maximum Oscillator Frequency	100			MHz	Appropriate ext components
O_A	Oscillator Amplitude	300	400	500	mV p-p	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{IL}	Low-Level Input Current			-0.4	mA	VccD = 5.25V V_I = 0.4V
V_{IH}	High-Level Input Current			20	µA	VccD = 5.25V V_I = 2.4V
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.9			V	I_{OH} = -400 µA
CPR_L	Charge Pump Rate	300	325	335	µA /(2π rad)	Low Gain
CPR_H	Charge Pump Rate	1.30	1.35	1.40	mA /(2π rad)	High Gain
CRPE	Clamp Release Phase Error	$\frac{-4\pi}{T_{OSC}}$		$\frac{+4\pi}{T_{OSC}}$	rad	Phase Mode T_{OSC} = Osc
		-2		+2	nsec	period (nsec)
PD_{CPLR}	Phase Detector, Charge Pump Linear Range	$-\pi$		$+\pi$	rad	
PD_{PDE}	Phase Detector,	$-\pi/10$		$+\pi/10$	rad	
	Phase Discrimination Error	$\frac{-T_{OSC}}{20}$		$\frac{+T_{OSC}}{20}$	usec	
V_{OLB}	Buffer, Integrator Output Low Voltage	1.70	1.90	2.20	V	
V_{OHB}	Buffer, Integrator Output High Voltage	6.30	6.60	6.80	V	
BW_{BI}	Buffer, Integrator Bandwidth	5.0			MHz	
I_{BL}	Buffer Input Leakage			100	nA	
U_{DS}	Data Separator Uncertainty (Note A.)			.05 x T_{OSC}		$T_{OSC} = 1/F_{OSC}$

Note A. The speed designator -XX corresponds to FOSC during test, or the Device Test Frequency (DTF). For Multiple Frequency (CDR) applications, U_{DS} is guaranteed over the frequency range 0.5* DTF to 1.1* DTF.

SYMBOL	PARAMETER	RANGE		UNITS	CONDITION
SDLDC	SYNC DATA Leading DATA CLK	$(T_{osc}/2 + 2.3)$	± 5	nsec	
SDL1FVFOH	SEP DATA Leading 1FVFO HIGH	T_{osc}	±10	nsec	
SCL1FVFO	SEP CLK Leading 1FVFO	T_{osc}	±10	nsec	

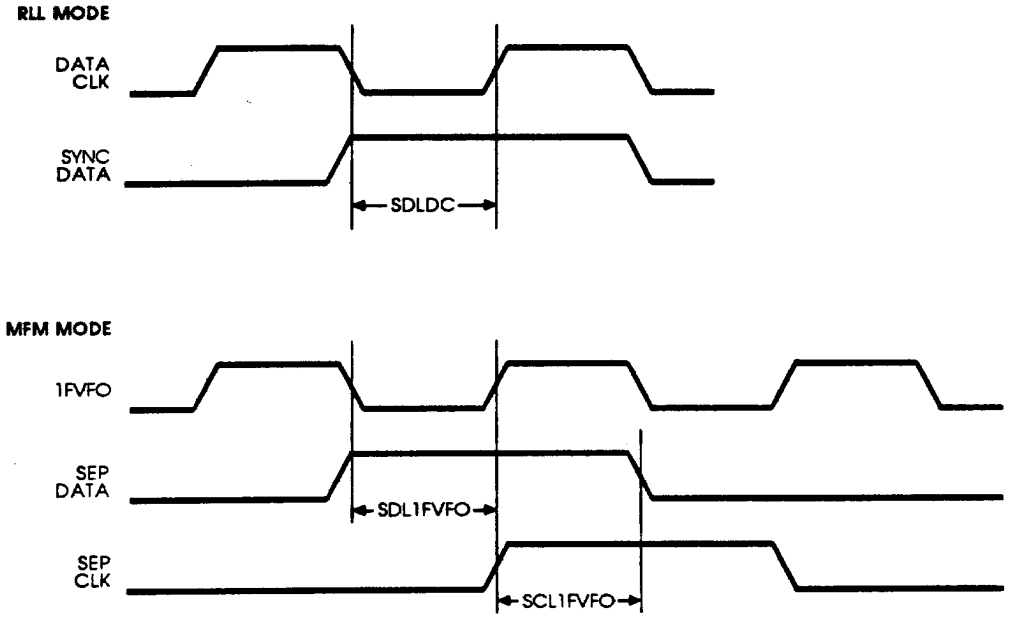
Data Separator Uncertainty and Available Window Margin

Data Separator Uncertainty characterizes the maximum error which may exist in a device from a particular speed group. Data Separator Uncertainty includes DC offset and one standard deviation total jitter, assuming normally distributed jitter. It is measured in a "dynamic" environment, emulating worst-case bit-shift of alternating "early" and "late" data bits from a disk drive, representing the true data recovery capability of the device. In the AIC-6225A, the Data Separator Uncertainty is less than 5% of the oscillator period.



T_{OSC} = OSCILLATOR PERIOD
M_W = AVAILABLE WINDOW MARGIN
U_{DS} = DATA SEPARATOR UNCERTAINTY
$M_W = T_{OSC}/2 - U_{DS}$

Data Clock Output Timing



External Component Selection

TABLE 1. FIXED COMPONENTS

C3	0.1 µF	+80/-20 Multilayer Ceramic
C7	0.01 µF	+80/-20 Multilayer Ceramic
C10	0.01 µF	+80/-20 Multilayer Ceramic
C11	0.01 µF	+80/-20 Multilayer Ceramic
R1	4.99 kΩ	1% (100 ppm)
R3	100 kΩ	5%
CR1	MVAM109	Tuning Diode

Note: See Figure 2 for corresponding component labels

External Component Selection

TABLE 2. 2,7 RLL DATA TRANSFER RATE DEPENDENT COMPONENTS

DATA TRANSFER RATE	7.5 Mb/s	10 Mb/s	15 Mb/s	20 Mb/sL	25 Mb/s	UNITS	TOL
Data transfer rate dependent components							
C8	2200	800	1000	820	680	pF	5% X7R
C9	180	150	82	56	47	pF	5% X7R
R5	2	2	2.4	2.4	2.2	kΩ	5%
R2	3.3	2.7	1.8	1.3	1.0	kΩ	5%
C6	100	100	100	100	100	pF	5% NPO
C5	470	680	330	270	2700	pF	5% NPO
R4	200	130	91	62	39	Ω	5%
L1	1.8	1.0	0.47	0.27	0.15	µH	10%Shielded
Poles and zeros							
Wn	0.436	0.563	0.893	1.123	1.498	MRad/s	
Wz	0.210	0.256	0.385	0.475	0.625	MRad/s	
Wp1	2.77	3.33	5.08	7.44	9.67	MRad/s	
Wp2	3.03	3.70	5.55	7.69	10.00	MRad/s	
Attenuation at HF Data	-84	-84	-84	-83	-82	dB	
K01 Osc Gain	0.97	1.32	1.84	2.39	3.52	MHz/V	
PLL BW (-3 DB) in Preamble at High Gain	1.4	2.0	3.3	4.3	6.0	Mrad/s	

NOTES:

1. The above components are for an eight-byte, "3T" preamble (100100 repeating pattern). HF data corresponds to highest frequency data pattern.
2. The given oscillator components are set for the Motorola MVAM109 varactor (tuining) diode. Use of the AIC-6225A is not restricted to this tuning diode, but the oscillator components may need to be changed to accommodate other tuning diodes from Motorola, or "equivalent" tuning diodes from other manufacturers.
3. Clamp resistor R2 can be calculated from nominal oscillator frequency in MHz (f), and inductor value in H (L1), by employing the formula: $R2 = 5.28\ (L1 * f)^{1.11} - 11.72$ Ohms.
   For CDR application, the above formula becomes: $R2 = 5.28\ (L1 * f_c)^{1.11} - 11.72$ Ohms.
   where:
   $f_c = 0.8 * f_L + 0.2 * f_H$
   f_L: Oscillator frequency of lowest data rate
   f_H: Oscillator frequency of highest data rate

APPENDICES

A1 AIC-6225A SYSTEM CONFIGURATION

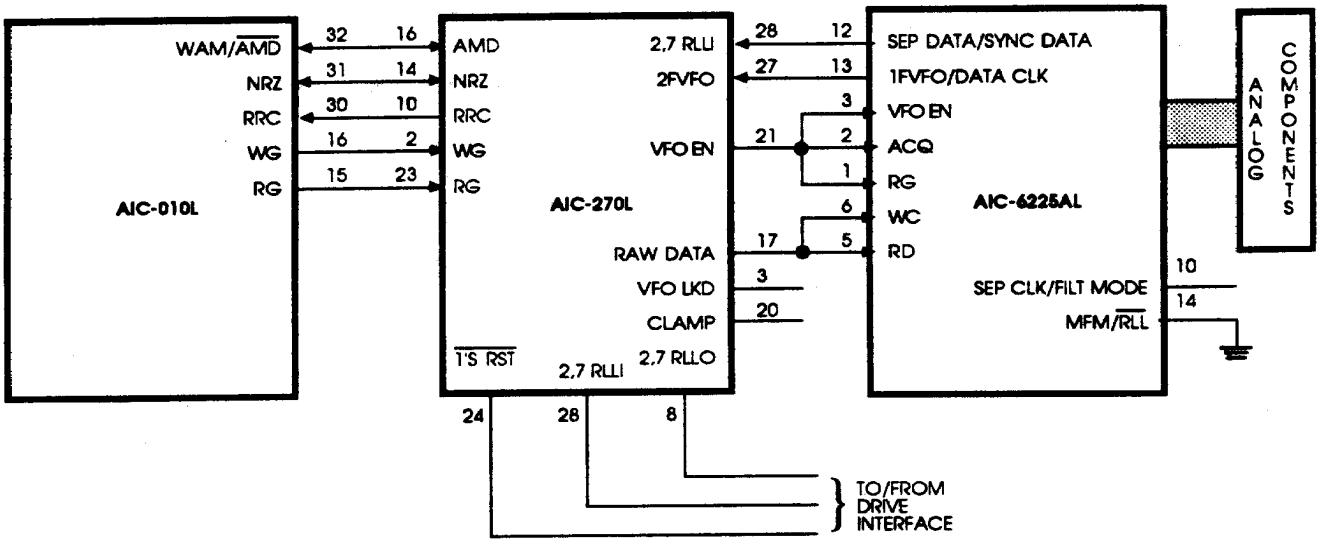


FIGURE A1-1. AIC-6225A CONFIGURED WITH AIC-270 FOR 2,7 RLL OPERATION

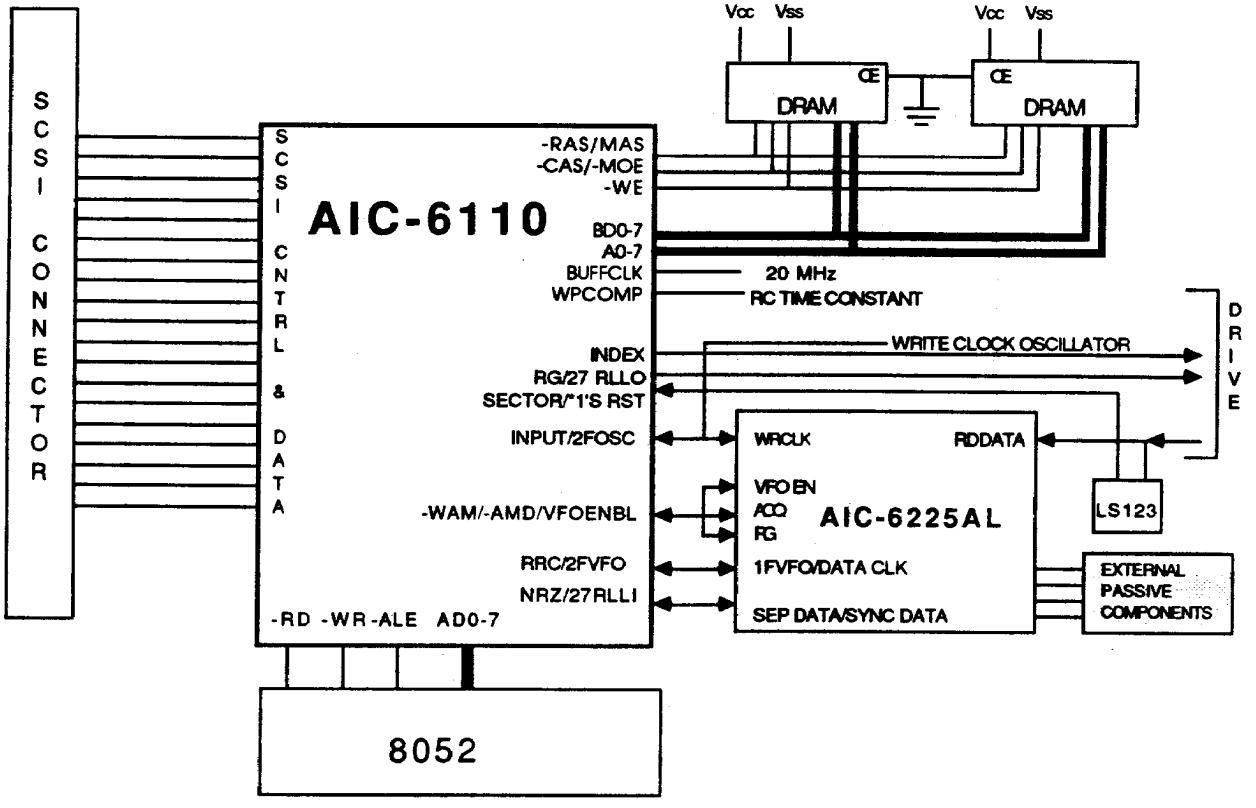


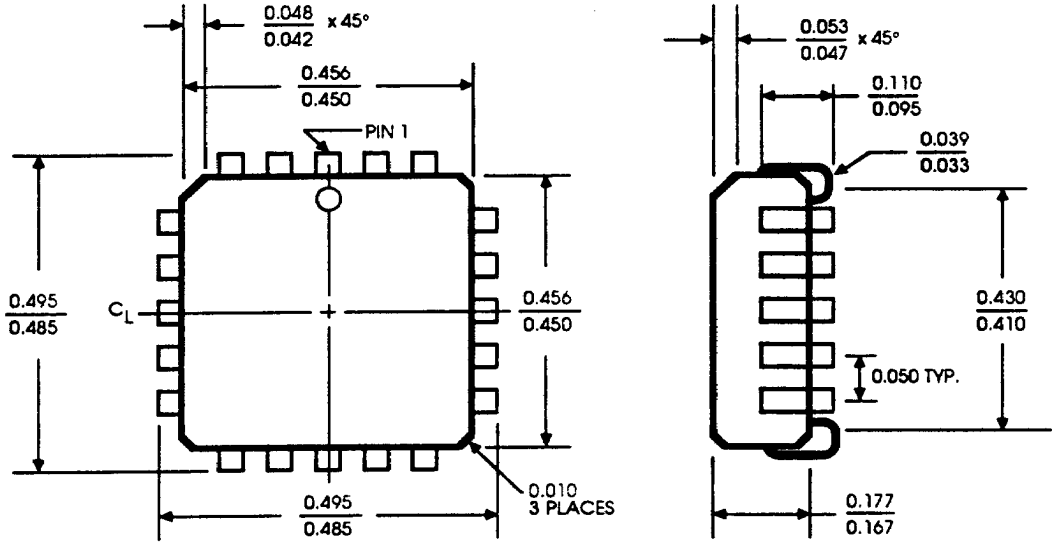
FIGURE A1-2. AIC-6225A CONFIGURED WITH AIC-270 FOR 2,7 RLL OPERATION

A2 LAYOUT SUGGESTIONS

While the AIC-6225A is a high-performance circuit containing both digital and analog elements, it has been carefully designed to minimize sensitivity to layout, given reasonable care and attention to a few common rules of high-frequency circuits. The degree of sensitivity to layout will increase to some extent as the frequency of the oscillator increases, but no more so than that typically observed in any circuit of comparable frequency using discrete components.

It is suggested that a small analog ground plane be formed around the AGND pin and that it surround those external components which contact analog ground. VccA, the analog-supply input, should be decoupled in the analog-ground plane. VccD, the digital supply, should be decoupled to digital ground. IGND and OGND are to be tied together by a standard width ground trace and then contacted to the analog ground plane using a standard width ground trace at the point where the analog-supply decoupling capacitor contacts the ground and as far away as practical from the points where all other external components associated with the AIC-6225A contact the analog-ground plane. No other contacts between the analog-ground plane of the data separator and any other system ground should be made. All leads should be short and wide, and care should be taken with the node at pin 16, which, at higher frequencies, is sensitive to loading by parasitic capacitance. Multilayer layout of this circuit should be avoided, but, if used, attention should be paid to parasitic coupling and loading between layers.

PACKAGING INFORMATION



28-Lead Plastic Surface Mount Package