MICROCOMPUTER ASSOCIATES, INC.

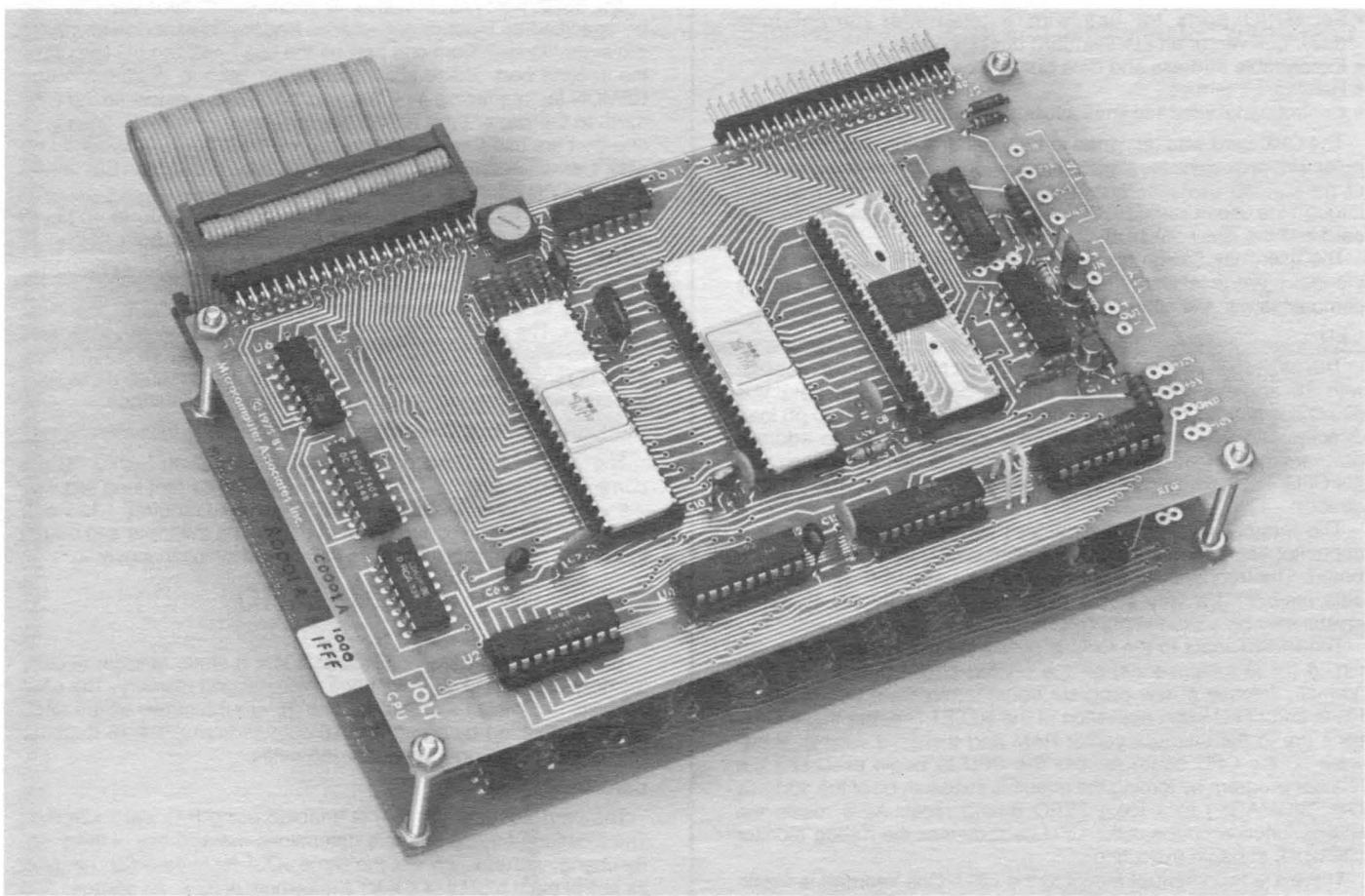
Product Catalog*

featuring

VT-100 CRT Terminal
VT-200 CRT Terminal with Tiny BASIC, Resident Assembler and Demon
Single Board Computers
and

JOLT

The newest generation microcomputer system with the exclusive on-board DEMON™ debug monitor. In kit form, you can build it, plug it in and talk to it in three hours or less . . . for unheard of low prices!



This is the fully assembled JOLT™ 4K System. The JOLT CPU card includes the powerful DEMON™ Debug Monitor.

* Catalog items and prices subject to change without notice.

JOLT SYSTEM DESCRIPTION

The JOLT system consists of a set of modular microcomputer boards which can be used singly or tied together to produce any desired microcomputer system configuration. The minimum system is one CPU board, which alone constitutes a viable computer system complete with central processor, I/O, interrupts, timer, read-write memory, and a complete software debug monitor in read-only-memory.

Additional boards in the JOLT system include a 4 K byte RAM, I/O, Power Supply and blank Universal Interface board. A large JOLT system could have up to 32 K bytes of RAM memory, up to 128 lines of bidirectional I/O and 16 interrupts.

JOLT boards come in kit form or assembled, and are ready to use in any form, from home hobby kits to industrial applications. All JOLT components are new, fully tested and fully warranted by MAI.

The currently available JOLT boards are described in greater detail on the following pages. Additional JOLT support under development includes:

- Keyboard/display board with audio cassette interface,
- TV interface board, and
- Resident assembler.

CPU CARD

General

The JOLT CPU card is a complete microcomputer on a single printed circuit board. When connected to a terminal, the CPU card provides everything necessary to begin writing, debugging and executing microcomputer programs. The salient features of the JOLT CPU card are:

- An MOS Technology MCS6502 NMOS microprocessor
- 512 bytes of program RAM, and 64 bytes of interrupt vector RAM
- 1 K bytes of mask programmed ROM containing DEMON, a powerful debug monitor
- 26 programmable I/O lines
- Internal RC clock, or crystal controlled clock with user supplied crystal
- Serial I/O ports for use with a teleprinter current loop drive/receiver, or an EIA standard driver/receiver
- Expandable address and data buses
- Hardware interrupt
- Control panel interface lines available on card connector

The CPU card was designed to be a general purpose microcomputer with provisions for expanding memory and interfacing to serial or parallel I/O devices. System expansion may be accomplished through the use of standard JOLT support cards (the JOLT memory card and the JOLT I/O card).

The user may design his own memory and I/O subsystems with the JOLT universal card. The form factor of the universal card is compatible with the other JOLT system printed circuit cards.

CPU

The MCS6502 CPU chip is a parallel 8-bit NMOS microprocessor with 16 address lines and an internal oscillator. The data bus (D0-D7) is bidirectional and will drive one TTL (1.6 ma, 130 pf) load directly. The 64 K byte (2^{16}) address space is used to address program memory and to select I/O devices for communication with the CPU. The address will also drive onto TTL (1.6 ma, 130 pf) load directly.

The internal oscillator operates in a "free run" mode with a capacitor and variable resistor supplied on the CPU printed circuit board. The frequency of oscillation may be adjusted with the variable resistor. If a very stable clock is required by the system a crystal may be added to the CPU board.

The RESET input to the CPU is pulled to logic ground by an RC circuit (t=33 milliseconds) on the printed circuit board. The CPU normally fetches a new program count vector from hex locations FFFC and FFFD upon activation of the RESET line, but these locations are in the interrupt vector RAM and therefore volatile. Hardware on the CPU board causes the CPU to begin executing the monitor program by forcing the effective sixteenth bit of the address bus (SIGMAG°) to a logic ZERO during reset. As a result, the RESET function on the JOLT CPU card causes the debug monitor (DEMON) to begin executing.

There are two interrupt inputs to the CPU. One interrupt is maskable under program control ($\overline{IRQ}$) and the other (NMI) is not.

A READY control line provides for asynchronous operation with slow memory or I/O devices.

The address bus (A0-A15), the data bus (D0-D7), the two phase clock (PIT, P2T), the reset line (*RESET), the interrupt lines (*IRZ, AND *NMI), and the ready line (RDY) are all available at the edge connector of the CPU card. The loading restrictions should be considered when using the signal lines driven by the CPU for external system expansion.

A more detailed description of the CPU inputs and outputs may be found in the MCS6500 hardware manual available from MOS Technology Inc.

Program RAM

There are 512 bytes of program RAM provided on the CPU card. The program RAM is hardwired addressed as the first 512 bytes of the CPU's 64 K of memory address space. It may become necessary to remove these RAM's from their sockets if a 4 K memory card is also hardwired in this address space. The program RAM on the CPU card uses NMOS RAM chips.

Monitor ROM and Interrupt Vector RAM

The monitor ROM is located in the last 1 K bytes of the lower half of memory space (first 32 K bytes). The interrupt vector RAM is located in the last 64 bytes of the 64 K memory address space.

The monitor ROM and the interrupt vector RAM as well as additional I/O are implemented with a single MPS 6530 chip.

Programmable User I/O

The programmable I/O lines available from the CPU card are provided by a Peripheral Interface Adapter (PIA) and a 6530 ROM chip.

The PIA has two 8-bit I/O ports with two interrupt-causing control lines each. Two jumpers are provided on the card which connects one or both PIA interrupt outputs to the CPU $\overline{IRQ}$ interrupt line. Refer to the CPU assembly drawing for proper identification of the jumpers. A Data Direction Register for each port determines whether each I/0 line is an input or an output. A detailed description of the PIA chip may be found in the MCS6500 Microcomputer Family Hardware Manual.

The 6530 ROM chip provides 10 additional I/O lines that may also be specified as input or output lines under program control. There are eight I/O lines from one port on the 6530 and two I/O lines from the second port. These I/O lines may be used in conjunction with DEMON for interfacing a high speed paper tape reader to the CPU card. In the paper tape reader application, the eight I/O lines from one port are used as inputs and two I/O lines from the second port are used to accomplish the handshake control between the reader and the CPU card.

The PIA is hardwired addressed as location 4000_{16} to 4003_{16} in the memory address space. Memory addresses from 4000_{16} to $5C03_{16}$ are allocated for PIA devices so that the JOLT system may be easily expanded to accommodate up to eight PIA chips.

The 6530 uses addresses from 6200_{16} to $6E07_{16}$ for eight I/O functions. The unused memory addresses occur because address bits A10 and A11 are ignored to simplify address decoding. The 6530 I/O lines may be referred to as Monitor I/O because these lines are commonly used for a high speed paper tape interface.

Standard Interface Circuits

The JOLT CPU card provides direct interfacing with a 20 ma current loop and RS232C terminal. The 20 ma current loop requires +5 v and −10 v whereas the RS232C interface requires +12 v and −10 v. Both interfaces are wired in parallel on the input and output thereby allowing both interfaces to be used simultaneously.

RAM CARD

General

The JOLT RAM card consists of 4 K x 8 static random access memory using 2111 (256 x 4) one microsecond memory. The card consists of 32-2111's organized into 16 groups of two where each group is enabled by one of the 16 outputs from the 4-16 decoder (74154). Each group represents 256 bytes.

Card Enable

The card decoder (74154) is enabled using P.C. card jumpers. The location of these jumpers determines the address of the card. By changing these jumpers the same JOLT RAM card can be used as any of eight blocks of 4 K for a maximum of 32 K. All address and data lines come from the J1 connector.

Address Buffers

Address lines A8-A15 are buffered on the card. A8-A11 are used to drive the 74154 decoder which selects the one of 16 pairs of 2111's. A12-A15 are complemented and used as possible input to the card enable gate (7400). A8-A15 are buffered using a CD 4049 inverting buffer. Address lines A0-A7 drive directly to the 2111's.

Control Lines

Two control lines are used on the RAM card, *WRITE and *RW. Both are negative (0 v) true signals and originate from the JOLT CPU card. *WRITE is normally high (+5 v) and goes to low (0 v) during any memory write operation for a duration equivalent to phase 2 (P2T). The properly decoded card and 2111 chip pair will be previously enabled and will consequently accept data to be written.

The *RW signal is normally low (0 v) indicating a read operation and goes high (+5 v) during a write operation. The duration of this signal is approximately one clock bit time.

PERIPHERAL INTERFACE (I/O)

General

The Peripheral Interface (I/O) Card allows further expansion of the JOLT I/O system. Two additional Peripheral Interface Adapter (PIA) chips are provided on each card. On-board decoding with jumper selection allows for convenient address selecting.

PIA's

Each of two PIA's provide 16 bidirectional TTL drive I/O lines and two interrupt-causing control lines. A Data Direction Register for each port determines whether each I/O line is an input or an output. Two jumpers, per PIA, are provided on the card which allow connection of one or both PIA interrupt outputs to the CPU $\overline{IRQ}$ interrupt line. Refer to the I/O assembly drawing for proper identification of the jumpers. A detailed description of the PIA chip may be found in the MCS6500 Microcomputer Family Hardware Manual.

On-Board Decoding

Jumper selectable decoding is provided on the card to allow the user to assign each PIA chip to one of eight possible locations.

POWER SUPPLY

General

The JOLT power supply is a compact, efficient source of d.c. voltage for the JOLT microcomputer system. The supply includes one printed circuit card and one transformer externally mounted. The card is compatible with the other JOLT cards (i.e. it is of the same size). The power supply will support various system configurations as will be shown later.

Basic Power Unit

The basic JOLT power unit supplies the following voltages and currents:

+12 v @ 1.5 a	25°C
+5 v @ 2.5 a	25°C
−10 v @ .4 a	25°C

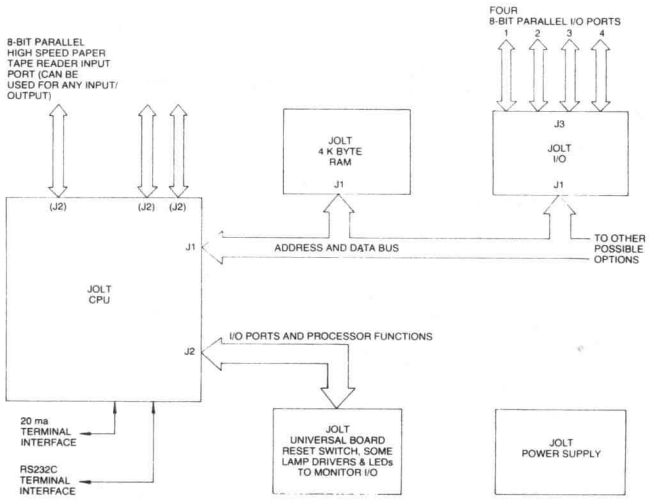
The +12 volts is unregulated supplying as much as 2.0 amps at +10 v. This supply becomes ideal for applications such as EIA-RS232C interfacing, led's, displays, MOS and CMOS logic, etc. where high regulation is not required.

The +5 volts uses an LSI voltage regulator supplying from 0-2.5 amps at +4.75 to +5.25 volts. Additional features such as current limiting, power limiting, and thermal shutdown makes this supply virtually burnout proof. The +5 volts is the most used voltage in the JOLT system. All TTL and MOS devices use +5 v with the exception of the EIA interface logic. A +5 v booster option is available which provides an additional 2.5 a at 25°C.

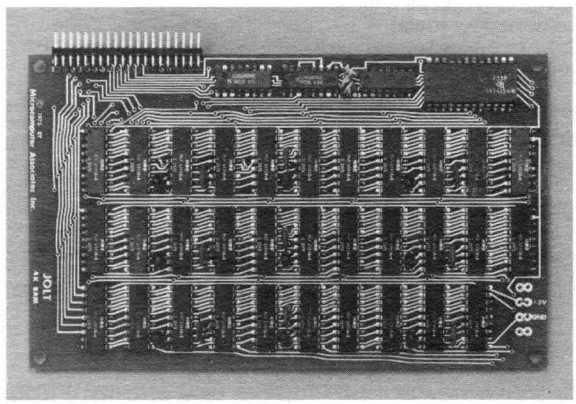
The −10 volts is also regulated with an LSI voltage regulator supplying from 0 to .4 amps at −9.6 to −10.4 volts. Typical applications for this supply include TTY interface, EIA-RS232C interface, PROMs, biasing memories, MOS and CMOS logic, etc.

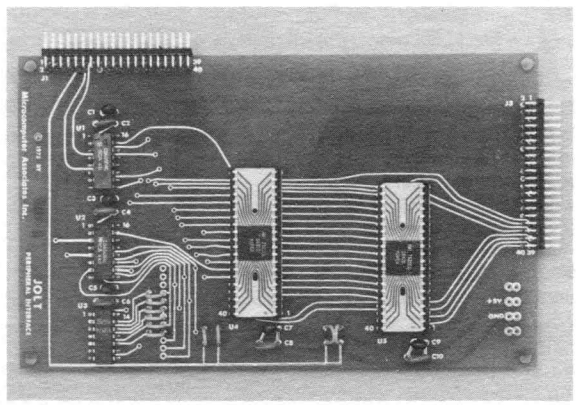
Typical Systems for JOLT Power Supply

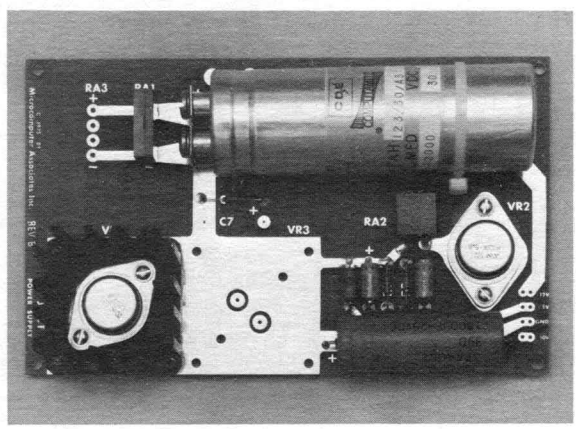
The following page shows several JOLT system configurations and the amount of current used by each. The +12 v and −10 v is not shown since they are only used on the CPU card and draw less than 50 ma each.



FUNCTIONAL BLOCK DIAGRAM







JOLT SPECIFICATIONS SUMMARY

CPU

- MOS Technology 6502 CPU
- MOS Technology 6530 with DEbug MONitor
- 750 KHZ clock operation-RC controlled or crystal controlled with user supplied crystal.
- 512 bytes RAM
- 64 bytes RAM-located at interrupt vector locations
- Expandable address & data lines
- Direct drive to 8 K bytes of memory
- 26 Programmable I/O lines-one standard TTL drive
- Two hardware interrupts
- Serial interface for 20 ma current loop and EIA RS232C
- 4.25" x 7" printed circuit card
- Compatible with other JOLT cards

RAM

- 4096 bytes Random Access Memory
- 1.0 microsecond access
- Card enable — jumper selectable in groups of 4096 bytes
- MOS inputs (address and data)
- TTL drive output (data)
- 4.25" x 7" printed circuit card
- Compatible with other JOLT cards

Peripheral Interface (I/O)

- 32 Programmable input/output lines
- TTL compatible inputs
- TTL drive outputs
- Programmable Direction Register for each I/O line
- Four interrupt-causing inputs
- Jumper control on CPU interrupts
- Two 6820 Peripheral Interface Adaptor (PIA) chips
- One of eight on-board decoding per PIA
- 4.25" x 7" printed circuit card
- Compatible with other JOLT cards

Power Supply

- Three voltage power supply (+12, +5, −10)
- 20 watt @ 25°C
- +12 v — unregulated
- 12 v @ no load 25°C
- 11 v @ 1.5 amps 25°C
- +5 v — regulated
- LSI voltage regulator
- 12.5 watts (2.5 amps) @ 25°C
- Internal current limiting
- Internal thermal limiting
- Low output impedance (.01Ω typical)
- −10 v — regulated
- LSI voltage regulator
- 4 watts (.4 amps) @ 25°C
- Internal current and thermal limiting
- Low output impedance (.02Ω typical)
- Transformer included
- 4.25" x 7" printed circuit card
- Compatible with other JOLT cards

With +5 v Booster Option

- Additional 12.5 watts (2.5 amps) @ 25°C

POWER SUPPLY REQUIREMENTS

CPU:	Typical	+5 v @ 470 ma
		−10 v @ 33 ma
		+12 v @ 19 ma
	Maximum	+5 v @ 903 ma
		−10 v @ 48 ma
		+12 v @ 25 ma
RAM:	Typical	+5 v @ 1.0 a
	Maximum	+5 v @ 1.9 a
I/O:	Typical	+5 v @ 140 ma
	Maximum	+5 v @ 275 ma

JOLT SYSTEM CONFIGURATION

System	Card	Typical Amps @ + 5 v 25° C		Jolt Supply
1	CPU	.5	1.5 a	Basic Unit
	4 K RAM	1.0		
2	CPU	.5	1.6 a	Basic Unit
	4 K RAM	1.0		
	I/O	.14		
3	CPU	.5	2.6 a	Basic Unit
	4 K RAM	1.0		
	8 I/O cards *	1.1		
4	CPU	.5	.64 a	Basic Unit
	I/O	.14		

SOFTWARE DEVELOPMENT

Debug Monitor

The JOLT CPU card comes complete with DEMON, MAI's debug monitor program. The program is located in the 1,024 byte, Read Only Memory (ROM) of the multi-function 6530 chip and is therefore completely protected against any alteration. DEMON provides a permanently available general purpose monitor program to aid users in developing hardware and software for MAI's JOLT series of microcomputers.

DEMON's Features Include:

- Self adapting to any terminal speed from 10-30 cps,
- Display and Alter CPU registers,
- Display and Alter Memory locations,
- Read and Write/Punch hexidecimal formatted data,
- Write/Punch BNPF format data for PROM programmers,
- Unlimited breakpoint capability,
- Separate non-maskable interrupt entry and identification,
- External device interrupts directable to any user location or defaulted to DEMON recognition,
- Capability to begin or resume execution at any location in memory,
- Completely protected, resident in Read Only Memory,
- Capability to bypass DEMON entirely to permit full user program control over system,
- High speed 8-bit parallel input option, and
- User callable I/O subroutines.

DEMON's Command Set Includes:

.R		Display registers (PC,F,A,X,Y,SP)
.M	ADDR	Display memory (8 bytes beginning at ADDR)
.:	DATA	Alters previously displayed item
.LH		Load hexidecimal tape
.WB	ADDR1 ADDR2	Write BNPF tape (from ADDR1 to ADDR2)
.WH	ADDR1 ADDR2	Write hexidecimal tape (from ADDR1 to ADDR2)
.G		Go, continue execution from current PC address
.H		Toggles high-speed-reader option (if its on, turns it off; if off, turns on)

Assembler and Instruction Simulator

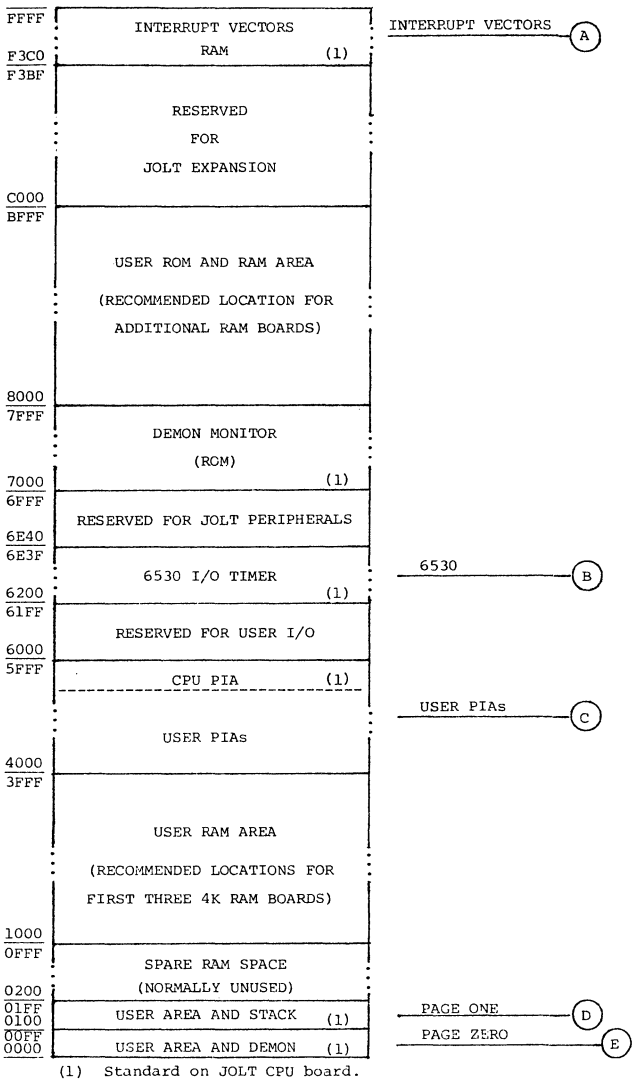
Assembler and instruction simulator programs are currently available on three major national time sharing networks; GE, NCSS and UCS. MOS Technology has also announced a resident assembler available by the end of 1975. MAI is tentatively planning to incorporate the resident assembler into the JOLT system.

Paper tape output from the time sharing assemblers is directly loadable into JOLT memory using the DEMON monitor load hex command.

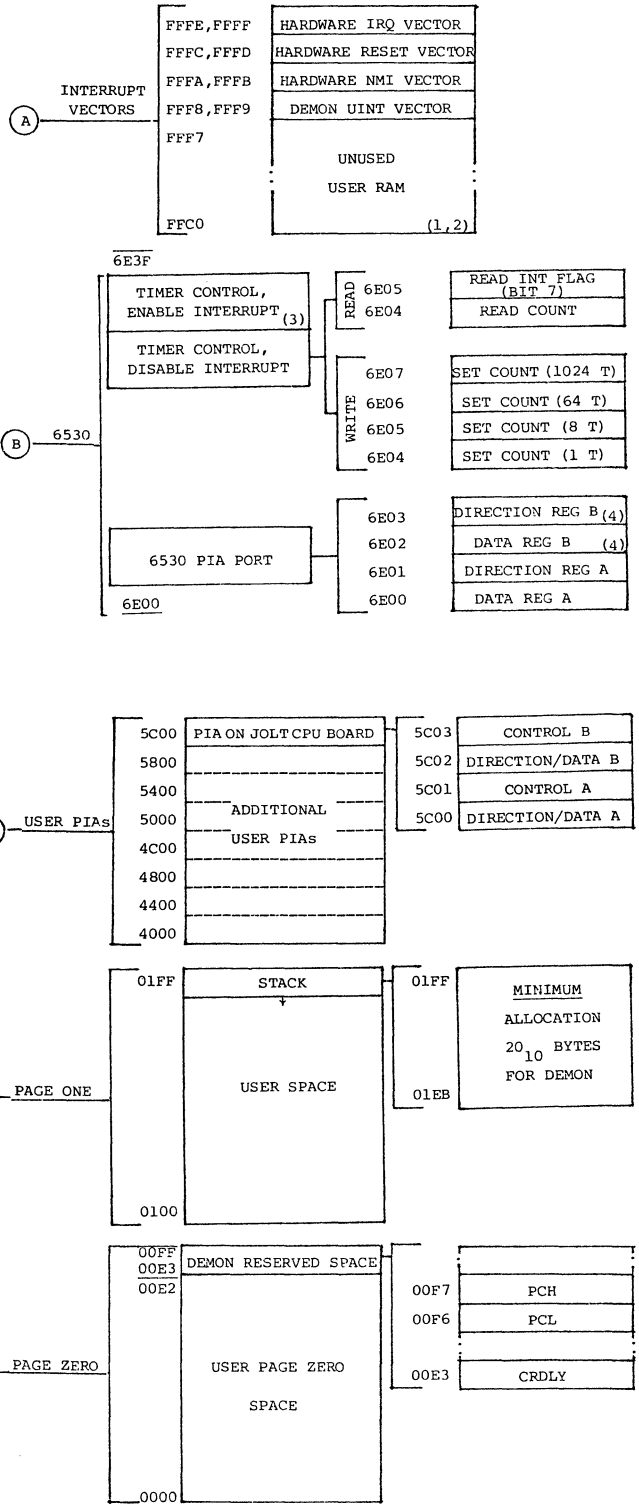
JOLT SYSTEM MEMORY MAP

The memory map on the following charts explains what functions have been assigned to each segment of the JOLT address space. It is recommended that users respect this space allocation when adding memory and peripherals to their JOLT systems. Space has been reserved for 32 K bytes of user RAM or ROM, seven additional PIA devices, and up to 512 user I/O device registers. Other areas are reserved for JOLT expansion, i.e., new JOLT peripherals and memory options will use these spaces. Users are advised to not use JOLT expansion space unless absolutely necessary.

Note that some areas used by the JOLT CPU board and PIA boards have more space indicated than there are registers or locations in the device occupying them. This is because these devices do not decode all address bits, or use some of the address bits for special functions. For example, the 6530 timer determines the time scale and interrupt enable/disable by the address used to access it. Thus, these "partly filled" areas are actually entirely used and are not available for other uses.



(1) Standard on JOLT CPU board.



(1) Standard on JOLT CPU board.

(2) Available to user—not used by DEMON.

(3) To get enable-interrupt address, add 0008_{16} to disable-interrupt address with corresponding functions.

(4) Reserved for DEMON use—TTY control and reset functions.

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND,X)			(IND),Y			Z,PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z,PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
ADC	A+M+C → A (1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3										✓	✓	✓	–	–	✓
AND	A∧M → A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3										✓	✓	–	–	–	–
ASL	C←7 6 5 4 3 2 1 0←0				0E	6	3	06	5	2	0A	2	1										16	6	2	1E	7	3													✓	✓	✓	–	–	–
BCC	BRANCH ON C=0 (2)																															90	2	2							–	–	–	–	–	–
BCS	BRANCH ON C=1 (2)																															B0	2	2							–	–	–	–	–	–
BEQ	BRANCH ON Z=1 (2)																															F0	2	2							–	–	–	–	–	–
BIT	A∧M				2C	4	3	24	3	2																															M7	✓	–	–	–	M6
BMI	BRANCH ON N=1 (2)																															30	2	2							–	–	–	–	–	–
BNE	BRANCH ON Z=0 (2)																															D0	2	2							–	–	–	–	–	–
BPL	BRANCH ON N=0 (2)																															10	2	2							–	–	–	–	–	–
BRK	(See Fig. 1)													00	7	1																									–	–	–	1	–	–
BVC	BRANCH ON V=0 (2)																															50	2	2							–	–	–	–	–	–
BVS	BRANCH ON V=1 (2)																															70	2	2							–	–	–	–	–	–
CLC	0 → C													18	2	1																									–	–	0	–	–	–
CLD	0 → D													D8	2	1																									–	–	–	–	0	–
CLI	0 → I													58	2	1																									–	–	–	0	–	–
CLV	0 → V													B8	2	1																									–	–	–	–	–	0
CMP	A–M (1)	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3										✓	✓	✓	–	–	–
CPX	X–M	E0	2	2	EC	4	3	E4	3	2																															✓	✓	✓	–	–	–
CPY	Y–M	C0	2	2	CC	4	3	C4	3	2																															✓	✓	✓	–	–	–
DEC	M–1 → M				CE	6	3	C6	5	2													D6	6	2	DE	7	3													✓	✓	–	–	–	–
DEX	X–1 → X													CA																											✓	✓	–	–	–	–
DEY	Y–1 → Y													88																											✓	✓	–	–	–	–
EOR	A ⊻ M → A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3										✓	✓	–	–	–	–
INC	M+1 → M				EE	6	3	E6	5	2													F6	6	2	FE	7	3													✓	✓	–	–	–	–
INX	X+1 → X													E8	2	1																									✓	✓	–	–	–	–
INY	Y+1 → Y													C8	2	1																									✓	✓	–	–	–	–
JMP	JUMP TO NEW LOC.				4C	3	3																													6C	5	3				–	–	–	–	–	–
JSR	(See Fig. 2)JUMP SUB				20	6	3																																			–	–	–	–	–	–
LDA	M → A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3										✓	✓	–	–	–	–

INSTRUCTIONS		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND,X)			(IND),Y			Z,PAGE,X			ABS,X			ABS,Y			RELATIVE			INDIRECT			Z,PAGE,Y			CONDITION CODES					
MNEMONIC	OPERATION	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	OP	N	#	N	Z	C	I	D	V
LDX	M → X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3										B6	4	2	✓	✓	–	–	–	–
LDY	M → Y (1)	A0	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3													✓	✓	–	–	–	–
LSR	0→7 6 5 4 3 2 1 0→C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3													0	✓	✓	–	–	–
NOP	NO OPERATION													EA	2	1																									–	–	–	–	–	–
ORA	A∨M → A	09	2	2	0D	4	3	05	3	2							01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3										✓	✓	–	–	–	–
PHA	A→ Ms S–1→S													48	3	1																									–	–	–	–	–	–
PHP	P→ Ms S–1→S													08	3	1																									–	–	–	–	–	–
PLA	S+1→S Ms→A													68	4	1																									–	–	–	–	–	–
PLP	S+1→S Ms→P													28	4	1																									(RESTORED)					
ROL	7 6 5 4 3 2 1 0 C				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3													✓	✓	✓	–	–	–
RTI	(See Fig. 1) RTRN. INT.													40	6	1																									(RESTORED)					
RTS	(See Fig. 2) RTRN SUB													60	6	1																									–	–	–	–	–	–
SBC	A–M–C̄ → A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3										✓	✓	(3)	–	–	✓
SEC	1 → C													38	2	1																									–	–	1	–	–	–
SED	1 → D													F8	2	1																									–	–	–	–	1	–
SEI	1 → I													78	2	1																									–	–	–	1	–	–
STA	A → M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3										–	–	–	–	–	–
STX	X → M				8E	4	3	86	3	2																															96	4	2	–	–	–	–	–	–
STY	Y → M				8C	4	3	84	3	2													94	4	2																	–	–	–	–	–	–
TAX	A → X													AA	2	1																									✓	✓	–	–	–	–
TAY	A → Y													A8	2	1																									✓	✓	–	–	–	–
TSX	S → X													BA	2	1																									✓	✓	–	–	–	–
TXA	X → A													8A	2	1																									✓	✓	–	–	–	–
TXS	X → S													9A	2	1																									–	–	–	–	–	–
TYA	Y → A													98	2	1																									✓	✓	–	–	–	–

(1) ADD 1 TO "N" IF PAGE BOUNDRY IS CROSSED.

(2) ADD 1 TO "N" IF BRANCH OCCURS TO SAME PAGE.
ADD 2 TO "N" IF BRANCH OCCURS TO DIFFERENT PAGE.

(3) CARRY NOT = BORROW.

X INDEX X
Y INDEX Y
A ACCUMULATOR
M MEMORY PER EFFECTIVE ADDRESS
Ms MEMORY PER STACK POINTER

\+ ADD
– SUBTRACT
∧ AND
∨ OR
⊻ EXCLUSIVE OR
✓ MODIFIED
– NOT MODIFIED
M7 MEMORY BIT 7
M6 MEMORY BIT 6

OP-CODE TABLE

LSD / MSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LSD / MSD
0	BRK	ORA-IND, X				ORA-Z, Page	ASL-Z,PAGE		PHP	ORA-IMM	ASL-A			ORA-ABS	ASL-ABS		0
1	BPL	ORA-IND, Y				ORA-Z, PageX	ASL-Z,Page,X		CLC	ORA-ABS,Y				ORA-ABS,X	ASL-ABS, X		1
2	JSR	AND-IND,X			BIT-Z,Page	AND-Z, Page	ROL-Z, Page		PLP	AND-IMM	ROL-A		BIT-ABS	AND-ABS	ROL-ABS		2
3	BMI	AND-IND,Y				AND-Z,Page,X	ROL-Z,Page,X		SEC	AND-ABS,Y				AND-ABS,X	ROL-ABS,X		3
4	RTI	EOR-IND,X				EOR-Z, Page	LSR-Z,Page		PHA	EOR-IMM	LSR-A		JMP-ABS	EOR-ABS	LSR-ABS		4
5	BVC	EOR-IND,Y				EOR-Z,Page,X	LSR-Z,Page,X		CLI	EOR-ABS,Y				EOR-ABS, X	LSR-ABS, X		5
6	RTS	ADC-IND, X				ADC-Z, Page			PLA	ADC-IMM			JMP-IND	ADC-ABS			6
7	BVS	ADC-IND, Y				ADC-Z,PageX			SEI	ADC-ABS,Y				ADC-ABS, X			7
8		STA-IND, X			STY-Z. Page	STA-Z. Page	STX-Z. Page		DEY		TXA		STY-ABS	STA-ABS	STX-ABS		8
9	BCC	STA-IND, Y			STY-Z.Page,X	STA-Z.Page,X	STX-Z.Page,Y		TYA	STA-ABS, Y	TXS			STA-ABS, X			9
A	LDY-IMM	LDA-IND, X	LDX-IMM		LDY-Z.Page	LDA-Z. Page	LDX-Z. Page		TAY	LDA-IMM	TAX		LDY-ABS	LDA-ABS	LDX-ABS		A
B	BCS	LDA-IND, Y			LDY-Z.PageX	LDA-Z.Page,X	LDX-Z. PageY		CLV	LDA-ABS, Y	TSX		LDY-ABS, X	LDA-ABS, X	LDX-ABS, Y		B
C	CPY-IMM	CMP-IND, X			CPY-Z.Page	CMP-Z. Page	DEC-Z. Page		INY	CMP-IMM	DEX		CPY-ABS	CMP-ABS	DEC-ABS		C
D	BNE	CMP-IND, Y				CMP-Z.Page,X	DEC-Z.Page,X		CLD	CMP-ABS, Y				CMP-ABS, X	DEC-ABS, X		D
E	CPX-IMM	SBC-IND, X			CPX-Z. Page	SBC-Z. Page	INC-Z. Page		INX	SBC-IMM	NOP		CPX-ABS	SBC-ABS	INC-ABS		E
F	BEQ	SBC-IND , Y				SBC-Z.Page,X	INC-Z.Page,X		SED	SBC-ABS, Y				SBC-ABS, X	INC-ABS, X		F

IMM - IMMEDIATE ADDRESSING – THE OPERAND IS CONTAINED IN THE SECOND BYTE OF THE INSTRUCTION.

ABS - ABSOLUTE ADDRESSING – THE SECOND BYTE OF THE INSTRUCTION CONTAINS THE 8 LOW ORDER BITS OF THE EFFECTIVE ADDRESS. THE THIRD BYTE CONTAINS THE 8 HIGH ORDER BITS OF THE EFFECTIVE ADDRESS.

Z. PAGE- ZERO PAGE ADDRESSING – SECOND BYTE CONTAINS THE 8 LOW ORDER BITS OF THE EFFECTIVE ADDRESS. THE 8 HIGH ORDER BITS ARE ZERO.

A. - ACCUMULATOR – ONE BYTE INSTRUCTION OPERATING ON THE ACCUMULATOR.

Z. PAGE,X - Z. PAGE,Y - ZERO PAGE INDEXED – THE SECOND BYTE OF THE INSTRUCTION IS ADDED TO THE INDEX - (CARRY IS DROPPED) TO FORM THE LOW ORDER BYTE OF THE EA. THE HIGH ORDER BYTE OF THE EA IS ZEROS.

ABS,X ABS,Y ABSOLUTE INDEXED. THE EFFECTIVE ADDRESS IS FORMED BY ADDING THE INDEX TO THE SECOND AND THIRD BYTE OF THE INSTRUCTION.

(IND, X) - INDEXED INDIRECT – THE SECOND BYTE OF THE INSTRUCTION IS ADDED. THE X-INDEX, DISCARDING THE CARRY. THE RESULTS POINTS TO A LOCATION ON PAGE ZERO WHICH CONTAINS THE 8 LOW ORDER BITS OF THE EA, THE NEXT BYTE CONTAINS THE 8 HIGH ORDER BITS.

(IND),Y - INDIRECT INDEXED – THE SECOND BYTE OF THE INSTRUCTION POINTS TO A LOCATION IN PAGE ZERO. THE CONTENTS OF THIS MEMORY LOCATION IS ADDED TO THE Y INDEX, THE RESULT BEING THE LOW ORDER EIGHT BITS OF THE EA. THE CARRY FROM THIS OPERATION IS ADDED TO THE CONTENTS OF THE NEXT PAGE ZERO LOCATION, THE RESULT BEING THE 8 HIGH ORDER BITS OF THE EA.

JOLT Microcomputer Products

ALL JOLT PRODUCTS ARE FULLY WARRANTED, COMPLETELY TESTED AND SHIPPED WITHIN 15 DAYS AFTER RECEIPT OF ORDER

JOLT CPU Card — Includes 8-bit NMOS MOS Technology 6502 CPU, which requires no clock, can directly address 65k of memory, has two index registers, 137 instructions with 11 "true" addressing modes, two interrupts and both single step and address halt capability. JOLT card is small — 4¼" x 7" — and has TTY and RS232C interface. Includes unique software 1k ROM Debugger/Monitor DEMON™, fully documented. DEMON self-adapts to any terminal speed from 10-30 CPS (110 to 300 baud). Allows display and alteration of CPU register **and** memory locations, plus allows read, write and punch of Hex formatted data — with write/punch BNPF format data for PROM programmers. DEMON has unlimited breakpoint capability and separate non-maskable interrupt entry and i.d. External device interrupts can be directed to any location, or can be defaulted to DEMON recognition. DEMON gives you a completely protected ROM resident debug/monitor; capability to begin execution at any location in memory; capability to bypass DEMON entirely to permit full user control over system; a high-speed 8-bit parallel input option; and user callable I/O subroutines. JOLT CPU CARD ALSO INCLUDES . . . fully static 512 bytes of RAM; 64 bytes interrupt vector RAM On-board I/O including TTY 20 ma current loop and RS232C interface, both full duplex; high speed reader interface lines and 24 fully programmable bidirectional I/O lines with full TTL drive and two bit-serial I/O lines. **JOLT INCLUDES SOFTWARE, HARDWARE AND ASSEMBLY MANUALS. AVAILABLE FOR IMMEDIATE SHIPMENT. $159 in kit form . . . $249 assembled.**

JOLT 2K PROM Card — Standard JOLT card size (4¼" x 7") with 8 1702A type sockets for up to 2,048 bytes of ultraviolet erasable PROM memory. On-board jumpers provided for assigning card to any 2K memory address space. Manual included. AVAILABLE FOR IMMEDIATE SHIPMENT. $149 assembled and tested.

JOLT 6502 Resident Assembler Program — One pass Resident Assembler designed for use on JOLT systems equipped with 2K PROM card and at lease 4K bytes of RAM memory. Delivered on 7 1702A PROMs ready to insert into PROM card. Never needs loading, always available, assembles immediately in one *single* pass as statements are entered either from paper tape or directly from terminal keyboard entry. Generates listing, object code placed directly into RAM. AVAILABLE FOR IMMEDIATE DELIVERY. User manual and paper tape editor (on paper tape) included. $395.

JOLT RAM Card — Fully static 4,096 bytes of RAM with 1 microsecond access time and on-board decoding. Hardware and assembly manuals included. AVAILABLE FOR IMMEDIATE SHIPMENT. **$199 kit . . . $285 assembled.**

JOLT I/O Card (Peripheral Interface Adapter) — 2 PIA LSI chips, 32 I/O lines, four interrupt lines, on-board decoding and standard TTL drive. Fully programmable. Manuals included. AVAILABLE FOR IMMEDIATE SHIPMENT. **$96 kit . . . $140 assembled.**

JOLT Power Supply — Operates at +5, +12 and −10 voltages. Supports JOLT CPU, 4k bytes of RAM and JOLT I/O card — or, CPU and 8 I/O cards. Manuals included. AVAILABLE FOR IMMEDIATE SHIPMENT. **$99 kit . $145 assembled.**

JOLT +5V Booster Option — Fits onto JOLT Power Supply card. Supports CPU, 16k bytes of RAM — or, CPU and 8k bytes RAM and 8 I/O cards — or, CPU and 4k bytes RAM and 16 I/O cards. Manuals included. AVAILABLE FOR IMMEDIATE SHIPMENT. **$25.**

JOLT Universal Card — Same size (4¼" x 7"), same form factor as other JOLT cards. Completely blank, drilled to accept 14, 16, 24 or 40 pin sockets. Used for additional user memory or I/O, control panels, TV interfaces, keyboards, LEDs, or other interface logic. **AVAILABLE FOR IMMEDIATE SHIPMENT. $25.**

JOLT Accessory Bag — Contains enough hardware to connect one JOLT card to another. Such necessary items as flat cable, connectors, card spacers, hardware, etc. AVAILABLE FOR IMMEDIATE SHIPMENT. $40.

JOLT Tiny BASIC — A subset of Dartmouth BASIC that resides in 2304 bytes of program memory. Includes LET, IF . . .THEN, INPUT, PRINT, GOTO, GOSUB, RETURN, END, REM, CLEAR, LIST, RUN, and functions RND (Random) and USR (User subroutine) that allows branching to assembly language subroutines with argument passing. User manual included. Available either in paper tape form for $25 or resident on 9 1702A PROMs for $270. (If ordered on PROMs, two 2K PROM Cards are required).

THE JOLT 4K SYSTEM . . . the functional, low-cost JOLT 4k system comes complete with the CPU card , PLUS a 4k read/write RAM memory card, PLUS all the connectors you need to assemble the kit. The price is an **unbelievably low $339.50!** A $383 value. (Add $175 for an assembled 4k system.)

THE POWERED JOLT 4K SYSTEM . . . Complete with a JOLT CPU card, 4k RAM card, JOLT power supply card, plus all the connectors required to put it all together. **The price is very, very low — just $429.50 (a $482 value) for the kit!** (Add $215 if you wish an assembled Powered JOLT 4K System.)

THE JOLT 8K SYSTEM . . . A big system and a bigger value. Includes a CPU card, two 4k RAM memory cards, and all the connectors and hardware required for assembling the kit. **The price is a super low $499.50!** An $582 value. (Add $250 if you wish a pre-assembled JOLT 8K System.)

THE POWERED JOLT 8K SYSTEM . . . A great bargain that — like all other JOLTs — interfaces with your TTY or RS232C terminal. Includes a CPU card, two 4k RAM cards, a JOLT Power Supply, a JOLT +5 Volt Booster, and all the accessories you need to put the cards together. **The price is only $599.50 (a $721 value) for the Powered JOLT 8K System Kit!** (Add $290 for an assembled system.)

JOLT Full Documentation — Due to popular demand we have made all JOLT construction and reference manuals available as a separate item. AVAILABLE NOW. $45.

(Prices subject to change without notice)

JOLT Systems

RAP -- 1.75K Byte Resident Assembler Program

The JOLT Resident Assembler Program (RAP) is designed for use on JOLT systems equipped with at least 4K bytes of RAM memory. RAP has some significant advantages over conventional assemblers:

1. Resident as part of the JOLT system on PROM chips.
   The assembler never has to be read into volatile memory before use. It, just like the DEMON monitor, is instantly available. In addition, costly time sharing services are not needed for cross assemblies.

2. Operates on one pass of the source code.
   The source tape is read in only once, thereby increasing assembler speed by a factor of two over conventional assemblers that make two or three passes over the source code.

3. Small in size.
   The assembler is smaller by a factor of 4 or 5 over comparable assemblers. Its size guarantees the smallest number of PROM chips needed and minimizes printed circuit board space requirements.

With the assembler PROM chips installed in your JOLT PROM board (at address E800 hex), the assembler may be activated by reading the source code input on the console input device and transfering to location E800 hex using the DEMON monitor.

As source code is being read in, a listing is produced on the console printer and the object code is generated directly into RAM at the addresses specified by the origin directive (.ORG). After the assembly is complete, the object code may be punched onto paper tape or executed directly using DEMON.

The assembler assumes RAM at locations 1FFF hex and lower to be available for symbol table usage. RAP uses an efficient symbol table algorithm and users can normally expect that about 4 to 6 bytes of RAM will be used for each symbol or that a 3000 byte program would use approximately 800 bytes for the entire symbol table (locations 1CE0 to 1FFF hex). This space need not be left unused if buffers, etc. are allocated to it.

The Resident Assembler Program is compatible with the MOS Technology Cross Assembler with the following exceptions:

1. Expressions and * (used for current program counter) are not allowed.
2. The .OPT and .PAGE pseudo operations are not implemented.
3. Octal and binary numbers are not implemented.
4. .ORG is used instead of *= to origin program.
5. .RES is used for reserving storage.

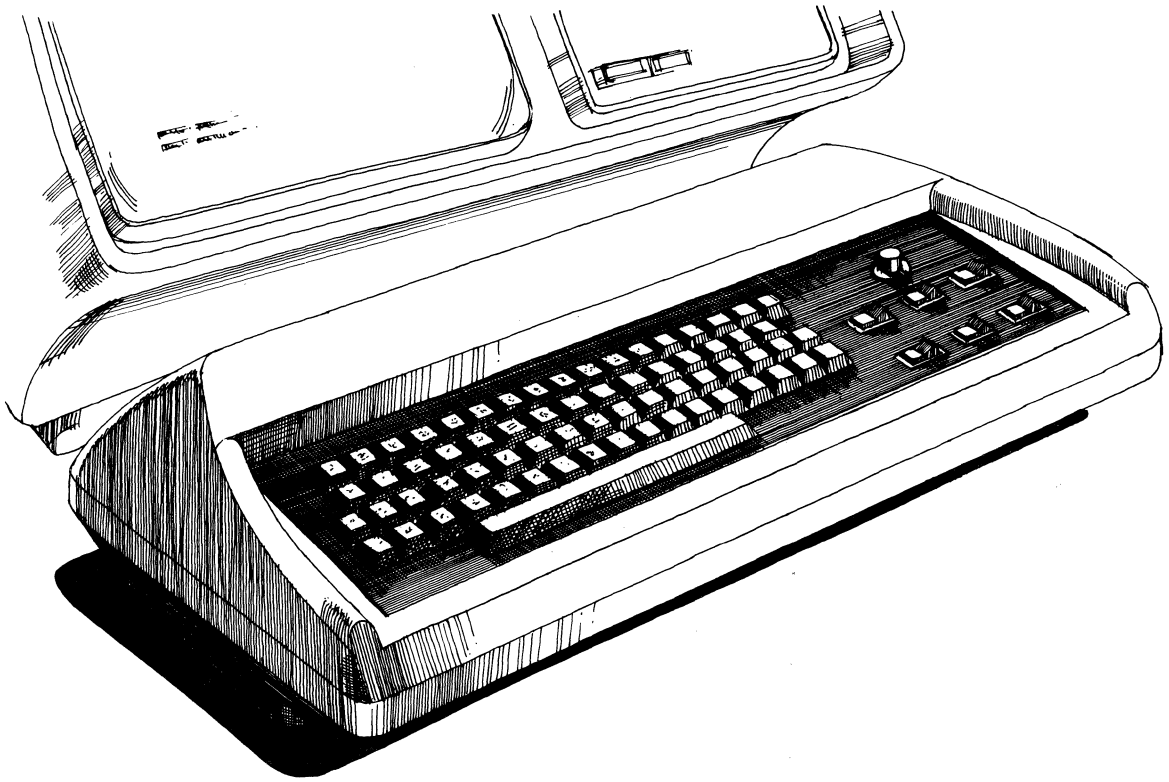
```
 *  7052 31 C0 FF 01 FF          Appendix B Revised  May 14, 1976
.:  E800
.G

                    ;       JOLT RESIDENT ASSEMBLER EXAMPLE
                    ;       ORG PSEUDO OPERATION
0000                        .ORG  $1F
001F                Z       .RES  0
001F                        .ORG  $1000
                    ;       IMMEDIATE OPERAND TYPES
1000  A9 2A        ABS     LDA  #42       ;DECIMAL
1002  69 2A                ADC  #$2A      ; HEX
1004  69 2A                ADC  #'*       ; ASCII
                    ;       ABSOLUTE OPERAND TYPES
1006  6D 0010              ADC  ABS       ; ABSOLUTE
1009  7D 0010              ADC  ABS,X     ; ABSOLUTE,X
100C  79 0010              ADC  ABS,Y     ; ABSOLUTE,Y
                    ;       INDIRECT OPERAND TYPES
100F  61 1F                ADC  (Z,X)     ; INDIRECT,X
1011  71 1F                ADC  (Z),Y     ; INDIRECT,Y
                    ;       ZERO PAGE OPERAND TYPES
1013  65 1F                ADC  Z         ; ZERO PAGE
1015  75 1F                ADC  Z,X       ; ZERO PAGE,X
                    ;       OTHER OPERAND TYPES
1017  0A                   ASL  A         ; ACCUMULATOR
1018  60            BACK    RTS            ; IMPLIED
                    ;       BRANCHES
1019  D0 FD                BNE  BACK      ; BACKWARD
101B  D0 00                BNE  FORWARD ; FORWARD
                    ;       JUMPS
101D  CA            FORWARD  DEX
101E  4C 1810              JMP  BACK      ; ABSOLUTE
1021  6C 0010              JMP   (ABS)  ;INDDREECT
                    ;       FORWARD REFERANCES
1024  0210                 .WORD FOR1
                    ;       UNDEFINED REFERANCE
1026  0210          FOR1    .WORD UNDEFINED
                    ;       PSEUDO OPERATIONS
1028                        .RES  4                      ; RESERVE STORAGE
102C  050F1F                .BYTE 5,$F,Z,'STRING'        ; DEFINE BYTES
1035                TEN     =     10                     ; EQUATE
1035  0A00CD                .WORD TEN,$ABCD,6500,256  ; DEFINE WORDS
                    ;       ERRORS
103D  C6 1F    M TEN        DEC  Z         ; MULTIPLY DEFINED SYMBOL
103F  71 00    S            ADC  (ABS),Y ; OPERAND SIZE TOO LARGE
1041  DA 0010  O            DEC  ABS,Y   ; IMPROPER OPERAND FIELD
1044  00       U            DCC  Z         ; IMPROPER OPERATION CODE
1045  D0 D8    R            BNE  Z         ; BRANCH OUT OF RANGE
                    ;       THE SYMBOL TABLE WILL BE PRINTED AFTER
                    ;       THE END PSEUDO OPERATION.
                    ;       THE LOCATION OR VALUE OF THE SYMBOL IS
                    ;       PRINTED FOLLOWED BY THE SYMBOL NAME.
1047                        .END
  1000  ABS
  1018  BACK
  101D  FORWARD
  1026  FOR1
  000A  TEN
1026  UNDEFINED
  001F  Z


 *  EE13 32 00 00 00 F3
.WH 1000 1046
;181000A92A692A692A6D00107D00107900106 11F711F651F751F0A05E6
;18101860D0FDD000CA4C18106C00102610021010 54FE70050F1F530797
;171030545249 4E470A00CDAB64190001C61F7100DA001000D0D807C3
.
```

VT 100
Video Terminal
Product Specification

MICROCOMPUTER ASSOCIATES INC.
2589 SCOTT BLVD. SANTA CLARA, CA 95050
TELEPHONE (408) 247-8940



FEATURES

- Standard RS 232 and 20 ma current loop interface
- ASCII keyboard input
- Video output
- 32 character x 16 line display
- 5 x 7 Character font
- Upper/lower case
- Eight cursor controls and bell
- Crystal controlled baud rates up to 9600
- Full duplex
- Standard with 2 pages, 512 chars/page
- Up to 16 pages of screen memory
- Auto/manual readback of screen memory
- Transmit/store control character switch

APPLICATIONS

- Standard low cost, general purpose terminal
- Teletypewriter replacement
- Development systems
- Hobby computers
- Timesharing terminal
- In-house computer systems
- Microcomputer Kits
- Dedicated Systems
- Industrial and process controllers
- Communications
- Instrumentation
- Local editing system
- Educational systems

TECHNICAL SPECIFICATIONS

The **VT100 Video Terminal** allows the user to communicate with most computers. The standard interface includes an **RS232 connection** as well as a **20 ma current loop.** Local **screen memory with readback** provides an added feature for all systems. The VT100 is a cost effective means for entering and retrieving data from any system.

KEYBOARD INPUT

A **full typewriter-like keyboard** with quality, easy-to-depress keys provides the standard ASCII character set including upper and lower case alphabetics. Two key roll-over enhances ease of operation. Switches include LOCAL/LINE, LINE TRUNCATION (ON/OFF), READBACK (START/STOP), TRANSMIT CONTROL CHARACTER (ON/OFF), and STORE RECEIVING CONTROL CHARACTER (ON/OFF). A rotary switch selects baud rates up to 9600

SCREEN OUTPUT

Video composite output allows easy connection to a standard monitor, R. F. converter, or the video section of a standard home television.

TERMINAL I/O

Two industry standard interfaces permit simple and easy connections to most existing computer systems. These are (1) an RS 232 voltage interface and (2) a 20 ma current loop teletypewriter interface. Both are readily accessible on the rear panel.

SCREEN MEMORY

A **32 character x 16 line screen** (page) makes viewing easy and comfortable. The standard unit comes with 2 pages of memory (1024 characters) expandable to 16 pages.

READBACK

The readback feature allows the user to **read all or part of the screen memory** to his terminal output line (RS232 or 20 ma current). This allows a user to transfer data to the terminal, modify the data using cursor control commands and then read the data back to the main computer system. The readback feature also allows the VT100 to perform **local editing** without tieing up the main computer system.

CURSOR CONTROLS

Eight cursor controls are available via the keyboard. These are Advance (move right), Backspace (move left), Up, Down (line feed), Carriage Return, Home (move to upper left of screen), Erase Screen, Page Advance (automatic at end of previous page).

OTHER FEATURES

A **local line switch** allows local entry of data before transferring to the main system using the Readback mode. A speaker is used to respond to the **Bell control command.**

READY TO USE

The VT100 is **assembled and tested** and warranted to meet all specifications over the commercial temperature range. Full documentation is provided.

VT-200

The VT-200 not only has all the features of the VT-100 but includes a resident 6502 microcomputer system, a resident debug/monitor, resident assembler, resident TINY BASIC and 1K x 8 of random access memory (RAM). This addition allows the VT-200 to become the most powerful compact terminal system available today. For more detailed information on the VT-200 contact Microcomputer Associates.

```
10 REM DISPLAY 64 RANDOM NUMBERS
20 REM  < 100 ON 8 LINES
30 LET I=0
40 PRINT RND (100)
50 LET I=I+1
60 IF I/8*8=I THEN PRINT
70 IF I<64 THEN GOTO 40
80 END

100 REM PRINT HEX MEMORY DUMP
109 REM INITIALIZE
110 A=-10
120 B=-11
130 C=-12
140 D=-13
150 E=-14
```

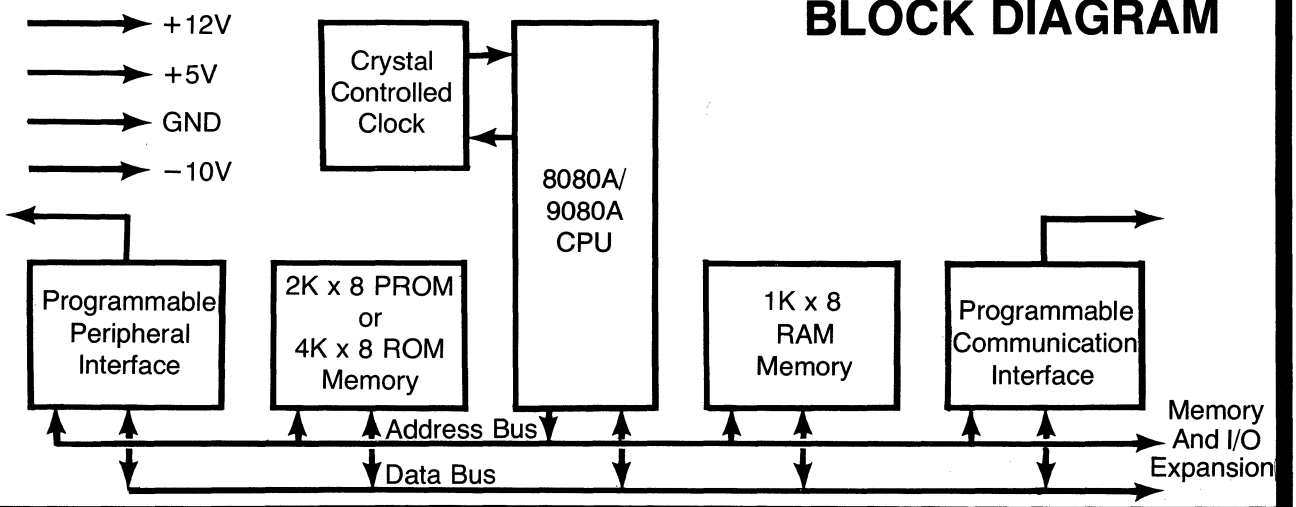
```
    I  SALES
30M I  FORECAST
    I                    XX
    I                    XX
    I              XX    XX
20M I              XX    XX
    I              XX XX XX
    I        XX    XX XX XX
    I        XX    XX XX XX    XX
10M I        XX    XX XX XX    XX
    I  XX    XX    XX XX XX    XX
    I  XX    XX    XX XX XX    XX
    I  XX    XX    XX XX XX    XX
    I  XX    XX    XX XX XX    XX
 0  ----------------------------
_      75  76  77  78  79  80
```

8080A/9080A SYSTEM CARD PRODUCT SPECIFICATION

MICROCOMPUTER ASSOCIATES INC.
2589 SCOTT BLVD. SANTA CLARA, CA 95050
TELEPHONE (408) 247-8940

Microcomputer Associates Inc.'s 8080A/9080A system card is the smallest, most powerful 8080A/9080A microcomputer-based system card available on today's OEM market. A full set of additional boards such as RAM cards, PROM cards, I/O cards and power supplies, allow the system card user to tailor a system to his specific needs. The availability of software for this popular microprocessor makes the MAI system card one of the most cost effective solutions to a designer's microprocessor problem.

BLOCK DIAGRAM



FEATURES

- 8 Bit N-Channel CPU
- Crystal Controlled Clock
- 1K x 8 Static RAM
- 2K x 8 PROM Sockets or 4K x 8 Mask ROM
- Programmable Peripheral Interface
- Asynchronous/Synchronous Receiver Transmitter
- +12, +5, −10 Volt Operation (−5 V optional)
- 24 Bidirectional I/O Lines
- DMA Capability
- Interrupt Capability
- 0°C to 70°C Operation
- Compact 4.25" x 7" Card Size
- Fully Assembled and Tested

APPLICATIONS

- Industrial Process Controllers
- Stand Alone Microcomputer Systems
- Intelligent Terminals
- Data Communications
- Business Systems
- Programmable Calculators
- Video Controllers
- Semiconductor Test Systems
- "Smart" Controllers
- Medical Instrumentation
- Traffic Light Controllers
- Video Games
- Intelligent Instrumentation

TECHNICAL SPECIFICATIONS

MICROPROCESSOR

The **8080A/9080A** microprocessor is an **8 BIT PARALLEL PROCESSOR** unit. A sixteen bit program counter allows for direct addressing of up to 64K bytes of memory. Six general purpose registers and an accumulator, coupled with a powerful instruction set offers high software performance. The ability to provide priority vectored interrupts, binary, decimal, and double precision arithmetic, and a sixteen bit stack pointer gives the entire system true computing power. A **two microsecond cycle time** allows high performance capability.

ON BOARD CLOCK GENERATOR

A crystal controlled on-board clock provides the complete timing generation for the 8080A/9080A card. **Automatic power on reset** is provided to the CPU, as well as the entire system. Timing signals are generated for system synchronization.

PROGRAM MEMORY

Two sockets are available for two 8708 **1024 x 8 U.V. erasable PROMS.** A pin for pin mask programmed ROM, the 8308 is also available for large volume production runs where the 8708 is initially used. On board jumpers allow the same sockets to accept the AM9216 **2048 x 8 mask ROM** for a total of 4096 bytes of program memory. Program memory is expandable through a system connector.

RAM MEMORY

Standard with all cards are **1024 bytes of fully static random access memory.** The configuration addresses the RAM at low memory, however, an on board jumper allows the RAM to be placed in at upper memory for larger systems. RAM memory is expandable through the systems connector.

PARALLEL INPUT/OUTPUT

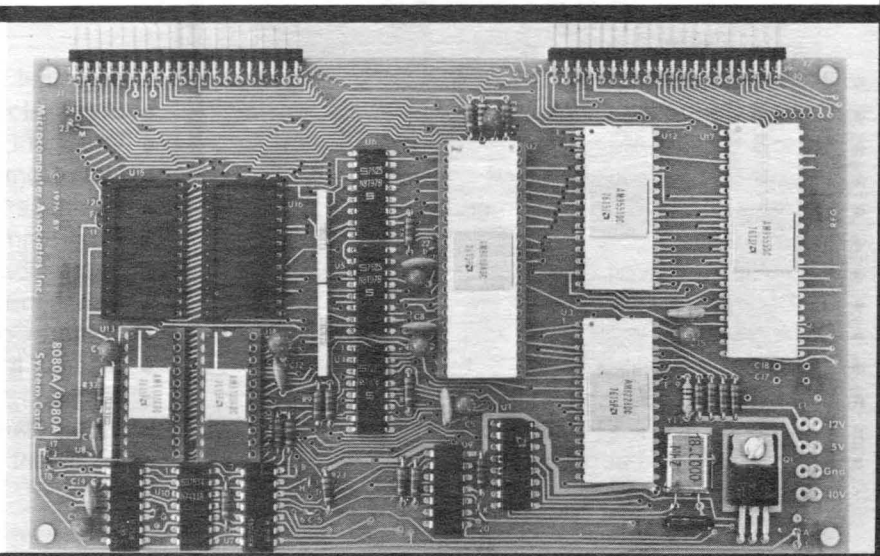
24 programmable I/O lines are available each individually software programmed in two groups of twelve. Direct bit set/reset capability eases control of interface. Completely TTL compatible INPUTS and OUTPUTS with drive currents of 2 mA. Parallel I/O lines are available on the I/O connector.

SERIAL INPUT/OUTPUT

A programmable communications interface chip provides both **synchronous and asynchronous serial modes of operation.** In the synchronous mode the device offers 5-8 bit characters, internal or external synchronization, and automatic sync insertion. In the asynchronous mode the device offers a selectable clock rate of 1, 16, or 64 times the baud rate, 1, 1½ or 2 stop bits, and false start bit detection. Baud rates of 56K in synchrous mode and 9.6K baud in asynchronous are possible. Baud rate clock must be provided external to card. Error detection of parity, overrun, and framing, as well as a fully duplex, double buffered receiver and transmitter are provided. Modem controls such as data set ready, data terminal ready, request to send, clear to send, are provided, as well as transmitter ready and receiver ready.

READY TO USE

All 8080A/9080A system cards are **assembled and tested**, and warranted to meet all specifications over the commercial temperature range (0°C to 70°C). Full documentation is provided.



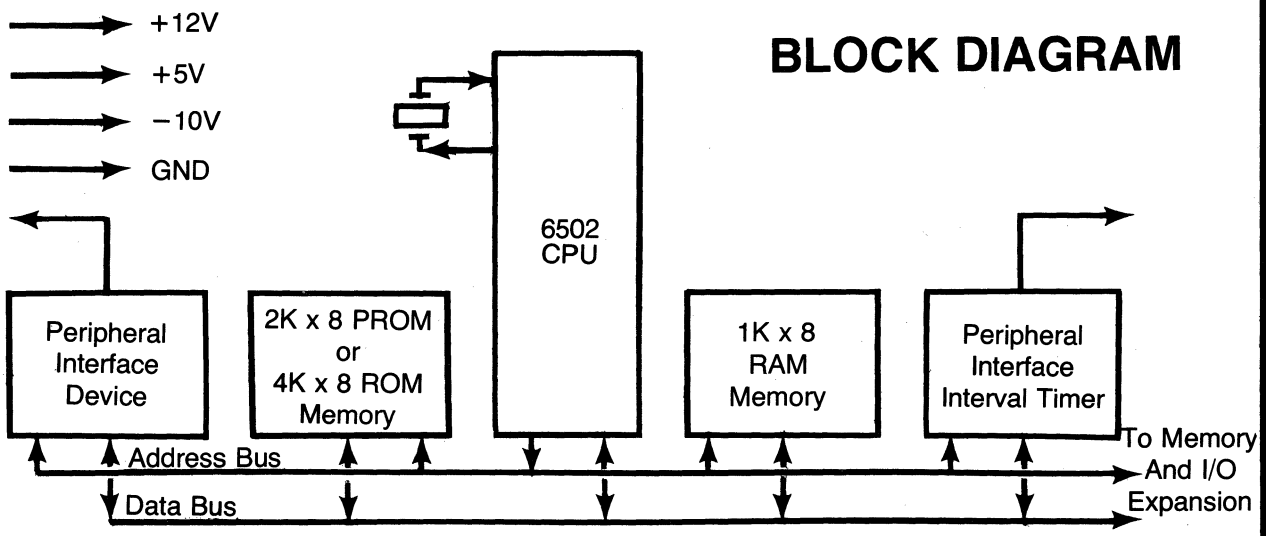
WRITE FOR VOLUME AND OEM DISCOUNTS

6502 SYSTEM CARD
PRODUCT SPECIFICATION

MICROCOMPUTER ASSOCIATES INC.
2589 SCOTT BLVD. SANTA CLARA, CA 95050
TELEPHONE (408) 247-8940

Microcomputer Associates Inc.'s 6502 System Card is the smallest most powerful 6502 microcomputer-based system card for the OEM market. A broad variety of additional boards, such as RAM cards, PROM cards, I/O cards, and power supply cards, all system compatible, allow the user to tailor a system to his specific needs. The 6502's powerful and versatile instruction set makes the MAI System Card one of the most cost effective solutions to a designer's microprocessor problem.

BLOCK DIAGRAM



FEATURES

- 8 Bit N-Channel CPU
- Crystal Controlled Clock
- 1K x 8 Static RAM
- 2K x 8 PROM Sockets or 4K x 8 Mask ROM
- Programmable Peripheral Interfaces
- Internal Timer
- +12, +5, −10 Volt Operation (−5V Optional)
- 32 Bi-directional I/O Lines
- DMA Capability
- Interrupt Capability
- 0°C to 70°C Operation
- Compact 4.25" x 7" Card Size
- Fully Assembled and Tested

APPLICATIONS

- Industrial Process Controllers
- Stand Alone Microcomputer Systems
- Intelligent Terminals
- Data Communications
- Business Systems
- Programmable Calculators
- Video Controllers
- Semiconductor Test Systems
- "Smart Controllers
- Medical Instrumentation
- Traffic Light Controllers
- Video Games
- Intelligent Instrumentation

TECHNICAL SPECIFICATIONS

MICROPROCESSOR

The 6502 microprocessor is an **8 Bit Parallel Processor** unit. A sixteen bit address bus allow addressing of up to 64K bytes of memory or I/O. The device has an **on chip oscillator**/buffer providing a two phase clock for the processor and system. An I/O oriented bus and register structure, coupled with a versatile instruction set offers high software performance. Two single level interrupts, DMA capability, a sixteen bit stack pointer and a peripheral oriented bus gives the entire system flexible computing power.

PROGRAM MEMORY

Two sockets are available for two 8708 **1024 x 8 U.V. erasable PROMS.** A pin for pin mask programmed ROM, the 8308 is also available for large volume production runs where the 8708 is initially used. On board jumpers allow the same sockets to accept the AM9216 **2048 x 8 mask ROM** for a total of 4096 bytes of program memory. Program memory is expandable through the system connector.

RAM MEMORY

Standard with all cards are **1024 bytes of fully static random access memory.** The configuration addresses the RAM at low memory, however, an on board jumper allows the RAM to be placed in at upper memory for larger systems. RAM memory is expandable through the systems connector.

PARALLEL INPUT/OUTPUT

32 parallel I/O lines are available for user interfaces. 16 lines originate from a 6820 I/O chip and 16 lines from a 6530 chip. Both devices connect to the main system data bus providing a flexible programmable interface. The 6820/6520 contains programmable data direction registers, two programmable control registers and four individually controlled interrupt lines. The 6530 also contains two programmable data direction registers allowing individual control for each I/O line. CMOS compatible outputs allow easy peripheral interfacing.

INTERVAL TIMER

The 6530 provides a software programmable interval timer capable of timing in various intervals from 1 to 262,144 clock periods. The timer contains three basic parts: a divide down register, programmable 8-bit register and flag logic. The interval timer can be programmed to count to 256 time intervals, each time interval can be either 1T, 8T, 64T or 1024T increments (T=system clock periods). When full count is reached the flag is set and can be tested with a read timer instruction.

READY TO USE

All 6502 system cards are **assembled and tested**, and warranted to meet all specifications over the commercial temperature range (0°C to 70°C). Full documentation is provided.

Your local representative

WRITE FOR VOLUME AND OEM DISCOUNTS

GENERAL INFORMATION

MAI was founded in April 1974. Since its inception, MAI has become the most diversified and versatile microcomputer company today. In its second year of operation, MAI has proven its capabilities in areas such as hardware and software design, manufacturing of standard and custom products, component and literature distribution, educational workshops and seminars, and publishers of the only total microcomputer news source, the MICROCOMPUTER DIGEST.

MANUFACTURING

MAI is dedicated to producing high quality, functional microcomputer boards and systems. These include special and custom designs as well as MAI's own standard products. MAI specializes in delivering tested, ready to use microcomputer systems, including all software.

DISTRIBUTION

In support of its manufacturing activities, MAI buys in large volumes and passes this savings on to its customers. MAI stocks or can acquire most microprocessor and microprocessor-related components. MAI also carries literature from participating major microprocessor manufacturers as well as most related books and material.

SOFTWARE

MAI is skilled in programming all major microprocessors. Its technical staff has performed application tasks from data acquisition and special monitor programs to development software and higher level languages. The ability to tradeoff software and hardware into a cost effective system is MAI's speciality.

HARDWARE

MAI designs hardware relating to all aspects of a microcomputer system, from CPU and memory cards to special I/O interfaces related to your application.

WORKSHOPS AND SEMINARS

MAI has conducted over 150 public and inhouse microcomputer courses including 4004, 8008, 8080 and PL/M workshops for the Intel Corp., as well as world-wide courses as faculty members of Integrated Computer Systems International. MAI has also presented many customized, on-site workshops and seminars that have spanned from a general introduction to microprocessors to presenting specific inhouse designs. MAI will be pleased to work with you to identify a suitable course outline.

MICROCOMPUTER DIGEST

In addition to providing the above technical microcomputer design and manufacturing services, Microcomputer Associates publishes monthly the MICROCOMPUTER DIGEST. This publication summarizes all activities in the microcomputer area, including foreign and domestic microcomputer developments, applications, main frame and peripheral product announcements, hardware and software design techniques, industry trends and predictions, literature reviews and interviews with notable personalities in the microcomputer industry.

Each quarter a supplementary REFERENCE INDEX is also mailed to Microcomputer Digest subscribers. This index includes a complete bibliography of all microcomputer related material during that quarter that has appeared in print, as well as a listing of microcomputer manufacturers and service organizations.

Once a year, the ANNUAL INDEX classifies and lists all articles printed in the Digest over the previous twelve month period.

Microcomputer Digest is distributed worldwide.

LATE PAYMENT PENALTY

All invoices not paid within 45 days of the invoice date are considered "overdue." The following penalties automatically occur on an overdue account.

1. All discounts on that invoice are voided. A new invoice for the amount of the discounts will be issued. The original invoice remains due and payable in full.
2. The amount of an overdue invoice shall not be included in any later computation of "Accumulated Dollar Schedule."
3. Future orders from the customer will be accepted only on a C.O.D. or cash with order basis until credit is reestablished to MAI's satisfaction.

TERMS

1. 2% 10 Days, Net 30 Days, FOB Santa Clara, CA 95050.
2. All orders subject to credit verification.
3. Discounts voided on invoices not paid in 45 days.
4. International orders must be prepaid or preceded by an irrevocable letter of credit. Minimum international order: $300.
5. All pricing, including volume, OEM and discounts, is established by Microcomputer Associates Inc. and is subject to change without notice.

VOLUME AND OEM PRICING

Microcomputer Associates Inc. quotes quantity orders for its products on the basis of customer product configuration, total quantities and delivery schedule. These quotations provide firm prices for up to 18 months. To qualify for factory quoted volume or OEM pricing an order must be for at least 50 units of one microprocessor system over a 12 month period or have a total list price value exceeding $25,000. Orders not meeting one of these qualifications will be priced according to the latest published price list and the dollar volume discount schedule.

BASE PRICE

The price basis for an order made under this policy is the published Price List in effect at the time a particular order is placed.

Microcomputer Associates Inc.

Manny R. Lemas
President

Ray M. Holt
Vice-President

NEWS

SUPER JOLT - A SUPER COMPACT SINGLE BOARD COMPUTER FEATURING OVER 5000 BYTES OF RESIDENT SYSTEM SOFTWARE.

Santa Clara, CA..... Microcomputer Associates Inc. has begun shipments of the SUPER JOLT card, the latest addition to their JOLT family of microcomputer card modules. SUPER JOLT, the most compact single board computer available, measures a mere 4¼" by 7" and contains the 8 bit 6502 microprocessor, 1,024 bytes static RAM, 32 bidirectional and programmable I/O lines, a 1 megahertz crystal controlled clock, an interval timer, 4 interrupts including a timer interrupt and a non-maskable interrupt, three serial interfaces: 20 ma current loop, RS232 and TTL, as well as 5,120 bytes of resident ROM program memory that includes a complete single pass Resident Assembler Program called RAP, a resident TINY BASIC interpretive language designed especially for JOLT systems and the 1,024 byte DEMON DEbug MONitor program.

The incredibly compact SUPER JOLT with its Resident Assembler Program can function as a single card development system permitting assemblies to be made with only a single pass of a source program from a terminal or via a TTY paper tape reader. Following

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assembly, the programs can be debugged using the debugging facilities of the DEMON DEbug MONitor program.

For those who prefer to use a higher level language, a subset of Dartmouth BASIC called TINY BASIC is available on board, which permits immediate entry and execution of TINY BASIC language programs. The ROM software has been designed so that most any I/O devices can be used.

By removing the RAP and TINY BASIC ROMs, the SUPER JOLT card becomes a compact general purpose microcomputer card suitable for any dedicated application. The vacated ROM sockets may be used for the user's programmed ROMs or for the user's programmed 2708 type PROMs.

Ray M. Holt, Executive Vice President of Microcomputer Associates and designer of the JOLT line of microcomputer products, states that "SUPER JOLT is certainly our best product to date. The card is intended principally for the industrial market, but will also attract the growing computer hobbiest market by providing a resident user oriented language in the form of TINY BASIC. Buffering for all address and data lines provides easy expansion to additional card modules."

Manny R. Lemas, MAI President added "With SUPER JOLT we've succeeded once again in providing the maximum amount of usable microcomputer product in the least amount of space. The most important feature of any microcomputer product is how easy is it to use. SUPER JOLT features over 5K of resident system software

including debugger, symbolic assembler and standard higher level language. Its a development system, prototyping system, a dedicated applications card, and a computer hobbiest's delight all rolled into one. It's, well in a word, it's SUPER."

SUPER JOLT is further supported by a complete family of existing JOLT card modules including 4K RAM, 2K 1702A PROM, Input/ Output, Power supply and Universal Card. A five slot card cage and an 8080 CPU card module substitute are also available. Soon to be announced are the A/D, D/A card and the cassette interface card.

Single unit pricing for the SUPER JOLT card, fully assembled and tested is $375 without RAP and TINY BASIC ROMs, and $575 with the ROMs. Quantity discounts are also available. Prices of other JOLT cards, in kit form begin as low as $96.

In the U.S. and Canada, JOLT products are available directly from Microcomputer Associates Inc. as well as participating computer stores and James Electronics. JOLT products are also distributed off shore in Japan, Australia, Taiwan, Great Britain, Spain, France, West Germany and the Netherlands.

For further information contact:

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