XCELL

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XILINX®
The Programmable Logic Company℠

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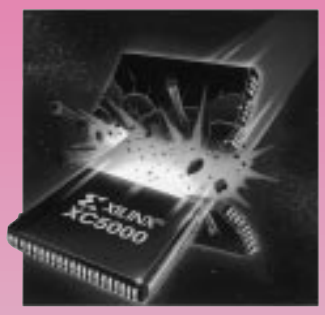

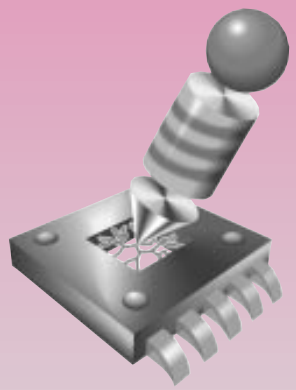

XSACETP is Coming!

Powerful new features such as the Floorplanner make the latest release of the XACT Development System a revolutionary combination of power and ease-of-use...

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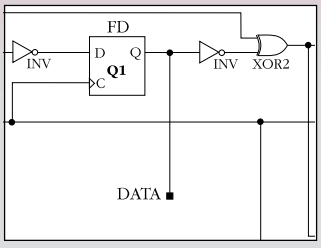
DESIGN TIPS & HINTS



Manchester Decoder

A high-speed, efficient serial decoder using Xilinx FPGAs uses eight-times oversampling to ensure fast and accurate interpretation of Manchester-encoded data...

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Total Cost and Time-to-Volume: The New Reality

By BRADLY FAWCETT ◆ Editor

While designers value the flexibility and convenience of a user-programmable device, the programmable elements and their associated control logic do exact a price in terms of silicon area. Thus, programmable devices generally cost more, on a per-piece basis, than equivalent-density custom and semi-custom ICs, such as masked gate arrays (although this gap is closing).

The choice between a high-density programmable device (an EPLD or FPGA) and a gate array often comes down to simple economics — designers want to use whichever one is most cost-effective for the application. However, determining the true "total cost" of a given technology in a given application is not at all a simple matter. If such an analysis includes only a comparison of unit prices at a given volume, the "break-even" point between FPGAs and gate arrays typically will be only a few hundred to a few thousand pieces — even if the extra NRE (non-recurring charges) associated with semicustom devices are amortized into the gate array price. But such an analysis falls far short of revealing the true cost of the respective technologies.

> *"...determining the true "total cost" of a given technology in a given application is not at all a simple matter"*

Many other factors affect technology costs. These include development tool costs, inventory costs, quality, vendor service, future component price reductions, design / market risks (i.e., will the design need to be modified after production shipments begin), and the potential for extra engineering and NRE costs due to design re-spins. Many of these costs can go unrecognized in a traditional cost analysis because they occur after the design cycle, or cut across many functional groups.

However, out of all the factors involved (including component costs), the two factors that tend to most heavily weight the programmable device vs. gate array cost analysis are engineering costs and time-to-market. In a typical scenario, studies suggest that these factors can move the "break-even point" between FPGAs and gate arrays to tens or even hundreds of thousands of units.

These factors are directly related. Engineering costs are higher and design cycles longer due to the extra steps required in semicustom IC development, especially exhaustive simulation and test vector generation. This, combined with the significantly longer lead times required to produce prototypes and production quantities of gate arrays, can significantly increase the time-to-market for that product, as compared to a programmable solution. As many studies have shown, in today's environment, even a small delay in time-to-market can have a significant

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GUEST EDITORIAL

The Xilinx-Neocad Merger

by CURT WOZNIAK ◆ President and Chief Operating Officer

The continued growth of the high-density, high-performance programmable logic market is increasingly dependent upon the capabilities of the development software. While continuing our efforts to make programmable logic devices faster, denser and less expensive, we also realize that the design software needs to be easier to use, must provide more powerful design and debug capabilities, and should be supplied to users in advance of device availability.

To help in the continuing efforts to achieve these goals, Xilinx recently announced the acquisition of NeoCAD, Inc., a developer of high-performance design software for FPGAs. Combining our strength in FPGA and EPLD programmable logic devices and process technologies with NeoCAD's advanced FPGA software technology, this merger will provide Xilinx users with access to even more powerful FPGA software design solutions. It is clear that NeoCAD can provide innovative technology that will accelerate software and hardware development efforts in order to keep pace with user demands. This increased capability will allow us to significantly enhance our industry-leading FPGA and EPLD solutions and bring new solutions to market more quickly.

We now face the challenge of combining the best of both the Xilinx and NeoCAD development system technologies. The next development system release from Xilinx and NeoCAD, XACT*step*, version 6, and NeoCAD Foundry V7.0, respectively, will ship as planned. We will continue to support all Xilinx and NeoCAD users with active software maintenance agreements. Migration paths to allow current NeoCAD users access to the XACT solution and XACT users access to the NeoCAD software will soon be established. *(See related article, page 21.)*

NeoCAD software will continue to be supported out of Boulder, Colorado. The former NeoCAD research and development team will remain in Boulder and comprise the nucleus of the Xilinx Boulder research and development site.

NeoCAD's software technology will be merged into future XACT releases to provide a flexible, technology-independent methodology that enables us to quickly support current and emerging architectures. Equally important, the NeoCAD FPGA technology evaluation capability, whereby users can perform "what if" scenarios and select the optimum device based on their cost, speed and density requirements, will also be incorporated within the XACT*step* software system. The development team in Boulder will develop software jointly with other Xilinx development teams worldwide; we will leverage this team's expertise and experience, and anticipate that they will take a leadership role in driving our overall software direction.

Programmable logic users demand a wide range of architectures and programming technologies to satisfy their product needs, and software is a key enabler in this regard. This merger underscores our continued commitment to provide a diverse suite of programmable logic solutions. Our vision of the Xilinx-NeoCAD merger is that we can combine the best aspects of our technologies and the talents of our employees to achieve a design system for our users that is the absolute best in the industry. **This is the vision on which Xilinx was founded.** ◆

NeoCAD INC

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impact on the overall profitability of a product. A late project's "total cost" will often be substantially higher than that of a project completed quickly.

Yet, it may be more accurate to think in terms of time-to-volume, rather than just time-to-market. Time-to-volume is a new term that reflects a product's total life cycle needs. The key is not only to get the product to market, but to quickly and seamlessly achieve required volume production price points. This is one of the key philosophies behind the Xilinx HardWire product line. FPGA devices can be used for development, debugging, prototyping, and initial production, thus speeding time-to-market. In higher volume, they can be directly replaced by less-expensive, mask-programmed HardWire devices, with no redesign effort or risk; engineering resources are free to move on to the development of the next product.

Improving time-to-volume is the major thrust of the upcoming XACT*step*, version 6 development system release. The focus is on accelerating all phases of the product development flow: design entry, design implementation (for the programmable logic), printed circuit board design, design debug, and product production. *(See related article on pages 17-18.)* Special attention has been paid to the often-overlooked design debug stage; surveys indicate that more than 50 percent of a designer's time is spent in design debug and change. So look for improved floorplanning tools and re-entrant "guide" options in PPR — to help ease the absorption of design changes late in the development cycle — and improved timing analysis and hardware debugging tools. Our goal is to provide the tools and technologies that will boost your productivity, reduce your total cost and shorten your time-to-volume. ◆

Xilinx ASIC Estimator Available for PC

Calculate the total cost of your project using Xilinx FPGAs, FPGAs and Xilinx HardWire gate arrays, or traditional mask-programmed ASICs. The Xilinx ASIC Estimator operates on IBM-compatible computers and allows you to enter your own specific costs. Download it via the Internet at `ftp://www.xilinx.com/pub/utilities`. The directory contains a `readme.est` file and the executable `estimate.exe`. You may also contact your local Xilinx sales representative for a floppy disk copy. ◆

FINANCIAL REPORT

Record Revenue in Fiscal Year 1995

Xilinx again achieved record revenues in fiscal year 1995 (April 1994-March 1995), reflecting the strength of our product line and the continued expansion of the programmable logic market. Fiscal 1995 revenues totaled $355.1 million, an increase of 38 percent over fiscal 1994.

For the fourth quarter (ending March 31, 1995), revenues reached a record $109.2 million, an increase of 45 percent from the same quarter one year earlier and up 20 percent from the immediately preceding quarter. This revenue growth was driven by continued demand for the high-speed XC3100, XC3100A and richly-featured XC4000 FPGA families, along with record revenues for custom HardWire devices. International revenues increased 49 percent from the preceding quarter, contributing more than 30 percent of total revenues.

"Xilinx is well-positioned as we enter fiscal 1996. We intend to double our number of architecture offerings and, with the NeoCAD union, we will be able to provide more powerful software solutions," noted Bernie Vonderschmitt, Xilinx CEO. "Looking forward, we remain optimistic about the overall growth of the high-density programmable logic market and our position within this market."

Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX. ◆

155 Mbit/s Codec Uses Xilinx FPGAs

UNIVERSITY OF SOUTH AUSTRALIA

The Satellite Communications Research Centre (SCRC) of the University of South Australia in Adelaide is a space industry development center sponsored by the Australian Space Office.

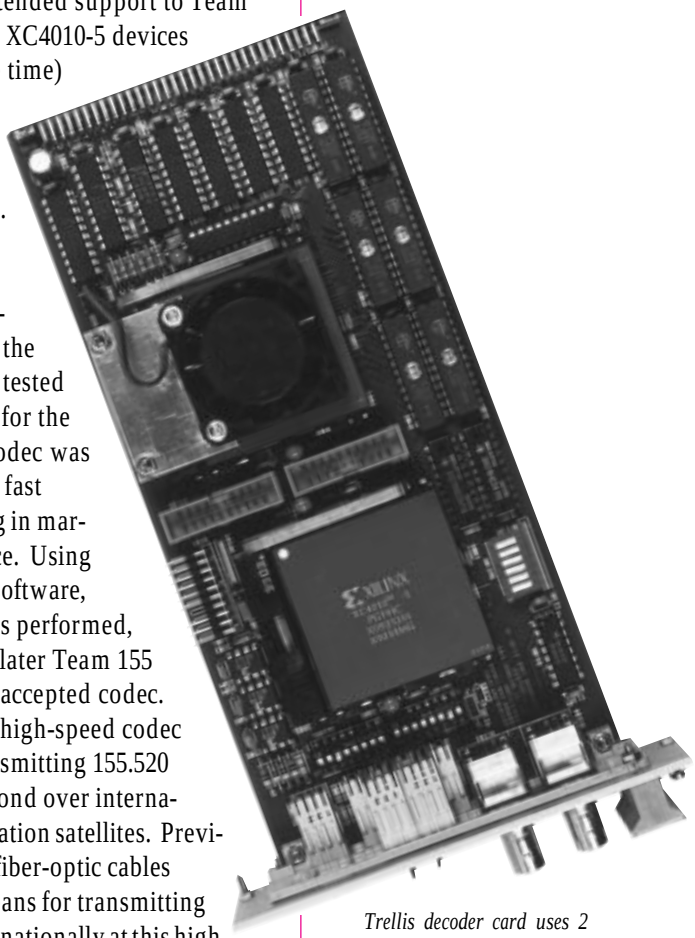
In May of 1992, the SCRC secured a contract from Intelsat to build a 155 Mbit/s codec in a worldwide competitive bid. Intelsat is the world's largest commercial satellite communications service provider, owned by 120 member nations. The 155 Mbit/s codec was the first major high technology research and development contract awarded to an Australian institution.

The task was to develop and prototype a forward error correcting codec that would allow transmission of the standard 155.52 Mbit/s broadband ISDN data rate over a 72 MHz satellite transponder. The use of Xilinx FPGA technology was key to successfully implementing the codec.

After getting the contract, a group of six engineers, nicknamed Team 155 and led by Dr. Steven S. Pietrobon, spent the next 18 months simulating, designing, building, and testing the codec. The key to the codec was the efficient implementation of a multi-dimensional trellis code. The encoder that added the information required to implement the code was incorporated in an XC4002A. The decoder that removes errors induced by noise in the channel is much more complicated and required two XC4010s. However, this is still much less complex than other coding schemes that require up to nine ASICs or ECL gate arrays and provide inferior performance.

SCRC's previous experience with XC3000 technology and the new features provided by the XC4000 architecture (especially the fast carry logic and on-chip RAM features) allowed Team 155 to put the decoder on two XC4010s in the time available. A standard Reed Solomon code also was used. An XC4003 and XC4005 were used to interface to available Reed Solomon codec chips and provide the interleaving, de-interleaving, and synchronization functions of the codec.

Viewlogic's WorkView and PowerView systems were both used for schematic capture and functional simulation of the FPGA designs; simulation was used extensively to test and debug the design before implementation. The use of X-BLOX™ and the reprogrammability of the Xilinx chips allowed design changes and improvements to be easily made and tested. Xilinx extended support to Team 155 by providing XC4010-5 devices (the fastest at the time) and the latest software upgrades as they became available. This was especially important during the acceptance tests when the codec was being tested with the modem for the first time. The codec was initially not quite fast enough, resulting in marginal performance. Using recently-arrived software, another route was performed, and a few hours later Team 155 had a faster and accepted codec.



Trellis decoder card uses 2 XC4010 FPGAs

The resulting high-speed codec is capable of transmitting 155.520 Megabits per second over international communication satellites. Previously, undersea fiber-optic cables were the only means for transmitting information internationally at this high data rate.

The codec is currently being licensed to EF Data in Tempe, Arizona, where it is being incorporated into their modems. After delivery of the modems later this year, Intelsat will test this modem/codec with the satellites. The prototype modem/codec has already been successfully tested using a ground-based version of their satellites. ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	PART NUMBER
CORPORATE		
High-Performance Computing Packet	*Application notes & brochure*	none
FPGAs		
Hi-Rel XC3000 Family Data Sheet	*Technical Data Sheet*	#0010244-01
XC1765D Data Sheet	*Technical Data Sheet*	#0010212-02
EPLDs		
EPLD Application Guide	*Application note & data sheets*	#0010237-01
HW-130 Overview	*Features & benefits*	#0010245-01
DEVELOPMENT SYSTEMS		
XACT*step*, version 6 Overview	*Features & benefits*	#0010101-04
Floorplanner Overview	*Features & benefits*	#0010246-01
Synopsys Interface Overview	*Features & benefits*	#0010154-05
Viewlogic ProSeries Interface Overview	*Features & benefits*	#0010166-03
Mentor Graphics Interface Overview	*Features & benefits*	#0010067-05
Cadence Interface Overview	*Features & benefits*	#0010247-01

New Edition of Xilinx Data Book

By the time you receive this issue of *XCELL*, a new revision of the *Xilinx Programmable Logic Data Book* will be available. Labeled the third edition, this new version has been updated to include new products, such as the XC3100A-1 FPGAs and the latest package options for the XC4000 family devices.

New, more complete information that helps users to manage heat dissipation more effectively was also added. *(See related article on page 25).*

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

3rd Canadian Workshop on Field-Programmable Devices (FPD '95)
May 29 - June 1
Montreal, Quebec, Canada

Designing Personal Communications Products
June 8-9: Seoul, Korea
June 12-13: Taipei, Taiwan
June 15-16: Beijing, China

32nd Design Automation Conference (DAC)
June 12-16
San Francisco, California

2nd GI/ITG Workshop on Field Programmable Devices
June 22 - 23
Karlsruhe, Germany

PLD Conference, Japan
July 19-21
Tokyo, Japan

IC Card Expo
July 24-26
Santa Clara, CA

Electronic Design Automation & Test Conference (EDA & T Asia)
Aug. 21-22: Beijing, China
Aug. 24-25: Seoul, Korea
Aug. 28-29: Hsinshu, Taiwan

5th International Workshop on Field Programmable Logic (FPL '95)
Aug. 29 - Sept. 1
Oxford, United Kingdom

8th Annual IEEE ASIC Conference (ASIC '95)
Sept. 18 - 22
Austin, Texas

European Design Automation Conference (EURO-DAC '95)
Sept. 18 - 22
Brighton, United Kingdom

XILINX RELEASED SOFTWARE STATUS - MAY 1995

Product Category	Product Description	Product Function	Xilinx Part Number	Previous Ver. Rel.	Current Version By Platform				Last Update
					PC1 *6.2*	SN2 *4.1.x*	AP1 *10.4*	HP7 *9.01*	
XILINX INDIVIDUAL PRODUCTS									
CORE FPGA	XC2,3,4K Support	Core Implementation	DS-502-xxx	5.02	5.10	5.10	5.10	5.10	01/95
CORE EPLD	XC7K Support	Core Implementation	DS-550-xxx	5.02	5.10	5.10		5.10	01/95
Floorplanner[4]	Hi-Density Des. Kit	Core Implementation	ES-HD4K-SN2	N/A		5.10			N/A
Mentor[2]	A.1-F	I/F and Libraries	DS-344-xxx	5.02		5.11	1.10	5.11	05/95
OrCAD[2]		I/F and Libraries	DS-35-xxx	5.00	5.10				01/95
Synopsys[2]		I/F and Libraries	DS-401-xxx	3.01b		3.20	3.01b	3.20	01/95
Viewlogic[2]	ProCapture	I/F and Libraries	DS-390-xxx	5.02	5.11				05/95
Viewlogic[2]	ProSim	I/F and Libraries	DS-290-xxx	5.02	5.11				05/95
Viewlogic[2]		I/F and Libraries	DS-391-xxx	5.10	5.11	5.11		5.11	01/95
XABEL[2]		Entry, Sim, Lib, Opt.	DS-371-xxx	5.00	5.10	5.10			01/95
X-BLOX[1]		Module Generation & Opt.	DS-380-xxx	5.00	5.10	5.10		5.10	01/95
Verilog[4]	2K, 3K, 4K, 7K Lib.	Models & XNF Trans.	ES-VERILOG-xxx			1.00		1.00	N/A
XILINX PACKAGES									
Mentor 8	Standard		DS-MN8-STD-xxx	5.02		5.10	1.10	5.10	01/95
OrCAD	Base		DS-OR-BAS-xxx	5.02	5.10				01/95
OrCAD	Standard		DS-OR-STD-xxx	5.02	5.10				01/95
Synopsys	Standard		DS-SY-STD-xxx	2.00		5.10	2.00	5.10	01/95
Viewlogic	Base		DS-VL-BAS-xxx	5.02	5.11				05/95
Viewlogic	Standard		DS-VL-STD-xxx	5.02	5.11	5.10		5.10	05/95
Viewlogic/S	Base		DS-VLS-BAS-xxx	5.02	5.11				05/95
Viewlogic/S	Standard		DS-VLS-STD-xxx	5.02	5.11				05/95
Viewlogic/S	Extended[3]		DS-VLS-EXT-xxx	5.02	5.11				05/95
XC5000 Pre-Rls.[4]	Standard	Core + VL Libraries	PR-VL-STD-xxx-5K	N/A	1.00	1.00			N/A
3rd Party	Standard	FPGA/EPLD Core	DS-3PA-STD-xxx	N/A	5.10	5.10		5.10	N/A
XILINX HARDWARE									
Device Pgmr.	PROM/EPLD/ XC8100 Pgmr.		HW-130	New	1.0	3Q95	-	3Q95	New
THIRD PARTY PRODUCTION SOFTWARE VERSIONS									
Cadence	Composer	Schematic Entry	N/A	4.3		4.3.3		4.3.3	N/A
Cadence	Verilog	Simulation	N/A	2.1		2.1.2		2.1.2	N/A
Cadence (Valid)	Concept	Schematic Entry	N/A	1.7		1.7-P4		1.7-P4	N/A
Cadence (Valid)	Rapidsim	Simulation	N/A	4.10		4.2		4.2	N/A
Mentor	Design Architect	Schematic Entry	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
Mentor	QuickSim II	Simulation	N/A	8.2_5		A.1-F	A.1-F	A.1-F	N/A
OrCAD	SDT 386+	Schematic Entry	N/A	1.10	1.20				N/A
OrCAD	VST 386+	Simulation	N/A	1.10	1.20				N/A
Synopsys	FPGA/Design Comp.	Synthesis	N/A	3.2a		3.2b	3.2b	3.2b	N/A
Viewlogic	ProCapture	Schematic Entry	N/A		5.0	5.3		5.3	N/A
Viewlogic	ProSim	Simulation	N/A		5.0	5.3		5.3	N/A
Data I/O	ABEL Compiler	Entry and Simulation	N/A		6.0	6.0			N/A
Data I/O	Synario	Entry and Simulation	N/A		2.0				N/A

NOTE: [1]FPGA Only [2]FPGA and EPLD [3]Includes ViewSynthesis v2.3.1
[4]Engineering software by request only

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - MAY 1995

Company	Product Name	Version	Function	Design Kit	FPGA Support	EPLD Support	X-BLOX Support
Acugen	Sharpen Sharpeye	2.55 2.55	Automatic Test Generation Testability Analysis	AALCA interface AALCA interface	✓ ✓		
ALDEC/Susie-CAD	Susie-Xilinx Active-Xilinx	2.0	Schematic Entry/Simulation Schematic Entry/Simulation	Xilinx Design Kit Xilinx Design Kit	✓ ✓	✓ ✓	✓ ✓
Aptix	System Explorer ASIC Explorer	2.0 2.0	System Emulation ASIC Emulation	Axess 2.0 Axess 2.0	✓ ✓		
Cadence (Valid)	Concept Rapidsim Composer Verilog FPGA Designer	1.7-P4 4.2 4.3.3 2.1.2 3.3	Schematic Entry Simulation Schematic Entry Simulation Synthesis	Xilinx Front End Xilinx Front End Xilinx Front End Xilinx Front End FPGA Synthesis	✓ ✓ ✓ ✓ ✓	✓ ✓ ✓ ✓	 ✓
Capilano	DesignWorks	3.1	Schematic Entry/Simulation	XD-1	✓		
Compass	Asic Navigator QSim X-Syn		Schematic Entry Simulation Synthesis	Xilinx Design Kit	✓ ✓ ✓		 ✓
CV (Prime)	Design Entry	2.0	Schematic Entry	Xilinx Kit	✓		
Data I/O	ABEL Synario	6.0 2.0	Synthesis Schematic Entry, Synthesis and Simulation	Xilinx Fitter Xilinx Fitter	✓ ✓	✓ ✓	 ✓
EPS	SIMETRI	2.0	Simulation	XNF2SIM	✓		
Escalade	Design Book		Design Entry		✓		
Exemplar Logic	CORE CORE/V-system	2.2 2.2	Synthesis Simulation	CORE CORE/V-system	✓ ✓	✓ ✓	✓
Flynn Systems	FS-ATG	2.6	Automatic Test Generation	FS-High Density	✓		
IBM-EDA	Boole-Dozer		Synthesis		✓		
IK Technology	G-DRAW G-LOG	5.0 4.03	Schematic Entry Simulation	GDL2XNF XNF2GDL	✓ ✓		
Ikos	2800/2900 Voyager	5.16 1.41	Simulation Simulation	Xilinx Tool Kit Xilinx Tool Kit	✓ ✓		
Intergraph	ACE Plus AdvanSIM-1076 VeriBest Sim EDM/DMM VeriBest Syn Synovation PLDSyn	12.2 12.0 12.2 12.3 12.2 12.1 12.0	Schematic Entry Simulation Simulation Design Flow Manager Synthesis Synthesis Design entry, synthesis sim.	Xilinx FPGA Design Kit Xilinx FPGA Design Kit Xilinx FPGA Design Kit Xilinx FPGA Design Kit Xilinx FPGA Design Kit SynLib included	✓ ✓ ✓ ✓ ✓ ✓ ✓	 ✓	✓ ✓ ✓ ✓
ISDATA	LOG/iC2 LOG/iC Classic	4.1 4.1	Entry Synthesis, simulation	Xilinx Fitter ODC	✓	✓ ✓	✓
IST (Alpine Design)	ASYL+	3.0	Synthesis	XNFinterface	✓	✓	
ITS	XNF2LAS	1a	Lasar model gen.	XNF2LAS	✓		
Logic Modeling (Synopsys Division)	Smart Model LM1200		Simulation Models Hardware Modeler	In Smart Model Library Xilinx Logic Module	✓ ✓	✓ ✓	
Logical Devices	CUPL	4.5	Synthesis	Xilinx Fitter	✓	✓	
Mentor Graphics	QuickSim II Design Architect Autologic	8.4 (A.x_F) 8.4 (A.x_F) 8.4 (A.x_F)	Simulation Schematic Entry Synthesis	Call Xilinx Call Xilinx Xilinx Synthesis Library	✓ ✓ ✓	✓ ✓ ✓	✓ ✓ ✓
MINC	PLDesigner-XL	3.3	Synthesis	Xilinx Design Module	✓		
Minelec	Ulticap	1.32	Schematic Entry	Xilinx Interface	2K,3K		
OrCAD	SDT 386+ VST 386+ PLD 386+	1.2 1.2 2.0	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx Call OrCAD	✓ ✓ ✓	✓ ✓	✓ ✓
Protel	Advanced Schematic	2.2	Schematic Entry	Xilinx interface	✓	✓	
Quad Design	Motive	4.0	Timing Analysis	XNF2MTV	✓		
Simucad	Silos III	92.115	Simulation	Included	✓		
Sophia Systems	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓	✓	✓
Synopsys	FPGA Compiler Design Compiler VSS	3.2 3.2 3.2	Synthesis Synthesis Simulation	Call Xilinx Call Xilinx Call Xilinx	3K,4K ✓ ✓	✓ ✓ ✓	✓ ✓ ✓

Continued

ALLIANCE PROGRAM - COMPANIES & PRODUCTS - MAY 1995 (con't)

Company	Product Name	Version	Function	Design Kit	FPGA Support	EPLD Support	X-BLOX Support
Synplicity	Synplify	2.5	Synthesis	Synplify	✓		✓
Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓		
Tokyo Electron	ViewCAD	5.0502a	FLDL to XNF	XNFGEN	✓		
Topdown Design	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓		
transEDA	TransPRO	1.2	Synthesis	Xilinx LIbrary	✓		
VEDA	Vulcan	4.5	Simulation	Xilinx Tool Kit	✓		
Viewlogic	ProCapture ProSim ProSynthesis	5.0 5.0 5.0	Schematic Entry Simulation Synthesis	Call Xilinx Call Xilinx Call Xilinx	✓ ✓ ✓	✓ ✓ ✓	✓ ✓
Viewpoint	VitalBridge VeriLink	1.0 1.0	Vital VHDL Verilog lib. back-annotation	VHDL I/F kit Verilog I/F kit	✓ ✓		
Visual Software Solutions	StateCAD	2.4	State diagram	Xilinx fitter	✓		
Zycad	Paradigm XP Paradigm RP		Gate-level simulation Rapid prototyping		✓ ✓		

ALLIANCE PROGRAM - PLATFORMS & CONTACTS

Company	Contact Name	*PLATFORM* PC	Sun	RS6000	HP7	Phone Number
Acugen	Peter de Bruyn Kops	✓	✓		✓	603-881-8821
Aldec/Susie-CAD	David Rinehart	✓				702-293-2271
Aptix Corporation	Wolfgang Hoeflich		✓		✓	408-428-6200
Cadence	Itzhak Shapira Jr.		✓	✓	✓	408-428-5739
Capilano Computing	Chris Dewhurst	✓		Macintosh		604-522-6200
Compass Design	Mahendra Jain				✓	408-434-7950
CV (Prime)	Kevin O'Leary				✓	617-275-1800
Data I/O	Dave Kohlmeier	✓	✓			206-881-6444
EPS	Michael Massa		✓		✓	617-487-9959
Escalade	Jerry Rau	✓				408-481-1308
Exemplar Logic	Stan Ng	✓	✓		✓	510-337-3700
Flynn Systems	Mike Jingozian	✓				603-891-1111
IBM-EDA	John Orfitelli			✓		914-433-9073
IK Technology	Hiroyuki Kataoka				✓	+81-3-3464-5551
Ikos	Brad Roberts		✓		✓	408-255-4567
Intergraph Electronics	Greg Akimoff	✓	✓		✓	415-691-6541
ISDATA	Ralph Remme	✓	✓		✓	+49-721-751087
IST	Gabriele Saucier	✓	✓		✓	+33-76-70-51-00
ITS	Frank Meunier		✓		✓	508-897-0028
Logic Modeling	Laura Horsey		✓		✓	503-531-2271
Logical Devices	David Mot	✓				303-279-6868
Mentor Graphics	Sam Picken		✓	✓	✓	503-685-1298
MINC	Lynne Dolan	✓	✓		✓	719-590-1155
Minelec		✓				+32-02-4603175
OrCAD	Troy Scott	✓				503-671-9500
Protel Technology	Matthew Schwaiger	✓				408-243-8143
Quad Design Tech.	Vern Potter		✓		✓	805-988-8250
Simucad	Richard Jones	✓				510-487-9700
Sophia Systems	Terry Wilfley	✓	✓		✓	408-943-9300
Synopsys	Lynn Fiance		✓	✓	✓	415-694-4102
Synplicity	Alisa Yaffa	✓	✓		✓	415-961-4962
Teradyne	Mike Jew		✓		✓	617-422-3753
Tokyo Electron	Shige Ohtani					+81-3-5561-7212
TopDown	ArtPisani	✓	✓	✓		603-888-8811
transEDA	James Douglas		✓		✓	+44-1703-255118
VEDA	George Sher		✓		✓	408-496-4516
ViewLogic	Preet Virk	✓	✓	✓	✓	508-480-0881
Viewpoint International	Ramesh Bhimarao	✓	✓		✓	408-954-7370
Visual Software	Ricky Escoto					305-346-8890
Zycad	David Allenbaugh		✓		✓	510-623-4451

COMPONENT AVAILABILITY CHART - MAY 1995

PINS	TYPE	CODE	XC2064	XC2018	XC2064L	XC2018L	XC3020	XC3030	XC3042	XC3064	XC3090	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003	XC4005	XC4006	XC4008	XC4010	XC4010D	XC4013	XC4013D	XC4025	XC4002A	XC4003A	XC4004A	XC4005A	XC4003H	XC4005H	XC5206	XC5210	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144
44	PLASTIC LCC	PC44	◆	◆				◆					◆										◆																					◆	◆	N	◆					
	PLASTIC QFP	PQ44																																											◆	◆	N						
	CERAMIC LCC	WC44																																											◆		◆	N	◆				
48	PLASTIC DIP	PD48	◆																																																			
64	PLASTIC VQFP	VQ64		◆	◆	◆							◆				◆						◆																																
68	PLASTIC LCC	PC68	◆	◆	◆		◆	◆				◆	◆									◆	◆																					◆				◆	◆				
	CERAMIC LCC	WC68																																											◆				◆	◆			
	CERAMIC PGA	PG68	◆																																																			
84	PLASTIC LCC	PC84		◆		◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆				◆	◆	◆	◆	◆		◆	◆		◆					◆	◆		
	CERAMIC LCC	WC84																																											◆					◆	◆		
	CERAMIC PGA	PG84		◆			◆	◆	◆			◆	◆	◆								◆	◆	◆																					◆									
100	CERAMIC QFP	CQ100					◆		◆																																													
	PLASTIC PQFP	PQ100					◆	◆	◆			◆	◆	◆								◆	◆	◆				◆	◆										◆	◆				N								◆	◆		
	PLASTIC TQFP	TQ100		◆				◆	◆														◆	◆																															
	PLASTIC VQFP	VQ100				◆							◆	◆			◆	◆					◆	◆															◆	◆															
	TOP BRZ. CQFP	CB100					◆		◆			◆		◆								◆	◆																	◆															
120	CERAMIC PGA	PG120																									◆										◆	◆	◆															
132	PLASTIC PGA	PP132						◆	◆				◆	◆									◆	◆																															
	CERAMIC PGA	PG132						◆	◆				◆	◆									◆	◆																															
144	PLASTIC TQFP	TQ144											◆	◆				◆	◆				◆	◆																◆	◆				N	N									
	CERAMIC PGA	PG144																																																				
156	CERAMIC PGA	PG156																										◆	◆											◆															
160	PLASTIC PQFP	PQ160							◆	◆				◆	◆									◆	◆	◆		◆	◆	◆	◆	◆	◆	◆	◆				◆	◆				◆	◆								◆	◆
164	CERAMIC QFP	CQ164								◆																																												
	TOP BRZ. CQFP	CB164								◆					◆										◆	◆		◆																											
175	PLASTIC PGA	PP175								◆					◆										◆	◆																															
	CERAMIC PGA	PG175								◆					◆										◆	◆																															
176	PLASTIC TQFP	TQ176													◆					◆					◆																															
184	CERAMIC PGA	PG184																																																				
191	CERAMIC PGA	PG191																												◆	◆									◆		◆													
196	TOP BRZ. CQFP	CB196																													◆																					
208	PLASTIC PQFP	PQ208								◆					◆										◆	◆		◆	◆	◆	◆	◆	◆	◆	◆				◆	◆				◆	◆								
	METAL MQFP	MQ208																												◆	◆		◆																			
223	CERAMIC PGA	PG223																							◆								◆		◆					◆		◆											
225	PLASTIC BGA	BG225																													◆	◆	◆	◆																		◆	◆
	WINDOWED BGA	WB225																																																			◆
228	TOP BRZ. CQFP	CB228																																◆																		
240	PLASTIC PQFP	PQ240																																◆	◆						◆		◆									
	METAL MQFP	MQ240																																◆		◆					◆											
299	CERAMIC PGA	PG299																																	◆																	
304	HI-PERF. QFP	HQ304																																	N																		

◆ = Product currently shipping or planned N = New since last XCELL

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS — MAY 1995

MANUFACTURER	MODEL	1736A/ 1765	17128	1736D/ 1765D	1716L/ 1765L	17128D	17256D	DIP8	PC20	SO8
ADVANTECH	PC-UPROG LABTOOL-48		V2.1 V1.0	V2.0 V1.0	V2.0 V1.0	V2.1 V1.0	V2.1 V1.0	X X	 PLCC2020-01	
ADVIN	PILOT-U24 PILOT-U28 PILOT-U32 PILOT-U40 PILOT-U84 PILOT-142 PILOT-143 PILOT-144 PILOT-145	10.53 10.53 10.53 10.53 10.53 10.73 10.73 10.73 10.73	10.76C 10.76C 10.76C 10.76C 10.76C 10.76C 10.76C 10.76C 10.76C	10.71 10.71 10.71 10.71 10.71 10.73 10.73 10.73 10.73	10.77 10.77 10.77 10.77 10.77 10.77 10.77 10.77 10.77	10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B	10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B 10.78B	X X X X X AM-1736 AM-1736 AM-1736 AM-1736	PX-20 PX-20 PX-20 PX-20 PX-20 PX-20 PX-20 PX-20 PX-20	SO-8 SO-8 SO-8 SO-8 SO-8 SO-8 SO-8 SO-8 SO-8
AVAL	PECKER-50 PKW5100		C C	C C				X X		
B&C MICROSYSTEMS INC.	Proteus-UP40	V3.4e	V3.4e	V3.5f	V3.7f	V3.7I	V3.7I	X	AMUPLC84	
BP MICROSYSTEMS	CP-1128 EP-1140 BP-1200	C C C	V2.17* V2.17 V2.17	V2.21c* V2.21c V2.21c	V2.34* V2.34 V2.34	V3.06 V3.06 V3.06	V3.06 V3.06 V3.06	FH28A FH40A SM48D	FH28A + 3rd Party FH40A + 3rd Party SM20P or SM84UP	FH28A + 3rd Party FH40A + 3rd Party 3rdParty
BYTEK	135H-FT/U MTK-1000 MTK-2000 MTK-4000	V42 V42 V42 V42	V51 V51 V51 V51	V51 V51 V51 V51	V51 V51 V51 V51			TC-824D TC-824D TC-824D TC-824D		
DATA I/O	UniSite/Site 40/48 UniSite/ChipSite UniSite/PinSite 2900 3900 AutoSite UniPak 2B ChipLab	V4.0 V4.0 V4.0 V2.1 V1.5 V1.5 V24 V1.1	V4.1 V4.1 V4.1 V2.2 V1.6 V1.6 V1.0	V4.1 V4.1 V4.1 V2.2 V1.6 V1.6 V1.0	V4.6 V4.6 V4.6 V3.4 V2.4 V2.4 V1.1	V4.8 V4.8 V4.8 V3.6 V2.6 V2.6 V2.0	V4.8 V4.8 V4.8 V3.6 V2.6 V2.6 V2.0	X X X X 0101 DIP-300-1 351B120 X	USBASE-PLCC USBASE-PLCC USBASE-PLCC 2900-PLCC 3900-PLCC PLCC-20-2	USBASE-SOIC USBASE-SOIC USBASE-SOIC 2900-SOIC 3900-SOIC 080801S300
DEUS EX MACHINA	XPGM	V1.00	V1.00	V1.00	V1.10	V1.10	0	3rd Party	3rd Party	
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ PROMAX	V1.3 V2.34	V1.5 V2.34	V1.5 V2.34	V1.5 V2.34	P 3Q/95 V2.34	P 3Q/95 V2.34	X X	 Module #4	
ELAN DIGITAL SYSTEMS	3000-145 5000-145 6000 APS	C C K2.01	C C K2.02	 K2.01	 K2.10	 K2.14	 K2.14	A116 A116 X	 PDi84UPLC	 PDi16USOI
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.30 V3.30	V3.30 V3.30	V3.30 V3.30	V3.30 V3.30	V3.50 V3.47	V3.50 V3.47	X PAC-DIP40	CNV-PLCC-XC1736 PAC-PLCC44	CVN-SOP-NDIP16
ICE TECHNOLOGY LTD	Micromaster 1000/1000E Speedmaster 1000/1000E Micromaster LV LV40 Portable Speedmaster LV	V1.1 V1.1	V3.00 V3.00 V3.00 P 2Q95 V3.00	V3.00 V3.00 V3.00 P 2Q95 V3.00	 V3.00 P 2Q95 V3.00	V3.00 V3.00 V3.00 P 2Q95 V3.00	V3.00 V3.00 V3.00 P 2Q95 V3.00	X X X X X	AD-1736/65-PLCC AD-1736/65-PLCC	
LINK COMPUTER GPHX	CLK-3100	V5.08	V5.08	V5.08				X17XXB	PLCC-17XX	SOIC-16
LOGICAL DEVICES	ALLPRO-40 ALLPRO-88 ALLPRO-88XR CHIPMASTER 3000 CHIPMASTER 5000 XPRO-1	V2.2 V2.2 V1.1 V2.0 V1.15 V1.01	 V2.3 V2.3 V2.1 V1.01	 V2.3 V1.3 V2.0 V1.01	 V2.3 V1.01	 V2.5 V2.3 	 V2.5 V2.3 	X X X X X MODXLN-173	OPTPLC-208 OPTPLC-208 OPTPLC-208 MODXLN-173	OPTSOI-080 OPTSOI-080 OPTSOI-080 OPTSOI-080 OPTSOI-080 MODXLN-173
MQP ELECTRONICS	MODEL 200 SYSTEM 2600 PINMASTER 48	C	6.45 P 2Q95 P 2Q95	6.45 P 2Q95 P 2Q95	6.45 P 2Q95 P 2Q95	6.46 P 2Q95 P 2Q95	6.46 P 2Q95 P 2Q95	AD13A-16 MP6 X		
MICRO PROSS	ROM 5000 B ROM 3000 U	C C	V1.70 V3.60	V1.70 V3.60				Mu 40		
NEEDHAM'S ELECTRONICS	EMP20	V1.5	V1.5	V2.37	V2.37	V2.37	V2.37	04B		
RED SQUARE	IQ-180 IQ-280 Uniwriter 40 Chipmaster 5000	C C C C		V8.2 V8.2 V8.2 V8.2						
RETNEL SYSTEMS	ZAP-A-PAL	C		V3.8J				Module #36		
SMS	Expert Optima Multisyte Plus48 Sprint Plus	B/93 B/93 B/93 B/93	A/94 A/94 A/94 A/94	A/94 A/94 A/94 A/94	A1/94 A1/94 A1/94	Cx/94 Cx/94 Cx/94	Cx/94 Cx/94 Cx/94	TOP40DIP " "	TOP1PLC or TOP3PLC/TOP3PLC "	
STAG	Eclipse Quasar	 10.76C	4.4 10.76C	V2.2 V10.76C	V4.3 V10.76C	V4.10.31 V10.78B	V4.10.31 V10.78B	EPU48D X	EPU84P AMPLCC20	
SUNRISE	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	X X	X X	X X
SUNSHINE	POWER-100 EXPRO-60/80	V8.18 V8.18	V8.18 V8.18	V8.18 V8.18	V8.18 V8.18	V8.18 V8.18	V8.18 V8.18	X X		
SYSTEM GENERAL	TURPRO-1 Turpro-1 F\X APRO	V2.21F V2.21F C	V2.21F V2.21F V2.14	V2.21F V2.21F V2.01	V2.21F V2.21F V2.12	V2.21F V2.21F S 2Q95	V2.21F V2.21F S 2Q95	DIP-Adapter DIP-Adapter X	P20-Adapter P20-Adapter X	
TRIBAL MICROSYSTEMS	TUP-300 TUP-400 FLEX-700	C C C	V3.31 V3.31 V3.31	V3.31 V3.31 V3.31	V3.37C V3.37C V3.37C	V3.47 V3.50 V3.47	V3.47 V3.50 V3.47	X X X	CNV-PLCC-XC1736 " "	
XELTEK	SuperPRO SuperPRO II	1.5B 1.5B	1.7C 1.7C	1.7D 1.7D	1.8 1.8	2.2A 2.2A	2.2A 2.2A	X* X*	20-PL/8-D-ZL-XC1736 20-PL/8-D-ZL-XC1736	16SO15/D6-ZL 16SO15/D6-ZL
XILINX	HW-112 HW-120 HW-130	C V5.00	V3.11 V5.00 V1.00	V3.31 V5.00 V1.00	V3.31 V5.00 V1.00	V5.0.0 P 6/95 V1.00	V5.0.0 P 6/95 V1.00	X HW-120-PRM HW-137-DIP8	HW-112-PC20 HW-120-PRM S 5/95	HW-112-SO8 HW-120-PRM S 5/95

C = Currently Supported, P = Planned, S = Scheduled Release Date, X=Package Supported

Programmer Support for Xilinx XC7200 EPLDs — May 1995

VENDOR	MODEL	7236	7236A	7272	7272A	PC44	PC68	PC84	PG84	Comments
Advantech	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0	X SDP-UNIV-44	SDP-7272-68 SDP-7272-68	SDP-7272-84 SDP-7272-84		
Advin Systems	Pilot-U40 Pilot-U84	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	10.77E 10.77E	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84	 AM-XC84G	
B&C Microsystems, Inc.	Proteus	V3.6j	V3.6j	V3.7h	V3.7h	AMUPLC84	AMUPLC84	AMUPLC84		
BP Microsystems	BP-1200	v2.32	v2.32	v2.34	v2.34	SM44P	SM68P or SM84UP	SM84P or SM84UP	SM84UGA	
DATA I/O	UniSite 2900 3900 AutoSite	v4.3 V3.4* v2.1 V2.4*	v4.6* V3.4* V2.4* V2.4*	v4.5 v2.3 v2.3	v4.5** v2.3** v2.3**	USBASE-PLCC PPI-0243 3900-PLCC PLCC-44-1	USBASE-PLCC PPI-0246 3900-PLCC PLCC-68-1	USBASE-PLCC PPI-0208 3900-PLCC PLCC-84-1		*7236A=PPI-0243 **7272A=PPI-0246 (PC68) **7272A=PPI-0247 (PC84)
Deus Ex Machina	XPGM	V1.00	V1.00	V1.00	V1.00	1	2	3		
Elan Digital Systems	6000APS	K2.04	K2.04	K2.06	K2.06	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi84PGx	
Electronic Engineering Tools	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	V2.1 P 6/95	V2.1 P 6/95	Module 05+PA44-84U Module 19 + H44	PA68-48A	PA84-48A		
Hi-Lo Systems Research	All-03A All-07	V3.01 V3.01	V3.01 V3.01	V3.00 V3.00	V3.00 V3.00	ADP-XC7236-PL44 PAC-PLCC44	ADP-XC7272-PL68 PAC-PLCC68	ADP-XC7272QPI-84		
ICE Technology Ltd.	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44 AD-XC7236-PLCC-44	AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68 AD-XC7272-PLCC-68	AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84 AD-XC7272-PLCC-84		
Logical Devices	ALLPRO-88 ALLPRO-88XR XPRO-1	2.2 1.35 1.01	V2.4 V2.4 1.01	2.2 1.35 1.01	V2.4 V2.4 1.01	C C MODXP1-44L	C C MODXP1-68L	C C MODXP1-84L	 MODXP1-84G	
MQP Electronics	SYSTEM2000 PINMASTER48	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 2Q95 P 2Q95	MP1	MP1	MP1		 Universal Programmer
Needham's Electronics	EMP20	V2.37	V2.37	V2.37	V2.37	19A+H44	20A+U68CB	20A+U84CB		
Stag	Eclipse	P 2Q95	P 2Q95	P 2Q95	P 2Q95	EPU84P+	EPU84P+	EPU84P+		
SMS	Expert Optima Multisyte	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	A1/94 A1/94 A1/94	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1	TOP1 TOP1 TOP1		
Sunrise Electronics	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	X X	X X	X X	X X	All adapters are custom All adapters are custom
Sunshine Electronics	POWER-100 EXPRO-60/80	V8.16 V8.16	V8.16 V8.16			CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44				
System General	TURPRO-1 TURPRO-1 F\X	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	v2.12 v2.12	P44 P44	P68 P68	P84 P84		
Tribal Microsystems	TUP-300 TUP-400 FLEX-700	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	v3.0 v3.0 v3.0	TUP-7236 TUP-7236 TUP-7236	TUP-7272 TUP-7272 PAC-PLCC68			 PAC-PLCC44
Xeltek	SUPERPRO SUPERPROII	1.7C 1.7C	2.2 2.2	2.1 2.1	2.1 2.1	XXC7236-44PL/40D XXC7236-44PL/40D	XXC7272-68PL/68D XXC7272-68PL/68D	XXC7272-84PL/84D XXC7272-84PL/84D		
Xilinx	HW-120 HW-130	V3.14 V1.00	V3.14 V1.00	V3.14 S 5/95	V3.14 S 6/95	HW-120-PC44 HW-132-PC44*	HW-120-PC68 S 5/95*	HW-120-PC84 S 5/95*	HW-120-PG84	*HW-12x EPLD adapters can be used on HW-130

C = Currently Supported (no version number) P = Planned Release S = Shipping Date

PROGRAMMER SUPPORT FOR XILINX XC7300 EPLDS — MAY 1995

VENDOR	MODEL	7318	7336	7354	7372	73108	73144	PC44	PC68	PC84	PQ44	PQ100	PG144	PQ160	PG184	BG225
ADVANTECH	PC-UPROG LabTool-48	V2.4 V1.0	V2.4 V1.0	V2.4 V1.0		 P 6/95		X SDP-UNIV-44	SDP-7354-68 SDP-7354-68	 X						
ADVIN SYSTEMS	PILOT-U40 PILOT-U84	10.78N 10.78B	10.78N 10.78B	10.78N 10.78B	10.78N 10.78B	10.79 10.79	P 3Q95 P 3Q95	USA-84 USA-84	USA-84 USA-84	USA-84 USA-84		AM-XC100Q AM-XC100Q	AM-XC144G AM-XC144G	AM-XC160Q AM-XC160Q		
B&C MICROSYSTEMS	Proteus	3.7k	3.7k	3.7k	P 3Q95	3.7k	P 3Q95	C	C	C						
BP MICROSYSTEMS	BP-1200	V3.01	V3.01	V3.01	V3.07	V3.06A		SM44P		FHSM84PX						
DATA I/O	2900 3900 UniSite AutoSite	V3.5 V2.5 V4.7 V2.5	V3.5 V2.5 V4.7 V2.5	V3.5 V2.5 V4.7 V2.5	 V2.6 V4.8 V2.6	 V2.6 V4.8 V2.6	 P 3Q95 P 3Q95 P 3Q95	2900-PLCC 3900-PLCC USBASE-PLCC PLCC-44-1	 3900-PLCC USBASE-PLCC PLCC-68-1	 3900-PLCC USBASE-PLCC PLCC-84-1	0529 0529 0529 0529	 0557 0557		 0558 0558		 PPI-1101 PPI-1101 PPI-1101
DEUS EX MACHINA	XPGM	V1.00	V1.00	V1.00	V1.10	V1.10	P 3Q95	5	6 (13 for 7372)	7				9		
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ PROMAX	V2.1 V2.34	V2.1 V2.34	V2.1 V2.34	V2.1 P 6/95			Module 04+PA44-48U Module #19 + H44	PA68-48B (7354) PA68-48C (7372)	PA84-48B						
ELAN	6000 APS	k2.13	k2.13	k2.13	k2.13	k2.13	P 3Q95	PDi84UPLC	PDi84UPLC	PDi84UPLC	PDi044QFx	PDi100QFx	PDi160QFx		PDi225BGx	
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.04 V3.02	V3.04 V3.02	V3.04 V3.02	V3.05 V3.01	V3.01 V3.00	P 3Q95 P 3Q95	ADP-XC7336-PL44 PAC-PLCC44	ADP-XC7372-PL68 PAC-PLCC68	ADP-XC73108-PL84						
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	VX1.00 VX1.00 VX1.00 VX1.00	P 3Q95 P 3Q95 P 3Q95 P 3Q95	AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44	AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68 AD-7354-PLCC-68 AD-7372-PLCC-68	AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44 AD-73XX-PLCC-44						
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR XPRO-1	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	V2.5 V2.5 1.01	P 3Q95 P 3Q95 P 3Q95	C C MODXP1-5444L	C C MODXP1-5468L	C C MODXP1-108L				MODXP1-160Q	MODXP1-184G	MODXP1-108B
MQP ELECTRONICS	SYSTEM 2000	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 3Q95	MP1	MP1	MP1						
PINMASTER 48	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 2Q95	P 3Q95										
NEEDHAM'S ELECTRONICS	EMP20	V2.37	V2.37	V2.37	V2.37	V2.37	P 3Q95	19B + H44	20A + U68CA	20A + U84CA						
SMS	EXPERT OPTIMA	C/94 C/94	C/94 C/94	C/94 C/94	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 3Q95 P 3Q95	TOP1 TOP1	TOP1 TOP1	TOP1 TOP1						
STAG	ECLIPSE	V4.10.31	V4.10.31	V4.10.31	V4.10.31	V4.10.31	P 3Q95									
SUNRISE	T-10 UDP T-10 ULC	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31	V3.31 V3.31		X X	X X	X X						
SUNSHINE	POWER-100 EXPRO-60/80	P 5/95 P 5/95	P 5/95 P 5/95		P 5/95 P 5/95	P 5/95 P 5/95		CNV-UNIVERSAL-PLCC44 CNV-UNIVERSAL-PLCC44								
SYSTEM GENERAL	TURPRO-1	V2.2	V2.2	V2.2	V2.2	V2.2	P 3Q95	C								
TRIBAL MICROSYSTEMS	ALL-07	V3.02	V3.02	V3.02	V3.01	V3.00	P 3Q95	PAC-PLCC44	PAC-PLCC68							
XELTEK	SUPERPRO SUPERPRO II	2.1 2.1	2.1 2.1	2.1 2.1	P 2Q95 P 2Q95	P 2Q95 P 2Q95	P 3Q95 P 3Q95	XXC7354-44PL/40D XXC7354-44PL/40D	XXC7354-68PL/40D XXC7354-68PL/40D							
XILINX	HW-120 HW-130	V5.00 V1.00	V5.00 V1.00	V5.00 V1.00	V5.00 S 5/95	V5.00 S 5/95	P 6/95 S 5/95	HW-126-PC44 HW-133-PC44	HW-126-PC68	HW-126-PC84	HW-126-PQ44	HW-126-PQ100	HW-126-PG144	HW-126-PQ160	HW-126-PG184	HW-126-BG225

C = Currently Supported (no version number) P = Planned Release

New XC4000 Family Speed Grade Offers Higher Performance

The XC4000 FPGA family will reach new performance levels with the introduction of the -3 speed grade this July. This speed improvement, along with upcoming architectural improvements, will expand the range of applications that can be addressed by this high-performance, full-featured FPGA family. The improved performance of the -3 devices also allows the XC4000 family to be fully PCI compliant.

In the typical application, the new -3 speed grade offers a 25 percent performance improvement over the previous XC4000 device speed record. System clock speeds of 70 MHz and higher will be achievable.

Digital signal processing is among the many high-performance applications that can be addressed by this high-speed FPGA technology. Video processors that previously required multiple DSP processors or large ASICs can be implemented in a single FPGA device. (An application note about FIR filter implementations in XC4000 FPGAs was recently released, and more DSP design support material is being prepared.). For more information, send E-mail inquiries to dsp@Xilinx.com ◆

MIL-STD-883B Compliant Serial PROMs

The XC1765D and XC17256D Serial Configuration PROMs are now available in full MIL-STD-883B compliant versions. These devices typically are used to store configuration data for Xilinx SRAM-based FPGAs, and are optimized for easy use with the FPGAs. As part of our commitment to the Hi-Rel (military, defense, and aerospace) market, Xilinx has long offered military temperature range versions, but in addition now provides fully compliant devices.

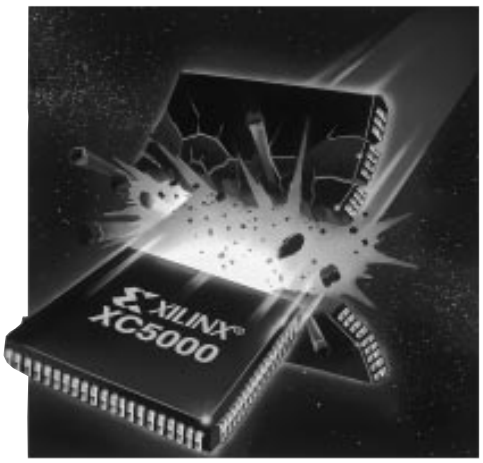
The XC1765D device holds 65,536 bits of data and can completely configure Xilinx FPGAs up to the density of the XC3090, while the XC17256D holds 262,144 bits of data and can completely configure any Xilinx FPGA up to the density of the XC4013. Multiple devices can be easily cascaded to support multiple FPGAs and / or multiple configurations.

Both devices are available in the 8-pin DIP package, and DESC SMDs (Standard Military Drawings) have been released. These devices are supported by a wide range of programmers available from Xilinx and leading third-party vendors. ◆

XC5200 FPGA Family Grows

The XC5200 FPGA family has been expanded to include the 2,500-gate XC5202 and the 4,000-gate XC5204. The XC5200 family now includes flexible, high-density FPGA devices ranging from 2,500 to 18,000 gates.

For lower-density designs that do not require the use of on-chip user RAM, the new XC5202 and XC5204 FPGAs provide a feature-rich solution. Like all members of the XC5200 FPGA family, these new devices include JTAG boundary-scan logic for enhanced testability, carry logic supporting fast arithmetic operations, and internal 3-state buffers for efficient on-chip busing capability.



All XC5200 devices offered in a common package *(see table)* are completely footprint compatible, allowing the easy migration to smaller or larger devices without changes to the PCB layout. The flexible VersaRing™ I/O interface delivers the industry's best pin locking capability for a high-density FPGA.

Please contact your local Xilinx sales representative for further information regarding software and component availability. ◆

Device	NEW XC5202	NEW XC5204	XC5206	XC5210	XC5215
Usable gates	2,200-2,700	3,900-4,800	6,000-7,500	10,000-12,000	14,000-18,000
VersaBlock matrix	8 x 8	10 x 12	14 x 14	18 x 18	22 x 22
Total CLBs	64	120	196	324	484
Total Flip-Flops	256	480	784	1,296	1,936
Total IOBs	84	124	148	196	244
10K Unit Pricing *(-6 speed grade, PC84)*	$9	$15	$25	$38	$68 (PQ208)
Availability	3Q95	3Q95	NOW	NOW	3Q95
Packages	PC84 PQ100 VQ100 TQ144 PG156	PC84 PQ100 VQ100 TQ144 PQ160 PG156	PC84 PQ100 TQ144 PQ160 PQ208 PG191	PC84 TQ144 PQ160 PQ208 PQ240 PG223	 PQ208 PQ240 HQ304 PG299

Introducing The New,
Low-Power XC7336Q EPLD

The latest addition to the fast-growing XC7300 EPLD family is a low-power version of the XC7336 called the XC7336Q.

The XC7336Q offers all of the benefits of the advanced XC7300 architecture, including 100 percent routing with 100 percent utilization, SMARTswitch, 24mA output drive and 3.3V / 5V level translation. Furthermore, like the other XC7300 family members, the XC7336Q-10 is 100 percent PCI compliant.

The XC7336Q differs from the standard XC7336 in terms of power consumption — the Q version consumes **60 percent less power**. Also, the XC7336Q is available only in -10, -12 and -15 speed grades.

PAL and GAL users are already familiar with the Q nomenclature — in the PAL / GAL world, a Q (for **Q**uarter power) CMOSPAL typically functions at one-fourth the I_{CC} of the equivalent PAL. Power-conscious PAL users will find the XC7336Q to be extremely appealing, as the XC7336Q will integrate three 22V10s while consuming only **one sixth** the power of those devices.

The XC7336Q EPLD is ideal for space-constrained electronic systems, including computing, peripherals and consumer applications. Board space and airflow limitations tend to make such applications highly sensitive to power consumption and system noise. Low I_{CC} specifications combined with low-profile packaging options make the XC7336Q a high integration PAL-like solution that fits small form factor and power constraints and enhances a design's overall reliability and noise immunity.

DEVICE	SPEED	LOWEST COST	LOWEST POWER	PACKAGES
XC7336 - 5,7,10,12,15	✔	✔		PC44. WC44. PQ44
XC7336Q - 10,12,15			✔	PC44, WC44, PQ44, VQ44

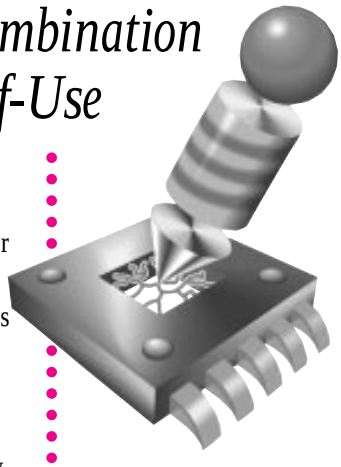
Above is a selection guide to help choose the best XC7336 product for your needs. Note that there are instances where the standard XC7336 is a better choice than the XC7336Q.

The XC7336Q will be fully supported (explicitly) in DS-550 Rev. 6.0. However, users can begin designs immediately with DS-550 v5.1 by using the standard XC7336 as the target device. Programming support on the HW-130 programmer will be available by the end of May, and all major third party programmers will be on-line in July.

Engineering samples of the XC7336Q will be available by the end of May, with volume shipments by the end of June. ◆

XACTstep VERSION 6

A Revolutionary Combination of Power and Ease-of-Use



The newest version of the Xilinx development system—named XACT*step*, version 6—combines power and ease-of-use to provide the highest-productivity tool set in the programmable logic industry. Targeted for shipment in August, 1995, XACT*step* runs under Microsoft Windows 3.1 on the PC and Motif on workstations.

XACT*step*, version 6 features six powerful, easy-to-use tools intended for a wide range of programmable logic designs. On one end of the spectrum, simple PAL replacements can be implemented in EPLDs using fully automatic techniques. At the other end of the spectrum, large, complex FPGA designs can be fine-tuned using a configurable flow engine and the programmable logic industry's first graphically-based, hierarchical floorplanner.

The new graphical user interface (GUI) in XACT*step* includes many features that shorten the learning curve and simplify design implementation and debug. With this GUI, programs are executed and options are set using tool bars and icons. Tool tips give instant descriptions of commands and on-line help provides more in-depth information. New report browsers display message files with "plain English" titles and allow the simultaneous viewing of multiple documents.

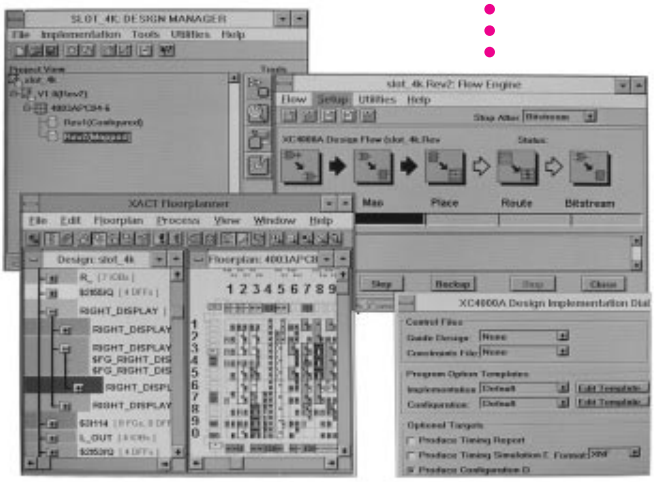
The results are faster implementation and debug cycles, a shorter learning curve and a dramatic boost in engineering productivity.

Six Powerful New Tools

XACT*step* contains six powerful new tools that accelerate design implementation, verification and debug cycles.

- The new *Design Manager* provides a complete project management environment for the XC2000, XC3000, XC3100, XC4000, XC5000 and XC7000 families. It supports unlimited version control and manages all the underlying files for each design revision.
- The configurable *Flow Engine* lets users choose the desired amount of control over the implementation process. Users can choose a fully automatic flow or set break points that allow the analysis and optimization of results before proceeding to the next step.

For each step in the implementation process, the automatic tools can be easily



directed to achieve the desired result. For example, the automatic placement and routing tools can be set to optimize the design or minimize run time; the selection is made using a slide bar that appears in a pop-up menu.

The entire collection of settings can be stored in a template for later use. New users can choose from standard templates provided with the system. Experienced users can create an unlimited number of custom templates and distribute these to other members of their group.

For users who don't want to take advantage of the new, easy-to-use interface,

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XILINX®

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all program options from XACT 5.0 can be entered using the old command line syntax.

- XACT*step* contains a new graphics-based, hierarchical *floorplanner*. With XACT-Floorplanner™, users can easily achieve "hand-crafted" levels of performance and density in FPGA designs. *(See related article on page 19).*

  Floorplanning is valuable for any design that has a high degree of structure or a large number of gates. With just a few minutes of basic floorplanning, designers can quickly place critically-timed logic and graphically plan the data flow. Placement is performed at a high level using the designs' hierarchy and a floorplan of the target device. Floorplanning also allows optimal use of specialized FPGA architectural structures like high-speed distributed RAM and internal three-state buffers. Users needing to maximize performance can easily implement a detailed floorplan employing proven optimization techniques like bus interleaving, register grouping and I/O pin alignment.

- The interactive *Timing Analyzer* makes it easy to analyze the designs' performance with custom timing reports. Using pop-up menus, the tool can generate reports that show the delay along any specific path or group of paths, such as all the paths of a certain type or those associated with specific clock signals. In addition, the *Timing Analyzer* can automatically compare the implemented design's actual performance to the goals entered using XACT-Performance™, and show the estimated maximum frequency for each clock in the design.

- The new *Hardware Debugger* provides for the verification of configuration data and the viewing of internal signal activity during system debug and test. It takes advantage of the re-programmable, SRAM-based devices by configuring the FPGA in-circuit using a cable connected to a host PC or workstation. After configuring the device, bitstream data is read back through the cable for automatic verification.

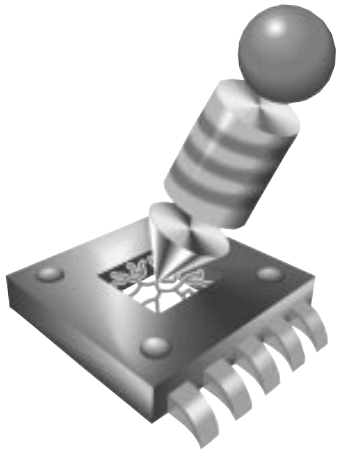
  While the device is running, an unlimited number of internal nodes can be viewed, with the results displayed in a wave-form window. By giving the hardware debugger control of the system clock, designers can easily step through state machines and other synchronous circuits to verify functionality.

- The new graphics-based *PROM Formatter* in XACT*step* creates PROM programming files. It chooses the best PROM size for the design, and automatically splits the data into multiple files if smaller PROMS are being used. Serial and byte-wide PROMS in four different formats are supported. If the target system includes a daisy chain of FPGAs, the PROM formatter graphically creates the load order and verifies the load sequence.

Free To Users On Maintenance

Registered Xilinx development system owners with an active software maintenance agreement will receive the XACT*step*, version 6 update automatically. *To check on the status of your maintenance agreement, call Xilinx customer service at 408-559-7778, or contact your local Xilinx sales office.* ◆

Full-Featured Floorplanner Boosts FPGA Performance



The new XACT*step*, version 6 release contains the industry's first graphics-based hierarchical floorplanner. Use of XACT-Floorplanner can result in dramatic improvement to FPGA performance, allowing designs to run at higher speed, or providing cost-savings by allowing the use of a slower speed grade device.

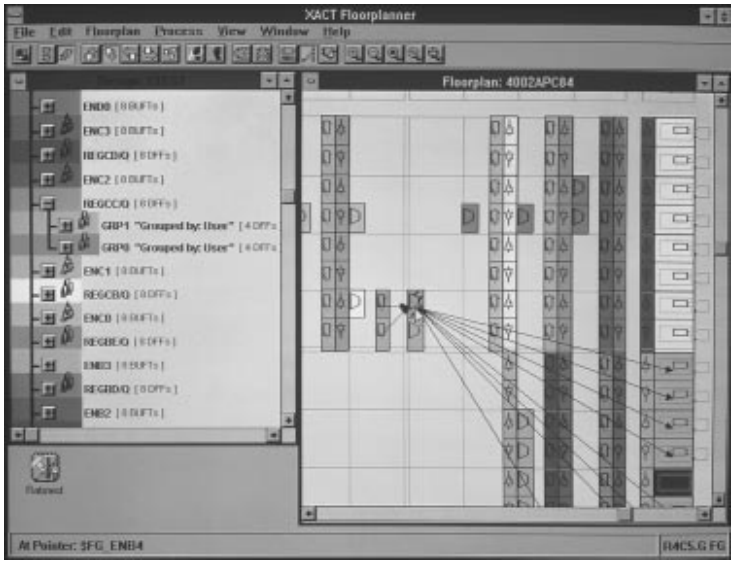
Floorplanning is particularly effective for designs that have a high degree of structure or a large gate density. Floorplanning can help optimize the use of special FPGA features such as the high-speed distributed RAM capability of the XC4000 FPGA family.

The Floorplanner features a "drag-and-drop" methodology that makes it easy to learn and use. A basic floorplan is created by dragging logic elements from the design and dropping them into locations on a picture of the die. Critically-timed logic can be pre-placed, and overall data flow can be planned. More-detailed floorplans allow the use of proven optimization techniques such as bus interleaving, register grouping and I/O pin alignment.

Many powerful features aid the designer. Users start with a **graphical view** of the designs' hierarchy. Each level of hierarchy is labeled with the original symbol from the schematic or hardware description language description, and is marked with the exact number of required FPGA resources. This view of the hierarchy can be enlarged or reduced to view any level of the design. A search and find utility makes it easy to locate specific logic elements.

When a logic element is "dropped" onto the die, the Floorplanner creates a **"ratsnest" view** of all its interconnections to previously-placed elements. Logic elements can be assigned to an area of the device so that the automatic "place and route" tools can then find an optimal placement of that logic within that area. For elements encompassing multiple FPGA resources, the Floorplanner can be directed easily to distribute the elements horizontally or vertically. Thus, logic structures can be aligned to use long line routing and internal three-state buffers efficiently.

For more-detailed floorplans, powerful commands make it easy to align or interleave busses or structured logic elements. Users re-order bits by simply changing the sort order. Complex alignments can be carried out by placing each bit separately.



Once the floorplanner finds the optimal placement for a given logic structure, it can be captured to a **Placement Map** and imposed on similar structures in the design — making it easy to "tile" repeated logic, or re-use portions of a design in future projects.

After completing the floorplan, commands are available to help analyze its efficiency. These commands also can be used to analyze a layout created by the automatic tools.

Continued on next page

Cadence Interface Now Available from Xilinx

"This reflects our continuing commitment to make top-down design methodologies more accessible to Xilinx users."

The interface software for linking the Cadence design tools to the Xilinx XACT-Development™ system, including Verilog libraries, can now be purchased directly from Xilinx. Support contracts also are available. This reflects our continuing commitment to make top-down design methodologies more accessible to Xilinx users. These interfaces and libraries are developed by Cadence and require Cadence licenses (except for ES-Verilog). There are several product configurations, as described below:

ES-Verilog (No Charge)

This package includes the Verilog simulation models and XNF2Verilog translator. Interested users who have an in-warranty DS-502 or any "standard package" on workstations can request ES-Verilog directly through Xilinx customer service.

DS-381-SN2 (or HP7)-C

This product includes:

- Concept and Composer schematic symbols
- Verilog-XL and RapidSIM simulation models
- Netlist translators for these Cadence schematic editors and simulators

The software and documentation for the DS-381 package is already included on the Cadence compact disk that holds the other Cadence products (CD "9404" or later). Therefore, immediate access to DS-381 is available upon purchasing the license to enable it — nothing is shipped to the purchaser. *Please contact your local Xilinx sales representative for more information on how to order this license.*

DS-CDN-STD-SN2 (or HP7)-C

This product includes:

- DS-381 package (as described above)
- Xilinx 3PA package (the core implementation tools for Xilinx FPGAs and EPLDs, including X-BLOX)

Because users already have the DS-381 software and on-line documentation on their Cadence CD, only the 3PA package will be shipped after purchase. *Please contact your local Xilinx representative for information on how to order this package.*

DS-381 Product Evaluation

Any Cadence user with a "9404" or later CD can evaluate Xilinx software for 90 days by requesting a 90 day temporary license from your local Xilinx sales office.

Maintenance Contracts

Cadence customers can now move their support contract for the Cadence interface software to Xilinx by purchasing the SC-381 or SC-CDN-STD support packages. However, no updates are planned until the next release of the XACT® tools (XACT*step*, version 6); it is recommended that users maintain their Cadence maintenance contract until then. ◆

Floorplanner

Continued from previous page

The **Check Floorplan** command verifies resource allocation, three-state buffer alignment and CLB packing. If errors or warnings are found, a dialog box is used to navigate to the problem spot with a single click of the mouse. For more-detailed analysis, ratsnest views can be generated for any resource, along with routing congestion maps for any CLB(s).

Whether the design requires a few minutes of basic floorplanning or a detailed analysis and optimization, the Floorplanner can provide a tremendous boost in designer productivity and significant improvements in FPGA performance and density.

The Floorplanner can be used for XC3000A, XC3100A, XC4000, and XC5000 FPGA designs. Registered XACT development system owners with active software maintenance agreements will receive the Floorplanner in the XACT*step*, version 6 update targeted for August shipment. ◆

Upgrading to NeoCAD FPGA Foundry

Both the XACT Development™ System and NeoCAD's FPGA Foundry™ are available for implementing designs in the XC3000 and XC4000 FPGA families. Each has its respective strengths; for some high-density designs, the XACT system produces a better implementation; for others, the NeoCAD system generates a better solution.

It will take some time for the combined companies to integrate these products into a single development system. In the meantime, some current XACT users may be interested in adding the FPGA Foundry to their tool suite — particularly those users implementing very high-density FPGA designs.

For users with in-warranty XACT systems, special upgrade pricing has been established in order to allow add-on purchases of the FPGA Foundry software. Upgrade prices range from $2,700 to $3,000 (U.S.), dependent on the platform (PC or workstation). For users purchasing new systems, an "Advanced" system that contains both the XACT and FPGA Foundry software is available. *Please contact your local Xilinx sales representative for ordering codes and pricing for both new packages and upgrades.*

Designers purchasing such an upgrade should be aware that these are two different development system suites, with their own licenses, user interfaces, documentation, and packaging. Both support X-BLOX™, the Unified Libraries, and XNF file formats, but FPGA Foundry does not support XACT-Performance or the upcoming XACT-Floorplanner™. The FPGA Foundry system supports only the XC3000 (and its deriviatives — XC3000A, XC3100, XC3100A) and XC4000 FPGA families. It is available for the Windows, HP, SunOS and Solaris operating systems.

Users should review their needs with their local Xilinx Field Application Engineer before purchasing the upgrade to FPGA Foundry or the Advanced packages. ◆

Solaris Support Status

According to Sun, all programs compiled for SunOS 4.1x should work under Solaris 2.3 (and higher) in emulation mode. XACT software, for the most part, fits this category. Even though Xilinx has performed no formal testing with the Solaris operating system, some users are designing successfully with XACT-SN2 products under Solaris.

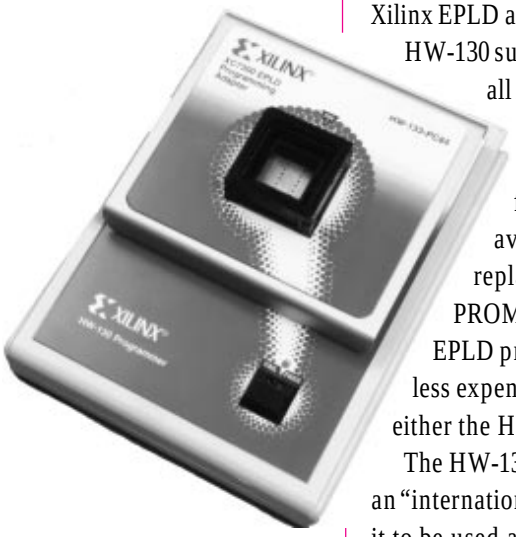
However, there are a few known problems when running under Solaris 2.3:

- FLEXLM License Manager: Running XACT under Solaris, requires a special version of the Highland License Manager program, flexlm, compiled for Solaris. This software can be requested from the Xilinx Hotline and e-mailed directly to the user.
- Mentor Interface: The gen_sch8 and xblxgs programs do not work under Solaris.
- XChecker: XChecker bitstream download and debugging are not expected to work with Solaris. Therefore, this program must be used on a SunOS machine or on a different platform (e.g., a PC).

FPGA Foundry from NeoCAD supports Solaris and is available now as an option for Xilinx users that require immediate Solaris support.

With the recent merger of Xilinx and NeoCAD, plans are being developed to support Solaris with a future combined product. ◆

HW-130 Xilinx Universal Programmer Now Available



The new HW-130 universal Xilinx device programmer is now available for Xilinx EPLD and serial PROM users. The HW-130 supports the programming of all Xilinx EPLD and serial PROM products, and will support the XC8100 FPGA family when it becomes available. This new product replaces the HW-112 serial PROM programmer and HW-120 EPLD programmer. The HW-130 is less expensive, smaller and faster than either the HW-120 or HW-112.

The HW-130 programmer comes with an "international" power supply, allowing it to be used anywhere in the world. Four versions are available *(see chart)*; varying only in the power cord supplied. The programmer comes complete with the cable that connects the HW-130 to its host PC. A full range of package adaptors is available, although the HW-130 can use most of the existing HW-120 adaptors. ◆

ORDERING PART NUMBER	PRODUCT FAMILY	SUPPORTED PACKAGE
HW-130-PC1-01	U.S., Asia	
HW-130-PC1-02	Europe	
HW-130-PC1-03	U.K.	
HW-130-PC1-04	Japan	
HW-130-CAL	Calibration	
HW-132-PC44	XC7200	PC44
HW-133-PC44	XC7300	PC44
HW-133-PQ44	XC7300	PQ44
HW-132-PC68	XC7200	PC68
HW-133-PC68	XC7300	PC68
HW-132-PC84	XC7200	PC84
HW-133-PC84	XC7300	PC84
HW-133-PQ100	XC7300	PQ100
HW-133-PQ160	XC7300	PQ160
HW-137-DIP8	XC1700	DD8/PD8
HW-137-PC20/SO8	XC1700	PC20/SO8

Full XC7000 EPLD Support Available from ISDATA

The leading European PLD compiler, ISDATA, has completely integrated an XC7000 fitter into its latest software, LOG / iC2. This design path provides designers with a seamless, easy-to-use, efficient and cost effective design environment for XC7000 EPLDs.

The LOG / iC2 development tool offers design entry, logic synthesis and simulation using the LOG / iC-HDL, schematic capture and / or VHDL in a hierarchical, graphical environment. The design can be targeted to any XC7000 device using the Xilinx-developed fitter. This flow is illustrated in the figure above.

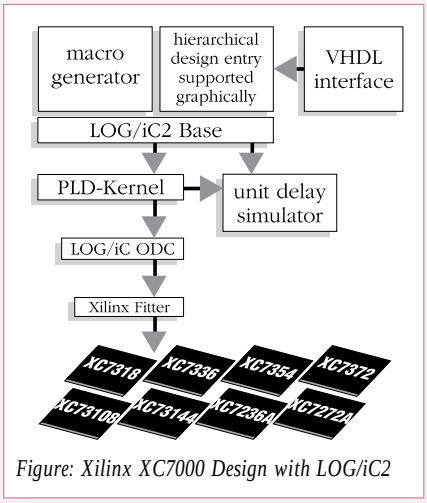


Figure: Xilinx XC7000 Design with LOG/iC2

Industry's Best "Pin Fixing" EPLDs

The XC7000 family of EPLDs offer the industry's fastest speeds (t_{PD} = 5ns) with the architectural benefit of 100 percent routability with 100 percent utilization. With this new fitter now embedded within the ISDATA tool, designers can quickly and easily implement designs with these high performance devices.

Ordering Information

The XC7000 fitter is included in the ISDATA Open Design Converter (ODC) package, and can be used with both the LOG / iC Classic and LOG / iC2 development systems. The required software for LOG / iC2 users is shown in Table 1 and can be ordered by calling ISDATA GmbH in Germany (49-721-751088) or ISDATA Inc. in the U.S. (510-531-8553). Existing LOG / iC Classic owners can upgrade their software and obtain the XC7000 fitter by ordering the upgrades shown in Table 2. ◆

Table 1. LOG/iC2 Software for XC7000 Support

LOG/iC2 Base: ..... Part # 70100
LOG/iC2 PLD Kernal: ..... Part # 72000
LOG/iC2 Open Design Converter: ..... Part # 72100

Table 2. Software Upgrades for LOG/iC Classic

LOG/iC Plus ..... Part # 10200
or
LOG/iC Perfect ..... Part # 12200
LOG/iC Open Design Converter ..... Part # 12500

Designing FPGAs with HDLs and Synthesis Tools

As the size and complexity of FPGA-based designs continue to grow, some users are turning to hardware design languages (HDLs) and logic synthesis tools to enter their designs.

To effectively use an HDL, users must understand the language syntax as well as the potential and limitations of this design entry method, especially when creating generic code intended for different devices.

To aid in this process, Xilinx is preparing a comprehensive *HDL Synthesis Design Guide for FPGAs* which will be available to users around mid-year. It will describe design methodologies and illustrate them with design examples. The guide is intended to help HDL users produce successful FPGA designs.

This article gives a brief description of some of the advantages of HDL-based design, and then briefly reviews some of the material included in the forthcoming design guide.

HDL Advantages

HDLs and synthesis tools allow the logic designer to enter designs at a higher level of abstraction, much like the software engineer who programs in 'C' instead of assembly language. The designer specifies the needed system-level functions, whereupon error-free gate level implementations are generated by the synthesis tool, freeing the designer for more creative tasks.

Users look to high-level languages and logic synthesis to provide an efficient means of migrating designs between technologies — the design's high-level description is not necessarily bound to a given device architecture or process technology. Like schematics, HDL-based designs also are self-documenting since the HDL file is the functional description of the design.

Logic synthesis tools and FPGAs complement each other in providing a flexible design environment. With HDLs, decisions can be tested early in the design cycle through functional simulation of the HDL description. Design changes are made easily, allowing experimentation and the exploration of architectural trade-offs. Synthesis tools then convert the HDL description to a gate-level implementation for the target FPGA architecture.

FPGAs further enhance this design flexibility by allowing the user to implement and test the design at the workbench. Typically, the synthesis compilation time is short enough to allow for exploration of design trade-offs at their gate-level implementation. SRAM-based FPGAs can be reprogrammed an unlimited number of times, so multiple iterations of the design can be implemented with no additional hardware cost.

FPGA-Optimized Synthesis Tools

For a top-down, HDL-based design methodology to be useful, the synthesis tools must be effective in producing a gate-level design for the target technology. Synthesis algorithms for FPGAs can be dramatically different from those used for gate arrays. Fortunately, many synthesis tools have special optimi-

Continued on next page

> *"HDLs and synthesis tools allow the logic designer to enter designs at a higher level of abstraction, much like the software engineer who programs in 'C' instead of assembly language."*

HDLs and Synthesis Tools

Continued from previous page

zation algorithms for Xilinx FPGAs.

For example, in the Synopsys FPGA Compiler, logic is synthesized into the building blocks of the FPGA: function generators (look-up tables) and registers. The FPGA Compiler reports the area utilization and critical path delays in terms of CLBs, not gates. This guarantees a high level of correlation between the reported area / speed numbers and the actual results after implementation by the place and route tools.

To address the demand for effective synthesis tools, Xilinx initiated its Synthesis Syndicate Program about two years ago, a program to assist and encourage third-party EDA vendors in developing synthesis tools for Xilinx components.

ASIC vs. FPGA Design

The methods and techniques used in ASIC design are not always best for FPGAs. ASICs typically have more gates and routing resources than FPGAs. Since ASICs have a large number of available logic resources, inefficient code that results in a larger-than-necessary number of gates often can be tolerated. When designing FPGAs, the results of inefficient coding will be magnified.

"Device performance and area utilization can be optimized by creating HDL code that takes advantage of special FPGA architectural features."

Language Issues

Not all the constructs available in an HDL may be applicable to FPGA design. For example, VHDL, which was originally developed as a simulation language and later adopted for IC design, includes a "wait" statement instructing a VHDL simulator to wait for a specified time before a condition is executed. This statement does not synthesize to any components. In a design that includes this statement, the functionality of the simulated design may not match the functionality of the synthesized design.

Various synthesis tools may also use different subsets of the VHDL language. Furthermore, constraints and compiling options can perform differently, depending on the target device.

Using FPGA System Features

Device performance and area utilization can be optimized by creating HDL code that takes advantage of special FPGA architectural features such as global resets, wide decoders, on-chip memory and carry logic — common knowledge for experienced FPGA users. However, users must learn how to access these features in an HDL-based design. Some must be "instantiated" into the code (that is, the user must explicitly specify that these resources are to be used by embedding directives within the HDL code). The user must therefore be familiar with the target FPGA architecture. The code is architecture-specific and not easily transferred to other devices.

Hierarchical Design

Hierarchical design is important in the implementation of an FPGA, particularly during floorplanning and debugging, or when using incremental design techniques. Large designs (greater than 5,000 gates) should be partitioned into smaller modules. The size and the contents of the modules can affect synthesis and implementation results.

HDL Design Flow

The design flow for FPGAs when using HDLs is very similar to that of ASICs. The basic steps are listed below:

1. Entry of the HDL code; the design should be evaluated for inefficient coding styles and for possible usage of FPGA system features.
2. Functional simulation with a VHDL or Verilog simulator. Xilinx provides VITAL compliant simulation modules that can be used with the Synopsys VSS simulator.

CONTINUED

3. Synthesis of the design's modules into XNF or EDIF netlists. The area and speed requirements should be specified before the design is synthesized.
4. Translation of the XNF file or EDIF file into a Xilinx Unified Library XNF file.
5. Functional simulation with a gate-level simulator (optional).
6. Floorplanning of structured design elements such as RPMs and on-chip memory blocks to improve routability and performance (optional).
7. Implementation of the design with the automated "place & route" tools.
8. Timing simulation with a gate-level simulator.

In summary, an increasing number of FPGA users are adopting top-down design methodologies using HDLs and logic synthesis. While still not a panacea, synthesis technology is starting to live up to its promise of enabling efficient, high-level FPGA design. ◆

Measuring Speed and Temperature

All CMOS circuits experience increased signal delay with increasing chip temperature, typically about a one percent speed degradation for every three degrees centigrade temperature increase. This is a basic phenomenon, and cannot be changed by any manufacturer.

A chip's temperature is affected by ambient temperature and device power dissipation. More specifically:

$$T_j = T_A + P_D * \theta_{JA}$$

That is, the silicon junction temperature exceeds the ambient temperature by the product of the dissipated power multiplied by the thermal resistance of the package. This thermal resistance is primarily a function of package size, package material, internal package structure and air velocity.

SRAM-based FPGAs have no significant static power consumption. Practically all internal power dissipation is due to the dynamic charging and discharging of capacitive nodes. This makes it impossible to generalize the device power consumption of Xilinx FPGAs; it can vary by orders of magnitude, depending on the application. Years ago, the power consumption was always relatively low because FPGAs were limited to less than 5,000 gate density, were often not used fully and employed clocks of 20 to 30 MHz. Today, capacity has increased beyond 20,000 gates, better software allows utilization of up to 100 percent, and clock rates can go well beyond 50 MHz. As a result, power dissipation can be several watts for the largest FPGA devices running at full speed.

This has rendered the traditional 70°C specification unsatisfactory for most demanding applications.

Xilinx has responded to this problem. We are now testing commercial devices at 85°C and industrial devices at 100°C. The new edition of the *1994 Data Book* (3rd edition) provides derating factors for higher junction temperatures (0.35 percent per °C for XC4000 devices, 0.30 percent per °C for XC3000 and XC2000 devices). The thermal resistance for the various device / package combinations, with derating values for airflow, are listed in this new edition as well.

The change to the higher test temperatures was implemented in April. All devices with date codes 9512 or later are tested in this new manner.

SRAM-based or antifuse-based FPGA performance parameters cannot be guaranteed at a specified ambient temperature, independent of power consumption and package type. Depending on the design, the clock rate and the package, the device junction temperature might vary by more than 50°C.

It is our goal to provide clearly-defined device parameters that are meaninful for the user. ◆

Board Level Simulation with

Board-level simulation capability has been added to the OrCAD VST simulator in the latest release, OrCAD VST 386+ v1.20. Users can now simulate a board-level design containing multiple Xilinx FPGAs and EPLDs.

For board-level simulation, create each Xilinx design in its own directory. Within each directory, route, back-annotate and simulate the design at the chip level. After each design has been verified, create a separate board-level directory and enter the board-level design. Copy the simulation files (.VST, .DBA) for the individual devices into the board-level directory. A board-level simulation can then be performed in the board directory. The procedures are as follows:

Create the Simulation Model Library

In order to simulate designs in VST v1.20, each device source file (.DSF) must be compiled in the VST v1.20 format. If you plan to simulate designs from different Xilinx families together or include components from other vendors on a single board design, add those DSFs to the simulation model library using OrCAD VST's *Add Device Model* command for each file. The DSFs for Xilinx are available on the Xilinx BBS as ORCSRC.ZIP. The source files are also available on the XACT 5.1 CD under XBBS\SWHELP\ORCSRC.ZIP.

"Once the custom symbol library is in place, the board level schematic can be created using the normal OrCAD SDT procedures."

Prepare Individual Chip Designs

Each FPGA / EPLD design should be captured in OrCAD SDT 386+ using normal procedures. When labeling the signals connected to the I / O pads, use easy-to-identify, intuitive names to facilitate the process of creating a chip symbol to represent the FPGA / EPLD. For board-level simulation, these signal names provide the points of connectivity to the board-level wires. Create names of 14 characters or fewer to prevent the software from creating shorter, random aliases.

After a design has been completed, use the following commands to generate the simulation files:

1: xmake <design>
(for EPLD designs, replace xmake with xemake)
2: xsimmake -f oft <design>
(for EPLD designs, replace OFT with OET)

Once the simulation files are created and the design verified, copy the simulation files (<design>.VST, <design>.DBA) to the board directory.

Create a Library of Chip Symbols

Before preparing the board level schematic, create a library of symbols to represent each device on the board (the procedure is described on pages 3-8 through 3-10 of the *XACT OrCAD Interface User Guide*, April 1994). Make certain that the symbol's pin names match the underlying I / O signal names. In addition to the user I / O signals, pins for the global signals must be added. The names of the global signals are:

- For the XC2000 and XC3000 FPGA devices, the global reset signal is GR.
- For the XC4000 FPGA devices, global set / reset is GSR, and global tristate is GTS *(if STARTUP is used, GSR and/or GTS are replaced with user signals).*
- For the XC7000 EPLD devices, global set / reset is PRLD.

Prepare the Board Level Design

Once the custom symbol library is in place, the board level schematic can be created using the normal OrCAD SDT procedures. In addition to the user-created library, the board design may also use libraries from other vendors if their DSF files have been included. Once the board design has been captured, run ANNOTATE on the schematic to update the reference designators for the symbols in the schematic. Then, from within SDT, edit the

CONTINUED

OrCAD VST

SHEETPART NAME for each Xilinx device symbol to add the following:

EXTERNALVIEW=<design>.SCH

where <design> is the root schematic worksheet for that particular chip. After adding the 'externalview' to all Xilinx devices, save the schematic, and then run INET on the board schematic to create the board-level INF simulation netlist.

Simulate the Board Level Design

Prior to simulating the board-level design, set the SIMULATE local configuration to *Use all delay annotation files (include separate dba files).* Verify that the library prefix for the digital simulation tools points to the simulation model library created in the *Create the Simulation Model Library* section above. Simulate the board-level design using <board>.INF as the connectivity database.

A detailed application note with sample design files is available on the Xilinx BBS (Bulletin Board System) under the filename: VSTBSIM.ZIP. The application note is also available via the Xilinx XDOCS system (email xdocs@xilinx.com, document key 23012). ◆

Configuration Checklist Available

A new, preliminary application note discussing FPGA configuration issues is now available on both the XFACTS and XDOCS technical support systems. The application note is intended to help determine if you have a configuration problem and, if so, suggest likely solutions. (It complements the already-exisiting application note, "FPGA Configuration Guidelines," document #0010229-01).

To get the current revision of this new document via Fax from XFACTS, please call 408-879-4400 from a touch-tone telephone and press "1" to get more information; this document is number 23021. If you are using the XDOCS E-mail system, this document can be ordered by sending the command "SEND 23021" as the subject line or in the body of a message addressed to xdocs@xilinx.com. (To learn the basics of XDOCS, please mail xdocs@xilinx.com with the word help in the subject line.)

This application note navigates you through a number of questions. Initially, you must determine if the problem is related to the configuration process or the functionality of the configured FPGA (Is there a problem with the functionality of a correctly-configured device, or has the configuration actually failed?)

There are several clues as to whether or not the FPGA has been successfully configured:

1. **INIT—** If configuring from power-up, does INIT go through a single positive transition from Low to High? If the FPGA is not working after it is reprogrammed, is there a single negative transition (High to Low) on INIT, followed by a single positive-going transition?
2. **DONE —** Does DONE go High?.
3. **I/Os** —Are your I/Os at their active post-configuration levels? HDC is High during configuration, and LDC should be Low during configuration. Most other pins have weak pullups during configuration. If you configure the device to pass a clock signal in through an input and out through an output pad, does the output pin toggle at the end of configuration? If you configure one user I/O to drive Low at the end of configuration, and another to drive High, are both I/Os driving the proper logic levels at the end of configuration?
4. **Flip-Flops —** Are your flip-flops toggling?

If you can answer YES to these questions, you can be fairly certain that your FPGA has been configured properly, and that the problem involves the functionality of your design, not the configuration method.

Please note that this document is preliminary and feedback is very much appreciated; feedback can be sent by E-mail to hotline@xilinx.com or by FAX to 408-879-4442. ◆

General

Q: The Technical Support Hotline hours are Monday through Friday, 8:00AM - 5:00PM Pacific time. Is there any way to get technical help outside of these hours?

A: Xilinx has implemented a fax-back system and an automated email server, both of which operate 24 hours a day. These systems will give you access to the same database used by the Technical Support Engineers.

The XFACTS automated fax-back system can send solution records and application notes directly to your fax machine. Using a touch-tone phone, call 1-408-879-4400 and press "1" to get more information.

The XDOCS email server can send the same information via the internet. For more information on this system, send an email to xdocs@xilinx.com, with the word help in the subject line.

Q: When I try to install the software on my PC, I get the message "Corrupted file on your media. DSxxx cannot be completely installed." What should I do?

A: The Install program will give this error message if it cannot write a file or if it cannot verify a file that it has just tried to write. There are three possible causes of this message:

1) You don't have write privileges to the target directory.
Not having write privileges prevents the program from being able to open a new directory or overwrite existing DOS files, so check to make sure none of the file attributes have been set to read-only. If you are installing on a network drive, make sure you are logged in as someone who can write to the destination area.

2) The PC has run out of memory below 640KB.
In addition to being able to start the Install program itself, PCs must have enough memory to decompress the data files stored on the CD or disks. Remove some drivers from the CONFIG.SYS and AUTOEXEC.BAT files, reboot the PC, and try the installation again. If the Install program gets further but still fails, remove more drivers and try again.

3) Problems exist with the setup of the CD-ROM drive.
We have seen multiple cases, especially with the MSCDEX drivers, where the CD-ROM drive software has not been installed correctly. Check to be sure that the proper parameters are set for the driver. If all else fails, call the Technical Support Hotline at 1-800-255-7778 for more assistance.

XABEL

Q: While running AHDL2X v5.0 on a Pentium 90 MHz PC, I receive a message indicating that my key is not authorized to run XABEL. What could be the cause of this problem?
(Note: This question appeared in XCELL #16 with an incorrect description of the solution.)

A: The XABEL 5.0 package includes executables supplied to Xilinx by Data I/O. Unfortunately, these programs were compiled with an older version of the Rainbow key software and will not run on some faster machines, like the Pentium-90MHz and IBM PS/2 platforms. These programs have been re-compiled and updated in the XACT 5.1 release. They also are available on the Xilinx BBS as XABEL.ZIP.

Synopsys

Q: I am just starting my first Xilinx design with the Synopsys FPGA Compiler. How should I set up my .synopsys_dc.setup file?

A: Below is a sample .synopsys_dc.setup file for doing an XC4000 family design. Be sure to edit the search path so that it points to the correct location of the libraries.

```
/* EXAMPLE FPGA COMPILER STARTUP FILE - .synopsys_dc.setup */
/* FOR XC4000/A/H/D PARTYPES    */
search_path = { .       \
        <DS401-XACT-Directory>/synopsys/libraries/syn \
        <SYNOPSYS_Directory>/libraries/syn}
link_library = {xprim_4005-5.db xprim_4000-5.db xgen_4000.db \
        xio_4000-5.db xfpga_4000-5.db}
target_library = {xprim_4005-5.db xprim_4000-5.db xgen_4000.db \
        xio_4000-5.db xfpga_4000-5.db}
symbol_library = xc4000.sdb
define_design_lib WORK -path ./WORK
define_design_lib xblox_4000 -path \
        <DS401-XACT-Directory>/synopsys/libraries/dw/lib/fpga
synthetic_library = {xblox_4000.sldb standard.sldb}
compile_fix_multiple_port_nets = true
xlnx_hier_blknm = 1
xnfout_library_version = "2.0.0"
bus_naming_style = " percents< percentd>"
bus_dimension_separator_style = "><"
bus_inference_style = " percents< percentd>"
```


OVERVIEW OF TECHNICAL SUPPORT FACILITIES

Automated Support Systems

To provide timely support for new, high-growth markets, Xilinx Applications has established a series of E-mail addresses to direct technical inquiries or to request information packets.

Currently, these E-mail addresses include:

Digital Signal Processing applications ..... dsp@xilinx.com
PCI-bus applications ..... pci@xilinx.com
Plug and Play ISA applications ..... pnp@xilinx.com
Asynchronous Transfer Mode applications ..... atm@xilinx.com
General questions should still be routed to ..... hotline@xilinx.com
PCMCIA card applications ..... pcmcia@xilinx.com
Reconfigurable logic/computing applications ... reconfig@xilinx.com

Other Xilinx interactive services include the XDOCS automated document server, the XFACTS fax server, and the Xilinx World Wide Web home page.

To access the XDOCS E-mail document server, send an E-mail to xdocs@xilinx.com with "help" as the only item in the subject header. You will automatically receive full instructions via E-mail. The Xilinx home page is available at http://www.xilinx.com. The XFACTS fax server is available by calling 1-408-879-4400.

Hotline Support, United States

Customer Support Hotline: 800-255-7778
Hrs: 8:00 a.m. - 5:00 p.m. Pacific time
Customer Support Fax Number: 408-879-4442
Avail: 24 hrs/day-7 days/week
Electronic Technical Bulletin Board: 408-559-9327
Avail: 24 hrs/day-7 days/week
Customer Service: ..... 408-559-7778, ask for customer service
For software updates, authorization codes, documentation updates, etc.

Hotline Support, Europe

UK , LONDON OFFICE
telephone: (44) 1932 349402
fax: (44) 1932 333530
Bulletin Board Service: (44) 1932 333540
e-mail: ukhelp@xilinx.com

FRANCE, PARIS OFFICE
telephone: (33) 1 3463 0100
fax: (33) 1 3463 0109
e-mail: frhelp@xilinx.com

GERMANY, MUNICH OFFICE
telephone: (49) 89 991 5490
fax: (49) 89 904 4748
e-mail: dlhelp@xilinx.com

3.3 Volt Programmable Logic Market Survey

We are investigating the low voltage (3.3 V) market. If you are using or anticipate using 3.3 V programmable logic devices in the future, please take a couple of minutes to fill out this short survey and send it back to us. Return your survey via FAX at 408-879-4676, or mail to:

Daniel Chan
Product Marketing
Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124

We sincerely appreciate your time and effort.

Manchester Decoder in 3 CLBs

Xilinx FPGA architectures are ideal for implementing high-speed, efficient serial decoders. For example, the circuit illustrated below uses an eight-times oversampling clock to decode Manchester-encoded data. The circuit requires only three CLBs in any XC3000, XC3100 or XC4000-type device, and only two CLBs in an XC5200 device.

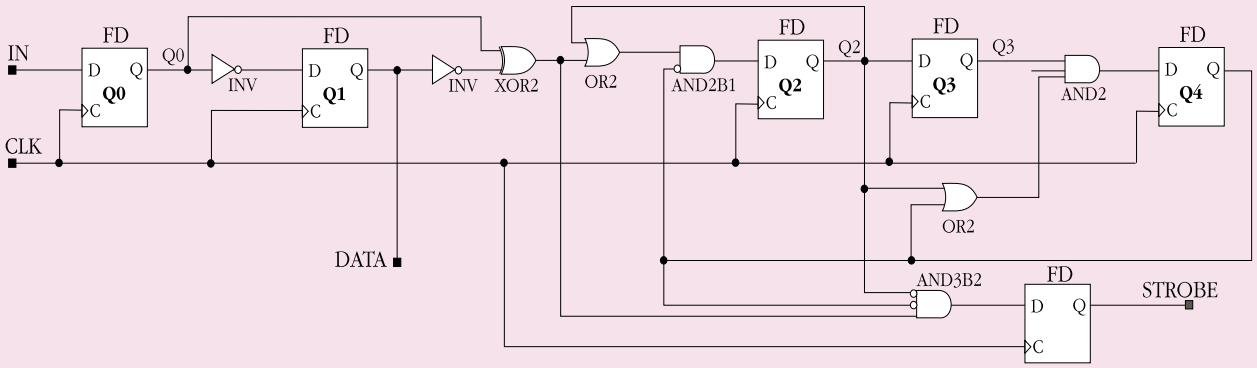
Manchester code is a self-clocking code with a minimum of one and a maximum of two level transitions per bit. A Zero is encoded as a Low-to-High transition, a One is encoded as a High-to-Low transition. Between two identical bits of data there is an extra level transition which must be ignored by the decoder. The decoder, therefore, needs some information about the bit timing. Typically, the decoder has a clock with timing that is a known multiple of the encoding clock.

This design assumes a decode clock at nominally eight times the incoming data rate. After detecting a valid transition, the circuit ignores further transitions for six clock periods. Thus, the circuit tolerates substantial frequency errors between encoder and decoder.

Q0 and Q1 are XORed to detect any incoming level change. Q2 / Q3 / Q4 form a divide-by-six Johnson counter that locks up in the 000 state. (The illegal 010 state is also detected and changed to 000 on the next clock edge.) When the Johnson counter has timed out and is in the 000 state, any incoming level transition generates a pipelined STROBE signal which qualifies Q1 as DATA. On the next clock edge, the Johnson counter changes to 100, which terminates the strobe. For the following five clock periods, any incoming level changes are detected, but the XOR output is ignored. When the Johnson counter again reaches 000, it locks up and enables the XOR signal. Any simultaneously or subsequently detected level change starts a new operation as described above.

The decoder clock can be asynchronous to the incoming data, but must be faster than five times the incoming bit rate (in order to detect the next bit transition), and slower than 12 times the incoming bit rate (in order to suppress the between-bit transition). The nominal decode clock frequency should, therefore, be eight times the incoming data rate.

The circuit has been simulated for worst-case performance in excess of 200 MHz clock rate (25 MHz incoming data rate) in an XC3120-2 device. The circuit uses only three CLBs — less than 5 percent of the logic available in an XC3120 FPGA, and less than 1 percent of an XC3190 device. ◆



3.3 V Fax Back Survey

To: Daniel Chan, Product Marketing Manager, Xilinx Inc.

Please FAX your completed survey to (408) 879-4676 or mail to the address below by July 28 to be automatically eligible to win a Sony Watchman!

Personal (optional): Name _____ Company _____ Phone: ( ) _____

1. In which market(s) do you participate?

❑PCMCIA ❑Computer Systems
❑PCI ❑Memory Systems
❑ATM ❑Computer Peripherals
❑Hand-held instruments
❑ Other _____

2. Your company size (annual sales)?

❑ < $10 million
❑ $10 million - $100 million
❑ > $100 million

3. Which type of 3.3V IC products do you think you need or will need for your designs?

❑ 3.0V to 3.6V (regulated power supply)
❑ 2.7V to 3.6V (unregulated power supply)

4. In terms of the 3-V Programmable Logic Device market, please rank the following features in order of importance *(1 - highest importance, 9 - lowest importance):*

__ - speed of device / system clock rate
__ - quiescent current
__ - power consumption / dissipation
__ - supply voltage 3.0V - 3.6V Vcc only
__ - 5V tolerance (3V Vcc with 5V or 3V I/O)
__ - package style (PLCC, TQFP...)
__ - operating temperature (Commercial, Industrial, Military)
__ - price
__ - gate density

5. What is the predominant package style desired for a 3-V PLD device?

❑PLCC ❑VQFP ❑PQFP
❑TQFP ❑ _____

6. What is your typical I/O requirement for a 3-V programmable logic device (check one of the following for a and b)?

a) ❑ < 86 I/O ❑ 87 - 100 I/O
❑ 100 - 150 I/O ❑ > 150 I/O
b) ❑ GTL ❑ TTL ❑ CMOS

For questions 7 - 11, please indicate the attributes that you estimate will be needed in 3.3V programmable logic devices to meet your requirements.

7. Ambient operating temperature?

❑ Commercial: 0°C to 70°C
❑ Industrial: -40°C to 85°C
❑ Military: -55°C to 125°C

8. Estimated gate density per device?

(Select one column for each row.)

Gates	< 3K	3K - 6K	6K - 10K	> 10K
Today				
1997				
2000				

9. Maximum quiescent current? *(Select one column per row).*

	< 1µA	1µA-1mA	1mA-10mA	> 10mA
Today				
1997				
2000				

10. System clock speed? *(Select one column for each row.)*

System Clock	< 33 MHz	34-50 MHz	51-66 MHz	67-100 MHz	> 100 MHz
Today					
1997					
2000					

11. Supply voltage-I/O option? *(Select one row for each column.)*

	Today	1996	1997
IC with single operating voltage anywhere from 3V to 5V (speed degradation at lower voltage)			
Dual supply - 5V core and 3V or 5V I/O			
Single 3V supply with 5V tolerant I/O			
Single 3V supply only with 3V I/O			
Other core and I/O combination:			

If you choose not to fax this survey, mail it to:

Daniel Chan, Product Marketing
Xilinx Inc., 2100 Logic Drive, San Jose, CA 95124

Corporate Headquarters
Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Tel: 408-559-7778
Fax: 408-559-7114

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Surrey KT147DU
United Kingdom
Tel: 44-1-932-349401
Fax: 44-1-932-349499

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2-8-5, Hatchobori,
Chuo-ku, Tokyo 104
Japan
Tel: 81-3-3297-9191
Fax: 81-3-3297-9189

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