WD76C30A/LV Peripheral Controller, Interrupt Multiplexer, and Clock Generator Device

WESTERN DIGITAL

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 DESCRIPTION

1.1 WD76C30ALV FEATURES

- Two fully programmable and independent serial I/O ports, configurable as PC/AT compatible (WD16C452) or PS/2 compatible (WD16C552)
  - o Loopback controls for communications link fault isolation for each ACE
  - o Line break generation and detection for each ACE
  - o Complete status reporting capabilities
  - o Generation and stripping of serial asynchronous data control bits (start, stop, parity)
  - o Programmable baud rate generator and Modem control signals for each port
  - o Programmable baud rate generator input clock
  - o Optional 16 byte FIFO buffers on both transmit and receive of each port for CPU relief during high speed data transfer
  - o Programmable FIFO threshold levels of 1, 4, 8, or 14 bytes on each port
- Parallel port configurable as a fully Centronics or PS/2 compatible, bidirectional parallel port
- Independently programmable parallel port
- Interrupt multiplexing logic
  - o Selectable multiplexing logic for connecting PC/AT interrupt request lines to the single chip Western Digital System AT controllers
- Clock generation circuitry
  - o 80287 coprocessor clock generation
  - o Western Digital System Controllers and floppy controller clock generation
  - o 8042 keyboard clock generation
- Fast Parallel Port (FPP) Function (100-Pin package only)
- 3.3 Volt operation
- Built-in testability features
- Hardware or software controllable sleep mode
- CMOS implementation for high speed and low power requirements
- Pulse extension on IRQ inputs
- 84-pin PQFP package
- 100-pin SQFP package

1.2 GENERAL

The WD76C30ALV device provides three functional groups, Peripheral Controller, Interrupt Multiplexer and Clock Generator.

The low power CMOS WD76C30ALV is a single device solution which provides interrupt multiplexing logic, clock generation, two serial ports and one bidirectional parallel port. The WD76C30ALV[SK] can be configured to operate as a Fast Parallel Port (FPP).

Interrupt multiplexing logic interfaces the PC/AT interrupt request lines with the single chip Western Digital System Controller.

Integrated clock generation circuitry uses the 48 MHz input signal to generate the 1.8462, 3.072 and 8.0 MHz clocks used internally for the two serial ports, a 9.6 MHz signal used for the keyboard controller and floppy controller, a programmable duty/frequency clock for the 80287 coprocessor and a 16 MHz clock for driving the single chip Western Digital System Controller and floppy controller.

For low power implementations such as laptops, oscillator disable and sleep modes are available to power down unused logic.

The WD76C30ALV is capable of operating on a 5 volt supply or a combined 5 volt and 3.3 volt supply. The WD76C30ALV requires a 5 volt supply for the parallel port, while the core logic can operate on either a 3.3 or 5 volt supply.

The bidirectional parallel port is software configurable as either a PC/AT or a PS/2 compatible port. The parallel port data lines and open drain printer signals have high current drive capabilities.

Each ACE is programmable as either a WD16C550 or WD16C450 compatible device. Each WD16C550 configured ACE is capable of buffering up to 16 bytes of data upon reception, relieving the CPU of interrupt overhead. Buffering of data also allows greater latency time in interrupt servicing

which is vital in a multitasking environment. Each ACE has a maximum recommended data rate of 512 Kbaud.

1.3 PERIPHERAL CONTROLLER

The peripheral controller is functionally equivalent to the WD16C452/552. The mode of operation of the serial ports and parallel port is selectable via the Mode Select Register. Each serial port is configurable as either a FIFO enhanced ACE (WD16C550 compatible) or a standard ACE (WD16C450). The parallel port is configurable as either a PS/2 bidirectional parallel port or a PC/AT compatible parallel port. A detailed description of the Mode Selection Register is presented in Section 5.5.

1.4 FAST PARALLEL PORT

The WD76C30ALV[SK] provides the ability to operate one parallel port device on a cable length of two meters, providing a 2.0 MByte Fast Parallel Port (FPP) with an 8 MHz AT-bus and a 2.5 MByte FPP with a 10 MHz AT-bus.

The FPP has the option of operating with zero wait states for maximum data transfer capability.

The Fast Parallel Port feature is only provided by the 100-pin SQFP packaged device.

1.5 PACKAGING

WD76C30ALV[SK]	100-PIN SQFP
WD76C30ALV[LD]	84-PIN PQFP

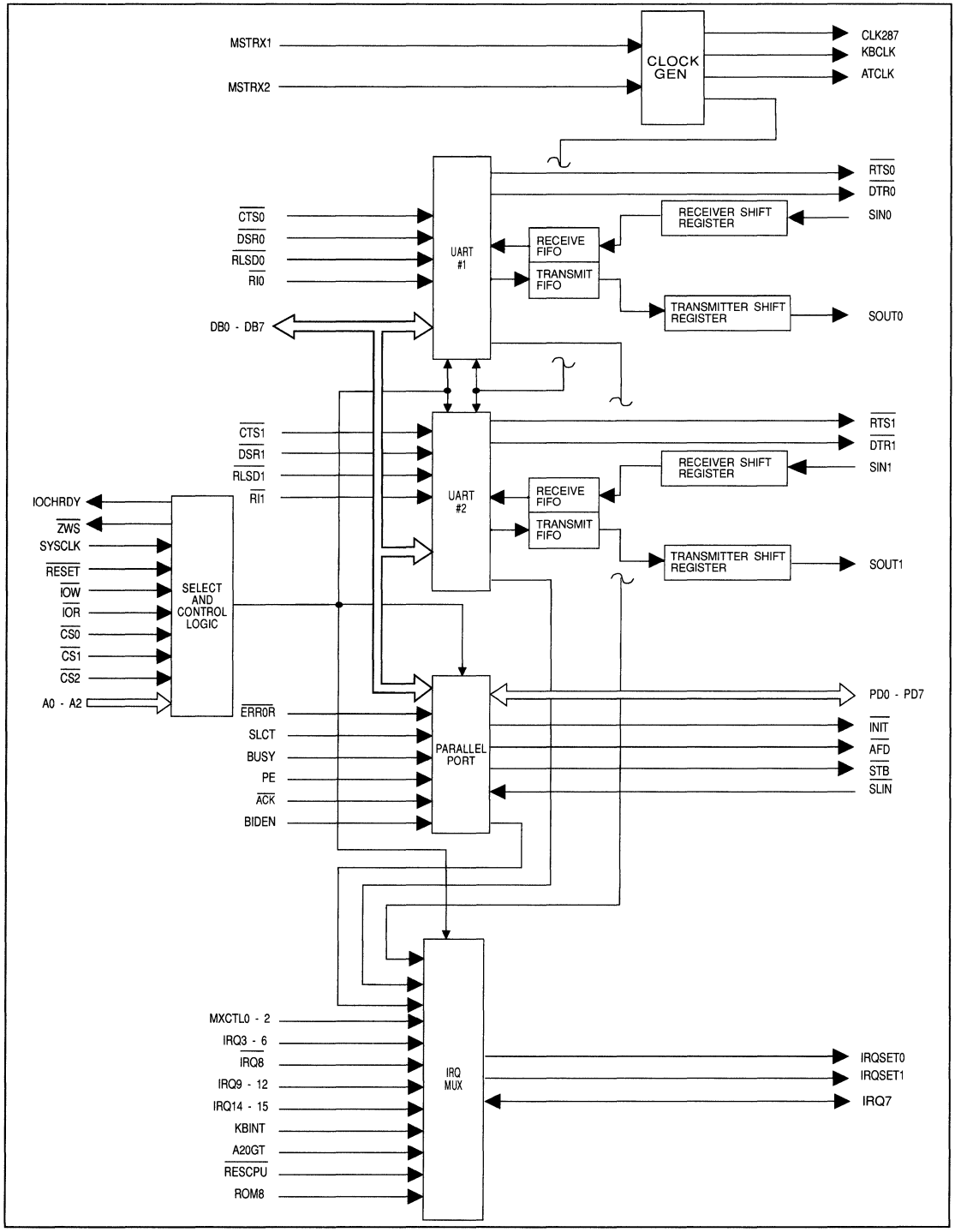


FIGURE 1-1. WD76C30ALV BLOCK DIAGRAM

2.0 SIGNAL DESCRIPTION

A drawing of the 84-pin PQFP package, showing the pin and signal locations, is provided in Figure 2-1. A drawing of the 100-pin SQFP package, showing the pin locations only, is provided in Figure 2-2. Table 2-1 provides a list of signal to pin assignments for the 100-pin SQFP package. Table 2-2 provides a description of the signals controlled by the 84-pin PQFP and 100-pin SQFP package. The DC operating characteristics and timing are presented in section 6.

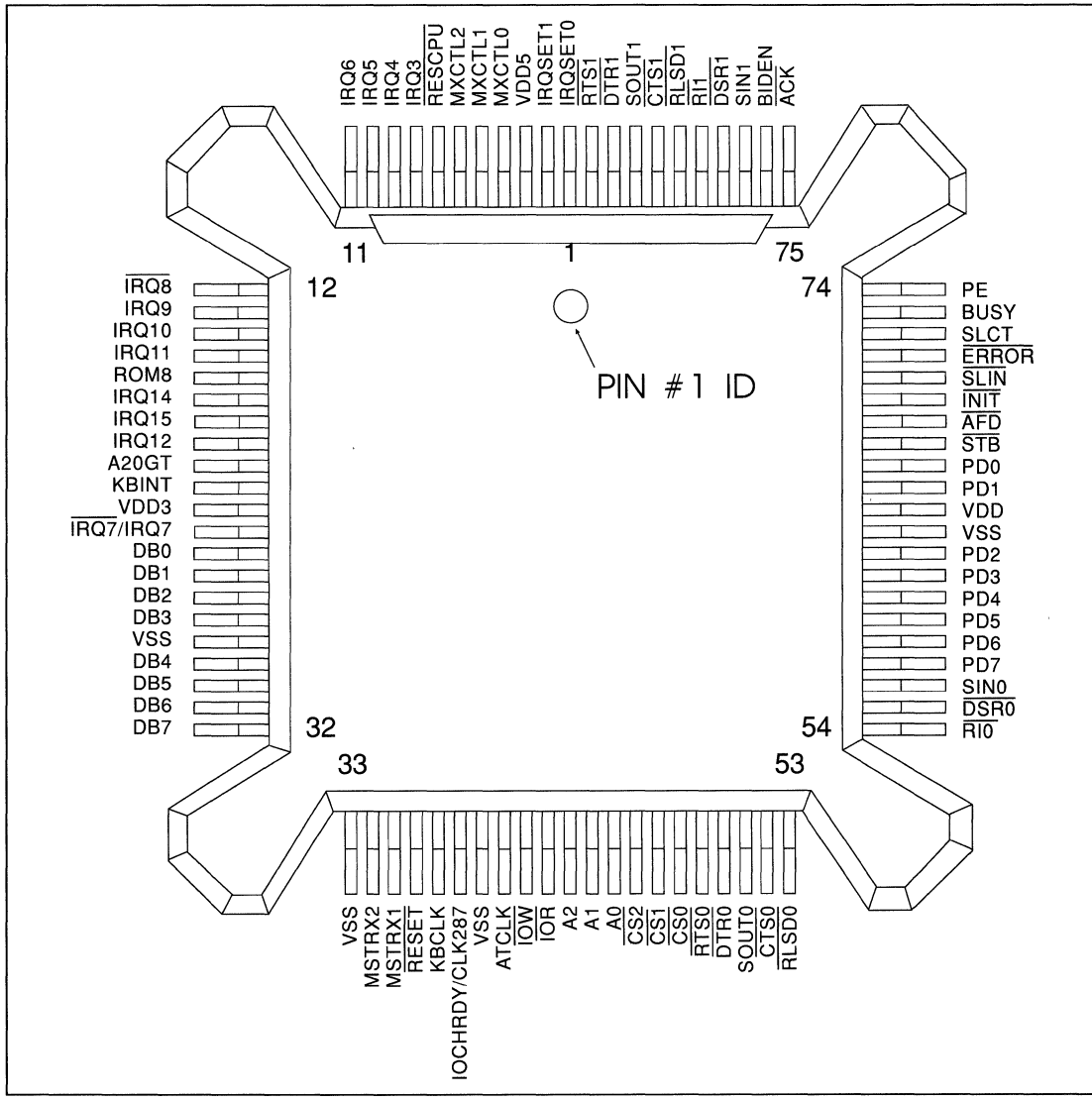


FIGURE 2-1. 84-PIN PQFP - SIGNAL/PIN ASSIGNMENT

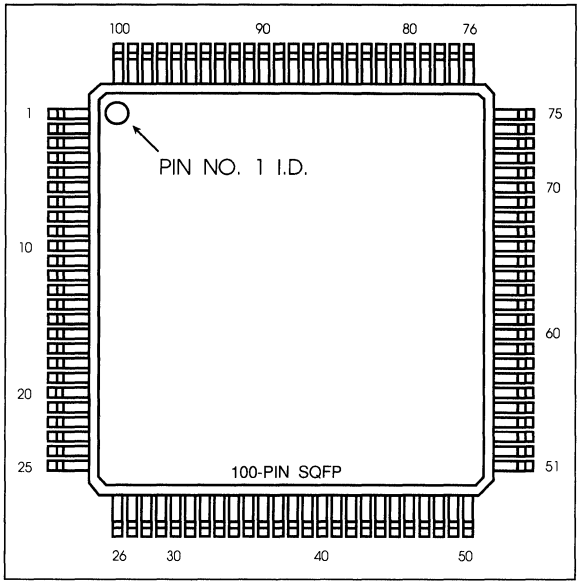


FIGURE 2-2. 100-PIN SQFP PACKAGE

PIN - NAME	PIN - NAME	PIN - NAME	PIN - NAME
1 - N.C.	26 - N.C.	51 - N.C.	76 - N.C.
2 - N.C.	27 - IRQ8	52 - ZWS	77 - N.C.
3 - ACK	28 - IRQ9	53 - VSS	78 - N.C.
4 - BIDEN	29 - IRQ10	54 - MSTRX2	79 - DSR0
5 - SIN1	30 - IRQ11	55 - MSTRX1	80 - SIN0
6 - DSR1	31 - SYSCLK	56 - RESET	81 - PD7
7 - RI1	32 - ROM8	57 - KBCLK	82 - PD6
8 - RLSD1	33 - IRQ14	58 - CLK287/IOCHRDY	83 - PD5
9 - CTS1	34 - IRQ15	59 - VSS	84 - PD4
10 - SOUT1	35 - IRQ12	60 - ATCLK	85 - PD3
11 - DTR1	36 - A20GT	61 - IOW	86 - PD2
12 - RTS1	37 - KBINT	62 - IOR	87 - VSS
13 - IRQSET0	38 - VDD3	63 - A2	88 - VDD
14 - IRQSET1	39 - IRQ7/IRQ7	64 - A1	89 - PD1
15 - VDD5	40 - DB0	65 - A0	90 - PD0
16 - MXCTL0	41 - DB1	66 - CS2	91 - STB
17 - MXCTL1	42 - DB2	67 - CS1	92 - AFD
18 - MXCTL2	43 - DB3	68 - CS0	93 - INIT
19 - RESCPU	44 - VSS	69 - RTS0	94 - SLIN
20 - IRQ3	45 - DB4	70 - DTR0	95 - ERROR
21 - IRQ4	46 - DB5	71 - SOUT0	96 - SLCT
22 - IRQ5	47 - DB6	72 - CTS0	97 - BUSY
23 - IRQ6	48 - DB7	73 - RLSD0	98 - PE
24 - N.C.	49 - N.C.	74 - RI0	99 - N.C.
25 - N.C.	50 - N.C.	75 - N.C.	100 - N.C.

TABLE 2-1. 100-PIN SQFP - SIGNAL/PIN ASSIGNMENTS

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
76 - 4	BIDEN	I	**Bidirectional Enable** When de-asserted, BIDEN enables the parallel port data lines as outputs. When asserted, BIDEN works in conjunction with the DIR bit (see Table 4-3) to control the direction of the parallel port data bit.
78 - 6 55 - 79	$\overline{DSR1}$ $\overline{DSR0}$	I	**Data Set Ready 1 and 0** The communication link asserts these signals to indicate that it is ready to exchange data with the associated Asynchronous Communications Element (ACE). Bit 5 of the associated Modem Status Register represents the logical state of $\overline{DSR(1:0)}$.
79 - 7 54 - 74	$\overline{RI1}$ $\overline{RI0}$	I	**Ring Indicator 1 and 0** When asserted, these signals indicate that a ringing signal for the associated ACE is being received by the Modem or data set. This logical value is represented by bit 6 of the associated Modem Status Register.
80 - 8 53 - 73	$\overline{RLSD1}$ $\overline{RLSD0}$	I	**Received Line Signal Detect 1 and 0** The Data Circuit-terminating Equipment (DCE) asserts these signals when the associated ACE is receiving a signal that meets its signal quality conditions. Bit 3 of the associated Modem Status Register represents this value.
82 - 10 51 - 71	SOUT1 SOUT0	O	**Serial Data Output 1 and 0** SOUT1 is the transmitted Serial Data Output from ACE#1 to the communication link. SOUT0 is the transmitted Serial Data Output from ACE#0 to the communication link. The SOUT signals are set to a marking condition (logical 1) upon a Master Reset.
77 - 5 56 - 80	SIN1 SIN0	I	**Serial Data Inputs 1 and 0** SIN1 is the received Serial Data Input from the communication link to ACE#1. SIN0 is the received Serial Data Input from the communication link to ACE#0. Data on the serial data inputs are disabled when exercising loop back mode and internally connected to their respective SOUT lines.
83 - 11 50 - 70	$\overline{DTR1}$ $\overline{DTR0}$	O	**Data Terminal Ready 1 and 0** When asserted, the Data Terminal Ready informs the Modem or Data Set that the associated ACE is ready to receive. This value is controlled by bit 0 of the Modem Control Register.

TABLE 2-2. SIGNAL DESCRIPTION

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
84 - 12 49 - 69	$\overline{RTS1}$ $\overline{RTS0}$	O	**Request To Send 1 and 0** When asserted, the Request To Send informs the Modem or Data Set that the associated ACE is ready to transmit data. This value is controlled by bit 1 of the Modem Control Register. During reset $\overline{RTS0}$ controls the input thresholds of all inputs capable of operating at 3.3 volts. $\overline{RTS0}$ = 0 - Mixed Mode 3.3 volt operation $\overline{RTS0}$ = 1 - Normal 5 volt operation There is a small internal pullup resistor that is activated when the output is disabled during reset. The minimum value of this resistor at 3.3 volts is 180K.
81 - 9 52 - 72	$\overline{CTS1}$ $\overline{CTS0}$	I	**Clear To Send 1 and 0** The DCE asserts the $\overline{CTS(1:0)}$ to signal the associated ACE that a remote device is ready to transmit. This value is represented by bit 4 of the Modem Status Register.
32 - 48 31 - 47 30 - 46 29 - 45 27 - 43 26 - 42 25 - 41 24 - 40	DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0	I/O	**Data Bits** The Data Bits are tristate, bidirectional communication lines between the WD76C30ALV and Data Bus. DB0 is the least significant bit and the first serial bit to be transmitted or received.
43 - 63 44 - 64 45 - 65	A2 A1 A0	I	**Address lines A2, A1, A0** Address Lines A2, A1 and A0 are used to select the registers internal to the WD76C30ALV.
41 - 61	$\overline{IOW}$	I	**Input/Output Write Strobe** When $\overline{IOW}$ is asserted, data is written to the Port's addressed register from the Data Bus (DB7:0). The register is addressed by Address Lines A(2:0). ACE#0, ACE#1 or the Parallel Port is selected by $\overline{CS0}$, $\overline{CS1}$ or $\overline{CS2}$ respectively.
42 - 62	$\overline{IOR}$	I	**Input/Output Read Strobe** When $\overline{IOR}$ is asserted, data is read from the Port's addressed register and placed on the Data Bus (DB7:0). The register is addressed by Address Lines A(2:0). ACE#0, ACE#1 or the Parallel Port is selected by $\overline{CS0}$, $\overline{CS1}$ or $\overline{CS2}$ respectively.
48 - 68	$\overline{CS0}$	I	**Chip Select 0** $\overline{CS0}$ when asserted, selects serial port 0.
47 - 67	$\overline{CS1}$	I	**Chip Select 1** $\overline{CS1}$ when asserted, selects serial port 1.
46 - 66	$\overline{CS2}$	I	**Chip Select 2** $\overline{CS2}$ when asserted, selects parallel port.

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
36 - 56	$\overline{\text{RESET}}$	I	**Reset** When asserted, $\overline{\text{RESET}}$ forces the WD76C30ALV into an idle mode in which all serial data activities are terminated. The IRQ MUX is forced into a non-compatible mode. The WD76C30ALV remains in the idle state until programmed to begin data activities.
57 - 81 58 - 82 59 - 83 60 - 84 61 - 85 62 - 86 65 - 89 66 - 90	PD7 PD6 PD5 PD4 PD3 PD2 PD1 PD0	I/O	**Parallel Data Port** Bidirectional data port, providing parallel input and output to the parallel port.
67 - 91	$\overline{\text{STB}}$ ④	I/O	**Line Printer Strobe** When not in the FPP mode, asserting $\overline{\text{STB}}$ signals the line printer to latch the data currently on the parallel port, PD(7:0). When in the FPP mode, $\overline{\text{STB}}$ indicates a read/write operation to/from the parallel port is taking place. $\overline{\text{STB}}$ = 0 - Indicates a write to the parallel port. $\overline{\text{STB}}$ = 1 - Indicates a read from the parallel port.
68 - 92	$\overline{\text{AFD}}$ ④	I/O	**Line Printer Autofeed** When not in the FPP mode, asserting $\overline{\text{AFD}}$ signals the line printer to autofeed continuous form paper. When in the FPP mode, $\overline{\text{AFD}}$ indicates a data transfer operation to/from the parallel port is taking place. $\overline{\text{AFD}}$ = 0 - Indicates a data transfer. $\overline{\text{AFD}}$ = 1 - Indicates no data transfer.
69 - 93	$\overline{\text{INIT}}$ ①	I/O	**Line Printer Initialize** When asserted, $\overline{\text{INIT}}$ signals the line printer to begin an initialization routine.
70 - 94	$\overline{\text{SLIN}}$ ④	I/O	**Line Printer Select** When not in the FPP mode, asserting $\overline{\text{SLIN}}$ selects the line printer. When in the FPP mode, $\overline{\text{SLIN}}$ indicates an address transfer operation to/from the parallel port is taking place. $\overline{\text{SLIN}}$ = 0 - Indicates an address transfer. $\overline{\text{SLIN}}$ = 1 - Indicates no address transfer.

① This output is open drain with internal pull-up.
④ When not in FPP mode, these outputs are open drain with internal pull-up. When in FPP mode, these outputs are tristate buffers. They have sourcing capability of 10 mA at Voh of 2.4 volts in 3.3 volt operation.

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
71 - 95	$\overline{\text{ERROR}}$	I	**Line Printer Error** The printer asserts $\overline{\text{ERROR}}$ to inform the parallel port of a deselect condition, PE or other error condition.
72 - 96	SLCT	I	**Line Printer Select** The line printer asserts SLCT when it has been selected.
73 - 97	BUSY	I	**Line Printer Busy** The line printer asserts BUSY when it is performing an operation.
74 - 98	PE	I	**Line Printer Paper Empty** The line printer asserts PE when it is out of paper.
75 - 3	$\overline{\text{ACK}}$	I	**Line Printer Acknowledge** The line printer asserts $\overline{\text{ACK}}$ to confirm that the data transfer from the WD76C30ALV to the printer was successful.
4 - 16 5 - 17 6 - 18	MXCTL0 MXCTL1 MXCTL2	I	**IRQ MUX Control** MXCTL(0:2) are encoded select signals generated by the Western Digital System Controller for sampling the IRQ inputs.
8 - 20 9 - 21 10 - 22 11 - 23 12 - 27 13 - 28 14 - 29 15 - 30 19 - 35 17 - 33 18 - 34	IRQ3 IRQ4 IRQ5 $\overline{\text{IRQ6}}$ $\overline{\text{IRQ8}}$ IRQ9 IRQ10 IRQ11 IRQ12 IRQ14 IRQ15	I	**IRQ MUX Inputs** These 11 interrupt signals, along with $\overline{\text{IRQ7}}$, $\overline{\text{RESCPU}}$, ROM8, KBINT and A20GT, are multiplexed into IRQSET0 and IRQSET1 at a period rate defined by MXCTL(0:2). During reset, $\overline{\text{IRQ8}}$ determines whether pin 38/58 represents CLK287 or IOCHRDY. $\overline{\text{IRQ8}}$ high, pin 38/58 represents CLK287 $\overline{\text{IRQ8}}$ low, pin 38/58 represents IOCHRDY

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
23 - 39	IRQ7/$\overline{IRQ7}$	I/O	**Interrupt Request 7** IRQ7/$\overline{IRQ7}$ is an input to the IRQ MUX when the WD76C30ALV is not in the Stand Alone Mode. IRQ7/$\overline{IRQ7}$ is output as the Parallel Port Interrupt when the WD76C30ALV is in the Stand Alone Mode (refer to section 5.6, 5.7). When operating as the Parallel Port Interrupt, IRQ7/$\overline{IRQ7}$ is a tristate signal and must be enabled by bit 4 in the Write Control Register (refer to section 4.3). When the Parallel Port Interrupt is PC/AT compatible, this signal is IRQ7 and is asserted at the rising edge of ACK and de-asserted at the falling edge of $\overline{ACK}$. When the Parallel Port is PS/2 compatible, this signal is $\overline{IRQ7}$ and is asserted at the rising edge of $\overline{ACK}$ and de-asserted at the rising edge of $\overline{IOR}$, while reading the Parallel Port Status Register.
7 - 19	$\overline{RESCPU}$	I	**Reset CPU** The keyboard controller asserts $\overline{RESCPU}$ when the CPU should be reset.
16 - 32	ROM8	I	**8-Bit ROM** ROM8 is multiplexed into the IRQSET1 signal and, when asserted, indicates to the Western Digital System Controller that the system ROM is eight bits, when de-asserted it is 16 bits.
- 31	SYSCLK	I	**SYSTEM CLOCK** SYSCLK provides synchronization timing for $\overline{ZWS}$ and IOCHRDY. Not featured in the 84-pin PQFP device.
21 - 37	KBINT	I	**Keyboard Interrupt** KBINT is multiplexed into the IRQSET1 signal and indicates to the Western Digital System Controller that a keyboard interrupt is pending.

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
20 - 36	A20GT	I	**Address 20 Signal** A20GT is multiplexed into the IRQSET1 signal and reflects the state of the address 20 signal. This allows compatibility with the 8086 and 80286 processors when addressing memory in the 64 Kbyte boundary above 1 Mbyte.
35 - 55	MSTRX1 ②	I	**Master Clock 1** The MSTRX1 signal can be driven by either a 16 MHz crystal or 48 MHz TTL oscillator.
34 - 54	MSTRX2 ②	O	**Master Clock 2** MSTRX2 is connected to the 16 MHz crystal to generate MSTRX1 for the clock generation circuitry. This pin is left disconnected if Master Clock 1 is being driven by a 48 MHz TTL oscillator.
38 - 58	CLK287/ IOCHRDY	O	**80287 Clock - I/O Channel Ready** Whether this pin functions as CLK287 or IOCHRDY is dependent upon the state of $\overline{IRQ8}$ during Reset or the number of times the P38TB bit in the Clock Selection Register has been programmed a one. **80287 Clock** CLK287 clock drives the 80287 coprocessor. CLK287 is programmable via the Clock Selection Register. A variety of clock frequencies and duty cycles provide compatibility with a variety of 8087 or 80287 compatible coprocessors. **I/O Channel Ready** IOCHRDY adds wait states to the AT-Bus when a Fast Parallel Port device (FPP) is busy.
37 - 57	KBCLK	O	**Keyboard Clock** KBCLK is a 9.6 MHz clock used to drive the keyboard controller. This signal can be used to drive the WD37C65 Floppy Disk Controller for systems not using the WD76C20A Storage Controller.
40 - 60	ATCLK	O	**AT Clock** ATCLK is a 16 MHz clock used to drive the ATCLK input to the Western Digital System Controller. AT Clock provides a fixed reference that allows the PC/AT bus state machine to run with 8 MHz compatible timing. This signal can be used to drive the Floppy Disk Controller in the WD76C20A Storage Controller.
② Third overtone of 16 MHz crystal is used to generate the 48 MHz clock.			

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

PIN NUMBER PQFP - SQFP	MNEMONIC	I/O	DESCRIPTION
1 - 13 2 - 14	IRQSET0 IRQSET1	O	**Interrupt Request Set 0, 1** These signals are outputs of the IRQ multiplexing logic. When in the Stand Alone Mode, IRQSET0 and IRQSET1 become the tristate interrupt outputs from Serial Port 0 and 1, respectively. (Refer to section 5.6)
- 52	$\overline{ZWS}$	O	**Zero Wait State** When operating in the FPP mode, $\overline{ZWS}$ reduces the default cycle time, thereby increasing the transfer rate for the AT bus. $\overline{ZWS}$ is enabled by the Mode Selection Register described in section 5.5 and is not featured in the 84-pin PQFP device.
28 - 44 33 - 53 39 - 59 63 87	VSS	I	**Ground**
3 - 15	VDD5	I	**+5 volt supply for the parallel port logic only.**
64 - 88	VDD	I	**+3.3 volt or +5 volt supply for the core logic.**
22 - 38	VDD3	I	**+3.3 volt or +5 volt supply for the I/O ring.**
- ③	③ Pins 1, 2, 24-26, 49-51, 75-78, 99, 100 of the SQFP package are not connected.		

TABLE 2-2. SIGNAL DESCRIPTION (Continued)

3 .0 SERIAL PORT REGISTERS

The WD76C30ALV contains two serial ports, therefore, the following registers exist in duplicate, one per port.

3.1 SERIAL PORT REGISTER ADDRESSING

3.1.1 Chip Select ($\overline{CS0}$, $\overline{CS1}$)

When $\overline{CS0}$ is low, registers for serial port 0 can be accessed, and when $\overline{CS1}$ is low, registers for serial port 1 can be accessed. No more than one $\overline{CS}$ ($\overline{CS0}$, $\overline{CS1}$, or $\overline{CS2}$) should ever be low at any time, unless all three are low for Sleep Mode.

Power Down Reset:
In the Parallel Port, asserting Mode Selection Register

bit 3 (PUD) described in section 5.5, causes the ACE to reset to the condition listed in Table 3-2.

Software Reset:
A software reset is performed by writing to the Divisor Latches, forcing the transmitter and receiver to an idle mode. Registers are not reset by this operation. Prior to enabling interrupts, the LSR and RBR registers should be read to clear out any data, returning them to a known state without resetting the system.

Chip Select ($\overline{CS0}$, $\overline{CS1}$) and register select (A0, A1, A2) signals must be stable for the duration of a read or write operation.

3.1.2 Register Select (A0, A1, A2)

To select a register for read or write operation, see Table 3-1.

NOTE

Divisor Latch Access Bit (DLAB) is the MSB of the Line Control Register. DLAB must be programmed high (logic 1) by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer Register (read)
0	0	0	0	Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable Register
X	0	1	0	Interrupt Identification Register (read)
X	0	1	0	FIFO Control Register (write)
X	0	1	1	Line Control Register
X	1	0	0	Modem Control Register
X	1	0	1	Line Status Register (read only)
X	1	1	0	Modem Status Register
X	1	1	1	Scratch Pad Register
1	0	0	0	Divisor Latch Register (least significant byte)
1	0	0	1	Divisor Latch Register (most significant byte)

TABLE 3-1. REGISTER ADDRESSING

3.2 ACE OPERATIONAL DESCRIPTION

3.2.1 Master Reset

Asserting $\overline{\text{RESET}}$ on pin 36/56 causes the ACE to reset to the condition listed in Table 3-2.

3.2.2 ACE Accessible Registers

The system programmer has access to any of the registers as summarized in Table 3-3. For individual register descriptions, refer to the following pages under register heading.

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset or PUD = 1	All Bits Low (0:3 forced and 4:7 permanent)
Interrupt Identification Register	Master Reset or PUD = 1	Bit 0 is High and Bits 1:3; 6 and 7 are forced Low. Bits 4 and 5 are Permanently Low
Line Control Register	Master Reset or PUD = 1	All Bits Low
Modem Control Register	Master Reset or PUD = 1	All Bits Low
Line Status Register	Master Reset or PUD = 1	All Bits Low, except Bits 5 and 6 are High
Modem Status Register	Master Reset or PUD = 1 Modem Signal Inputs	Bits 0:3 Low, Bits 4:7 at Input Signal
Divisor Latch (low order byte)	Writing into the Latch	Data
Divisor Latch (high order byte)	Writing into the Latch	Data
$\overline{\text{SOUT}}$	Master Reset or PUD = 1	High
$\overline{\text{RTS}}$	Master Reset or PUD = 1	High
$\overline{\text{DTR}}$	Master Reset or PUD = 1	High
RCVR FIFO Counter	MR or FCR1• FCR0 or ΔFCR0 or PUD = 1	All Bits Low
XMIT FIFO Counter	MR or FCR2 • FCR0 or ΔFCR0 or PUD = 1	All Bits Low
FIFO CONTROL	Master Reset or PUD = 1	All Bits Low
D(7:0) Data Bus Lines	In Tristate Mode, Unless $\overline{\text{IOR}}$ = Low	Tristate Data (ACE to CPU)
Address Selection Register	Master Reset	All Bits Low
Clock Selection Register	Master Reset	All Bits Low
CLK Disable Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Serial Port Interrupt Selection Register	Master Reset	All Bits Low
Parallel Port Interrupt Selection Register	Master Reset	All Bits Low
Mode Selection Register	Master Reset	All Bits Low
Parallel Port Control	Master Reset or PUD = 1	Bits 7:6 High, Bits 5:0 Low
Parallel Port Data	Master Reset or PUD = 1	All Bits Low
Parallel Port Status	None	
$\overline{\text{SLIN}}$, $\overline{\text{INIT}}$, $\overline{\text{AFD}}$, $\overline{\text{STB}}$,	Master Reset or PUD = 1	High, Low, High, High

* Reset disables the Stand Alone Mode *
PUD is bit 3 of the Mode Selection Register

TABLE 3-2. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

	REGISTER ADDRESS ②					
	DLAB = 0 A(2:0) = 0 Read Only	DLAB = 0 A(2:0) = 0 Write Only	DLAB = 0 A(2:0) = 1	DLAB = X A(2:0) = 2 Read Only	DLAB = X A(2:0) = 2 Write Only	DLAB = X A(2:0) = 3
	REGISTER TITLE					
Bit No.	Receiver Buffer Register	Transmitter Holding Register	Interrupt Enable Register	Interrupt Identification Register	FIFO Control Register	Line Control Register
0	Data Bit 0	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending (IP)	FIFO Enable (FEWO)	Word Length Select Bit 0 (WLS0)
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit 1 (IID)	Rcvr FIFO Reset (RFR)	Word Length Select Bit 1 (WLS1)
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ERLSI)	Interrupt ID Bit 2 (IID)	Transmitter FIFO Reset (TFR)	Number of Stop Bits (STB)
3	Data Bit 3	Data Bit 3	Enable Modem Status Interrupt (EDSSI)	Interrupt ID Bit 3 (IID) ①	Not Used	Parity Enable (PEN)
4	Data Bit 4	Data Bit 4	0	0	Reserved	Even Parity Select (EPS)
5	Data Bit 5	Data Bit 5	0	0	Reserved	Stick Parity (STP)
6	Data Bit 6	Data Bit 6	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (LSB)(RFTL)	Set Break Control (SBR)
7	Data Bit 7	Data Bit 7	0	FIFO Enabled ① (FERO)	Rcvr FIFO Trigger Level (MSB) (RFTL)	Divisor Latch Access Bit (DLAB)

① These bits are 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30ALV SERIAL PORT REGISTERS

9

	REGISTER ADDRESS ②					
	DLAB = X A(2:0) = 4	DLAB = X A(2:0) = 5	DLAB = X A(2:0) = 6	DLAB = X A(2:0) = 7	DLAB = 1 A(2:0) = 0	DLAB = 1 A(2:0) = 1
	REGISTER TITLE					
Bit No.	Modem Control Register	Line Status Register	Modem Status Register	Scratch Pad Register	Divisor Latch (LSB)	Divisor Latch (MSB)
0	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Not Connected (NC)	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Interrupt (Int)	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 3	Bit 11
4	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	0	Error in RCVR FIFO ① (EIRF)	Received Line Signal Detect (RLSD)	Bit 7	Bit 7	Bit 15

① This bit is 0 in Character Mode. ② See Table 3-1

TABLE 3-3. ACCESSIBLE WD76C30ALV SERIAL PORT REGISTERS (Continued)

3.3 LINE CONTROL REGISTER

The Line Control Register provides control over the word length, number of Stop Bits, Parity, Break Control and selection of the Receiver Buffer, Transmitter Holding Register and Interrupt Enable Register.

Address A(2:0) = 3, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
DLAB	SBR	STP	EPS	PEN	STB	WLS1	WLS0

Signal Name	Default After Master Reset
All signals	0

Bit 7 - DLAB, Divisor Latch Access

DLAB = 0 -
Access the Receiver Buffer, Transmitter Holding Register or Interrupt Enable Register.

DLAB = 1 -
Access the Divisor Latches of the Baud Rate Generator during a Read or Write operation.

Bit 6 - SBR, Set Break Control

The SBR feature enables the CPU to alert a terminal in a computer communications system.

SBR = 0 -
Serial Output (SOUT) follows the output of the transmitter.

SBR = 1 -
The Serial Output (SOUT) is forced to the Spacing (logic 0) State and remains there (until reset by a low-level SBR), regardless of other transmitter activity.

Bit 5 - STP, Stick Parity

STP = 0 -
When parity is enabled by PEN (bit 3), it is represented as indicated by the state of EPS (bit 4).

STP = 1 -
When parity is enabled by PEN, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by EPS.

Bit 4 - EPS, Even Parity Select

EPS = 0 -
When PEN (bit 3) equals 1 and STP equals 0, an odd number of logic 1's are transmitted or checked in the data word bits and Parity bit.

EPS = 1 -
When PEN equals 1 and STP equals 0, an even number of bits are transmitted or checked.

Bit 3 - PEN, Parity Enable

PEN = 0 -
No parity is generated or checked.

PEN = 1 -
Parity is generated on transmitted data or checked on received data between the last data word bit and Stop bit of the serial data. The Parity bit is used to produce an even or odd number of 1's when the data word bits and the Parity bit are summed.

Bit 2 - STB, Number Of Stop Bits

This bit specifies the number of Stop Bits in each transmitted serial character.

STB = 0 -
One Stop Bit is generated in the transmit data.

STB = 1 -
When WLS1 and WLS0 (bits 1 and 0) select a 5-bit word length, 1-1/2 Stop bits are generated.

When WLS1 and WLS0 select a 6, 7 or 8-bit word length, two Stop bits are generated.

Bits (1:0) - WLS1, WLS0, Word Length Select

WLS1 and WLS0 specify the number of bits in each transmitted or received serial character.

WLS1	WLS0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

3.4 ACE PROGRAMMABLE BAUD RATE GENERATOR

The ACE contains a programmable Baud Rate Generator with a programmable input clock of 1.843 MHz, 3.0 MHz or 8 MHz clocks, as well as a 48 MHz input for test purposes. The output frequency of the Baud Generator is 16 times the baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load. Loading of either divisor Latch forces the Transmitter and Receiver into the Idle Mode. The transmitter does not enter the Idle Mode until after the character in the shift register has been transmitted. It may take up to eight input clocks after loading either divisor latch before the new baud rate becomes effective.

Tables 3-4, 3-5 and 3-6 illustrate the use of the Baud Generator with three different driving frequencies. One is referenced to a 1.8432 MHz clock, another is a 3.072 MHz clock and the third is an 8.0 MHz clock.

NOTE

The maximum operating frequency of the Baud Rate Generator is 8.0 MHz.

The data rate should never be greater than 512 Kbaud.

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.690
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.860

TABLE 3-4. BAUD RATES USING 1.8432 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.230
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

TABLE 3-5. BAUD RATES USING 3.072 MHz CLOCK

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 TIMES CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	10000	—
75	6667	0.005
110	4545	0.010
134.5	3717	0.013
150	3333	0.010
300	1667	0.020
600	833	0.040
1200	417	0.080
1800	277	0.080
2000	250	—
2400	208	0.160
3600	139	0.080
4800	104	0.160
7200	69	0.644
9600	52	0.160
19200	26	0.160
38400	13	0.160
56000	9	0.790
128000	4	2.344
256000	2	2.344
512000	1	2.344

TABLE 3-6. BAUD RATES USING 8.0 MHz CLOCK

3.5 LINE STATUS REGISTER

The Line Status Register provides status information to the CPU concerning the data transfer.

Address A(2:0) = 5, DLAB = X - Read

7	6	5	4	3	2	1	0
EIRF	TEMT	THRE	BI	FE	PE	OE	DR

Signal Name	Default After Master Reset
EIRF	0
TEMT	1
THRE	1
BI	0
FE	0
PE	0
OE	0
DR	0

Bit 7 - EIRF, Error in RCVR FIFO

EIRF = 0 -
When in Character Mode, EIRF is always 0.

When in FIFO Mode, a 0 indicates no error in the RCVR.

EIRF = 1 -
There is at least one parity error, framing error or break indication in the FIFO. EIRF is set to 0 when the Line Status Register is read and there are no additional errors in the FIFO.

Bit 6 - TEMT, Transmitter Empty

TEMT = 0 -
When in the Character Mode, at least one byte has been written into the Transmitter Holding Register.

When in the FIFO Mode, at least one byte has been written into the XMIT FIFO.

TEMT = 1 -
When in the Character Mode, the Transmitter Holding Register and Transmitter Shift Register are idle (empty).

In the FIFO Mode, the XMIT FIFO and XMIT Shift Registers are empty.

Bit 5 - THRE, Transmitter Holding Register Empty

Character Mode:

THRE indicates that the ACE is ready to accept a new character for transmission. THRE also causes the ACE to issue an interrupt to the CPU when the Transmit Holding Register Empty interrupt enable is set high.

THRE = 0 -
The CPU has loaded the Transmitter Holding Register.

THRE = 1 -
A character has been transferred from the Transmitter Holding Register into the Transmitter Shift Register.

FIFO Mode:

Normally

THRE responds immediately when the XMIT FIFO is emptied or when the first character is written into the XMIT FIFO.

The first transmitter interrupt after changing the first bit of FIFO Control Register will be immediate if the Transmit Holding Register Interrupt is enabled.

Exception

The Transmitter FIFO empty indications are delayed one character time, minus the last Stop Bit time, whenever the Transmitter FIFO is empty and there have not been at least two characters in Transmitter FIFO at the same time since the last time that Transmitter FIFO was empty.

THRE = 0 -
At least one character has been written into the XMIT FIFO.

THRE = 1 -
The XMIT FIFO is empty.

Bit 4 - BI, Break Interrupt

BI indicates that the received character is a Break.

BI = 0 -
The CPU read the contents of the Line Status Register. Restarting after a break is received requires the SIN pin to be high for at least one half bit time.

BI = 1 -
When in the Character Mode, the received data input has been held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start Bit + data bits + Parity + Stop Bits).

When in FIFO Mode, BI is associated to the particular character in the FIFO, and is set when the associated character is in the top of the FIFO.

Bit 3 - FE, Framing Error

FE indicates that the received character did not have a valid Stop Bit.

FE = 0 -
The CPU read the contents of the Line Status Register.

FE = 1 -
In the Character Mode, the Stop Bit following the last data bit or parity bit was detected as a zero bit (Spacing Level).

In the FIFO Mode, an FE is associated with a particular character in the FIFO and is set when the associated character is at the top of the FIFO.

Bit 2 - PE, Parity Error

PE indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit.

PE = 0 -
The CPU read the contents of the Line Status Register.

PE = 1 -
In the Character Mode, a parity error has been detected.

In the FIFO Mode, a parity error is associated with a particular character in the FIFO, and PE is set when the associated character is at the top of the FIFO.

Bit 1 - OE, Overrun Error

OE indicates that an Overrun Error occurred.

OE = 0 -
The CPU read the contents of the Line Status Register.

OE = 1 -
In the Character Mode, the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register. This destroyed the previous character.

When in FIFO Mode, an OE occurs after the RCVR FIFO is full and the Receiver Shift Register has completely received the next character. An OE is indicated to the CPU as soon as it happens. The character in the shift register will be written over but nothing will be transferred to the FIFO.

Bit 0 - DR, Receiver Data Ready

DR = 0 -
In the Character Mode, the CPU read the data in the Receiver Buffer Register.

In the FIFO Mode, the receiver FIFO is empty.

DR = 1 -
In the Character Mode, a complete incoming character has been received and transferred into the Receiver Buffer Register.

In the FIFO Mode, a complete incoming character has been received and transferred into the RCVR FIFO.

NOTE

Bits 4 through 1 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected and Receiver Line Status interrupt is enabled. All bits of the Line Status Register, except bit 7, can be set or reset by writing to the register.

9

3.6 INTERRUPT IDENTIFICATION REGISTER

The ACE has an interrupt capability that allows for complete flexibility in interfacing with all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels. Listed according to their priority the four levels of interrupt conditions are:

Receiver Line Status
Received Data Ready
Transmitter Holding Register Empty
Modem Status

Information indicating that a prioritized interrupt is pending and source of that interrupt is stored in the Interrupt Identification Register (IIR).

The IIR, when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. Bits (3:0) are further described in Table 3-7.

Address A(2:0) = 2, DLAB = X - Read only

7	6	5	4	3	2	1	0
FERO		0	0	IID			IP

Signal Name	Default After Master Reset
FERO	00
IID	000
$\overline{IP}$	1

Bits (7:6) - FERO, FIFO Enable

The FERO bits identify whether the FIFO Control Register bit 0, has placed the device in the Character Mode or FIFO Mode.

FERO = 0 0 -
The device is in the Character Mode

FERO = 1 1 -
The device is in the FIFO Mode.

Bits (5:4) - These bits are always logic 0.

Bits (3:1) - IID, Interrupt ID

The IID bits identify the highest priority interrupt pending (see Table 3-7).

Bit 0 - $\overline{IP}$, Interrupt Pending

The $\overline{IP}$ bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending.

$\overline{IP}$ = 0 -
An interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.

$\overline{IP}$ = 1 -
No interrupt is pending and polling (if used) continues.

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS			
Bit 3	IID Bit 2	Bit 1	$\overline{IP}$ Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	0	1	—	None	None	—
0	1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register or FIFO dropping below the trigger level
1	1	0	0	Second	Character Timeout Identification	No Characters have been input or removed from RCVR FIFO during the last 4 character times, and at least one character occupies it during this time.	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	0	Fourth	Modem Status	Clear to Send or Data Set or Ring Indicator or Received Line Signal Detect	Reading the Modem Status Register

TABLE 3-7. INTERRUPT CONTROL FUNCTIONS

3.7 INTERRUPT ENABLE REGISTER

When INT (bit 3 of Modem Control Register) is a logic 1, the Interrupt Enable Register controls the selection of the four interrupt sources of the ACE, making it possible to separately activate the device's internal Interrupt signals.

It is possible to disable the entire interrupt system, or selected interrupts by configuring bits three though zero of the Interrupt Enable Register.

Disabling the interrupt system inhibits the Interrupt Identification Register and the active internal interrupt signal. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

Address A(2:0) = 1, DLAB = 0 - Read and Write

7	6	5	4	3	2	1	0
0	0	0	0	EDSSI	ERLSI	ETBEI	ERBFI

Signal Name	Default After Master Reset
All signals	0

Bits (7:4) - These four bits are always set to 0 by the hardware.

Bit 3 - EDSSI, Enable Modem Status Interrupt

EDSSI = 0 -
Disables the Modem Status Interrupt.

EDSSI = 1 -
Enables the Modem Status Interrupt.

Bit 2 - ERLSI, Enable Receiver Line Status Interrupt

ERLSI = 0 -
Disables the Receiver Line Status Interrupt.

ERLSI = 1 -
Enables the Receiver Line Status Interrupt.

Bit 1 - ETBEI, Enable Transmitter Holding Register Empty Interrupt

ETBEI = 0 -
Disables the Transmitter Holding Register Empty Interrupt.

ETBEI = 1 -
Enables the Transmitter Holding Register Empty Interrupt.

Bit 0 - ERBFI, Enable Received Data Available Interrupt

ERBFI = 0 -
Disables the Received Data Available Interrupt.

ERBFI = 1 -
Enables the Received Data Available Interrupt.

3.8 SCRATCH PAD REGISTER

This 8-bit register does not control or report status on any part of the ACE. It can be used by the programmer as a general purpose register.

Address A(2:0) = 7, DLAB = X - Read and Write

7	6	5	4	3	2	1	0

Signal Name	Default After Master Reset
All signals	None

3.9 FIFO CONTROL REGISTER

The FIFO Control Register is used to enable the FIFO Mode, clear FIFOs, set the RCVR FIFO trigger levels and select the mode of DMA signaling.

Address A(2:0) = 2, DLAB = X, Write only

7	6	5	4	3	2	1	0
RFTL		Reserved		Not Used	TFR	RFR	FEWO

Signal Name	Default After Master Reset
All signals	0

Bits (7:6) - RFTL, RCVR FIFO Trigger Level

RFTL controls the trigger level of the Received Data Available Interrupt.

RFTL 7	6	Trigger Level (bytes)
0	0	- 01
0	1	- 04
1	0	- 08
1	1	- 14

Bits (5:4) - Reserved for future use and should be programmed to zeros.

Bit 3 - Not Used

In the WD16C550 this is the DMS bit.

Bit 2 - TFR, Transmitter FIFO Reset

Writing a one to TFR clears all characters from the XMIT Error FIFO and resets its counters and this bit to 0. The shift register and XMIT FIFO are not cleared.

Bit 1 - RFR, Receiver FIFO Reset

Writing a one to RFR clears all characters from the RCVR Error FIFO and resets its counters and this bit to 0. The shift register and RCVR FIFO are not cleared.

Bit 0 - FEWO, FIFO Enable

FEWO = 0 -
XMIT and RCVR FIFOs are disabled

FEWO = 1 -
XMIT and RCVR FIFOs are enabled. When changing from Character Mode to FIFO Mode, data in the FIFOs does not automatically clear. Setting or resetting FEWO clears all characters from the RCVR Error FIFO and resets the XMIT and RCVR FIFO counters to 0. FEWO must be set to 1 before setting TFR and RFR or they will not be programmed. As illustrated by the following boolean equation, FEWO along with SP_FIFO in the Mode Selection Register determine whether the Character Mode or FIFO Mode is selected.

Character Mode = $\overline{FEWO} + \overline{SP\_FIFO}$
FIFO Mode = FEWO • SP_FIFO

3.10 MODEM CONTROL REGISTER

The Modem Control Register controls the interface with the Modem, data set or a peripheral device emulating a Modem.

Address A(2:0) = 4, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
0	0	0	LOOP	INT	NC	RTS	DTR

Signal Name	Default After Master Reset
All signals	0

Bits (7:5) - These three bits are always set to 0 by the hardware.

Bit 4 - LOOP, Loopback Mode

This bit provides a loopback feature for diagnostic testing of the ACE. Selecting the Loopback Mode results in the following setup (Refer to Figure 3-1):

- The transmitter Serial Output (SOUT) is set to a logic 1 (high) state.
- The receiver Serial Input (SIN) is disconnected.
- The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.

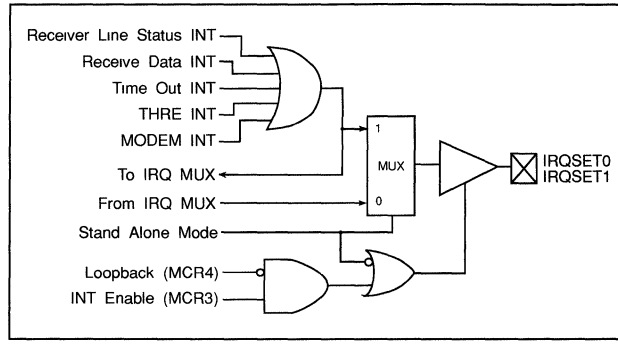


FIGURE 3-1. INTERRUPT SIGNAL LOGIC

- The four Modem Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$ and $\overline{RI}$) are disconnected, and the Modem Control Register bits (3:0) are internally connected to the four Modem Control inputs.

While in the Stand Alone and Loopback Mode, the IRQSET outputs are tristated (see Figure 3-1). In the Loopback Mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and receive data paths of the ACE.

In the Loopback Mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The ACE Modem interrupt system can be tested by writing into the lower four bits of the Modem Status Register.

To return to normal operation, the registers must be reprogrammed for normal operation and then LOOP (bit 4) reset to a logic 0.

LOOP = 0 -
Normal Mode.

LOOP = 1 -
Loopback Mode.

Bit 3 - INT, Interrupt

INT enables the IRQSET output when in the Stand Alone Mode. In Loopback Mode this bit is connected internally to bit 7 of the Modem Status Register (Refer to Figure 3-1).

INT = 0 -
The IRQSET output is tristated.

INT = 1 -
The IRQSET output is enabled in the Stand Alone Mode.

Bit 2 - NC, No external connection.

In the Loopback Mode, this bit is connected internally to bit 6 of the Modem Status Register.

Bit 1 - RTS, Request To Send

Bit 1 controls the $\overline{RTS}$ signal. In the Loopback Mode, this bit is connected internally to bit 4 of the Modem Status Register.

RTS = 0 -
$\overline{RTS}$ is set to a logic one.

RTS = 1 -
$\overline{RTS}$ is set to a logic zero.

Bit 0 - DTR, Data Terminal Ready

Bit 0 controls the $\overline{DTR}$ signal. In the Loopback Mode, this bit is connected internally to bit 5 of the Modem Status Register.

DTR = 0 -
$\overline{DTR}$ is set to a logic one.

DTR = 1 -
$\overline{DTR}$ is set to a logic zero.

NOTE

The $\overline{DTR}$ output of the ACE may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding Modem or data set.

3.11 MODEM STATUS REGISTER

The Modem Status Register provides the current state of the control lines from the Modem (or peripheral device) to the CPU. In addition to this current-state information, bits 3 through 0 of the Modem Status Register provide change information. These bits are set to a logic 1 whenever a control input from the Modem changes state. They are reset to logic 0 whenever the CPU reads the Modem Status Register.

Address A(2:0) = 6, DLAB = X - Read and Write

7	6	5	4	3	2	1	0
RLSD	RI	DSR	CTS	DRLSD	TERI	DDSR	DCTS

Signal Name	Default After Master Reset
RLSD	X
RI	X
DSR	X
CTS	X
DRLSD	0
TERI	0
DDSR	0
DCTS	0

Bit 7 - RLSD, Received Line Signal Detect

RLSD is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

In the Loopback Mode (bit 4 of the Modem Control Register set to 1) this bit is connected internally to bit 3 of the Modem Control Register (INT).

Bit 6 - RI, Ring Indicator

RI is the complement of the Ring Indicator ($\overline{RI}$) input. In the Loopback Mode (bit 4 of the Modem Control Register set to 1) this bit is connected internally to bit 2 of the Modem Control Register.

Bit 5 - DSR, Data Set Ready

DSR is the complement of the Data Set Ready ($\overline{DSR}$) input. In the Loopback Mode (bit 4 of the Modem Control Register set to 1) this bit is connected internally to bit 0 of the Modem Control Register (DTR).

Bit 4 - CTS, Clear To Send

CTS is the complement of the Clear to Send ($\overline{CTS}$) input. In the Loopback Mode (bit 4 of the Modem Control Register set to 1) this bit is connected internally to bit 1 of the Modem Control Register (RTS).

Bit 3 - DRLSD, Delta Received Line Signal Detector

DRLSD is the Delta Received Line Signal Detector (DRLSD) indicator.

DRLSD = 0 -
The $\overline{RLSD}$ input to the WD76C30ALV has not changed state since the last time it was read by the CPU.

DRLSD = 1 -
The $\overline{RLSD}$ input to the WD76C30ALV has changed state since the last time it was read by the CPU.

Bit 2 - TERI, Trailing Edge of Ring Indicator

TERI is the Trailing Edge of Ring Indicator (TERI) detector.

TERI = 0 -
The $\overline{RI}$ input to the WD76C30ALV has not changed from an On (logic 1) to an Off (logic 0) condition.

TERI = 1 -
The $\overline{RI}$ input to the WD76C30ALV has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 1 - DDSR, Delta Data Set Ready

DDSR is the Delta Data Set Ready (DDSR) indicator.

DDSR = 0 -
The $\overline{DSR}$ input to the WD76C30ALV has not changed state since the last time it was read by the CPU.

DDSR = 1 -
The $\overline{DSR}$ input to the WD76C30ALV has changed state since the last time it was read by the CPU.

Bit 0 - DCTS, Delta Clear to Send

DCTS is the Delta Clear to Send (DCTS) indicator.

DCTS = 0 -
The CTS input to the WD76C30ALV has not changed state since the last time it was read by the CPU.

DCTS = 1 -
The CTS input to the WD76C30ALV has changed state since the last time it was read by the CPU.

NOTE

Setting bits 3, 2, 1, or 0 to a logic 1 generates a Modem Status Interrupt.

3.12 FIFO OPERATION NOTES

3.12.1 FIFO Interrupt Mode Operation

When FEWO and ERBFI are 1 (bit 0 of the FIFO Control Register and bit 1 of the Interrupt Enable Register), the following RCVR interrupts will occur.

1. A FIFO timeout interrupt occurs when the following is true:

   a. There is at least one byte in the RCVR FIFO.

   b. No character has been received in four continuous character times (if two stop bits are being used, the second one is included in this time delay).

   c. The most recent CPU read from the FIFO has exceeded four continuous character times.

   The timeout counter is proportional to the baud rate. After a timeout interrupt, the interrupt is cleared and the timer is reset when the CPU reads a character from the RCVR FIFO.

2. When the RCVR FIFO reaches its programmed trigger level, the receive data interrupt is set. This interrupt is cleared as soon as the FIFO level falls below the trigger level.

3. When the XMIT FIFO is empty, the THRE interrupt is set and is reset when one character is written to the XMIT FIFO.

3.12.2 FIFO Polling Mode Operation

The FIFO Polling Mode is initialized when FEWO is 1 and EDSSI, ERLSI, ETBEI and ERBFI are 0 (bit 1 of the FIFO Control Register and bits (3:0) of the Interrupt Enable Register). In polling mode, the user can poll the LSR directly to check the transmitter and receiver status. Since the receiver and transmitter are controlled separately, either one or both can be in polling mode.

There is no trigger level reached or timeout condition indicated on the interrupt pin in the FIFO Polling Mode. However, the RCVR and XMIT FIFOs are still fully capable of holding characters.

3.12.3 FIFO Pointer

The RCVR FIFO has an internal pointer that automatically points to the RCVR Data byte and associated Status byte to be read. Reading the RCVR Data byte increments the internal counter, while reading the Status byte does not, therefore, the Status byte should always be read prior to reading the Data byte associated with it.

4.0 PARALLEL PORT DESCRIPTION

The parallel port supports Centronics type printers. When $\overline{CS2}$ is asserted, the parallel port is selected, allowing access to all parallel port control and status registers. (Refer to Tables 4-1 and 4-2.)

A(2:0)	$\overline{IOR}$	$\overline{IOW}$	REGISTER SELECTED FPP DISABLED ②	REGISTER SELECTED FPP ENABLED ② AND ADDRESS SELECT REGISTER BITS (2:0) ≠ 111	REGISTER SELECTED FPP ENABLED ② AND ADDRESS SELECT REGISTER BITS (2:0) = 111
000	1 0	0 1	Data - Write Data - Read	Data - Write Data - Read	Data - Write Data - Read
001	1 0	0 1	Invalid Status - Read	Invalid Status - Read	Invalid Status - Read
010	1 0	0 1	Control - Write Control - Read	Control - Write Control - Read	Control - Write Control - Read
011	1 0	0 1	Address Select Register - Write Address Select Register - Read	Address Select Register - Write Address Select Register - Read	Address Select Register - Write Address Select Register - Read
100	1 0	0 1	Data - Write Data - Read	FPP Data - Write FPP Data - Read	FPP Data - Write FPP Data - Read
101	1 0	0 1	Invalid Status - Read	FPP Data - Write FPP Data - Read	FPP Data - Write FPP Data - Read
110	1 0	0 1	Control - Write Control - Read	FPP Address - Write FPP Address - Read	FPP Data - Write FPP Data - Read
111	1 0	0 1	Data Access Register - Write Data Access Register - Read ①	Data Access Register - Write Data Access Register - Read ①	FPP Data - Write FPP Data - Read ①

① A(2:0), $\overline{IOR}$ and $\overline{IOW}$, in conjuction with bits 2:0 of the Address Selection Register, select one of six registers. See section 5.1.

② Mode Selection Register bit 4 = 0 disables FPP.

TABLE 4-1. PARALLEL PORT ($\overline{CS2}$ = 0) REGISTER ADDRESS

BIT NO.	READ DATA 0	WRITE DATA 0	READ STATUS 1	READ CONTROL 2	WRITE CONTROL 2
0	Data Bit 0	Data Bit 0	1	STB ③	STB ③
1	Data Bit 1	Data Bit 1	1	AFD ③	AFD ③
2	Data Bit 2	Data Bit 2	$\overline{INT}$ ①	$\overline{INIT}$	$\overline{INIT}$
3	Data Bit 3	Data Bit 3	$\overline{ERROR}$	SLIN ③	SLIN ③
4	Data Bit 4	Data Bit 4	SLCT	IRQ ENB	IRQ ENB
5	Data Bit 5	Data Bit 5	PE	1	DIR ②
6	Data Bit 6	Data Bit 6	$\overline{ACK}$	1	NC
7	Data Bit 7	Data Bit 7	$\overline{BUSY}$	1	NC

① This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 is a 1), Otherwise the bit is always a 1.

② This bit is only available when the parallel port bus is PS/2 compatible (Mode Selection Register bit 1 is a 1).

③ STB, AFD and SLIN must be set to 0 for FPP reads and writes to function correctly.

TABLE 4-2. ACCESSIBLE PARALLEL PORT REGISTERS

4.1 DATA REGISTER

This read/write register is used to write to or read data from the Parallel Port Data Bus.

Register select - Write:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A(1:0) = 0

Register select - Read:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A(1:0) = 0

7	6	5	4	3	2	1	0
Parallel Bus Data							

Signal Name	Default After Master Reset
All signals	0

Bits (7:0)

These bits represent the data being written to or read from the Parallel Port Data Bus.

4.2 STATUS REGISTER - READ

The contents of this read only register represents the status of the corresponding Parallel Port pins (refer to Tables 2-1, 4-2 and Figure 2-1).

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A(1:0) = 1

7	6	5	4	3	2	1	0
BUSY	$\overline{ACK}$	PE	SLCT	$\overline{ERROR}$	$\overline{INIT}$	1	1

Signal Name	Default After Master Reset
$\overline{BUSY}$	X
$\overline{ACK}$	X
PE	X
SLCT	X
$\overline{ERROR}$	X
$\overline{INIT}$	0
Bits (1:0)	1

Bit 7 - BUSY

Bit 6 - $\overline{ACK}$, Acknowledge

Bit 5 - PE, Parity Error

Bit 4 - SLCT, Select

Bit 3 - $\overline{ERROR}$

Bit 2 - $\overline{INIT}$, Interrupt

$\overline{INIT}$ represents the status of the Parallel Port's internal interrupt signal. This bit is only available when the parallel port interrupt is PS/2 compatible (Mode Selection Register bit 2 equals 1) otherwise it is a 1.

Bits (1:0)

These bits are set to one by the hardware.

4.3 CONTROL REGISTER - WRITE

The Control Register is used to write to the associated lines and, with the exception of bits (7:5), may be read by a Control Register - Read operation. See section 4.4. STB, AFD and SLIN must be set to 0 for FPP reads and writes to function correctly.

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A2 = X, A(1:0) = 2

7	6	5	4	3	2	1	0
NC	NC	DIR	IRQ _ENB	SLIN	$\overline{INIT}$	AFD	STB

Signal Name	Default After Master Reset
Bits (7:6)	X
DIR	0
IRQ_ENB	0
$\overline{SLIN}$	0
$\overline{INIT}$	0
AFD	0
STB	0

Bits (7:6) - Not connected

Bit 5 - DIR, Direction

DIR works in conjunction with the BIDEN pin to determine the direction of the parallel port data bus (refer to Table 4-3). DIR only functions when the parallel port bus is PS/2 compatible as indicated by the Mode Selection Register bit 1 = 1.

Port Mode	BIDEN Pin 76/4	Direction Bit 5	Port Direction	Compatibility
Extended	1	0	Write *	PS/2
Extended	0	X	Write *	PS/2
Extended	1	1	Read *	PS/2
Compatible	1	N/A	Read *	PC/AT
Compatible	0	N/A	Write *	PC/AT

* Read and write refer to internal WD76C30ALV reading and writing the Parallel Port.

TABLE 4-3. PARALLEL PORT OPERATION MODES

Bit 4 - IRQ_ENB, Interrupt Enable

IRQ_ENB = 0 -
Parallel Port Interrupt is not enabled.

IRQ_ENB = 1 -
Parallel Port Interrupt is enabled.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

4.4 CONTROL REGISTER - READ

Bits (4:0) are read/write bits and represent the state as set by a Control Register - Write operation. Bit 5 (DIR) is a write only bit, and, along with bits (7:6), are always represented with a 1. See section 4.3

Register select:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A2 = X, A(1:0) = 2

7	6	5	4	3	2	1	0
1	1	1	IRQ _ENB	SLIN	$\overline{INIT}$	AFD	STB

Signal Name	Default After Master Reset
Bits (7:5)	1
IRQ_ENB	0
$\overline{SLIN}$	0
$\overline{INIT}$	0
AFD	0
STB	0

Bits (7:5)

These bits are set to one by the hardware.

Bit 4 - IRQ_ENB, Interrupt Enable

IRQ_ENB = 0 -
Parallel Port Interrupt is not enabled.

IRQ_ENB = 1 -
Parallel Port Interrupt is enabled.

Bit 3 - SLIN, Line Printer Select

Bit 2 - $\overline{INIT}$, Line Printer Initialize

Bit 1 - AFD, Line Printer Autofeed

Bit 0 - STB, Line Printer Strobe

9

5.0 INTERRUPT, CLOCK AND MODE SELECTION REGISTERS

The internal registers used for the interrupt multiplexing, clock selection and mode selection are accessed in a two step process, using two address locations in the Parallel Port Register. First, the address for the desired register to be accessed is written into the Address Select Register located at address three of the Parallel Port. Then the data to be read from or written to the selected register is accessed through the Data Access Register (see Table 4-1), located at address seven in the Parallel Port. It is not necessary for these write operations to follow each other.

5.1 ADDRESS SELECTION REGISTER

Register select - Read:
$\overline{CS2}$ asserted - $\overline{IOR}$ asserted - $\overline{IOW}$ de-asserted
Address A(2:0) = 3

Register select - Write:
$\overline{CS2}$ asserted - $\overline{IOR}$ de-asserted - $\overline{IOW}$ asserted
Address A(2:0) = 3

7	6	5	4	3	2	1	0
TEST BIT	SER_PRT_1 CLK		SER_PRT_0 CLK		DAT_ACC_REG		

Signal Name	Default After Master Reset
All signals	0

Bit 7 - Testbit

The Testbit replaces the Serial 1, Serial 0 and Parallel Port interrupt signals to the internal interrupt multiplexer with the SLCT, BUSY and PE signals, respectively.

Bits (6:5) - SER_PRT_1 CLK, Serial Port 1 Clock

These bits select the input clock used by serial port 1.

SER_PRT_1 CLK

6	5	Serial Port 1 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits (4:3) - SER_PRT_0 CLK, Serial Port 0 Clock

These bits select the input clock used for serial port 0.

SER_PRT_0 CLK

4	3	Serial Port 0 Clock
0	0	1.8432 MHz
0	1	3.072 MHz
1	0	MSTRX1
1	1	8.0 MHz

Bits (2:0) - DAT_ACC_REG, Data access register name

These bits, in conjunction with address A(2:0) = 7, select one of the six registers listed below. See Table 4-1.

When all accesses are completed, this field should be set to the Parking Value (7). This prevents inadvertent accesses to the Data Access Register from disturbing the setup during normal operation.

DAT_ACC_REG

2	1	0	Data Access Register Name	Reset Mode
0	0	0	Clock Select Reg.	00H
0	0	1	Clock Disable Reg.	00H
0	1	0	Serial Port 0 Int. Selection Reg.	00H
0	1	1	Serial Port 1 Int. Selection Reg.	00H
1	0	0	Parallel Port Int. Selection Reg.	00H
1	0	1	Mode Selection Reg.	00H
1	1	0	Version Register	
1	1	1	Parking Value	

5.2 CLOCK SELECTION REGISTER

The Clock Selection Register is addressed by the Address Selection Register bits (2:0) = 0 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
Reserved			P38TB	P38SB	CLOCK CO-CPU		

Signal Name	Default After Master Reset
All signals	0

Bits (7:5) - Reserved for future use and should be programmed to 0.

Bit 4 - P38TB, Pin 38 Toggle Bit

P38TB provides a means of overriding the state of pin 38/58, as established by $\overline{IRQ8}$ at reset. If $\overline{IRQ8}$ is high during reset, pin 38/58 is used as CLK287. If $\overline{IRQ8}$ is low during reset, pin 38/58 becomes IOCHRDY. When FPP_EN = 1 (bit 4 of the Mode Selection Register) P38TB always reads as 0. When FPP_EN = 0, P38TB represents the last value written to it.

P38TB = 0 -
Pin 38/58 is not effected.

P38TB = 1 -
Writing a 1 to P38TB toggles the function of pin 38/58 as established at reset, or the previous write of 1 to P38TB. That is, if $\overline{IRQ8}$ selected CLK287, P38TB changes it to IOCHRDY and vice versa.

Bit 3 - P38SB, Pin 38 Status Bit

P38SB is a read only bit when FPP_EN = 1 and provides the current status of pin 38/58. When FPP_EN = 0, P38SB represents the last value written to it.

P38SB = 0 -
CLK287 selected.

P38SB = 1 -
IOCHRDY selected.

Bits (2:0) - CLOCK CO-CPU

These bits are used to select the desired frequency and duty cycle for supporting the 80287 coprocessor. Refer to Table 5-1 for the bit configurations.

5.3 SLEEP MODE

For low power consumption, the internal oscillators may be individually disabled via the Clock Disable Register described in section 5.4. For minimum power consumption, a sleep mode is offered which disables the 48 MHz clock, KBCLK, CLK287, ATCLK, Parallel Port (PD0:7), Data Bus (D0:7), all outputs, all pullups and, except for $\overline{CS0}$, $\overline{CS1}$, $\overline{CS2}$ and $\overline{RESET}$, all inputs. Although KBCLK, CLK287 and ATCLK are disabled during sleep mode, their outputs are held low with small pulldown transistors.

Sleep Mode is activated by hardware asserting all three Chip Selects ($\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$) simultaneously. All registers are preserved in the sleep mode. Sleep Mode is deactivated when one or more of the Select signals are de-asserted.

B2	B1	B0	CLK287 FREQUENCY	COPROCESSOR SUPPORTED
0	0	0	8 MHz, 33% Duty Cycle	8 MHz Intel 80287 8 MHz AMD 80C287
0	0	1	9.6 MHz, 33% Duty Cycle	10 MHz Intel 80287 10 MHz AMD 80C287 10 MHz AMD 80EC287
0	1	0	12 MHz, 33% Duty Cycle	12 MHz AMD 80C287 12 MHz AMD 80EC287
0	1	1	12 MHz, 50% Duty Cycle	12 MHz Intel 80C287A
1	0	0	16 MHz, 33% Duty Cycle	16 MHz AMD 80C287 16 MHz AMD 80EC287
1	0	1	16 MHz, 50% Duty Cycle	Future Expansion
1	1	0	Logic Low	CLK287 Stopped low
1	1	1	Logic High	CLK287 Stopped high

TABLE 5-1. CLOCK SELECTION REGISTER

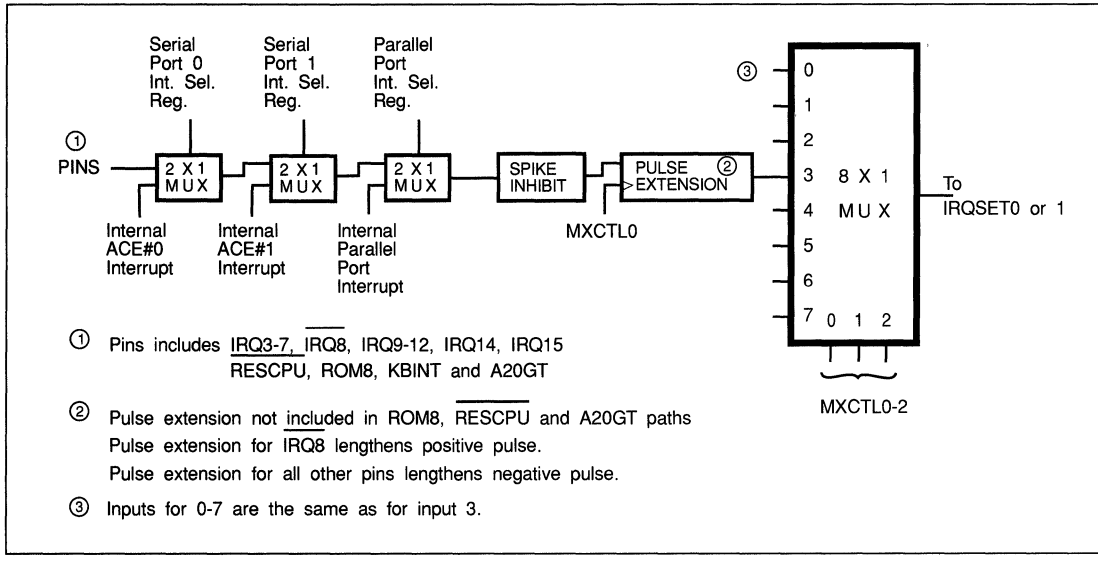


FIGURE 5-1. INTERRUPT MUX BLOCK DIAGRAM

5.4 CLOCK DISABLE REGISTER

The Clock Disable Register is addressed by the Address Selection Register bits (2:0) = 1 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
ISP1 CLK	ISP0 CLK			AT_ CLK	KB_ CLK	OSC_ DIS	

Signal Name	Default After Master Reset
All signals	0

Bit 7 - ISP1_CLK, Internal Serial Port 1 Clock

ISP1_CLK = 0 -
Internal Serial Port 1 clock is not disabled.

ISP1_CLK = 1 -
Internal Serial Port 1 clock is disabled.

Bit 6 - ISP0_CLK, Internal Serial Port 0 Clock

ISP0_CLK = 0 -
Internal Serial Port 0 clock is not disabled.

ISP0_CLK = 1 -
Internal Serial Port 0 clock is disabled.

Bit (5:4) - Reserved and should be programmed to 0.

Bit 3 - ATCLK

ATCLK = 0 -
ATCLK is not disabled.

ATCLK = 1 -
ATCLK signal is held at a logic low.

Bit 2 - KBCLK

KBCLK = 0 -
KBCLK is not disabled.

KBCLK = 1 -
KBCLK signal is held at a logic low.

Bit 1 - OSC_DIS, Oscillator Disable

OSC_DIS = 0 -
The 48 MHz oscillator is not disabled and, KBCLK, CLK287 and ATCLK are not frozen.

OSC_DIS = 1 -
The 48 MHz oscillator is disabled and, KBCLK, CLK287 and ATCLK are frozen.

Bit 0 - Reserved and should be programmed to 0.

NOTE

Asserting $\overline{CS0}$, $\overline{CS1}$ and $\overline{CS2}$ simultaneously disables the 48 MHz oscillator. Upon removing the disabling of the 48 MHz oscillator, it restarts itself within 30 ms. Logic prevents the internal OSC Clock from starting again until the 48 MHz oscillator is running at full amplitude.

5.5 MODE SELECTION REGISTER

The Mode Selection Register is addressed by the Address Selection Register bits(2 :0) = 5 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
$\overline{ZWS}$ _AT	$\overline{ZWS}$ _DT	BIDEN _OR	FPP _EN	PUD	ATPS2 _INT	ATPS2 _PP	SP_ FIFO

Signal Name	Default After Master Reset
All signals	0

Bit 7 - ZWS_AT, Zero Wait State Address Transfer

$\overline{ZWS}$_AT determines whether or not the WD76C30ALV[SK] will allow $\overline{ZWS}$ on pin 52 to be used to shorten the default cycle time and increase the transfer rate for FPP Address transfers.

$\overline{ZWS}$_AT = 0 -
Zero wait states cannot be activated for FPP address transfers.

$\overline{ZWS}$_AT = 1 -
Zero wait states can be activated for FPP address transfers.

Bit 6 - ZWS_DT, Zero Wait State Data Transfer

$\overline{ZWS}$_DT determines whether or not the WD76C30ALV[SK] will allow $\overline{ZWS}$ on pin 52 to be used to shorten the default cycle time and increase the transfer rate for FPP Data transfers.

$\overline{ZWS}$_DT = 0 -
Zero wait states cannot be activated for FPP data transfers.

$\overline{ZWS}$_DT = 1 -
Zero wait states can be activated for FPP data transfers.

Bit 5 - BIDEN_OR, BIDEN Override

BIDEN_OR = 0 -
BIDEN signal on pin 76/4 is not overridden.

BIDEN_OR = 1 -
BIDEN signal on pin 76/4 is overridden and DIR (bit 5 of the Control Register) gains total control of the direction of the Parallel Port, see Table 4-3.

Bit 4 - FPP_EN, Fast Parallel Port Enable

Enabling the Fast Parallel Port results in the outputs of Parallel Port control signals $\overline{AFD}$, $\overline{STB}$ and $\overline{SLIN}$ being changed to push-pull amplifiers and altering their functions. Reading bits 3 and 4 of the Clock Selection Register change and the definitions of addresses 4 through 7 of the parallel port change, see Table 4-1. Timings related to the Parallel Port and reads and writes of the data bus are appreciably enhanced. This feature is only available in the WD76C30ALV[SK].

FPP_EN = 0 -
Fast Parallel Port disabled.

FPP_EN = 1 -
Fast Parallel Port enabled.

Bit 3 - PUD, Power-up Power-down

PUD must always be high when powering down the ports by turning off VDD.

PUD = 0 -
The serial and parallel ports are in the power-up mode.

PUD = 1 -
The serial and parallel ports are in the power-down mode (see Tables 3-2 and 7-2).

With the exception of addresses 011 and 111 of the parallel port, all registers are reset. Also, the following signals are disabled: $\overline{DTR0}$, $\overline{DTR1}$, $\overline{RST0}$, $\overline{RST1}$, SOUT0, SOUT1, PD(7:0), BIDEN, $\overline{ERROR}$, $\overline{SLCT}$, $\overline{PE}$, $\overline{ACK}$, BUSY, $\overline{INIT}$, $\overline{SLIN}$, $\overline{STB}$ and $\overline{AFD}$.

Bit 2 - ATPS2_INT, PC/AT PS/2 Parallel Port Interrupt

ATPS2_INT = 0 -
The Parallel Port Interrupt signal is PC/AT compatible.

ATPS2_INT = 1 -
The Parallel Port interrupt signal is PS/2 compatible.

Bit 1 - ATPS2_PP, PC/AT PS/2 Parallel Port

ATPS2_PP = 0 -
The Parallel Port Bus is configured as a PC/AT compatible Parallel Port.

ATPS2_PP = 1 -
The Parallel Port Bus is configured as a PS/2 extended Parallel Port.

Bit 0 - SP_FIFO, Serial Port FIFO

SP_FIFO = 0 -
Both Serial Ports are configured to operate in non-FIFO mode (Character Mode).

SP_FIFO = 1 -
Both Serial Ports can operate in the FIFO mode if the applicable FEWO is set to 1. The FEWO bit is located in the FIFO Control Register described in section 3.9. The following boolean equation illustrates how to select the Character Mode or FIFO Mode.

Character Mode = $\overline{FEWO} + \overline{SP\_FIFO}$
FIFO Mode = FEWO • SP_FIFO

5.6 INTERRUPT MULTIPLEXER

The WD76C30ALV provides the logic required to interface the PC/AT interrupt request lines with the WD76C10A Single Chip AT Controller. The WD76C10A generates input signals MXCTL(2:0) and the WD76C30ALV uses these signals to select the IRQ inputs. Table 5-3 identifies the multiplexing sequence for the IRQSET0 and IRQSET1 signals. The output of the sampled IRQ inputs are provided on the IRQSET0 and IRQSET1 outputs (see Figure 5-2 IRQSET).

Negative pulse extension logic widens negative pulses on twelve of the sixteen MUX inputs. They are IRQ(3:7), IRQ(9:12), IRQ(14:15) and KBINT. Positive pulse extension logic widens a positive pulse on IRQ8. The pulse width is extended by five positive going edges on MXCTL0 from the leading edge of the pulse or three positive going edges on MXCTL0 from the trailing edge of the pulse, whichever lasts longer. Note that pulses in the opposite direction that don't include three rising MXCTL0 edges are never seen on IRQSET0 or IRQSET1. None of this pulse extension logic applies to RESCPU, ROM8 or A20GT (see Figure 5-1 Interrupt Mux Block Diagram).

When the appropriate bits in the Serial Port 0 Interrupt Selection Register (see section 5.7) are set to the Stand Alone Mode, the interrupt multiplexing logic is disabled. IRQSET0 and IRQSET1 are defined in Table 5-2. The Serial Port 0 Interrupt Selection Register and Serial Port 1 Interrupt Selection Register are used to assign Serial Port Interrupts to IRQ MUX inputs. The Parallel Port Interrupt Selection Register is used to assign the Parallel Port Interrupt to one IRQ MUX input.

IRQSET0 = Serial Port 0 Interrupt (tristate enabled by bit 3 of the Modem Control Register)

IRQSET1 = Serial Port 1 Interrupt (tristate enabled by bit 3 of the Modem Control Register)

IRQ7 = Parallel Port Interrupt (tristate enabled by bit 4 of the parallel port Write Control Register)

TABLE 5-2. STAND ALONE MODE

MXCTL 2	1	0	IRQSET0
0	0	0	$\overline{IRQ8}$
0	0	1	IRQ9
0	1	0	IRQ10
0	1	1	IRQ11
1	0	0	$\overline{ROM8}$
1	0	1	$\overline{RESCPU}$
1	1	0	IRQ14
1	1	1	IRQ15
MXCTL 2	**1**	**0**	**IRQSET1**
0	0	0	IRQ12
0	0	1	KBINT
0	1	0	A20GT
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

TABLE 5-3. MXCTL(2:0) IRQSET(0:1) MULTIPLEXING

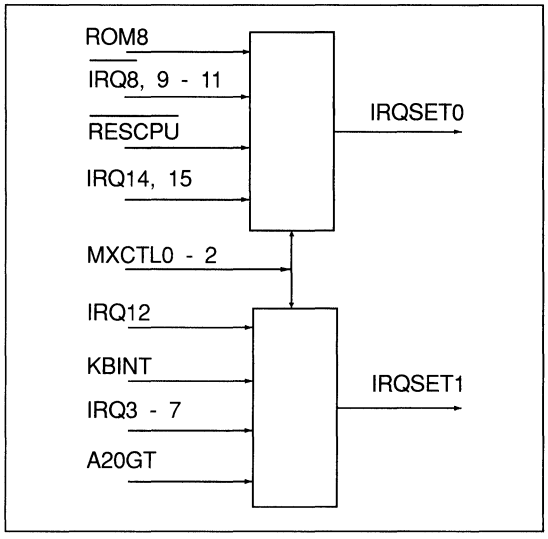


FIGURE 5-2. IRQSET - WHEN NOT IN STAND ALONE MODE

5.7 SERIAL PORT 0 INTERRUPT SELECTION REGISTER

The Serial Port 0 Interrupt Selection Register is addressed by the Address Selection Register bits (2:0) = 2 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				SP0_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits (7:4) - Reserved and should be programmed to 0.

Bits (3:0) - SP0_INT_SEL, Serial Port 0 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 0 Interrupt. The Stand Alone Mode may also be selected by these bits and applies to all ports.

Bits 4 and 3 of the Modem Control Register (refer to section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 0 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15
X	1	1	1	1	Stand Alone Mode

All other combinations are reserved.

5.8 SERIAL PORT 1 INTERRUPT SELECTION REGISTER

The Serial Port 1 Interrupt Selection Register is addressed by the Address Selection Register bits (2:0) = 3 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				SP1_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits (7:4) - Reserved and should be programmed to 0.

Bits (3:0) - SP1_INT_SEL, Serial Port 1 Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Serial Port 1 Interrupt.

Bits 4 and 3 of the Modem Control Register (refer to section 3.10) must be set as follows:

EN = (MCR bit 4 = 0 • bit 3 = 1)

EN	B3	B2	B1	B0	Serial Port 1 Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Serial Port 1 Interrupt Selection Register has priority over the Serial Port 0 Interrupt Selection Register. That is, Serial Port 1 interrupt replaces the Serial Port 0 interrupt when both registers select the same interrupt. The interrupts are not ORed.

5.9 PARALLEL PORT INTERRUPT SELECTION REGISTER

The Parallel Port Interrupt Selection Register is addressed by the Address Selection Register bits (2:0) = 4 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
				PP_INT_SEL			

Signal Name	Default After Master Reset
All signals	0

Bits (7:4) - Reserved and should be programmed to 0.

Bits (3:0) - PP_INT_SEL, Parallel Port Interrupt Select

These bits determine which IRQ MUX input is to be replaced by the internal Parallel Port Interrupt.

IRQ_ENB is bit 4 of the Parallel Port Control Register (refer to section 4.3) and must be set to 1.

IRQ EN	B3	B2	B1	B0	Parallel Port Interrupt Selection
X	0	0	0	0	Disabled
1	0	0	0	1	IRQ3
1	0	0	1	0	IRQ4
1	0	0	1	1	IRQ5
1	0	1	0	0	IRQ6
1	0	1	0	1	IRQ7
1	0	1	1	0	IRQ10
1	0	1	1	1	IRQ11
1	1	0	0	0	ROM8
1	1	0	0	1	IRQ15

All other combinations are reserved.

NOTE

The Parallel Port Interrupt Selection Register has priority over both of the Serial Port Interrupt Selection Registers. That is, the Parallel Port interrupt replaces the Serial Port 0 or 1 interrupt when the registers select the same interrupt. The interrupts are not ORed.

5.10 VERSION REGISTER

The Version Register is a read only register and contains the ones-compliment of the version of the WD76C30. FFH represents WD76C30/LV revision A, B and C. FEH represents WD76C30/LV revision D. FDH represents revision WD76C30ALV.

The Version Register is addressed by the Address Selection Register bits (2:0) = 6 and address bits A(2:0) = 7. See Table 4-1 and section 5.1.

7	6	5	4	3	2	1	0
Version Number							

Signal Name	Default After Master Reset
All signals	X

6 .0 ELECTRICAL SPECIFICATIONS

6.1 MAXIMUM RATINGS

Temperature Under Bias . . . . . 0°C (32°F) to 70°C (158°F)

Storage Temperature . . . . . -65°C (-85°F) to +150°C (302°F)

All Input or Output Voltages with respect to Vss . . -0.5V to +7.0V for parallel/serial port
-0.1V to +4.5V except for parallel/serial port

Power Dissipation . . . . . 180 mW

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Operating Characteristics.

6.2 CAPACITANCE

Ta = 25°C (77°F), f = 1.0 MHz,
VDD = 3.3, 5.5 volts, VDD3 = 3.3, 5.5 volts, VDD5 = 5.5 volts
VSS = 0 volts

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
Cxin	Clock Input Capacitance	15	20	pF	fc = 1 MHz
Cxout	Clock Output Capacitance	20	30	pF	
Cin	Input Capacitance	6	10	pF	Unmeasured Pins Returned to VSS
Cout	Output Capacitance	10	20	pF	Unmeasured Pins Returned to VSS

TABLE 6-1 CAPACITANCE

6.3 DC OPERATING CHARACTERISTICS - 5 VOLT OPERATION

Ta = 0°C (32°F) to +70°C (158°F), VDD/VDD3/VDD5 = 5V ± 10%
VSS = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	VDD5	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0 2.3	VDD5 VDD5	V V	Except MXCTL(2:0) MXCTL(2:0)
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB(0:7) Iol = 24 mA on PD(0:7) Iol = 20 mA on INIT, STB ,SLIN, AFD ① Iol = 24 mA on ZWS Iol = 12 mA on IOCHRDY Iol = 2.0 mA on other outputs
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB(0:7) Ioh = -15.0 mA on PD(0:7) Ioh = -0.55 mA on INIT, STB, SLIN, AFD Ioh = 20 mA on STB, SLIN, AFD ① Ioh = 4 mA on ZWS and IOCHRDY ③ Ioh = -0.2 mA on other outputs
Icc	Power Supply Current		80	mA	VDD3/VDD5 = 5.5V MSTRX1 = 48 MHz All other inputs = 5.5V All outputs floating Baud Rate = 512K Serial Port CLK = 8 MHz
Iil ②	Input Leakage		±15	µA	VDD3/VDD5 = 5.5V, VSS = 0.0V All other pins float
Icl	Clock Leakage				Vin = 0.0V, 5.5V
Idl	Data Bus Leakage (DB and PD)		±10	µA	Vout = 0.4V, Vout = 4.5V Data Bus in High Impedance State
Ioz	Tristate Leakage		± 20	µA	VDD3/VDD5 = 5.5V, GND = 0V, Vout = 0.0V, 5.5V
Vil (RES)	Reset Schmitt Vil		0.8	V	
Vih (RES)	Reset Schmitt Vih	2.3		V	

① When not in FPP mode, SLIN, AFD, STB and INIT outputs are all open collectors with 2.5K to 3.5 Kohm internal pullup resistors. In FPP mode SLIN, AFD and STB can source 20 mA in the high state. In PS/2 mode IRQ7 is also an open collector. When in Vol state, IRQ7 sinks a minimum of 10 mA.

② RESCPU, IRQ(3:7), IRQ8, IRQ(9:12), IRQ(14:15), ROM8, A20GT, KBINT and CS1 have nominally 300 µA pullups. These pullups, along with all others, are disabled when the 48 MHz oscillator is disabled by asserting CS0, CS1 and CS2 simultaneously. The pulldowns on KBCLK, ATCLK and CLK287 are enabled when the three chip selects are low and sink 40 mA min. RTS0 has a 190 Kohm pullup activated during reset, with the output driver disabled during that time.

③ ZWS and IOCHRDY are open collector outputs that drive high for two 48 MHz clocks on a rising transition.

TABLE 6-2. DC OPERATING CHARACTERISTICS - 5 VOLT OPERATION

6.4 DC OPERATING CHARACTERISTICS - 3.3 VOLT OPERATION

Ta = 0°C (32°F) to +70°C (158°F), VDD = +3.3V ± 10%, VDD3 = +3.3V ± 10%, VDD5 = +5V ± 10% VSS = 0V, unless otherwise specified.

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
Vilx	Clock Input Low Voltage	-0.5	0.8	V	
Vihx	Clock Input High Voltage	2.0	VDD5	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Vih	Input High Voltage	2.0 2.3	VDD5 VDD5	V V	Except MXCTL(2:0) MXCTL(2:0)
Vol	Output Low Voltage		0.4	V	Iol = 4.0 mA on DB(0:7) Iol = 12 mA on PD(0:7) Iol = 12 mA on $\overline{INIT}$, $\overline{STB}$,$\overline{SLIN}$, $\overline{AFD}$ ④ Iol = 24 mA on $\overline{ZWS}$ Iol = 12 mA on IOCHRDY Iol = 2.0 mA on other outputs
Voh	Output High Voltage	2.4		V	Ioh = -0.4 mA on DB(0:7) Ioh = -4.0 mA on PD(0:7) Ioh = -10 mA on $\overline{STB}$, $\overline{SLIN}$, $\overline{AFD}$. ④ Ioh = 4 mA on $\overline{ZWS}$ and IOCHRDY ③ Ioh = -0.55 mA on $\overline{INIT}$, $\overline{STB}$,$\overline{SLIN}$, $\overline{AFD}$ ④ Ioh = -0.2 mA on other outputs
Icc	Power Supply Current		50	mA	VDD/VDD3 = 3.6V, VDD5 = 5.5V MSTRX1 = 48 MHz All other inputs = 5.5V All outputs floating Baud Rate = 512K Serial Port CLK = 8 MHz
Iil ②	Input Leakage		±15	µA	VDD/VDD3 = 3.6V, VDD5 = 5.5V, VSS = 0.0V. All other pins float
Icl	Clock Leakage				Vin = 0.0V, 5.5V
Idl	Data Bus Leakage (DB and PD)		±10	µA	Vout = 0.4V, PD - Vout = 4.5V, DB - Vout = 3.0V Data Bus in High Impedance State
Ioz	Tristate Leakage		± 20	µA	VDD/VDD3 = 3.6V, VDD5 = 5.5V, GND = 0V Vout = 0.0V, 5.5V
Vil (RES)	$\overline{Reset}$ Schmitt Vil		0.8	V	
Vih (RES)	$\overline{Reset}$ Schmitt Vih	2.3		V	

For notes ② ③ refer to Table 6-2.

④ When not in FPP mode, $\overline{INIT}$, $\overline{STB}$, $\overline{SLIN}$ and $\overline{AFD}$ are open collector with 2.5K to 3.5 Kohm internal pullup resistors. In FPP mode $\overline{STB}$, $\overline{SLIN}$ and $\overline{AFD}$ can source 10 mA in the high state. In PS/2 mode $\overline{IRQ7}$ is also an open collector. When in Vol state $\overline{IRQ7}$ sinks a minimum of 5 mA.

TABLE 6-3. DC OPERATING CHARACTERISTICS - 3.3 VOLT OPERATION

6.5 AC OPERATING CHARACTERISTICS AND TIMING

Ta = 0°C (32°F) to +70°C (158°F),
VDD = +3.3, 5.0V ± 10%, VDD3 = +3.3, 5.0V ± 10%, VDD5 = 5.0V ± 10%
VSS = 0V

Table 6-4 lists the timing categories and their Figure and Table number.

FIGURE NUMBER	TABLE NUMBER	FIGURE TITLE
6-1	6-5	Receiver Timing
6-2	6-6	Transmitter Timing
6-3	6-7	Modem Control Timing
6-4	6-8	Read Cycle Timing
6-5	6-8	Write Cycle Timing
6-6	6-5	RCVR FIFO Signal Timing For First Byte
6-7	6-5	RCVR FIFO Signal Timing After First Byte (RBR already set)
6-8	6-9	Parallel Port Timing - No FPP Read/Write
6-9	6-9	Parallel Port Interrupt Timing - No FPP Read/Write
6-10	6-10	Clock Generation Timing
6-11	6-11	Interrupt MUX Timing - A
6-12	6-11	Interrupt MUX Timing - B
6-13	6-12	Default Read Timing (FPP) - $\overline{ZWS}$ Mode Disabled
6-14	6-12	Default Write Timing (FPP) - $\overline{ZWS}$ Mode Disabled
6-15	6-12	Read Timing With One Wait Sate (FPP) - $\overline{ZWS}$ Mode Disabled
6-16	6-12	Write Timing With One Wait State (FPP) - $\overline{ZWS}$ Mode Disabled
6-17	6-12	Default Read Timing (FPP) - $\overline{ZWS}$ Mode Enabled
6-18	6-12	Default Write Timing (FPP) - $\overline{ZWS}$ Mode Enabled
6-19	6-12	Fast Read Timing (FPP) - $\overline{ZWS}$ Mode Enabled
6-20	6-12	Fast Write Timing (FPP) - $\overline{ZWS}$ Mode Enabled
6-21	6-12	Parallel Port Interrupt Timing (FPP Read/Write)

TABLE 6-4. TIMING FIGURE/TABLE NUMBERS

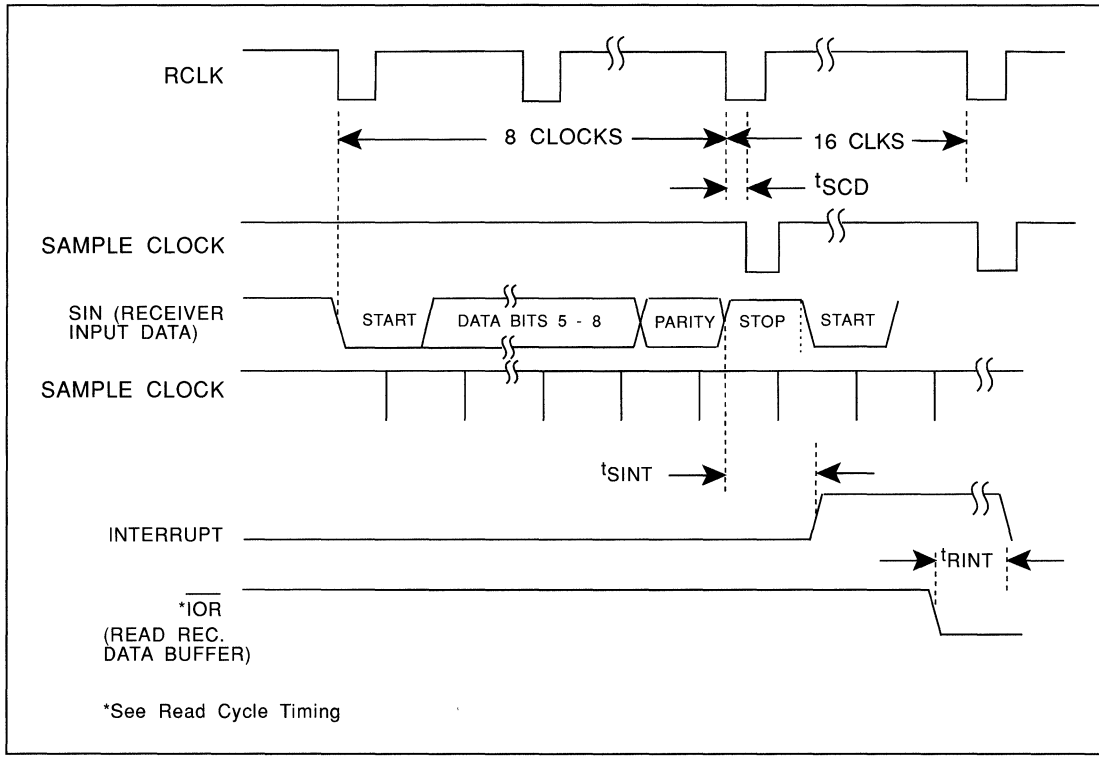


FIGURE 6-1. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
tSCD	Delay from RCLK ② to Sample Time		2	µs	
tSINT	Delay from Stop to Set Interrupt		17 ①	RCLK ② Cycles	100 pF Load
tRINT	Delay from $\overline{IOR}$ (RD RBR) Reset Interrupt		250	ns	100 pF Load

TABLE 6-5. RECEIVER TIMING

① When receiving the first byte in FIFO Mode, tSINT (only for timeout or trigger level interrupt) will be delayed 19 RCLK cycles. For a timeout interrupt, tSINT will be delayed 24 RCLK cycles.

② RCLK is an internal clock used for sampling serial in data. RCLK is equivalent to 16 times the baud rate clock.

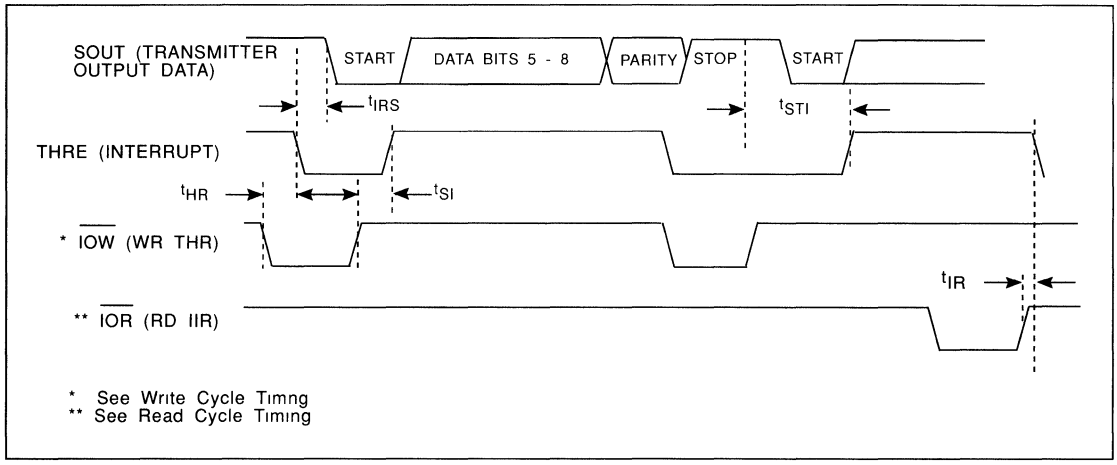


FIGURE 6-2. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{HR}	Delay from $\overline{IOW}$ (WR THR) to Reset Interrupt		175	ns	100 pF Load
t_{IRS}	Delay from initial INTR Reset to Transmit start	8	24	TCLK ① Clock Cycles	
t_{SI} ②	Delay from Initial Write to Interrupt	16	24	TCLK ① Clock Cycles	
t_{STI}	Delay from Stop to Interrupt (THRE)	8	8	TCLK ① Clock Cycles	
t_{IR}	Delay from $\overline{IOR}$ (RD IIR to Reset Interrupt (THRE)		250	ns	100 pF Load

TABLE 6-6. TRANSMITTER TIMING

① TCLK is an internal clock used for sending serial out data. TCLK is equivalent to 16 times the baud rate clock.

② In FIFO mode t_{SI} might extend to beginning of Stop Bit. See Line Status Register for details.

9

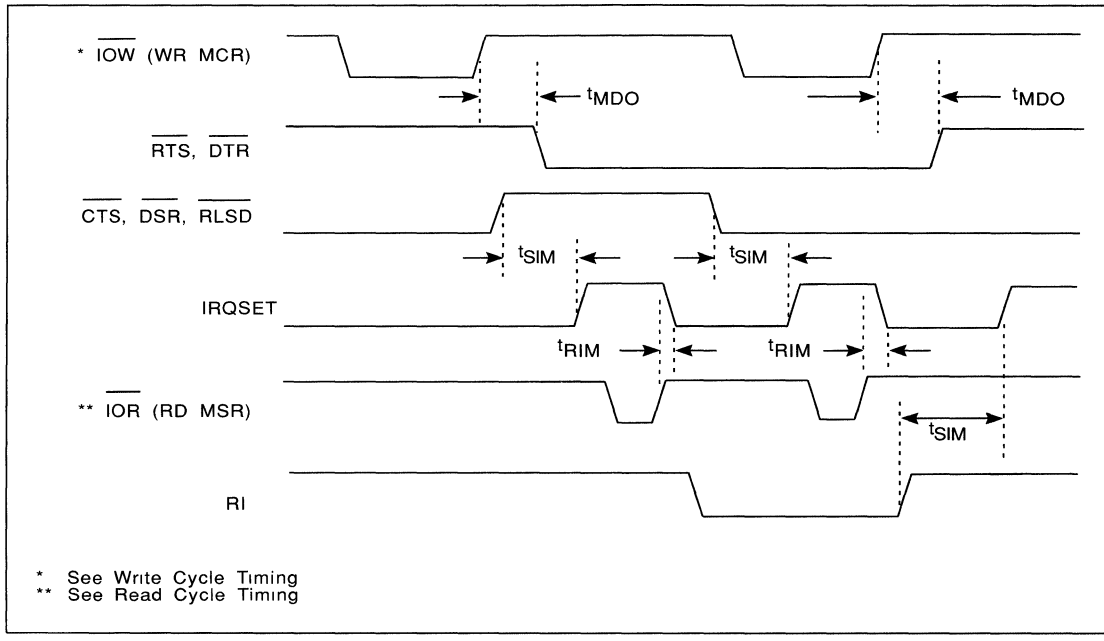


FIGURE 6-3. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{MDO}	Delay from $\overline{IOW}$ (WR MCR) to Output		200	ns	100 pF Load
t_{SIM}	Delay to Set Interrupt from Modem Input		250	ns	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{IOR}$ (RD MSR)		250	ns	100 pF Load

TABLE 6-7. MODEM CONTROL TIMING

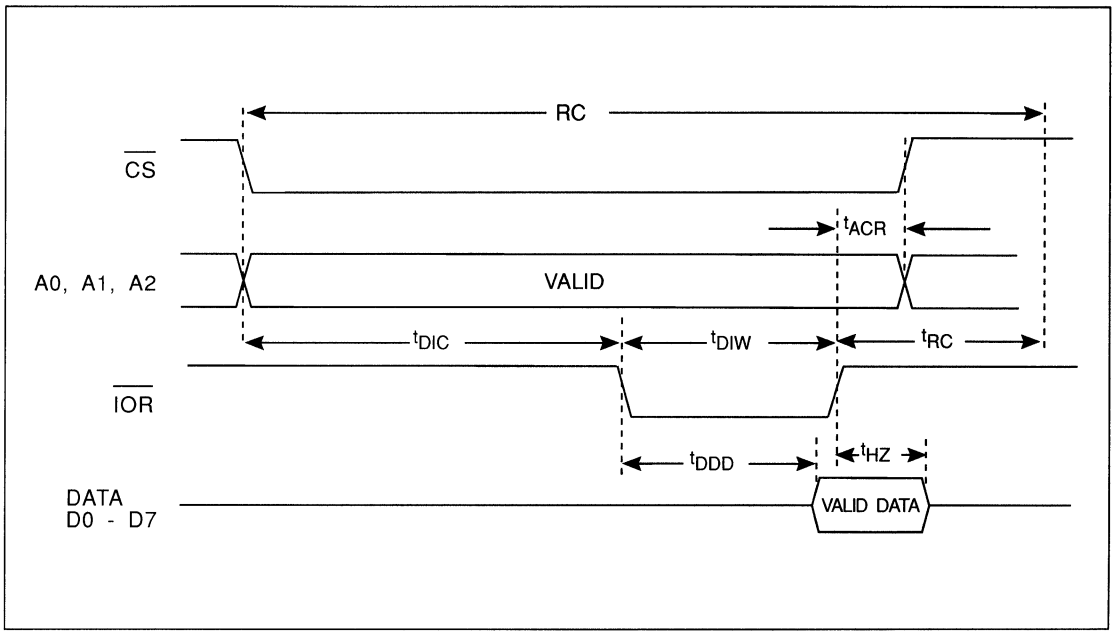


FIGURE 6-4. READ CYCLE TIMING

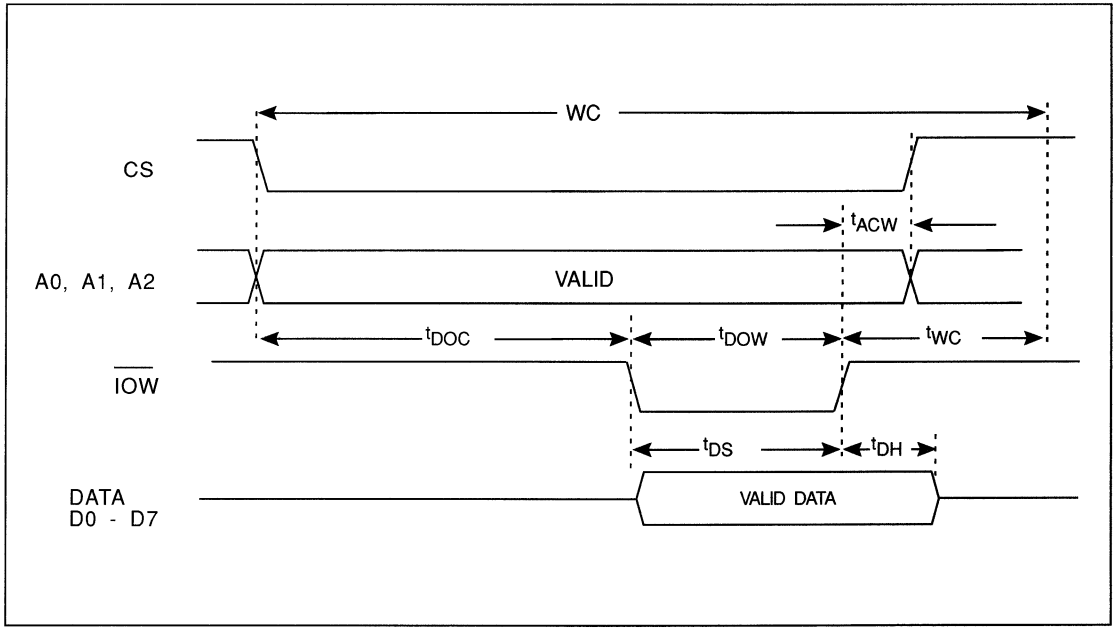


FIGURE 6-5. WRITE CYCLE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	1TTL Load
t_{RC}	Read Cycle Delay	125		ns	1TTL Load
RC	Read Cycle = $t_{DIC} + t_{DIW} + t_{RC}$ + 20 ns	300		ns	1TTL Load
t_{HZ}	$\overline{IOR}$ to Floating Data Delay	0	100	ns	1TTL Load
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	1TTL Load
t_{WC}	Write Cycle Delay	150		ns	1TTL Load
WC	Write Cycle = + t_{DOC} + t_{DOW} + t_{WC} + 20 ns	300		ns	1TTL Load
t_{DS}	Data Setup Time	30		ns	1TTL Load
t_{DH}	Data Hold Time	30		ns	1TTL Load
t_{DIC}	$\overline{IOR}$ DELAY from Select or Address	30		ns	1TTL Load
t_{DOC}	$\overline{IOW}$ Delay from Select or Address	30		ns	1TTL Load
t_{ACR}	Address and Chip Select Hold Time from $\overline{IOR}$	20		ns	1TTL Load
t_{ACW}	Address and Chip Select Hold Time from $\overline{IOW}$	20		ns	1TTL Load
t_{DDD}	Delay from $\overline{IOR}$ to data		100	ns	1 TTL Load
t_{MR}	Master Reset Pulse Width	1.0		µs	1 TTL Load
t_{PWRUP}	Delay from TTL Clock in to internal clock on power up.		50	µs	
t_{OSCUP}	Delay from OSC clock in to internal clock on power up.		30	ms	

TABLE 6-8. READ/WRITE CYCLE TIMING

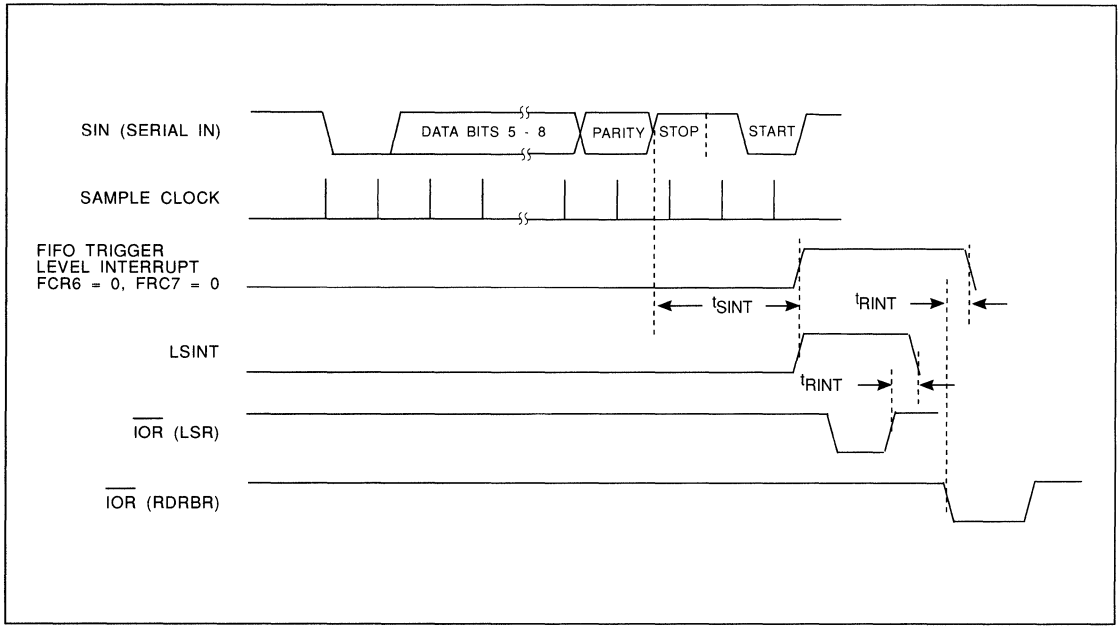


FIGURE 6-6. RCVR FIFO SIGNAL TIMING FOR FIRST BYTE

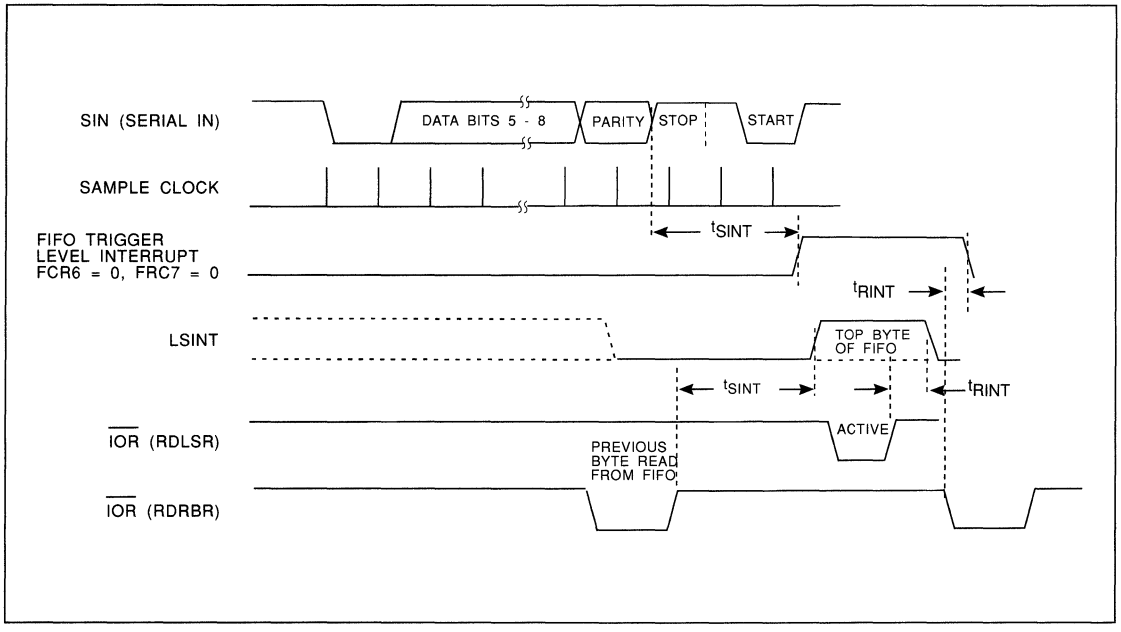


FIGURE 6-7. RCVR FIFO SIGNAL TIMING AFTER FIRST BYTE (RBR ALREADY SET)

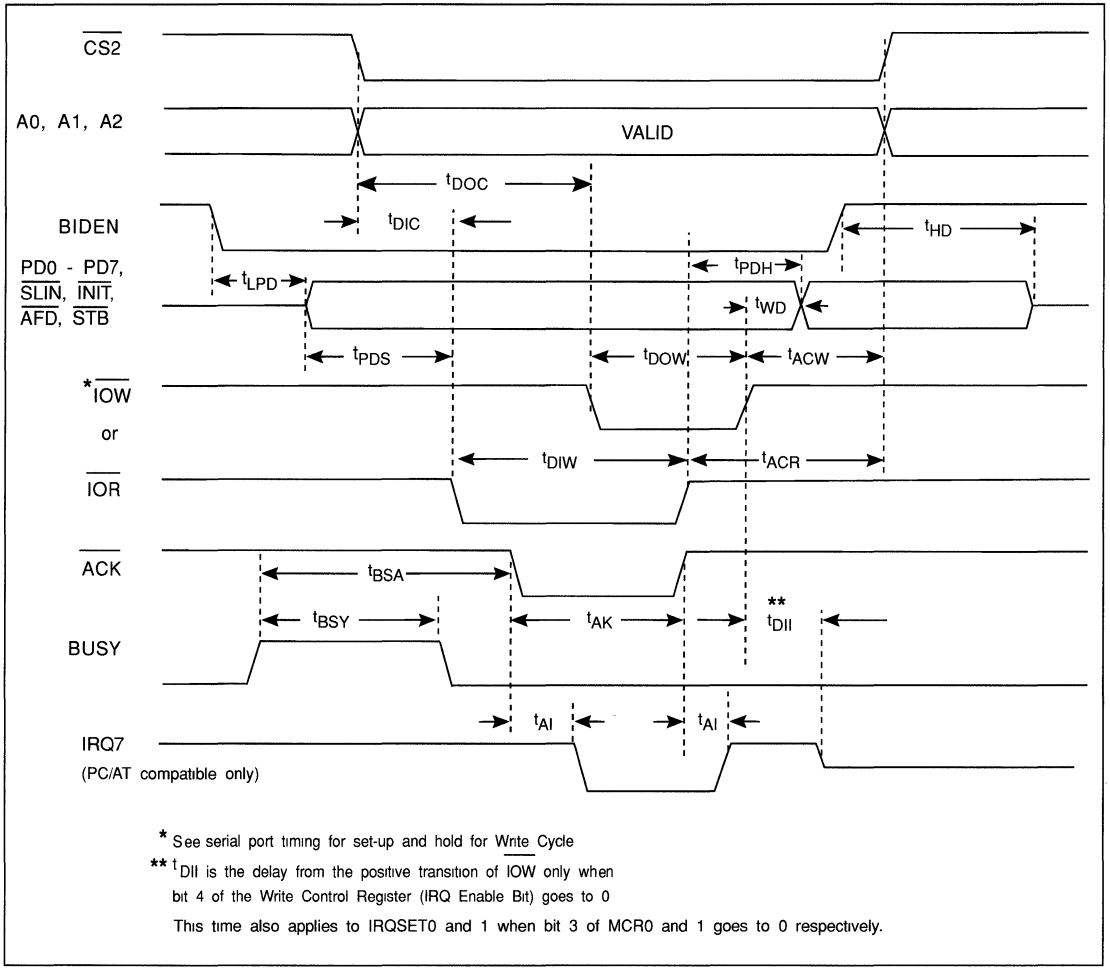


FIGURE 6-8. PARALLEL PORT TIMING - NO FPP READ/WRITE

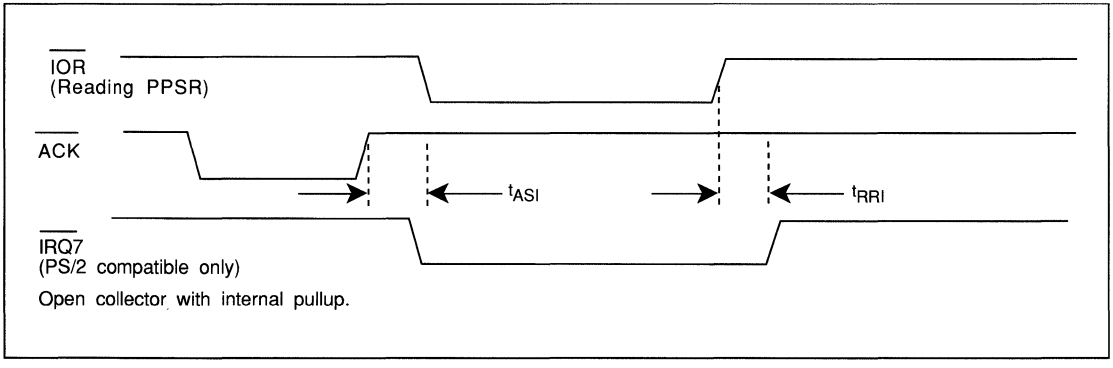


FIGURE 6-9. PARALLEL PORT INTERRUPT TIMING - NO FPP READ/WRITE

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
t_{DOC}	$\overline{IOW}$ Delay from Chip Select and Address	30		ns	
t_{DIC}	$\overline{IOR}$ Delay from Chip Select and Address	30		ns	
t_{WD}	$\overline{IOW}$ High to PD(0:7), $\overline{SLIN}$, $\overline{INIT}$, $\overline{AFD}$, $\overline{STB}$		1	µs	No External Pull-up Resistor and 50 pF Load
t_{HD}	BIDEN High to PD(0:7) Tristate		120	ns	50 pF Load
t_{LPD}	BIDEN Low to PD(0:7) Delay		100	ns	50 pF Load
t_{PDH}	PD(0:7) Hold Time from $\overline{IOR}$	100		ns	
t_{PDS}	PD(0:7) Setup Time from $\overline{IOR}$	100		ns	
t_{DOW}	$\overline{IOW}$ Strobe Width	100		ns	
t_{DIW}	$\overline{IOR}$ Strobe Width	125		ns	
t_{ACW}	Chip Select and Address Hold Time from $\overline{IOW}$	20		ns	
t_{ACR}	Chip Select and Address Hold Time from $\overline{IOR}$	20		ns	
t_{BSA}	BUSY Start to $\overline{ACK}$	0		ns	
t_{BSY}	BUSY Width	100		ns	
t_{AK}	$\overline{ACK}$ Width	100		ns	
t_{AI}	IRQ7 Delay from $\overline{ACK}$		60	ns	50 pF Load
tASI	$\overline{ACK}$ to set interrupt		60	ns	50 pF Load
t_{RRI}	Read Parallel Port Status Register (PPSR)		60	ns	50 pF Load
t_{DII}	$\overline{IOW}$ to Tristate	0	100	ns	50 pF Load

TABLE 6-9. PARALLEL PORT TIMING - NO FPP READ/WRITE

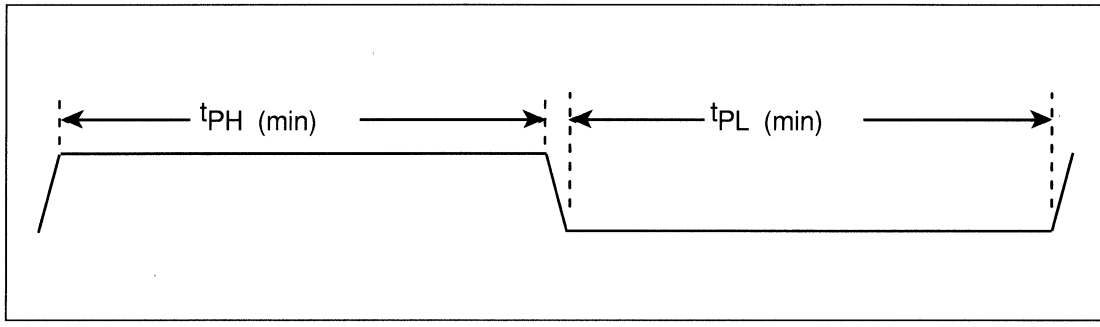


FIGURE 6-10. CLOCK GENERATION TIMING

CLOCK TYPE	tPH min. ns.	tPL min. ns.	FREQUENCY MHz	MAX. EDGE DELAY ① FROM MSTRX1 EDGE
CLK287 SEL				
0	40	68	8	100 ns
1	28	60	9.6	100 ns
2	20	50	12	100 ns
3	35	35	12	100 ns
4	14	35	16	100 ns
5	25	25	16	100 ns
KBCLK	50	33	9.6	100 ns
ATCLK	27	25	16	100 ns
MSTRX1	8	8	48	N/A

TABLE 6-10. CLOCK GENERATION TIMING

① All 50 pF loads

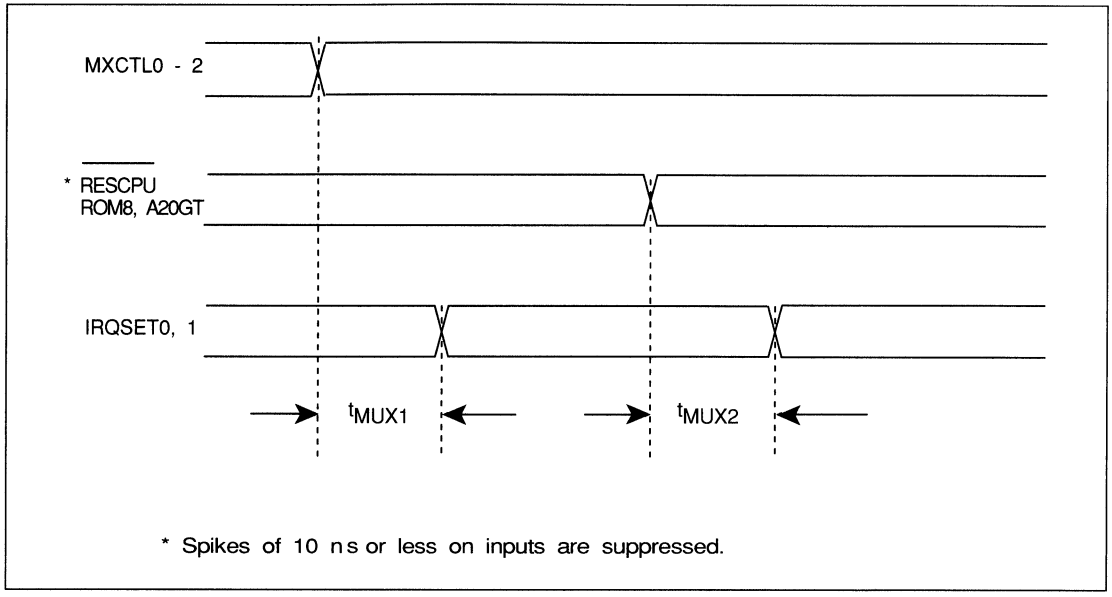


FIGURE 6-11. INTERRUPT MUX TIMING - A

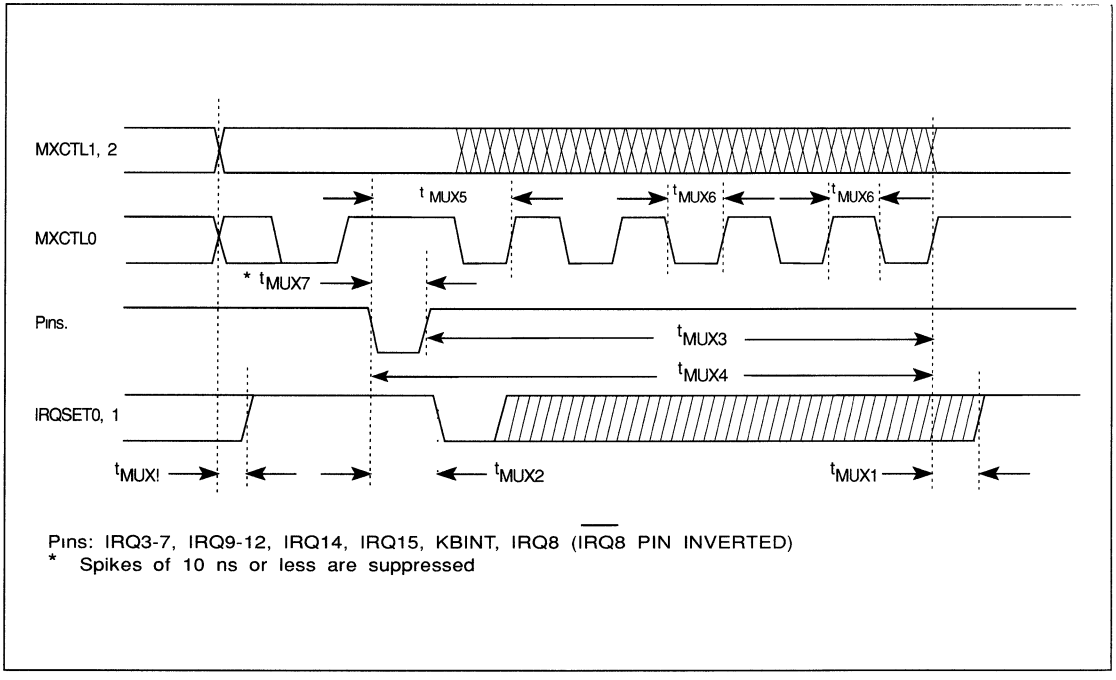


FIGURE 6-12. INTERRUPT MUX TIMING - B

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
$^tMUX1$	Delay from MUX control change		25	ns	50 pF load
$^tMUX2$	Delay from MUX input going low		125	ns	50 pF load
$^tMUX3$	Rising MXCTL0 clock edges required	3	5		
$^tMUX4$	Rising MXCTL0 clock edges required	5			
$^tMUX5$	MUX input setup time	100		ns	
$^tMUX6$	MXCTL(0:2) pulse width	40		ns	
$^tMUX7$	Pins pulse width	75		ns	

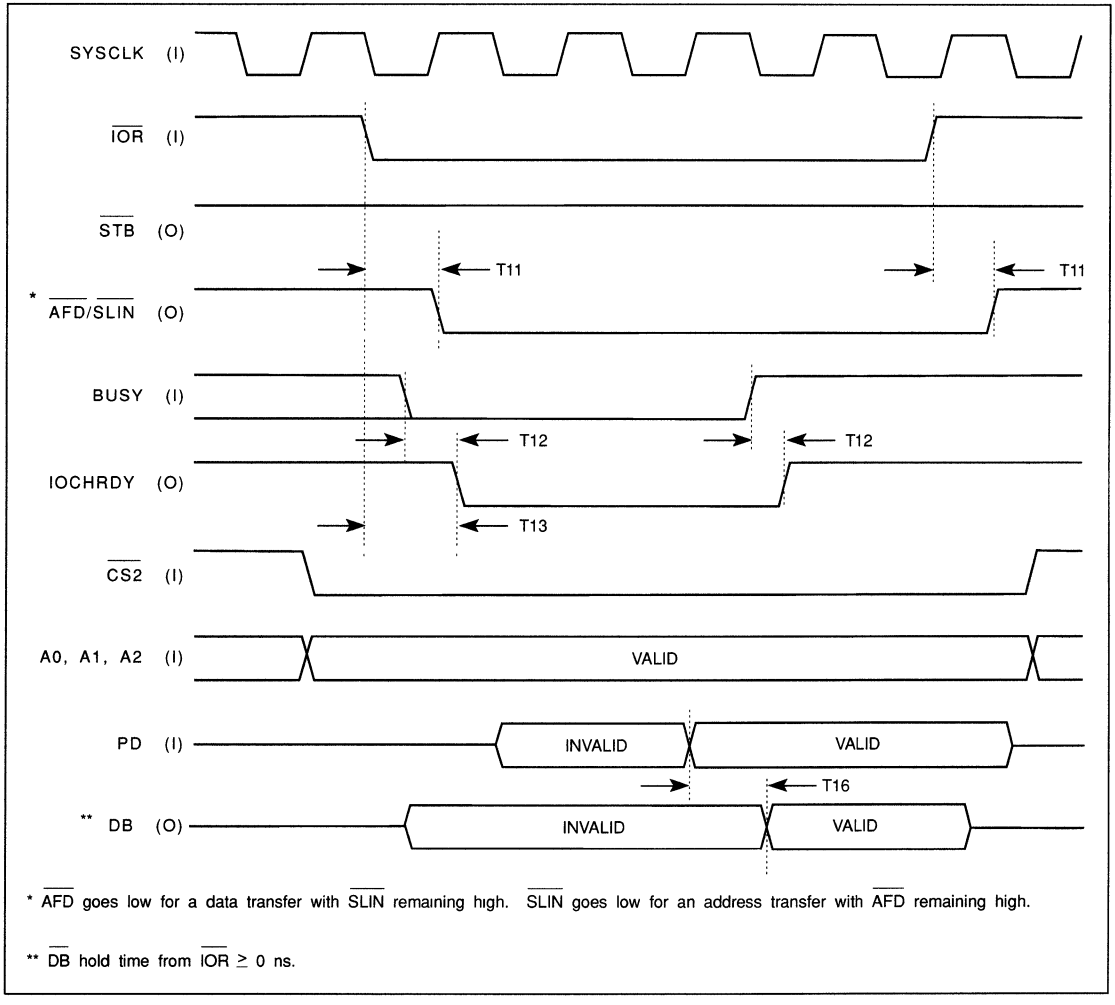
TABLE 6-11. INTERRUPT MUX TIMING

6.5.1 Fast Parallel Port Timing

To prevent IOCHRDY from overriding $\overline{ZWS}$ and provide more setup time for BUSY, IOCHRDY must not be driven low until two leading edges of SYSCLK after the assertion of $\overline{IOW}$ or $\overline{IOR}$.

IOCHRDY buffer is capable of 12 mA sinking and 4 mA sourcing current.

The parameters for Figures 6-13 through 6-21 are presented in Table 6-12, which follows Figure 6-21.



* $\overline{AFD}$ goes low for a data transfer with $\overline{SLIN}$ remaining high. $\overline{SLIN}$ goes low for an address transfer with $\overline{AFD}$ remaining high.

** $\overline{DB}$ hold time from $\overline{IOR}$ ≥ 0 ns.

FIGURE 6-13. DEFAULT READ TIMING (FPP) $\overline{ZWS}$ MODE DISABLED

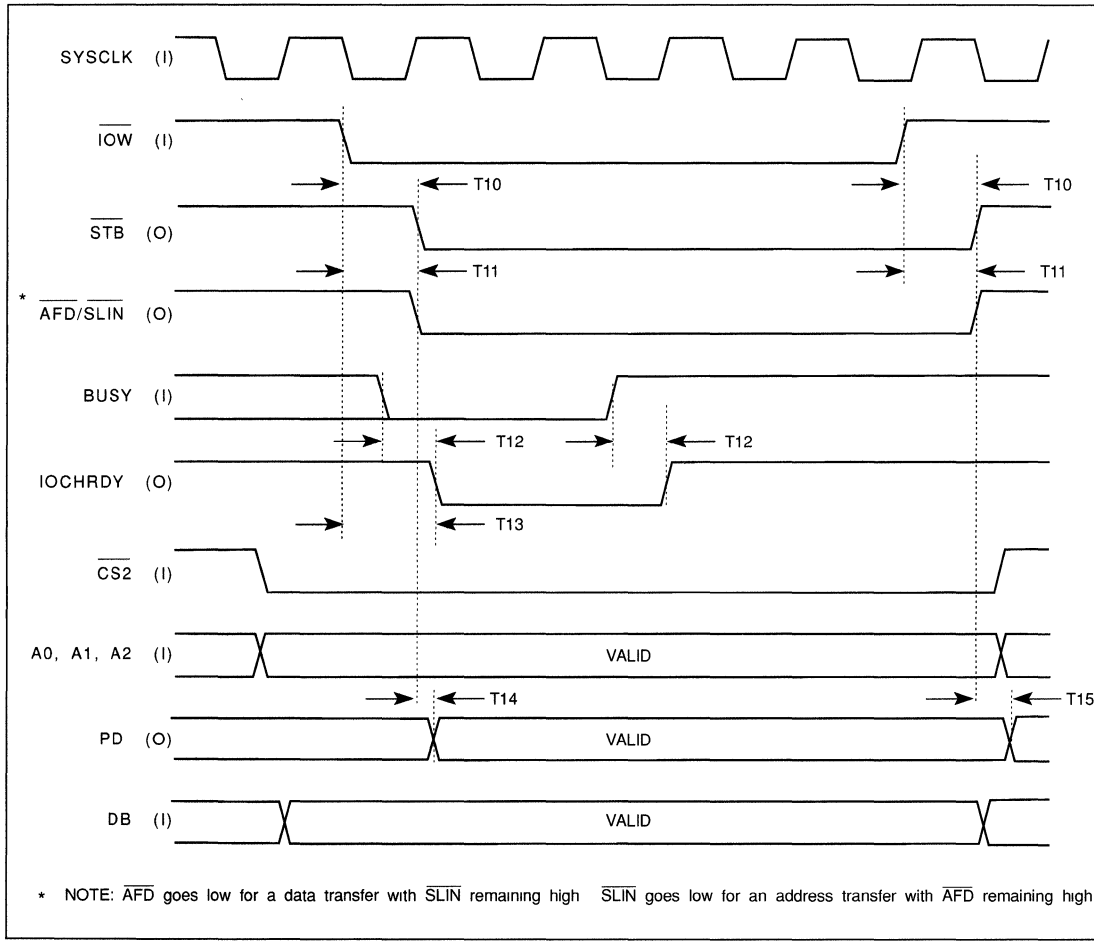


FIGURE 6-14. DEFAULT WRITE TIMING (FPP) ZWS MODE DISABLED

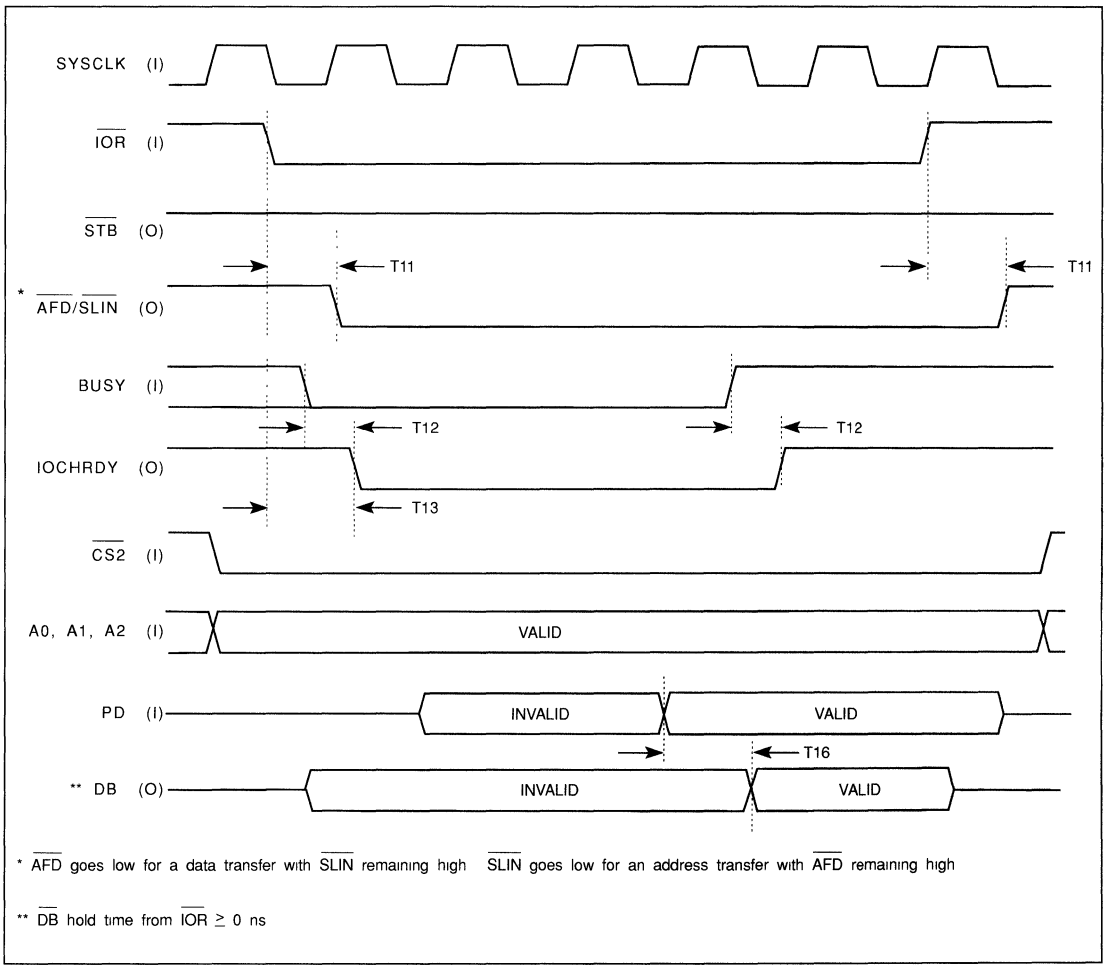


FIGURE 6-15. READ TIMING WITH ONE WAIT STATE (FPP) ZWS MODE DISABLED

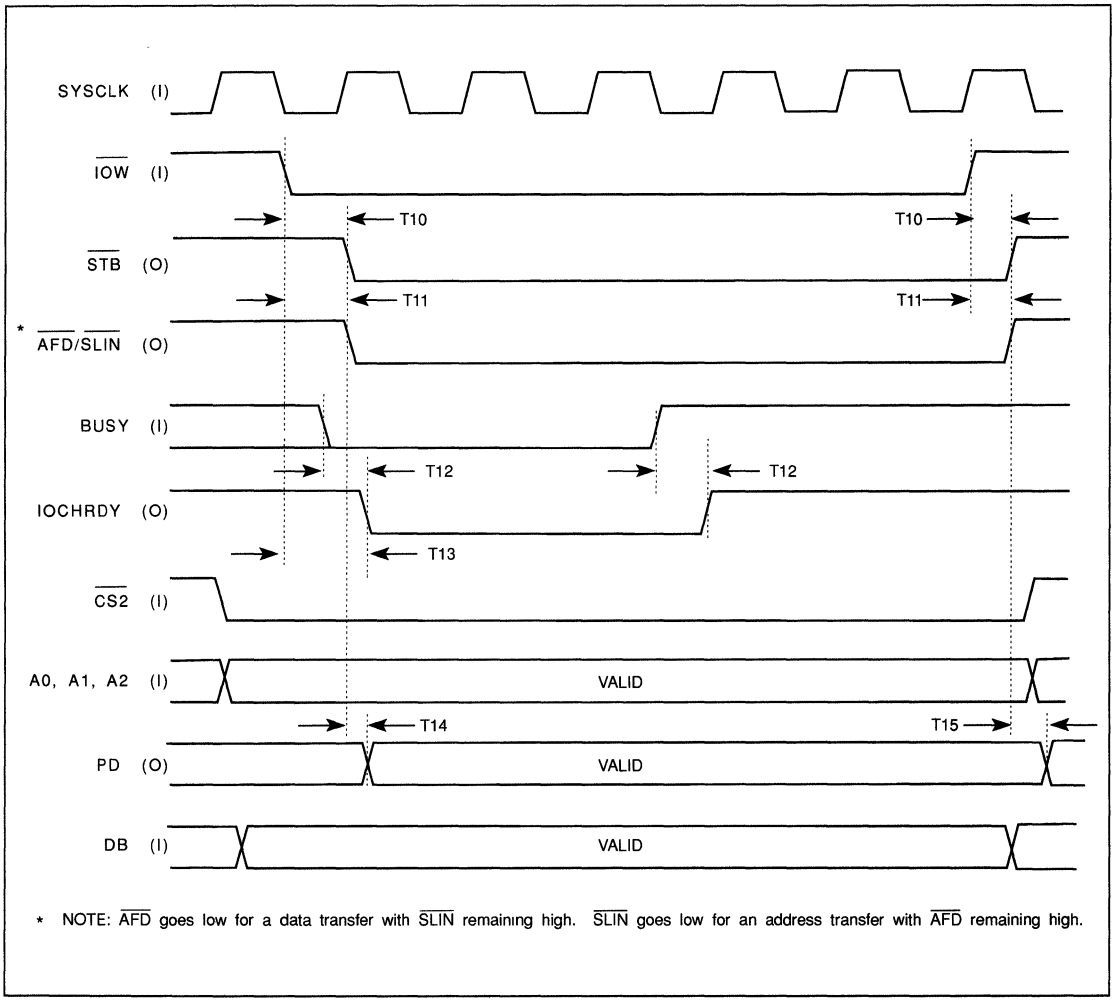
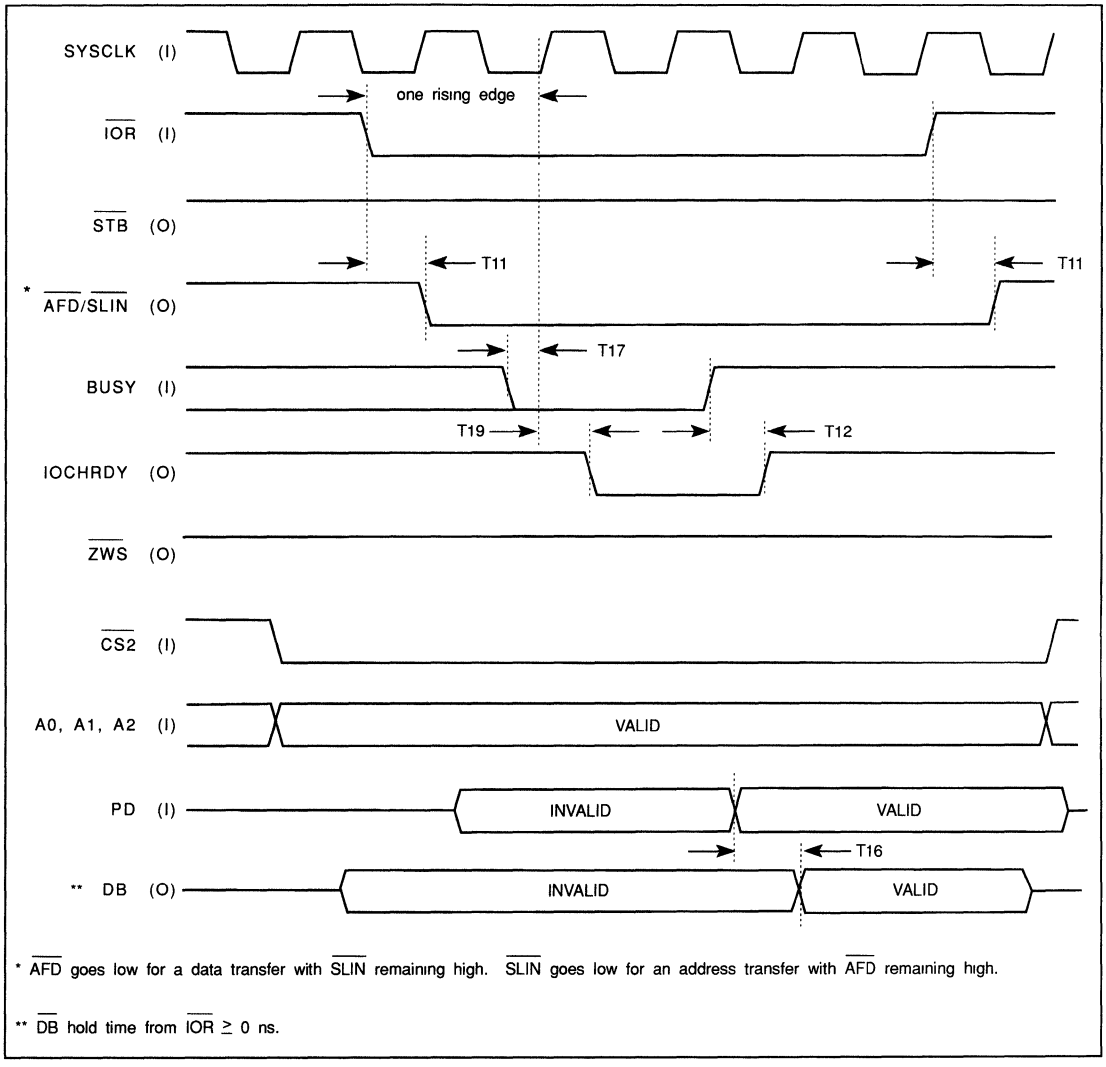


FIGURE 6-16. WRITE TIMING WITH ONE WAIT STATE (FPP) ZWS MODE DISABLED



* AFD goes low for a data transfer with SLIN remaining high. SLIN goes low for an address transfer with AFD remaining high.

** DB hold time from IOR ≥ 0 ns.

FIGURE 6-17. DEFAULT READ TIMING (FPP) ZWS MODE ENABLED

9

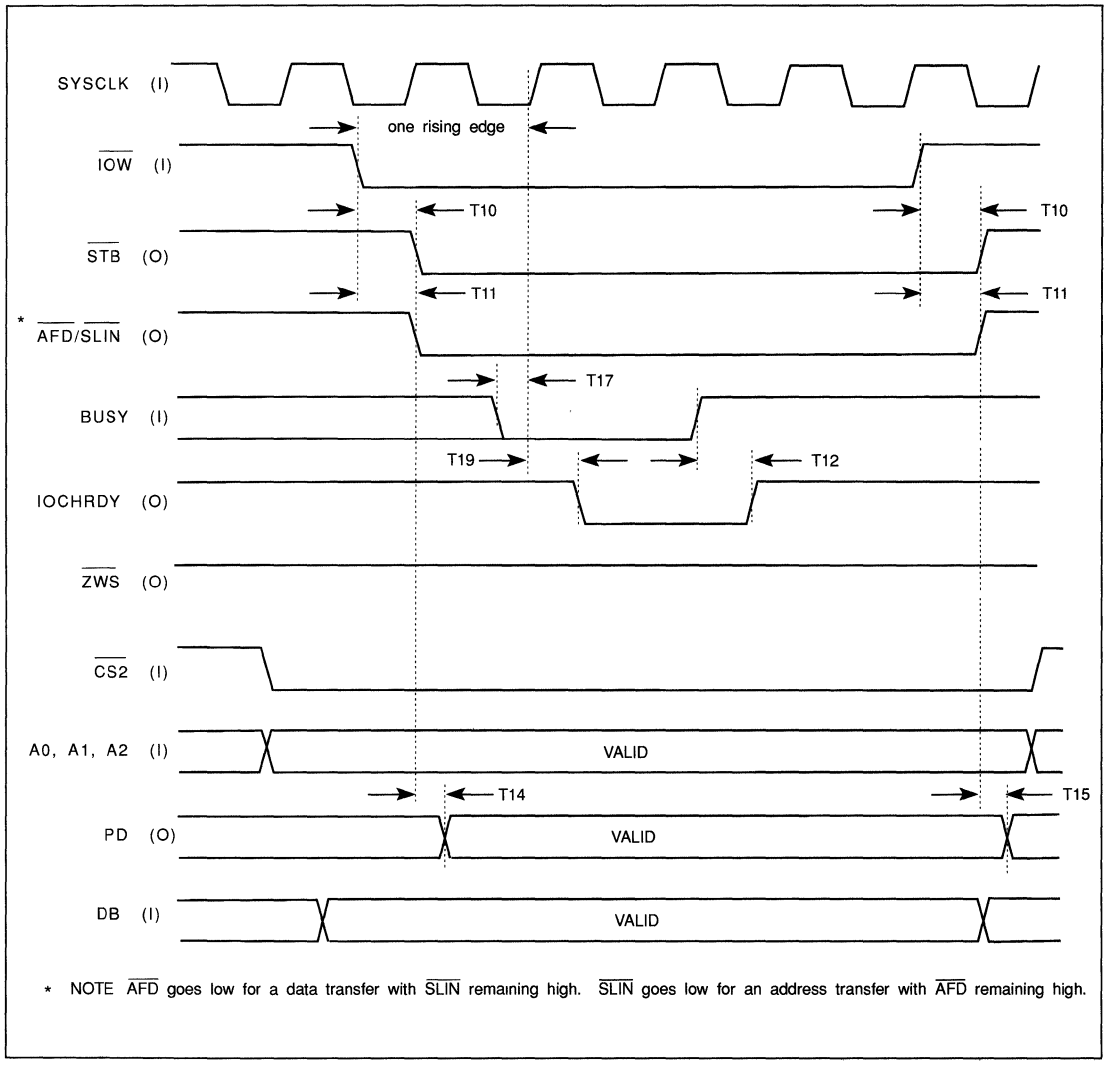
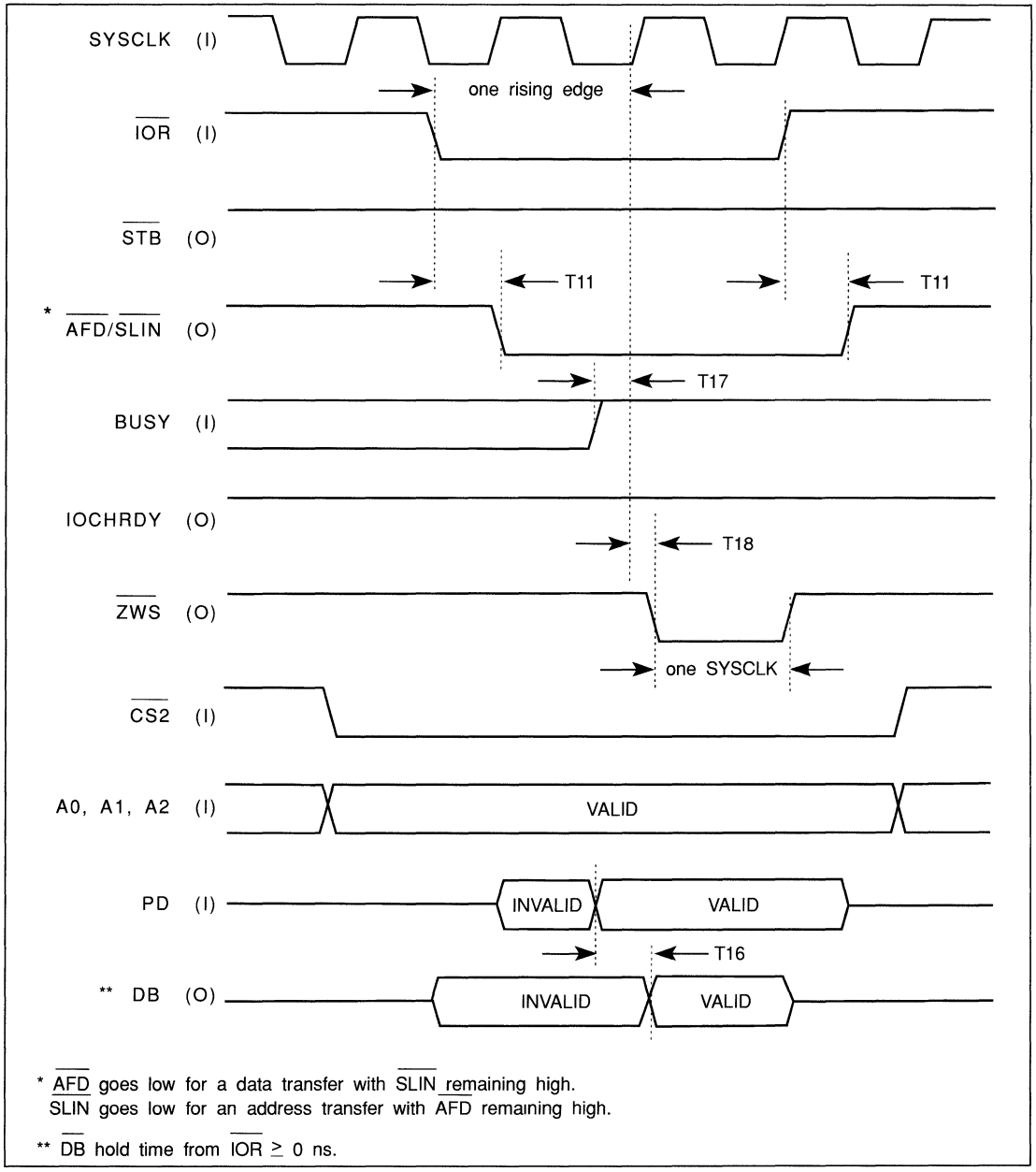


FIGURE 6-18. DEFAULT WRITE TIMING (FPP) ZWS MODE ENABLED

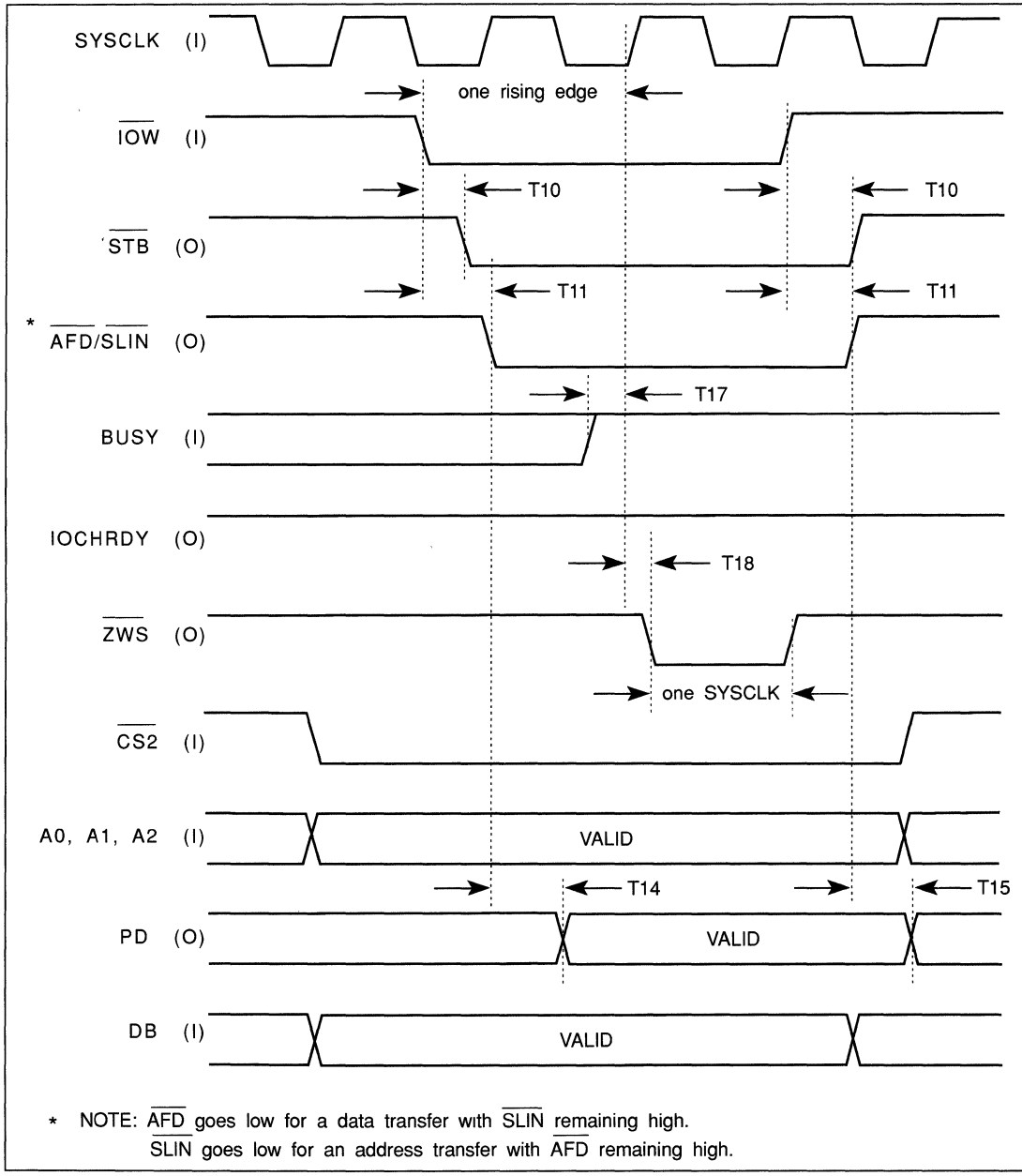


* AFD goes low for a data transfer with SLIN remaining high.
SLIN goes low for an address transfer with AFD remaining high.

** DB hold time from IOR ≥ 0 ns.

FIGURE 6-19. FAST READ TIMING (FPP) ZWS MODE ENABLED

9



* NOTE: AFD goes low for a data transfer with SLIN remaining high.
SLIN goes low for an address transfer with AFD remaining high.

FIGURE 6-20. FAST WRITE TIMING (FPP) ZWS MODE ENABLED

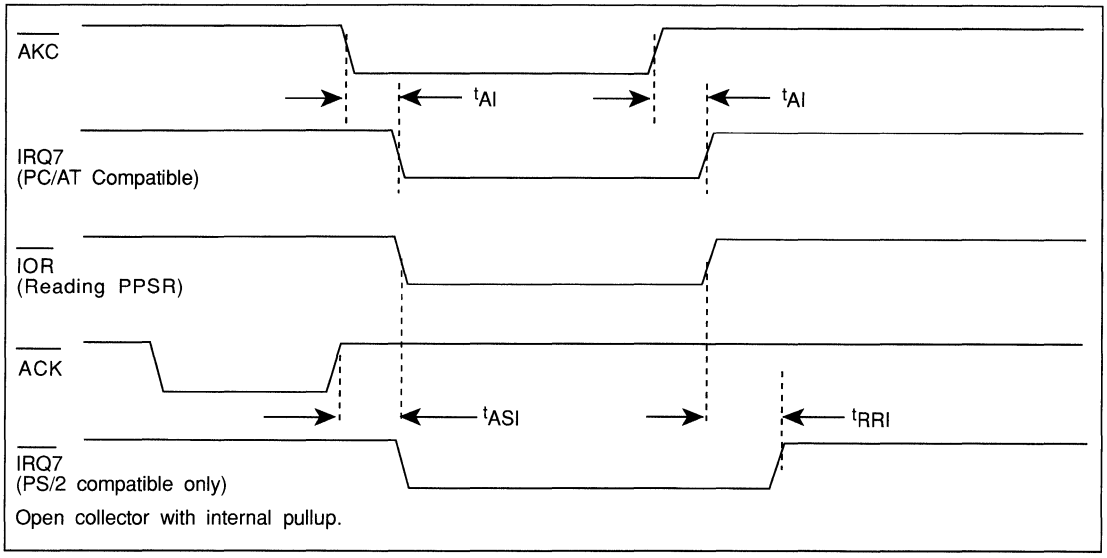


FIGURE 6-21. PARALLEL PORT INTERRUPT TIMING (FPP READ/WRITE)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	TEST CONDITIONS
T10	$\overline{IOW}$ to $\overline{STB}$ delay		30	ns	100 pF load
T11	$\overline{IOW}$/$\overline{IOR}$ to $\overline{AFD}$/$\overline{SLIN}$ delay		30	ns	100 pF load
T12	BUSY to IOCHRDY delay		30	ns	100 pF load
T13	$\overline{IOW}$/$\overline{IOR}$ to IOCHRDY		30	ns	100 pF load
T14	$\overline{STB}$/$\overline{AFD}$/$\overline{SLIN}$ to PD bus		15	ns	100 pF load
T15	PD Bus hold time from $\overline{STB}$/$\overline{AFD}$/$\overline{SLIN}$		50	ns	100 pF load
T16	PD Bus to DB Bus delay		80	ns	350 pF load
T17	BUSY setup to SYSCLK	15		ns	
T18	SYSCLK to $\overline{ZWS}$ delay		22	ns	100 pF load
T19	SYSCLK to IOCHRDY delay		50	ns	100 pF load
TAI	IRQ7 delay from $\overline{ACK}$		60	ns	50 pF load
TASI	$\overline{ACK}$ to set intrrupt		60	ns	50 pF load
TRRI	Read Parallel Port Status register		60	ns	50 pF load

TABLE 6-12. FPP TIMING

7.0 POWER NETWORKS

The WD76C30ALV Peripheral Controller logic and I/O buffers are powered by three individual power networks, each having their own power pins. The WD76C30ALV is capable of operating under 5 volts only, or a mix of 5 volts and 3.3 volts.

The power networks are divided into the following groups:

Core logic
3.3 volt I/O ring
5 volt parallel port I/O

This section provides a description of the three power networks, as well as a table showing the state of all pins at power down.

7.1 CORE LOGIC

The core logic consists of the serial and non-data parallel port logic. With the exception of the Parallel Port Data bus PD(7:0), all parallel port inputs are included in the core logic.

The parallel port input signals included in the core logic are:

BIDEN	$\overline{\text{ERROR}}$
SLCT	PE
BUSY	$\overline{\text{ACK}}$
$\overline{\text{STB}}$	$\overline{\text{AFD}}$
$\overline{\text{SLIN}}$	$\overline{\text{INIT}}$

The core logic is powered by the VDD power pins.

7.2 3.3 VOLT I/O RING

The 3.3 volt I/O ring consists of the Serial Port I/O, AT data bus, Interrupt Multiplexer I/O, all other outputs and all input buffers with the exception of the previously mentioned ten parallel port input buffers in the Core Logic.

The output buffers are:

$\overline{\text{SOUT(1:0)}}$	$\overline{\text{DTR(1:0)}}$
$\overline{\text{RTS(1:0)}}$	DB(7:0)
CLK287	IRQSET(1:0)
KBCLK	ATCLK

The input buffers are:

$\overline{\text{DB(7:0)}}$	$\overline{\text{IOR}}$	$\overline{\text{MXCLT(2:0)}}$
$\overline{\text{DSR(1:0)}}$	$\overline{\text{CS(2:0)}}$	$\overline{\text{RESCPU}}$
$\overline{\text{RI(1:0)}}$	$\overline{\text{RESET}}$	ROM8
$\overline{\text{RLSD(1:0)}}$	PD(7:0)	SYSCLK
$\overline{\text{SIN(1:0)}}$	$\overline{\text{IRQ(3:7)}}$	KBINT
$\overline{\text{CTS(1:0)}}$	$\overline{\text{IRQ8}}$	A20GT
$\overline{\text{A(2:0)}}$	IRQ(9:12)	
$\overline{\text{IOW}}$	IRQ(14:15)	

The 3.3 volt I/O ring is powered by the VDD3 power pins.

7.3 5 VOLT PARALLEL PORT I/O

The 5 volt parallel port consists of the Parallel Port outputs and, with the exception of the I/O databus, the ATBUS interface outputs.

The 5 volt Parallel Port output signals are:

PD(7:0)	IRQ7/$\overline{\text{IRQ7}}$
$\overline{\text{ZWS}}$	IOCHRDY
$\overline{\text{STB}}$	$\overline{\text{AFD}}$
$\overline{\text{SLIN}}$	$\overline{\text{INIT}}$

The 5 volt Parallel Port I/O logic is powered by VDD5 power pins.

7.4 SUPPORTED POWER NETWORK VOLTAGE COMBINATIONS

DESCRIPTION	VDD	VDD3	VDD5
5 volt operation only	5 volt	5 volt	5 volt
5 volt only, power down mode	0 volt	5 volt	5 volt
Mixed mode operation	3.3 volt	3.3 volt	5 volt
Mixed mode, power-down mode	0 volt	3.3 volt	5 volt
Mixed mode, suspend mode	3.3 volt	3.3 volt	3.3 volt
Mixed mode, power down, suspend mode	0 volt	3.3 volt	3.3 volt

No other combinations are allowed.

7.5 REQUIREMENTS FOR TYPICAL 3.3 VOLT LAPTOP DESIGNS

Table 7-1 represents the voltages applied to or expected from the WD76C30ALV's pins in a typical 3.3 volt design. The voltages listed for output pins are the required levels that those pins should drive out, not levels that might be applied to those pins from other sources. Voltages listed for bidirectional pins, such as the parallel port data bus, may represent input or output levels. The footnotes following table 7-1 supply a more detailed explanation.

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE		
			NORMAL	SER/PAR POWER DOWN	SUSPEND
Serial Ports					
	$\overline{DSR}(1:0)$	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
	$\overline{RLSD}(1:0)$	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
	SIN(1:0)	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
	$\overline{CTS}(1:0)$	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
	$\overline{RI}(1:0)$	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
	SOUT(1:0)	O	0 - 3.3V ③	Z ②	Z ②
	$\overline{DTR}(1:0)$	O	0 - 3.3V ③	Z ②	Z ②
	$\overline{RTS}(1:0)$	O	0 - 3.3V ③	Z ②	Z ②
AT Bus Interface ④					
RAD Bus	DB(7:0)	I/O	0 - 3.3V	0 - 3.3V	0 - 3.3V
System Address Bus	A(2:0)	I	0 - VDD5	0 - VDD5	0V or Z ⑤
I/O Strobes	$\overline{IOW}$, $\overline{IOR}$	I	0 - VDD5	0 - VDD5	0V or Z ⑤
	IRQ7/$\overline{IRQ7}$	I/O	0 - VDD5	0 - VDD5	0 - VDD5 ②
	$\overline{IRQ8}$	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	IRQ(15:14) IRQ(12:9) IRQ(6:3)	I	0 - VDD5	0 - VDD5	0 - VDD5 ②
	$\overline{ZWS}$	O	OD ⑥	Z ⑥	Z ② ⑥
	SYSCLK	I	0 - VDD5	0 - VDD5	0V or Z ②
	IOCHRDY/CLK287	O	0 - VDD5⑥/ 0 - 3.3V	Z ⑥ / 0 - 3.3V	Z ② ⑥/ Z
Parallel Port					
	BIDEN	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
Parallel Data Bus	PD(7:0)	I/O	0 - 5V ③	0V or Z/Z ⑤	0V or Z/Z ⑤
	$\overline{STB}$, $\overline{AFD}$, $\overline{INITD}$, $\overline{SLIN}$	I/O	0 - 5V ③	0 - 5V/Z ②	0 - 5V/Z ②
	$\overline{ERROR}$, $\overline{SLCT}$, PE, BUSY, $\overline{ACK}$	I	0 - 5V ①	0 - 5V ②	0 - 5V ②
IRQ Multiplexer					
	MXCTL(2:0)	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	IRQSET(1:0)	O	0 - 3.3V	0 - 3.3V	0 - 3.3V

TABLE 7-1. I/O VOLTAGE REQUIREMENTS

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE		
			NORMAL	SER/PAR POWER DOWN	SUSPEND
Miscellaneous					
	$\overline{\text{RESET}}$	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	$\overline{\text{CS}}$(2:0)	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	$\overline{\text{RESCPU}}$	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	ROM8	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	KBINT	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	A20GT	I	0 - 3.3V	0 - 3.3V	0 - 3.3V
	MSTRX1	I	0 - 3.3V ⑦	0 - 3.3V ⑦	0 - 3.3V or Z ⑦
	KBCLK	O	0 - 3.3V	0 - 3.3V	Z
	ATCLK	O	0 - 3.3V	0 - 3.3V	Z
Power					
3.3 Volt Serial/Parallel Core	VDD pin 64/88	N/A	3.3V	0V	0V
5 Volt Parallel Port	VDD5 pin 3/15	N/A	5V	5V	3.3V ⑧
3.3 Volt I/O Ring	VDD3 pin 22/38	N/A	3.3V	3.3V	3.3V

① This signal may be driven to 3.3 volts or 5 volts by a peripheral attached to the port or it may be connected to a device that is powered down.

② This signal is connected to a device that may be powered down. The input buffer (if I or I/O) should be internally disabled. The output buffer (if O or I/O) for this signal should be tristated.

③ This signal is connected to a device that may be powered down.

④ Power distribution to the AT bus is design dependent. Power to the AT bus connectors may be at 5 volts or 3.3 volts and may be switched off or remain on during suspend. In addition, the WD76C30ALV's VDD5 power pin may drop from 5 volts to 3.3 volts during suspend.

⑤ This signal is connected to a device that is powered down or tristated. The input buffer (if I or I/O) should be internally disabled. The output buffer (if O or I/O) for this signal should be tristated.

⑥ This signal is an open-drain output but actively drives high for two 48 MHz clocks on a rising transition. An external pullup is connected.

⑦ This level is for when MSTRX1 is driven by an external TTL oscillator.

⑧ During suspend, the system may be designed to lower 5 volts to 3.3 volts but not down to 0 volts.

TABLE 7-1. I/O VOLTAGE REQUIREMENTS (Continued)

SIGNAL NAME	① INPUT/ OUTPUT	② SERIAL ③ PARALLEL POWER DOWN	② FULL ③ POWER DOWN
$\overline{\text{DTR0}}$	O	OZ	OZ
$\overline{\text{DTR1}}$	O	OZ	OZ
$\overline{\text{RTS0}}$	O	OZ	OZ
$\overline{\text{RTS1}}$	O	OZ	OZ
SOUT1, 0	O	OZ	OZ
ATCLK ⑤ ⑦	O, P	O, PZ	OZ, PL
CLK287 ⑥ ⑦	O, P	O, PZ	OZ, PL
KBCLK ⑤ ⑦	O, P	O, PZ	OZ, PL
IRQSET1, 0	O	O	OZ
PD(7:0)	I, O	IX, OZ	IX, OZ
BIDEN ⑧	I, P	IX, PZ	IX, PZ
$\overline{\text{ERROR}}$	I	IX	IX
SLCT	I	IX	IX
PE	I	IX	IX
$\overline{\text{ACK}}$	I	IX	IX
BUSY	I	IX	IX
$\overline{\text{INIT}}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
$\overline{\text{SLIN}}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
$\overline{\text{STB}}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
$\overline{\text{AFD}}$	I, O, P	IX, OZ, PZ	IX, OZ, PZ
$\overline{\text{CS0}}$	I	I	I
$\overline{\text{CS2}}$	I	I	I
$\overline{\text{CS1}}$	I, P	I, PH	I, PZ
$\overline{\text{RLSD0}}$	I	IX	
$\overline{\text{CTS0}}$	I	IX	IX
$\overline{\text{RI0}}$	I	IX	IX
$\overline{\text{DSR0}}$	I	IX	IX
$\overline{\text{CTS1}}$	I	IX	IX
$\overline{\text{RLSD1}}$	I	IX	IX
$\overline{\text{RI1}}$	I	IX	IX
$\overline{\text{DSR1}}$	I	IX	IX
SIN1, 0	I	IX	IX
MXCTL(2:0)	I	I	IX
IRQ(3:6)	I, P	I, PH	IX, PZ
IRQ7/IRQ7	I, O, P	I, O, PH	IX, OZ, PZ
IRQ8	I, P	I, PH	IX, PZ
IRQ(9:12)	I, P	I, PH	IX, PZ
IRQ14, 15	I, P	I, PH	IX, PZ
ROM8	I, P	I, PH	IX, PZ
A20GT	I, P	I, PH	IX, PZ
$\overline{\text{ZWS}}$	O	OZ	OZ
IOCHRDY	O	OZ	OZ
SYSCLK	I	IX	IX

TABLE 7-2 STATE OF PINS AT POWER DOWN

SIGNAL NAME	① INPUT/ OUTPUT	② SERIAL ③ PARALLEL POWER DOWN	② FULL ③ POWER DOWN
$\overline{\text{KBINT}}$	I, P	I, PH	IX, PZ
$\overline{\text{RESCPU}}$	I, P	I, PH	IX, PZ
D(7:0)	I, O	I, O	IX, OZ
$\overline{\text{IOW}}$	I	I	IX
$\overline{\text{IOR}}$	I	I	IX
A(2:0)	I	I	IX
$\overline{\text{RESET}}$	I	I	I
MSTRX1 ④	I, O	I, OB	I, OH
MSTRX2	O	O	OL

①
BUFFER TYPE
I = Input buffer
O = Output buffer
P = Pullup or pulldown

②
POWER DOWN STATE
OZ = Tristate output
O = Driven output
OH = Output driven high
OL = Output driven low
OB = Output driven to oscillator BIAS point

I = Input enabled
IX = Input disabled, consumes no power, input between 0V and 5V
PH = Pullup enabled
PL = Pulldown enabled
PZ = Pullup or pulldown disabled

③ Serial/Parallel Power Down: PUD = 1(bit 3 of the Mode Selection Register described in section 5.5). Full Power Down: $\overline{\text{CS2}}$, $\overline{\text{CS1}}$ and $\overline{\text{CS0}}$ on pins 46/66, 47/67 and 48/68 are low simultaneously. This has priority over PUD.

④ When driven by a TTL oscillator, MSTRX1 requires an input low current (I_{il}) of approximately 1 mA. To eliminate this in full power down mode, the TTL oscillator driving MSTRX1 must be disabled or driven to +5 volts.

⑤ KBCLK and ATCLK can be programmed to stop with their outputs remaining low. Stopping is not synchronous and is separate from what happens during a full power down.

⑥ CLK287 can be programmed to stop with its output remaining either high or low. Stopping is synchronous and separate from what happens in full power down.

⑦ When entering full power down, the drivers for KBCLK, ATCLK and CLK287 are tristated and driven low by a pulldown FET that is only enabled during a full power down. This FET sinks a minimum of 45 µA, and drives the output low when connected to a CMOS input. Stopping is not synchronous.

⑧ BIDEN has an internal pullup so that applications requiring a high can leave it floating.

TABLE 7-2. STATE OF PINS AT POWER DOWN (Continued)

8 .0 PACKAGE DIMENSIONS

Figure 8-1. Illustrates the 84-Pin PQFP package showing the dimensions in inches.
Figure 8-2. Illustrates the 100-Pin SQFP package showing the dimensions in inches.

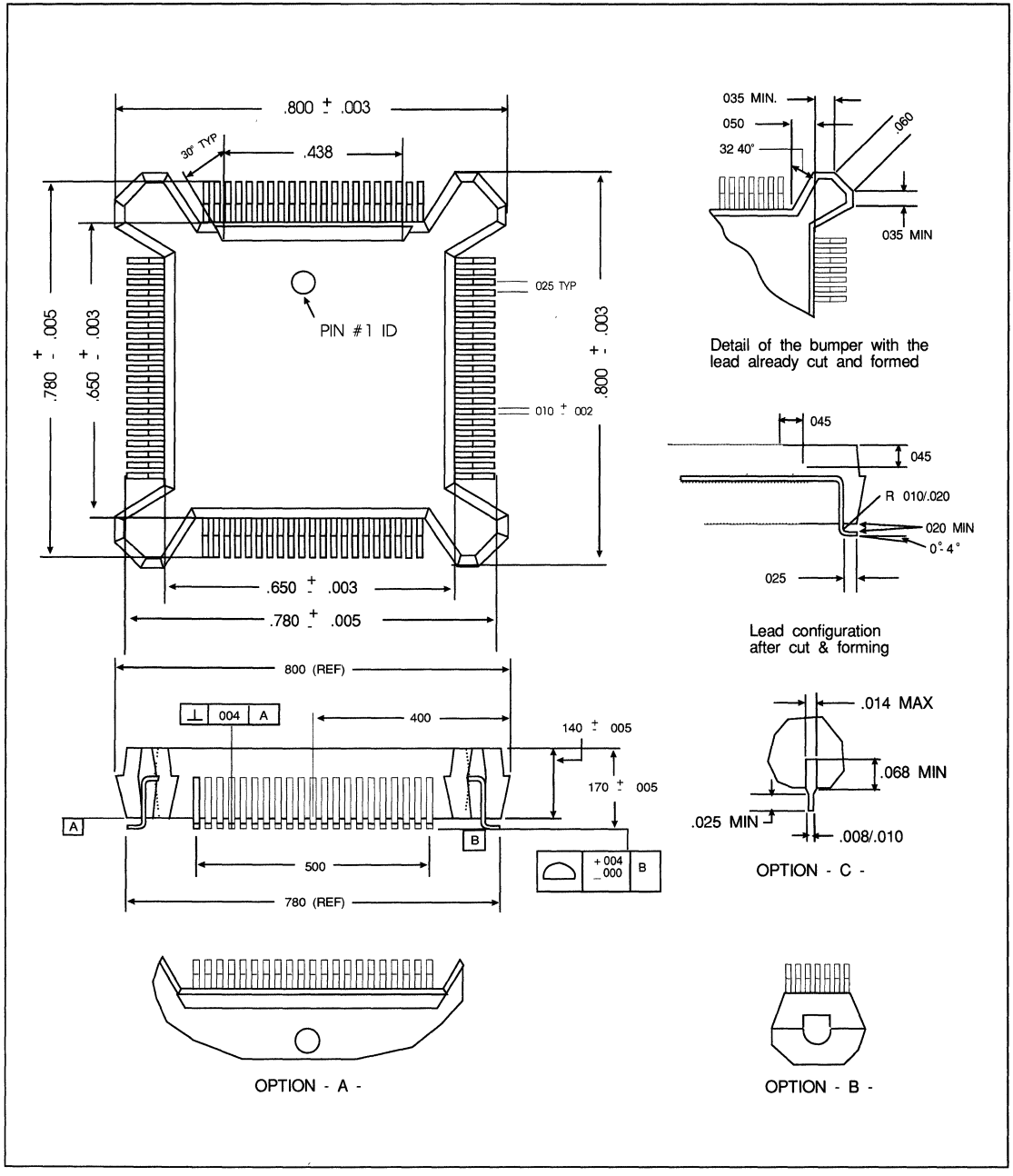


FIGURE 8-1. 84-PIN PQFP PACKAGE

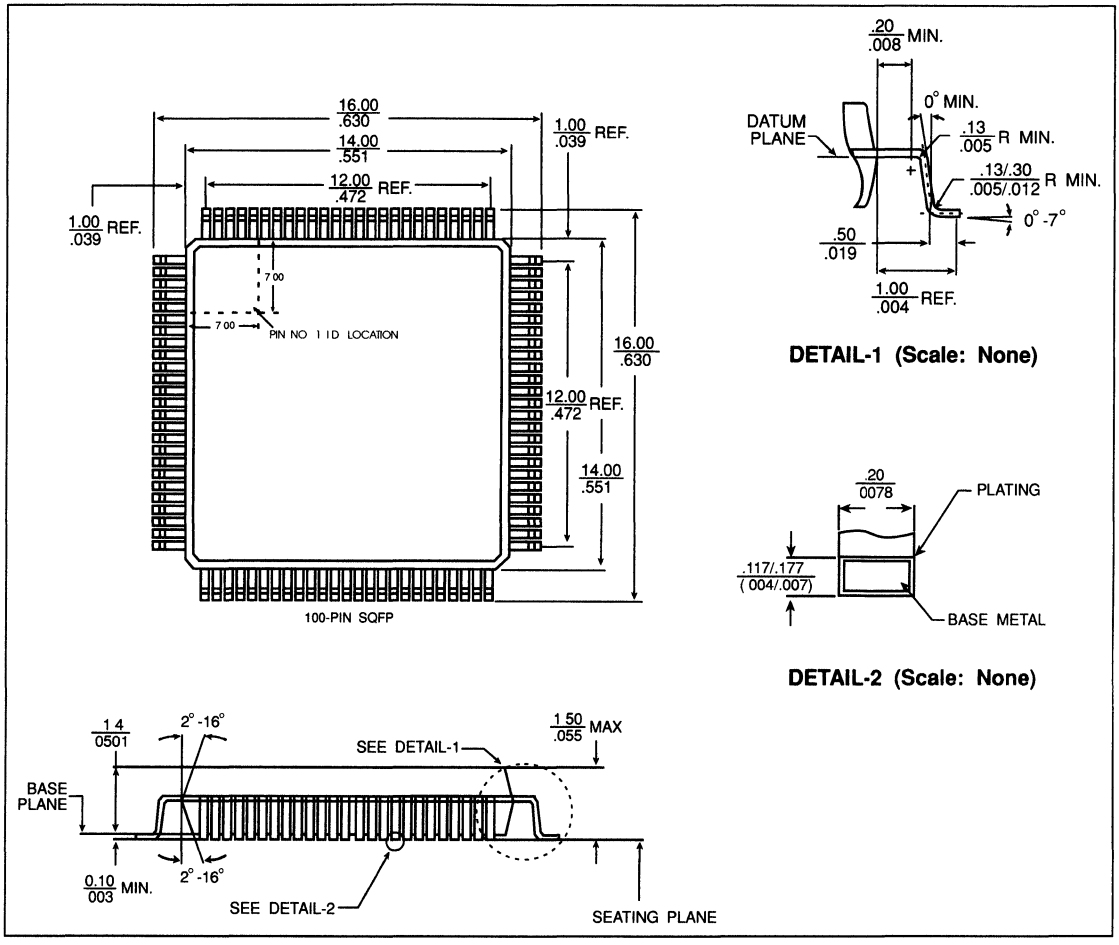


FIGURE 8-2. 100-PIN SQFP PACKAGE

9

9 .0 CRYSTAL MANUFACTURES (Partial List)

American Time Products Division
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Company
Eire, Pennsylvania 16508

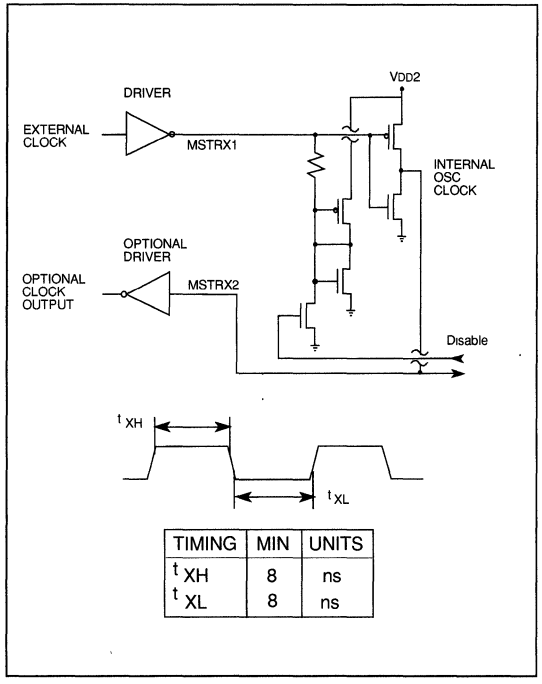
Cryster Crystals
Whitby, Ontario

Erie Frequency Control
Carlisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626

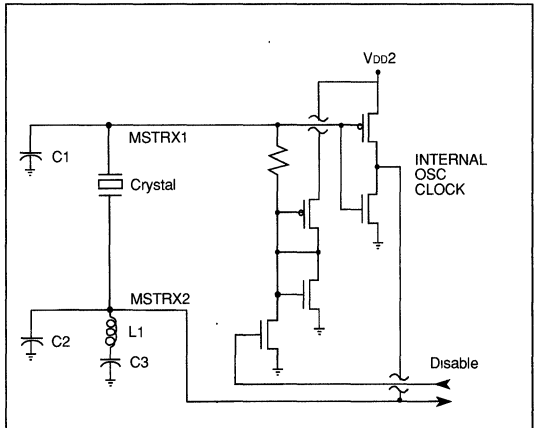
9.1 CRYSTAL SPECIFICATIONS

Series resonant frequency tolerance at 25° C	48.0 MHz ± 50 PPM
Series resonant frequency tolerance at 0° C TO 70° C	48.0 MHz ± 100 PPM
Mode of oscillation	Third overtone
Adjacent spurious frequency	20 db down, min.
Effective series resistance	80 ohms, max.
Shunt capacitance	5 pf max.
Drive level at room temperature	2000 microwatts
Operating temperature	0° C to 70° C
Insulation resistance	500M ohms/DC100V



TIMING	MIN	UNITS
tXH	8	ns
tXL	8	ns

FIGURE 9-1. EXTERNAL CLOCK INPUT (48 MHz MAX.)



L1	C1	C2	C3
33 uh 10% 5V	15 pF 5% 50V	10 pF 5% 50V	47 pF 5% 05V

Power up time after disable = 30 ms max

FIGURE 9-2. TYPICAL CRYSTAL OSCILLATOR NETWORK

APPENDIX
REVISION HISTORY - 1

This Revision History identifies the changes made from the document dated 11/19/91 to the document dated 6/10/92.

The major changes are:

- The WD76C30ALV is now packaged in an 84-pin PQFP and 100-pin SQFP package. The 84-pin PLCC has been deleted.
- Fast Parallel Port (FPP) function has been added.
- The WD76C30ALV is capable of operating at 5 volts or a combination of 5 volts and 3.3 volts, therefore the Appendix providing the low voltage specifications has been deleted and the specifications blended into section 6.
- References to WD76C10A has been changed to Western Digital System Controller.

SECTION	CHANGE
1.1 Features	Three features added, one modified.
1.2 General	Second paraghraph modified. Sixth paragraph added.
1.3 WD76C30/LV Differences	Section deleted.
1.3 Peripheral Controller	Was section 1.4
1.4 Fast Parallel Port	New
Figure 1-1	IOCHRDY, $\overline{ZWS}$ and SYSCLK added
2.0 Signal Description	Name changed from Pin Description. Text modified to represent elimination of the PLCC package, and the introduction of the PQFP and SQFP packages. Figure 2-1, Figure 2-2 and Table 2-1 new. Table 2-2 title changed to Signal Description and modified to represent 84-pin and 100-pin package, as well as FPP and power management.
3.4 ACE Programmable BAUD Rate Generator	Statement added to end of first paragraph.
Table 3-5	Last line added.
Table 4-1	New
Table 4-2	Note 3 added.
4.3 Control Register Write	Statement added to first paragraph. /4 added to Table 4-3.
5.2 Clock Selection Register	P38TB and P38SB added.
5.5 Mode Selection Register	$\overline{ZWS}$_AT, $\overline{ZWS}$_DT, BIDEN_OR and FPP_EN added.

SECTION	CHANGE
5.10 Version Register	Modified.
6.0 Electrical Specifications	Statement deleted.
6.1 Maximum Ratings	WD76C30 deleted from title. I/O voltages with respect to VSS and Power dissipation modified.
6.2 Capacitance	WD76C30 deleted from title. Vcc changed to Vdd and values modified.
6.3 DC Operating Characteristics - 5 Volt Operation	New.
6.4 DC Operating Characteristics - 3.3 Volt Operation	New.
6.5 AC Operating Characteristics And Timing	Was 6.4. Modified.
Table 6-4	Was Table 6-3. Modified.
Figure 6-8	No FPP Read/Write, added to caption.
Figure 6-9	No FPP Read/Write, added to caption.
Table 6-9	Was Table 6-8. No FPP Read/Write, added to caption.
6.5.1 Fast Parallel Port Timing	Entire section new, including Figures 6-13 through 6-21 and Table 6-12.
7.0 Power Networks	New.
7.1 Core Logic	New.
7.2 3.3 Volt I/O Ring	New.
7.3 5 Volt Parallel Port I/O	New.
7.4 Support Power Network Voltage Combinations	New.
7.5 Requirements For Typical 3.3 Volt Laptop Designs	New.
Table 7-1	New.
Table 7-2	Was Table 6-11, modified.
8.0 Package Dimensions	Was 7.0, 84-pin PLCC deleted.

REVISION HISTORY - 2

This Revision History identifies the changes made from the document dated 6/10/92 to the document dated 7/21/92.

SECTION	CHANGE
Table 2-2, page 7	Resistor values added to RTS(0:1).
Table 7-1, page 67	VDD5 suspend value changed. Note 9 modified. Note 8 deleted.