WD60C80

Error Detection and

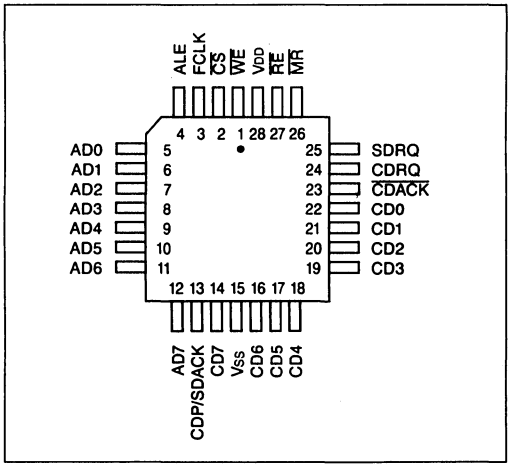
Correction Chip (EDAC)

WESTERN DIGITAL

WD60C80
Error Detection and Correction Chip (EDAC)

FEATURES

- High speed on-the-fly Reed-Solomon encoding and error detection up to 3 Mbyte/sec when clocked at 24 MHz. (Maximum clock frequency = 25.0 MHz)
  - —On-the-fly generation of check bytes and syndrome bytes. No latency associated with the code generation
  - —Programmable polynomial selections (degrees 4, 8, 16)
  - —Programmable interleave selections (1, 2, 3, 4, 5, 8, 10)
  - —Optional 4-byte GF(256) CRC
  - —Corrects up to 8-byte per interleave, or 80 bytes per sector
  - —Low redundancy overhead (7.8% for 1Kbyte sector, degree 16 and 5 interleaves, no CRC)
  - —Degree 16 and CRC polynomials are compatible with ANSI X3B11 standard
  - —Programmable sector size up to 2.5Kbyte (including data, CRC and ECC) in one-byte increments
  - —Write (ECC generation) and read (error detection) mode of operations
- Generates syndrome bytes compatible with the high-speed correction software algorithm licensed by Western Digital Corporation
  - —Zero latency delay for sectors with no error
  - —Supports correction of single byte error in 200 μsec using 8MHz 80188 microprocessor
- Fully independent processor port, allowing taskfile access at any time at all, independent of controller bus activity
  - —Full complement of programmable options and status information
  - —Status bytes with interleave-in-error number
  - —Supports simultaneous redundancy read/syndrome output transfers
- The internal 4-byte data path FIFO to capture data streams up to 1/5 the clock frequency (5.0 Mbyte/sec max.) without handshaking
  - —Optionally supports the parity bit on the controller bus
- The internal 20-byte syndrome FIFO to support continuous back-to-back transfer with minimal gap length
  - —Supports DMA or programmed I/O up to 1/5 the clock frequency (5.0 Mbyte/sec max.)
  - —Syndrome bytes can be directed to the controller bus to support single RAM application
- Low cost single chip Error Detection and Correction
- Protocol compatible with the WD60C40 PCM and WD10C00 Disk SerDes
- Using Hyperbolic Drivers™ to suppress power/ground transient noise
- Single +5V supply
- 28 pin PLCC package
- Implemented in 1¼ μm dual metal CMOS technology



WD60C80
DEVICE PINOUT

29

PIN DESCRIPTIONS

PIN	SYMBOL	PIN NAME	DESCRIPTION
1	$\overline{WE}$	Write Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile write operation by the processor.
2	$\overline{CS}$	Chip Select	TTL Input, Low Active; Controls the Taskfile access by the processor. The pin must be set high during the reset.
3	FCLK	Fast Clock	TTL Input; The primary clock input. f $\leq$25 MHz. The frequency must be greater than or equal to the nominal bit transfer rate for the application.
4	ALE	Address Latch Enable	TTL Input, High Active; The high level latches the multiplexed address vector on AD1-AD3 pins to the internal address register to control the Taskfile access.
5-12	AD0-AD7	Processor Data Bus	TTL Bidirectional, True Level; Multiplexed data/address bus used by the processor to access the internal Taskfile Registers and Syndrome transfer.
13	CDP/SDACK		TTL Bidirectional; Dual-Function Pin.
	CDP	CD bus Parity	TTL Bidirectional, True level; The parity bit input/output for the CD bus.
	SDACK	Syndrome DMA Acknowledge	TTL Input; Active Level Programmable. The external DMA controller indicating that the DMA cycle is granted.
14-22	CD0-CD7	Controller Data Bus	TTL Bidirectional, True Level; (Less Pin 15) Data, CRC, ECC bytes are transferred to/from the target disk controller via this bus. An option exists to use this bus for the Syndrome transfer.
15	VSS	Logic/Power Ground	
23	$\overline{CDACK}$	Controller Bus DMA Acknowledge	TTL Bidirectional, Low Active; During the data read phase, WD60C80 reads the data on CD bus while this signal (input) is active. During the redundancy read/write phases WD60C80 inputs/outputs the CRC/check bytes while this signal (output) is active.
24	CDRQ	Controller Bus DMA Request	TTL Input, High Active; DMA Request from the target disk controller. It is sampled and used for $\overline{REQ}$ ACK protocol between the WD60C80 and the controller/buffer manager during the redundancy read/ write phase of the operation.
25	SDRQ	Syndrome DMA Request	TTL Output, High Active; Indicates to the external DMA controller that syndrome bytes are ready to be transferred.
26	$\overline{MR}$	Master Reset	TTL Input, Low Active; Initializes the chip to the power-on default condition.
27	$\overline{RE}$	Read Enable	TTL Input, Low Active; ANDed with $\overline{CS}$, it controls the Taskfile read operation by the processor.
28	VDD	Power Supply	+5 V $\pm$ 10%

DESCRIPTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed, CMOS LSI, designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical for optical or magnetic disk drives, tape drives and communication links.

INTRODUCTION

The WD60C80 Error Detection And Correction (EDAC) device is a high-speed CMOS LSI designed to provide high power Reed-Solomon error correction code support for the applications where data integrity is critical.

The WD60C80 generates the Reed-Solomon code with the coefficients from GF(256) with the generator polynomials of degree four, eight or 16. It also generates 4-bytes GF(256) CRC code in order to (a) detect mis-corrections and (b) support extended correction to correct up to 16 bytes of error per interleave (depending on the polynomial degree chosen). The degree 16 polynomial and the CRC are the standard adopted by ANSI X3B11 committee to be used for optical disk storage.

Using degree 16 polynomials and 10 interleaves (interleave factors are programmable between one to 10 in seven steps), the WD60C80 can correct up to 80 bytes per sector of data with only 160 bytes of ECC overhead (164 if CRC is used).

The WD60C80 can be used to (a) generate ECC bytes (hereafter referred to as "check bytes" or "redundancies", interchangeably) by reading in the data field, or (b) generate the syndrome by reading the potentially erred data field and redundancies. The external processor needs to perform the actual data correction using the syndrome bytes. The software support is available from Western Digital Corporation.

The WD60C80 can be clocked as high as 25.0 MHz, and has the maximum byte/sec throughput of 1/8 the clock frequency. If this minimum clock frequency requirement is met, it can synchronize itself to the data flow and performs its function properly. Therefore, if an application calls for multiple data rates, this device can handle it without having its clock switched.

The WD60C80 can support the average data rate of up to three Mbyte/sec when clocked at 24 MHz, with the short burst (four bytes of less) of up to 4.8 Mbyte/sec. The code is generated on-the-fly at the data rate. It supports the sector size (including the check bytes and CRC) up to 2,550 bytes in one byte increment. Syndrome bytes can be transferred at the maximum speed of 4.8 Mbyte/sec when clocked at 24 MHz, and the internal 20-byte syndrome FIFO allows continuous back-to-back transfer of sectors with minimal inter-sector gap lengths.

In order to support the high data rate reliably, it employs the proprietary Hyperbolic Driver to suppress power/ground transient noise. The ground level transient noise is kept to less than 400 mV at all times.

The WD60C80 is applicable to all areas where error correction is important to maintain high data throughput and integrity such as controllers for optical or magnetic disk drives, tape drives and communication links.

The device is implemented using 1¼ μm double metal CMOS process, and packaged in a 28-pin PLCC. It requires a single + 5.0 Volt $\pm$ 10% supply and rated at the full specification in the temperature range of 0°C to 70°C.

ARCHITECTURE

The WD60C80 has two operation modes;
a) Read mode and
b) Write mode.

In read mode, it reads a full block of data and redundancies. The acquired data may contain errors, so it generates the redundancy code internally, and compares them with the acquired redundancies to generate syndrome bytes. These syndrome bytes, equal in number to the redundancy bytes, are transferred to the external processor, who will process the information and actually perform the error correction.

In write mode, the WD60C80 reads just the data bytes, generates redundancies, and appends them to the end of the data byte flow. This formatting function is performed on the bus by arbitrating between the WD60C80 and the external buffer manager.

The WD60C80 relies on an external processor to setup the desired configuration or to recover from operational failure by reading or writing the internal taskfile registers, there is a seperate 8-bit port for that purpose. This port can be accessed at any time regardless of the activity of the data/redundancy generator.

In order to perform the above functions, the WD60C80 has three distinctive interfaces.

a) The processor interface (ALE, $\overline{CS}$, $\overline{WE}$, $\overline{RE}$ pins)
b) The controller interface (CDRQ, $\overline{CDACK}$ pins)
c) The syndrome transfer interface (SDRQ, SDACK pins).

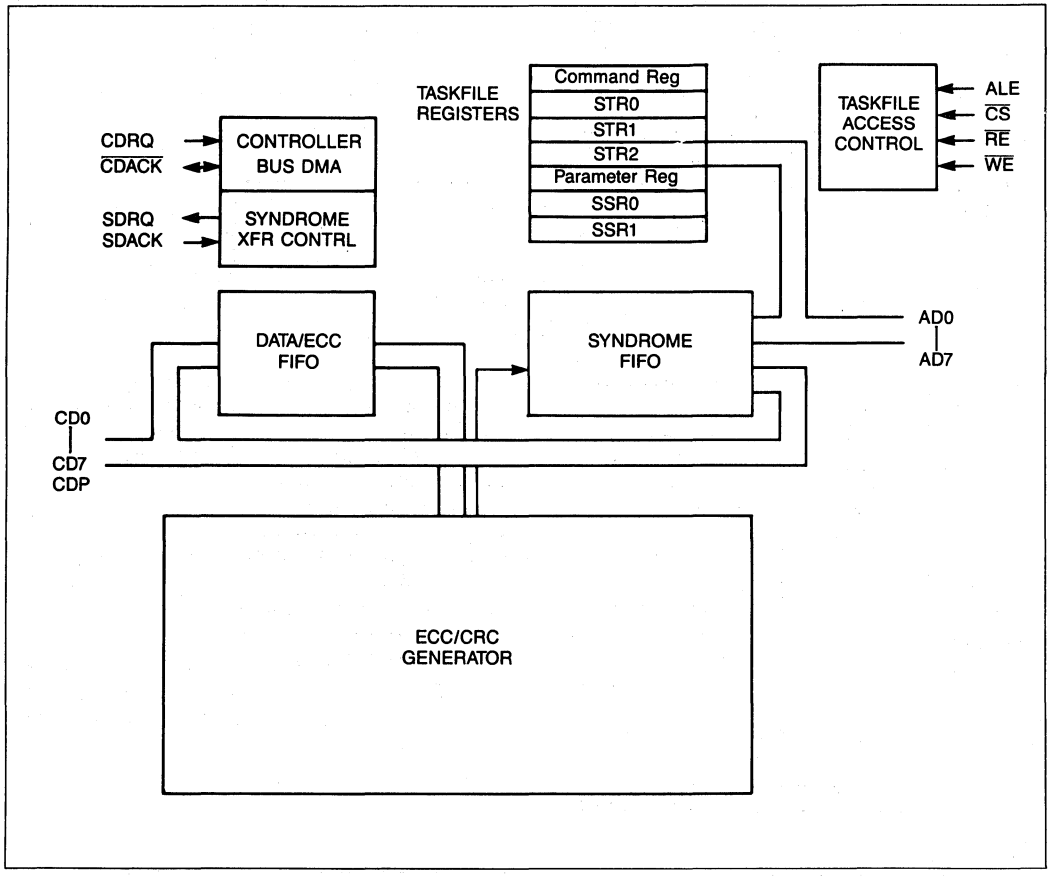
The controller bus and syndrome transfer interfaces are simple REQ-ACK protocol of a regular DMA controller. It has two physical ports or busses, eight bits wide each.

a) The processor bus (designated ADx in the pin description)
b) The controller bus (designated CDx in the pin description).

The controller interface works exclusively on the controller bus, (designated as CDx in the pin-out description) handling the target (e.g., disk controller) data reads and writes, while the processor interface works exclusively for the processor bus, and used to access the internal taskfile registers. The syndrome transfer interface works on either the processor bus or the controller bus, depending on the chosen option, to transfer syndrome/status bytes during the read operation.

The controller bus has an optional ninth bit, which is used as the parity bit for higher data integrity. The WD60C80 can generate and check for odd parity on each byte read/written. It is activated by properly setting the Parameter Register.

Because the device is packaged in a 28-pin PLCC, two pin functions are multiplexed on one physical pin and hence not available at the same time. If the parity generation/checking is to be supported on the controller bus, the DMA mode syndrome transfer must be given up, since SDACK (Syndrome DMA Acknowledge) and CDP (Controller Bus Parity bit) are assigned the same pin. This pin can be only programmed to function as one of the two. Some DMA devices (most ones with memory to memory transfer capability) and integrated processors (such as Intel™ i80188/86) have their DMA function implemented like a programmed I/O (i.e., generates Address and $\overline{RE}$ or $\overline{WE}$, rather than issuing a DMA $\overline{Acknowledge}$), which allows for syndrome DMA transfer and parity checking at the same time.



WD60C80 SIMPLIFIED BLOCK DIAGRAM

Data/ECC FIFO is bidirectional, allowing the data and ECC/CRC bytes to pass through in the appropriate directions. It is four-byte deep, and has special control logic that lets a data byte pass through right into the ECC and CRC generator if the FIFO is empty, in order to improve the overall throughput.

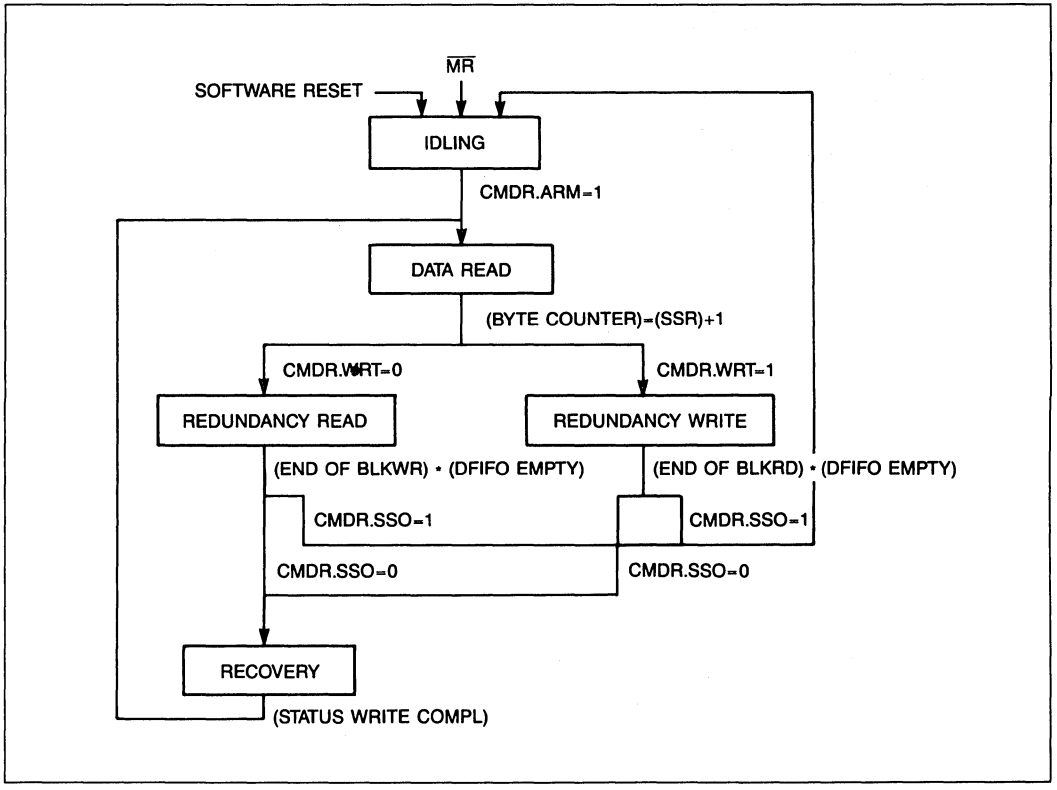
Syndrome FIFO is unidirectional (read-only) FIFO used to smooth the transfer of CRC residue, syndrome and status bytes. Its output can be directed to either the controller bus or the processor bus.

There are seven taskfile registers on the processor bus. They can be read/written at any time, independent of the controller bus activity, allowing the external processor to interact with the device without any special protocol.

Control Sequences

The WD60C80 has five independent states as listed below:

1) Idling	WD60C80 is completely dormant.
2) Data Read	WD60C80 reads data bytes from the CDbus.
3) Redundancy Write	WD60C80 writes ECC/CRC to the CDbus.
4) Redundancy Read	WD60C80 reads ECC/CRC from the CDbus.
5) Recovery	End of a block and reinitialize for the next.



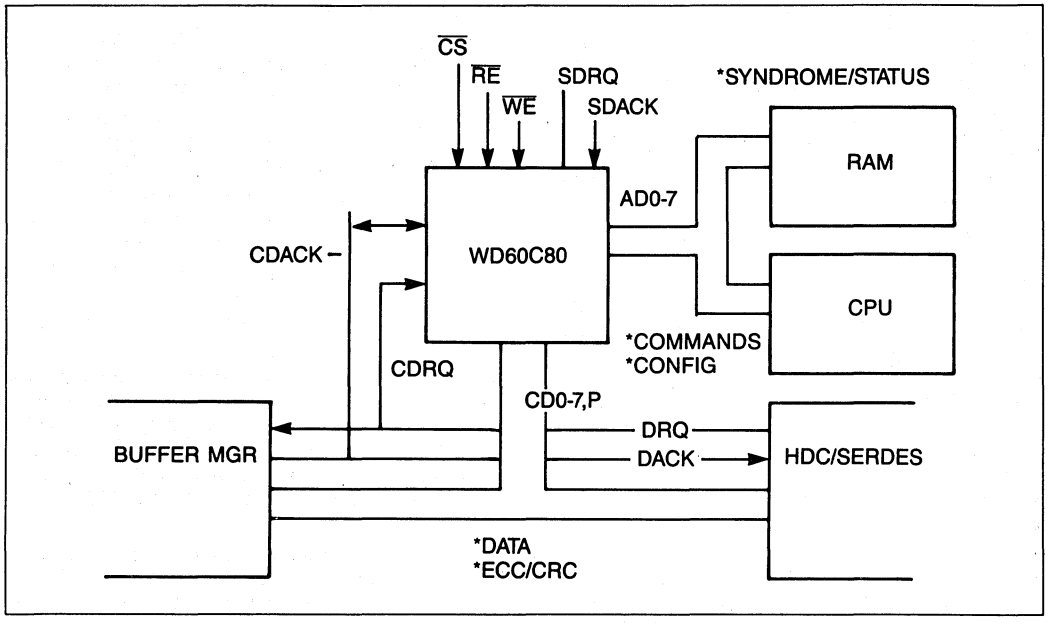
WD60C80 BASIC CONTROL FLOW DIAGRAM

(END OF BLKWR) = All ECC/CRC bytes written out to the data/ECC FIFO.
(END OF BLKRD) = All ECC/CRC bytes processed and the last syndrome byte is output to the syndrome FIFO.
(STATUS WRITE COMPL) = The final status bytes written to the syndrome FIFO.

The operational details and the hardware protocol on the bus transactions on each state are described in the following sections.

Basic Topology

The WD60C80 is designed to be placed between a buffer manager and a target peripheral device (e.g., disk serdes). It is assumed that the buffer manager and the target will transfer the data bytes using REQ-ACK protocol. The buffer manager is normally the DMA master, with the target peripheral being the permanent slave.



WD60C80 BASIC TOPOLOGY

The WD60C80 listens to the CD bus and (when ARMed), picks up a byte every time CDACK pulses, as a valid data byte. When all data bytes are read and processed, the WD60C80 becomes a temporary bus master (i.e., it performs the REQ-ACK protocol with the target peripheral device) and transfers the ECC and CRC bytes. Unless it is used with a buffer manager device such as the WD60C40 that has a special arbitration mode with WD60C80, some external support logic is required between the buffer manager DMA and the WD60C80 to give this device the control of the bus during Redundancy Read/Write phases.

During the Redundancy Read phase, the WD60C80 generates syndrome bytes equal in number with the ECC bytes. They are output through (by default,) the processor bus to the CPU memory. It performs the REQ-ACK protocol with the external DMA controller (in DMA mode) as a slave device. Optionally, the syndrome bytes can be output through the controller bus, though due to the external bus arbitration overhead, the throughput of the transfer will be much lower in this case.

Controller Bus Interface

The "Controller Bus" refers to the CD0 through CD7 pins plus the optional CDP pin which is multiplexed with SDACK function. They are used to connect the WD60C80 to the bus between the buffer manager device and the target peripheral controller device. Depending on the option chosen, it can also be a port to transfer the syndrome/status bytes during the READ operation. This bus behaves in three different manners depending on the state the device is in.

Data Read Phase

The data read phase (state) is entered when the ARM bit of the command register is set high. The WD60C80 CD bus behaves passively in this mode, with all the CDx pins and the CDACK pin being inputs. CDRQ pin is inactive in this phase. When the CDACK signal (issued by the buffer manager) becomes active (low), the WD60C80 grabs the data byte on the CD0 through CD7 pins and stores it into the internal FIFO. Care should be taken that it does not necessarily get the data byte at the trailing edge of the CDACK pulse, but can actually gets it anytime after four clock cycles after the leading edge of the pulse.

This is done to speed up the internal processing of the data, to shrink the blank time between the Data Read Phase and the Redundancy Write Phase. Also it should be noted that the $\overline{CDACK}$ pulse needs to be wider than 2.0 clock cycles to insure a proper read.

The average transfer cycle on the controller bus during this phase should not exceed one eighth of the WD60C80 clock frequency, which is the rate at which the device processes a byte. But in order to be more flexible, the transfer cycles can proceed at the maximum rate of one fifth the clock frequency (e.g., at 25.0 MHz clocking, up to 5 Mbyte/sec) for a short span, up to about 10 bytes in length. A longer burst than that can result in a data FIFO overflow.

If the average data rate is slower than one eighth the clock frequency, then the WD60C80 will slow down automatically and synchronize itself to the bus transaction. Therefore, there is no need to tweak the clock frequency of the device to match any special data rate, as long as the frequency is high enough.

Redundancy Write Phase

The WD60C80 enters the Redundancy Write Phase (State) if the WRITE operation is chosen in the command register, and the prescribed number of bytes (in the sector size register) are read from the controller bus and finished processing inside the ECC generator.

In this phase, the WD60C80 performs REQ-ACK protocol with the target peripheral device, outputting the generated ECC and CRC bytes to the controller bus. The $\overline{CDACK}$ pin as well as all the CDx pins become outputs, and CDRQ input gets activated, the WD60C80 becoming the temporary bus master. Unless it is used with a buffer manager like the WD60C40 which knows when to release the bus, some external support logic is necessary between the buffer manager and the WD60C80, isolating the buffer manager from the DMA protocol to transfer the ECC/CRC bytes. In particular, the DACK output of the buffer DMA device must be tri-stated.

Notice when the WD60C80 shifts from the Data Read Phase to the Redundancy Write Phase, there is more than a "Byte Time (eight clock cycles)" before the first ECC/CRC byte can be output after the last data byte is loaded. The worst case latency of 12 clock cycles if the data FIFO is empty prior to receiving the last data byte; the best case is ten clock cycles.

Some target devices such as a disk serdes cannot tolerate the data transfer latency longer than one byte time, so some extra support logic between the WD60C80 and the target controller device is necessary to support those devices. A few examples for this logic are:

1) Place a data holding register or FIFO in front of the target device so that the controller won't run out of data before the WD60C80 can output the first ECC/CRC bytes. This register should be bidirectional, for dealing with the Read operation.
2) Set the WD60C80's clock frequency high enough so that the worst case switch-over time is narrower than the "one byte time" of the target controller device. This method is applicable if the required data rate is significantly less than the specified maximum clock frequency of the WD60C80.

After the WD60C80 takes over the bus, it transfers the ECC/CRC bytes pretty much at the target data rate (eight clock cycles/byte, if FCLK frequency is matched to the target data rate). If it is requested and there are a few bytes accumulated in the data FIFO, then it can transfer as fast as six clock cycles/byte.

Notice it does not cause a FIFO overflow, if the CDRQ pin is held inactive (low) for an extended period of time. The WD60C80 will stop generating redundancies when the FIFO is full.

When all the ECC bytes are generated and the data FIFO becomes empty (i.e., all of them are transferred to the target device), then the WD60C80 changes its state to the Recovery Phase. The $\overline{CDACK}$ pin becomes an input again, and the final status information is output to the Syndrome FIFO, where the processor can read it.

The WD60C80 changes its state to either the Data Read Phase for the next block if the Multiple Sector Operation is selected, or to the Idling Phase if the Single Sector Operation is selected.

Redundancy Read Phase

The WD60C80 enters Redundancy Read Phase (State) if READ operation is chosen in the command register and the last data byte is input through the controller bus, then processed internally.

Similar to the Redundancy Write Phase, it performs REQ-ACK protocol with the target controller device as a temporary bus master, but to read CRC/ECC the part of the block. Same restrictions and support logic requirements apply as the Redundancy Write case. Notice at the end of the block, it takes longer to get ready for the next block in the READ operation than the WRITE operation, because the data/ECC FIFO may become full when the last ECC byte is read from the controller bus, due to the read-ahead feature on this device. If the transfer is taking place at the WD60C80 data rate or less, and therefore not utilizing the read-ahead feature, then it should take just as long as the WRITE mode operation to get back to the Data Read Phase of the next block (Multiple Sector Operation).

If extra CDRQs are generated by the target controller at the end of the block, the WD60C80 will generate spurious $\overline{CDACK}$ pulse and loads whatever is on

the CD bus at the time. Since the internal state machine knows how many ECC bytes it should process, it will not fetch these spurious bytes from the FIFO. This prevents the FIFO from becoming empty, and consequently, prevents the WD60C80 from going into Recovery Phase. This can cause a system hang-up, so care should be taken.

When the Syndrome-on-the-Controller-Bus option is selected, the syndrome output also takes place on this bus, physically. The transfer is controlled by the SDRQ pin (output) and SDACK pin (input), and the bus arbitration between the two channels of the DMA is expected to be done external to this device. When two transfers collide on the bus, neither transfer takes place and consequently, both transfers are broken. This is an option meant for a low cost application where data buffer and the syndrome information share the same physical RAM, and it is not expected to be used for high throughput applications, where a large overhead associated with the DMA arbitration cannot be tolerated.

Processor Bus Interface

The processor bus refers to the AD0 through AD7 pins controlled by ALE, $\overline{CS}$, $\overline{RE}$ and $\overline{WE}$ pins. Depending on the options, the SDRQ and SDACK pins also control this bus. This bus is used primarily by the external processor to setup the operation modes/configurations of the WD60C80 as well as reading the operational/error status of the device. It is also used as the port to transfer syndrome/status bytes during the READ operation, by default.

Internal Register Interface

The internal taskfile read/write interface is native to the Intel 8085, 80186, 80188 and 8051 series of processors. Other processors with multiplexed address/data bus can be readily supported, but some external logic is needed to support processors with non-multiplexed bus.

In order to ease the interfacing to the 16-bit processors, some of which insist on even or odd boundaries for byte accesses, all internal registers of the WD60C80 are mirrored on even and odd addresses.

The processor can read any register at any time, without disturbing the internal operation. Before writing to any of these registers, however, it is suggested to soft reset the device (set the RST bit on the command register). If any options or configurations are changed while the device is active, it can disrupt the current operation, and in the worst case, it can hang up (The soft reset is effective even in the case of hang up). Consequently, it is suggested that all setups are made before the command register is written with the ARM bit set active.

When the Syndrome FIFO is read by the processor, care should be taken that the $\overline{CS}$ $\overline{RE}$ signal is wider than 2.0 clock cycles of the WD60C80, or it can upset the internal FIFO pointers. This situation is usually detected by the Syndrome/Status stream that is longer than expected. Because the pointer information cannot be accessed from the outside of the device, it is not possible to detect when the error happened, leading to a possible miscorrection.

Syndrome/Status Transfer

When the WD60C80 is operating in the READ mode, it generates syndrome bytes as it reads ECC bytes from the target controller device through the controller bus. They can be read using either PIO (programmed I/O) mode access, where the access is made just like another register read, or DMA mode, where the SDRQ pin and the SDACK pin are used to perform REQ-ACK protocol.

Code Description and Performance

The WD60C80 implements Reed Solomon error correcting code of degree 16, distance 17, long distance code. There are 16 redundancy (ECC) bytes generated per interleave, and it is capable of correcting up to eight symbol (byte) errors per interleave in any combinations of random and burst errors. This polynomial is compatible with the ANSI X3B11 error detection and correction encoding standard for 5¼ inch optical storage devices.

The 32-bit CRC code covered by the same format standard is also supported. The same CRC polynomial is used regardless of the selection of the ECC polynomials.

In addition, to support high density magnetic storage devices which do not require such a wide correction span, degree four and eight polynomials are provided for smaller ECC overhead (four and eight bytes per interleave, respectively), narrower correction span (two and four bytes per interleave, respectively), and shorter correction time (software dependent).

The device supports seven different interleave factors to optimize between the ECC overhead and correctable burst error length, once a proper polynomial is chosen. It supports one (no interleave), two, three, four, five, eight and 10-way interleaving. Because the coefficients of the generator polynomial is chosen from the GF(256), there can be only 255 symbols or bytes, per interleave including the ECC bytes. For that reason, the data field length of a block cannot exceed 255 times the interleave factor, less ECC/CRC overhead.

(The Maximum Data Field Length)
= 255 X (Interleave Factor) –
(ECC Overhead)–(CRC Overhead)

Number of ECC/Syndrome Bytes generated
(ECC Overhead)

Polynomial	Interleave Factors 1	2	3	4	5	8	10
Degree 16	16	32	48	64	80	128	160
Degree 8	8	16	24	32	40	64	80
Degree 4	4	8	12	16	20	32	40 (Bytes)

CRC Overhead = 0 if CRC is disabled.
= 4 if CRC is enabled.

Example:
For Degree 16, 10 interleave, no CRC,
(The Maximum Data Field Length)
= 255 X 10–160–0
= 2,390 Bytes

When used on 512-data-byte physical block, degree 16 polynomial, with five-way interleave with the CRC enabled, there are 103 data bytes in the first two interleaves and 102 bytes in the last three interleaves. The interleaves 0, 2, 3 and 4 include a byte each of CRC, which are also protected by the ECC, then each interleave has 16 bytes of redundancy (ECC).

EXAMPLE BLOCK FORMAT
(Degree 16, five interleaves, with CRC)

INTERLEAVE

0	1	2	3	4	
D0	D1	D2	D3	D4	→ ROW 0 PARITY
D5	D6	D7	D8	D9	→ ROW 1 PARITY
D10	D11	D12	D13	D14	→ ROW 2 PARITY
D15	D16	D17			→ ROW 3 PARITY
		D507	D508	D509	→ ROW 101 PARITY
D510	D511	CRC0	CRC1	CRC2	→ ROW 102 PARITY (UP TO D511)
CRC3	R0	R1	R2	R3	
R4	R5	R6	R7	R8	USED TO COMPUTE CRC0-CRC3
R9					
					LEGENDS:
		R71	R72	R73	D0-D511: 512 BYTES DATA
					CRC0-CRC3: 4 BYTES CRC
R74	R75	R76	R77	R78	CR0-R79: 80 BYTES ECC
R79					

They are output to the target peripheral controller in the order of D0 through D511, CRC0 through CRC3, R0 through R79.

29

Supported Polynomials

This section contains the definition of the polynomials supported by the WD60C80. Knowledge of the Reed-Solomon Code is assumed.

Finite Field Definition

This definition is common to all the polynomials including CRC.

Let β^i represent elements of a finite field generated by the polynomial over GF(2):

$p(x) = X^8 + X^5 + X^3 + X^2 + 1$

The elements of the finite field employed by the code are:

$\alpha^i = (\beta^i)^{88}$

ECC Generator polynomial for degree 16

Degree 16, distance 17, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=120}^{135} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 92 160 86 11 68 2 1 167 1 2 68 11 86 160 92 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Sixteen bytes per interleave.

Guaranteed Correction Span: Eight random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 8

Degree eight, distance nine, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=124}^{131} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 114 71 86 130 86 71 114 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Eight bytes per interleave.

Guaranteed Correction Span: Four random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

ECC Generator polynomial for degree 4

Degree four, distance five, self-reciprocal, with coefficients from GF(256)

$$g(x) = \prod_{i=126}^{129} (x + \alpha^i)$$

ECC Generator polynomial coefficients in decimal are:
1 64 61 64 1

Code Type: Long distance, interleaved, Reed-Solomon code operating on one byte symbols.

Redundancy: Four bytes per interleave.

Guaranteed Correction Span: Two random symbol (byte) errors per interleave.

Special Considerations:
1) Redundancy bytes are inverted before writing.
2) The shift register implementing the code is initialized to zero.

CRC Generator polynomial

The data field CRC code is specially constructed so that its residue can be adjusted as correction occurs. When correction is complete, the residue shall have been adjusted to zero.

Degree four, distance five, coefficients from GF(256)

$$g(x) = \prod_{i=136}^{139} (x + \alpha^i)$$

CRC Generator polynomial coefficients in decimal are:
1 232 194 35 198

Code Type: Reed-Solomon CRC operating on bytes.

Redundancy: Four bytes per sector, regardless of the number of interleave.

Statistical Detection Capability: The data field CRC code fails to detect an uncorrectable sector with probability of 2.3E-10 undetected uncorrectable sectors per uncorrectable sector.

Special Considerations:
1) The CRC code is applied to the XOR sum of data bytes across the interleaves.
2) Redundancy bytes are not inverted before writing.
3) The shift register implementing the code is initialized to zero.

Probability of uncorrectable error

Uncorrectable error rate is defined as the ratio of uncorrectable events to total bits transferred, and expressed in the formula below:

(Uncorrectable Error Rate)

$$= \frac{\text{Block Errors}}{\text{Bit}} = \frac{1}{kn} \sum_{i>e}^{n} \binom{n}{i} p^i (1-p)^{n-i}$$

where $\binom{n}{r} = \frac{n!}{r!\,(n-r)!}$

- n = Interleave length in symbols
- e = Maximum number of symbol errors correctable per interleave
- k = Symbol width in bits (8 bits for WD60C80)
- p = Raw symbol error probability (symbol errors/symbol)

(This formula is quoted from "Product Description for the NG8510", Data Systems Technology.)

It is assumed that error bursts occur at random intervals and each burst is assumed to affect a single symbol (one byte). If error bursts cluster or if error bursts span more than one symbol, the actual uncorrectable error rate will be greater. If each burst

is assumed to affect two symbols, the uncorrectable error rate becomes twice, and so on. A more complex computation is required when each burst is assumed to affect more than the number of interleaves employed.

Miscorrection Probability

Miscorrection probability of the code is 1.6E-6. Only those error events where the number of symbols in error in a single interleave exceeds eight are subject to miscorrection. The probability of transferring undetected erroneous data is the product of the probability of having more than eight errors in an interleave and the miscorrection probability of the code. For the degree 16 code, this probability is 7.7E-23 for a raw burst error rate of 1.0E-4.

Correction Software Support

The WD60C80 requires a companion software algorithm. This algorithm normally resides in the ROM of the external processor. Western Digital licenses the software implementing the required algorithm.

Internal Register Description

The WD60C40 has seven internal taskfile registers to set its operation modes, select programmable options and configurations, and report operational status. They are all accessed through the processor port using standard CPU interface with multiplexed address/data bus.

Register Map

The internal taskfile registers are mapped by the lower 4-bits of multiplexed address lines. For ease of interfacing to 16-bit processors, some of which require byte accesses to be on even or odd address boundaries, all registers are mirrored on even and odd addresses.

The address bits are latched by the internal address register which retains its contents until the next access, upon the ALE pulse input. Hence if a processor does not have a multiplexed bus, it can load the register address first by pulsing the ALE pin, then perform a read or a write in the next instruction.

A3,A2,1,0	HEX	SYMBOL	NAME	R/W,R/O	WIDTH
000X	0,1	CMDR	Command Register	R/W	8 bits
001X	2,3	STR0	Status Register 0	R/O	8 bits
010X	4,5	STR1	Status Register 1		8 bits
011X	6,7	STR2	Status Register 2		8 bits
100X	8,9	PRMR	Parameter Register	R/W	8 bits
101X	A,B	SSR1	Sector Size Register	R/W	4 bits
110X	C,D	SSR0	Sector Size Register		8 bits
111X	E,F		Syndrome FIFO	R/O	8 bits

Command Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CMDR	FT	SCB	CRC	SSO	WRT	ARM	RSV	RST

The Command Register is a Read/Write register that is used to set the WD60C80's operating mode. Since this register is used to activate/deactivate the device, writing to this register should be the last in the set up procedure.

Bit 0 RST–Software Reset/Abort Current Operation
Setting this bit high forces the internal reset logic to be activated, and the WD60C80 will halt current operation and clear itself to the default state. The following items are cleared:

- Command Register except RST bit.
- Parameter Register.
- Sector Size Registers.
- Status Registers.
- All internal state machines.
- Both (Data, Syndrome) internal FIFOs.

This bit does not clear by itself, so it needs to be set and then reset later by the external processor. It needs to be left set longer than four cycles of the input clock.

Bit 1 RSV – Reserved
This bit is reserved for a future enhancement.

Bit 2 ARM – Activate WD60C80 Function
This bit, when set high, activates the internal state machine of the WD60C80 to begin its operation by listening to the CD-bus activity. When low, the device is completely dormant. The taskfile should be initialized and set up prior to setting this bit.

Bit 3 WRT – Write Operation
When set high, the WD60C80 performs a write operation i.e., reads a block of data and outputs specified CRC/ECC. If it is low (default after reset), it performs a read operation (i.e., reads a block of data), CRC and ECC and generates a block of syndrome bytes, to be read by the external processor.

Bit 4 SSO – Single Sector Operation
When set high, the WD60C80 will operate on one block of data before clearing the ARM bit and disabling itself. The external processor has to activate the device before it can process another block. All other register content will be preserved.
When low (default after reset), it stays active and processes consecutive blocks of data until the ARM bit is externally cleared to a low.

Bit 5 CRC – CRC Encoding Enable
When set high, the WD60C80 activates its internal 32-bit CRC generator on read and write operations for extended correction and lower miscorrection probability. It adds four extra bytes to each block, between the data field and the redundancy field.

When low (default after reset), it disables the CRC generator.

Bit 6 SCB – Syndrome Transfer on Controller Bus
When set high, the WD60C80 directs the syndrome byte output to the controller bus (CDx pins) during the read operation thus enabling the user to share a single RAM for storing read/write data and syndrome information. Notice the option is valid only if the DMA transfer option is selected on the Parameter Register.

The parity check/generation option therefore is not available. When this mode of operation is chosen, it is the system designer's responsibility to arbitrate the controller bus between the data/ECC transfer and syndrome transfer. Due to this overhead, the actual throughput of the bus tends to be low, and the application should be limited to a low transfer rate environment.

When it is low (default after reset), the device directs the syndrome bytes through the processor bus, and the external processor or DMA device can perform the transfer with either PIO or DMA option

Bit 7 FT – FIFO Threshold ON

When set high, the WD60C80 delays setting the SDRQ pin until at least 10 bytes are accumulated inside the syndrome FIFO. This guarantees the burst DMA transfer of at least 10 bytes, reducing bus arbitration overhead between the processor and the DMA device, when the bus bandwidth requirement is high.

When set low (default after reset), the device sets SDRQ every time there is a byte in the syndrome FIFO. In either case, the SDRQ will clear itself when the last byte in the FIFO is being read.

Parameter Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PRMR	PCD	SDH	DMA	PS1	PS0	IS2	IS1	IS0

The Parameter Register is a Read/Write register that is used to set the operating configuration of WD60C80.

Bit 0-2 IS0-2 – Interleave Factor Selection Code
These three bits are used to specify the interleave factor of the ECC. For more details on interleaving.

IS2	IS1	IS0	Interleave Factor
0	0	0	5 (Default after reset)
0	0	1	10
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	8
1	1	X	1 (i.e., no interleaving)
(X = Don't Care)			

Bit 3-4 PS0-1 – Polynomial Selection Code
These two bits are used to specify the ECC polynomials to be used for the WD60C80 operation.

PS1	PS0	Polynomial
0	0	Degree 16 (Default after reset)
0	1	Degree 8
1	X	Degree 4
(X = Don't Care)		

Bit 5 DMA – Syndrome DMA Transfer Option
(Parity Check/Generation Disable) If this bit is set high, it enables the DMA mode operation on the syndrome transfer during the read, and disables the parity checker/generator. The DMA mode and parity checking are mutually exclusive options, because they share the same pin (CDP/SDACK) for their function. For DMA mode operation, this pin functions as SDACK, along with SDRQ, to perform Request-Acknowledge protocol.

The syndrome bytes will be output through the processor or the controller bus depending on the selection made in the Command Register. Notice this is the only way to direct the syndrome to the controller bus.

If this bit is set low (default after reset), then the syndrome transfer is performed in PIO (Programmed I/O) mode, where the external processor/DMA device accesses the syndrome FIFO as an internal register through the processor bus. An ALE pulse must be used to latch the address of the syndrome FIFO (0E Hex), then the device activates $\overline{CS}$ and $\overline{RE}$ to read it. Notice that to properly shift the internal FIFO pointer, $\overline{CS}$ $\overline{RE}$ pulse width must be wider than two FCLK cycles. In this mode, the CDP/SDACK pin becomes

the parity bit for the controller bus (CDx pins). When a byte is output from this bus, an odd parity (the total number of "high" bits in the nine bit field is odd) is output on this pin. If parity check is also enabled (see PCD bit), the WD60C80 will inspect the incoming data for odd parity (odd number of "high" bits at the CD0-CD7 and CDP pins) at the trailing edge of $\overline{\text{CDACK}}$ signal (input).

Using the PIO access method, the external processor can read the syndrome FIFO regardless of DMA bit setting. However, it can upset the byte count of the a DMA device if the processor tries to read the FIFO concurrently.

Bit 6 SDH – SDACK Pin Polarity Option (High Active)

This bit is used to control the polarity of SDACK pin, when DMA option is selected. When set high, the SDACK becomes a high active signal.

If set low, it becomes a low active signal, much like the $\overline{\text{CDACK}}$ pin. It defaults to active low after reset.

Bit 7 PCD – Parity Check Disable Option

This bit disables the parity checker, while leaving the parity generator ON. In order for this bit to be effective, the DMA bit must be set low, or both parity checker and generator is disabled.

After reset, this bit is set low, enabling the parity checker.

Sector Size Register

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
SSRO	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0
SSR1					SS11	SS10	SS9	SS8

(INTERLEAVE FACTOR + 1) ≤ (SSR) ≤ (INTERLEAVE FACTOR X 255) – 1

The Sector Size Register is a Read/Write register that is used to set the length of the data field of a block. The register is 12-bit long, divided into the least significant 8-bit and the most significant 4-bit registers. The external processor is expected to set these registers to (number of data bytes - 1) prior to ARMing the device.

The contents of these registers are not decremented on each byte transferred, but rather, used to compare with the output of the internal data byte counter. Therefore, once they are loaded, the value stays intact until another value is loaded. This makes it convenient for multiple sector operation.

Example:

In order to set for the data field length of 1,024 bytes,
(Sector Size Register) = 1,024 - 1 = 1,023 = 3FF Hex
Store FF Hex to SSR0
Store 03 Hex to SSR1

Although it is a 12-bit register, the maximum data field length is limited to 255 times the specified interleave factor. This limitation is imposed by the finite field theory, which limits the length of any interleave to be less than or equal to 255 bytes due to the usage of coefficients from GF(256). The WD60C80 hardware requires at least one byte of data in each interleave to insure proper operation, therefore the minimum data field length is one plus the interleave factor. Violation of this rule may lead to all-zero CRC and all-FF(Hex) ECC bytes.

Example:

If degree 16, 10 interleave is selected,
11 ≤ (SECTOR SIZE REGISTER) ≤ 2,389.
The total sector length (less ID field) is:
(SECTOR SIZE REGISTER) + 1 + 4 (CRC BYTES) + 160 (ECC BYTES)

(SECTOR SIZE REG) + 1	4	160 Bytes
DATA FIELD	CRC	ECC

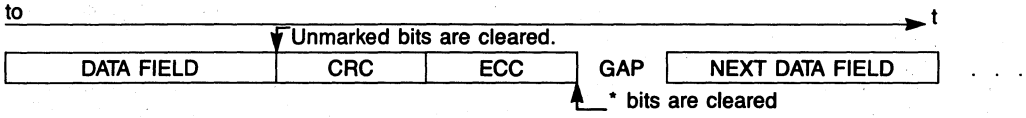
Status Registers

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
STRO	N/U	N/U	PERR*	DFO*	SFO	EERR	SDRQ!	BUSY!
STR1	I7E	I6E	I5E	I4E	I3E	I2E	I1E	I0E
STR2	N/U	CERR	PERR*	DFO*	SFO	EERR	I9E	I8E

N/U = Not Used

All bits are cleared at the end of the data field except:
* marked bits clear at the end of the current block.
! marked bits are real time signals and not latched.

29



The Status Registers are Read-Only registers that report operational status and error conditions of WD60C80. The values of STR1 and STR2 at the end of each block are also sent to the syndrome FIFO to be read by the host processor during read or write operations to check for any failures. STR0 is intended for general checking of the operational status of the device, so a few bits of information are covered in both STR0 and STR2.

Byte 0 Bit 0 BUSY – Device Busy
This is a real time signal indicating the active status of the WD60C80. When ARM = 1 is written to the command register, this bit is set high, indicating the active status. When a single sector operation is specified, this bit is cleared at the end of each block. Otherwise it stays ON until the ARM bit is externally cleared or reset/abort is activated.

Byte 0 Bit 1 SDRQ – Syndrome Transfer DMA Request

This is a real time signal indicating the syndrome FIFO has syndrome/status bytes inside and ready for transfer. This is similar to the SDRQ pin, except it ignores the FIFO threshold option. It is intended to be used with the PIO mode of syndrome transfer operation.

Byte 0 Bit 2 EERR – ECC Error Found
Byte 2 Bit 2
This is a latched status indicating that during the read operation, the device found a discrepancy(ies) between the internally generated ECC and retrieved ECC.

When this bit is set high, one or more of the "Interleave n in error" bits should also be set high. If there is an error(s), this bit is set during the ECC field of the block in question, and stays valid until the end of the data field of the next block.

Byte 0 Bit 3 SFO – Syndrome FIFO Overflow
Byte 2 Bit 3
This is a latched status indicating that during the read operation, the syndrome FIFO suffered an overflow due to insufficient access by the processor or DMA device. A syndrome byte is generated every time a redundancy byte is received and processed, and the system is expected to read them out at least at the data rate. The syndrome FIFO is 20-byte deep to smooth out the traffic on the bus, but most operations generate more than 20 bytes of syndrome/status. When an overflow occurs, the syndrome transfer logic still delivers the correct number of bytes, but there will be several garbage bytes among those transferred. This bit stays valid until the end of the data field of the next block.

Byte 0 Bit 4 DFO – Data FIFO Overflow
Byte 2 Bit 4
This is a latched status indicating that during the read or write operation, the data FIFO suffered an overflow, due to excessive transfer on the controller bus, or the FCLK frequency is too low. The device is expected to be clocked at least eight times the required data rate in byte/sec, and it is capable of supporting a 10-byte burst of 1/5 the clock frequency. Since the WD60C80 does not have any means of handshaking during the data read phase, any transfer rate adjustment must be made between the buffer manager and the target device, such as a disk controller, on the controller bus. When the overflow occurs, the device typically appears to be operating properly, except it has this error flag set and most likely generates wrong CRC and ECC codes. This bit stays valid till the end of the current block.

Byte 0 Bit 5 PERR – Parity Error Detected on Controller Bus

Byte 2 Bit 5
This is a latched status indicating parity error detection on the controller bus during the read or write operation. During the data read phase (if PIO option is selected and Parity Check is enabled), the WD60C80 checks for odd parity on the controller bus at the trailing edge of the $\overline{\text{CDACK}}$ signal (input). An odd parity is when you an have odd number of "high" bits in the nine-bits field (CD0-CD7, CDP). If any error is detected, this flag is set and stays valid until the end of the current block. This error flag, however, does not disturb other operations of the device, so its operation will complete as normal. It is the responsibility of the system firmware to analyze and recover from the error.

Byte 1 Bit 0 I0E – Interleave 0 in Error
This is a latched status indicating an ECC error(s) is detected in the first interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 1 I1E – Interleave 1 in Error
This is a latched status indicating an ECC error(s) is detected in the second interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 2 I2E – Interleave 2 in Error
This is a latched status indicating an ECC error(s) is detected in the third interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 3 I3E – Interleave 3 in Error
This is a latched status indicating an ECC error(s) is detected in the fourth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 4 I4E – Interleave 4 in Error
This is a latched status indicating an ECC error(s) is detected in the fifth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 5 I5E – Interleave 5 in Error
This is a latched status indicating an ECC error(s) is detected in the sixth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 6 I6E – Interleave 6 in Error
This is a latched status indicating an ECC error(s) is detected in the seventh interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 1 Bit 7 I7E – Interleave 7 in Error
This is a latched status indicating an ECC error(s) is detected in the eighth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 0 I8E – Interleave 8 in Error
This is a latched status indicating an ECC error(s) is detected in the ninth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

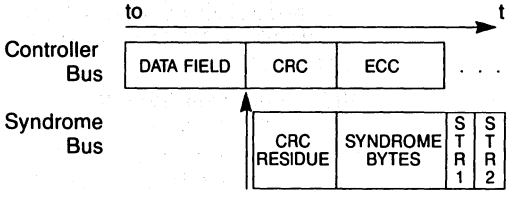
Byte 2 Bit 1 I9E – Interleave 9 in Error
This is a latched status indicating an ECC error(s) is detected in the tenth interleave, during the read operation. The processor should be able to find non-zero syndrome bytes belonging to this interleave. The bit is set during the ECC field and stays valid until the end of the data field of the next block.

Byte 2 Bit 6 CERR – CRC Error Detected
This is a latched status indicating a CRC error is detected during the read operation. The processor should be able to find non-zero CRC residue. This bit is set during the CRC field and stays valid until the end of the data field of the next block.

Syndrome FIFO

Syndrome FIFO is a Read-Only 20-byte deep FIFO register used to transfer syndrome / status bytes during the read operation. It can be accessed either in DMA or in PIO mode, by setting up the Parameter Register properly. Even if it is set up for DMA mode transfer, the processor can still read it through PIO mode access, but the reverse is not true. Its status is indicated by the SDRQ pin and the SDRQ bit in the status register byte 0.

Timing Relationship between the Data flow and Syndrome Transfer



Syndrome FIFO cleared

During the read operation, the host must read through this FIFO, four bytes of CRC residue (if CRC option is set), syndrome bytes (number of bytes varies depending on the ECC polynomial and the interleave factor) and two bytes of final status (copies of status register byte 1 and 2, at the end of the block), in that order. During the CRC and ECC field, one byte is generated every eight FCLK cycles, and accumulated in this FIFO. It is the host's responsibility to read them out before the FIFO overflow occurs, or he can lose several syndrome bytes.

Number of Syndrome Bytes generated

	Interleave Factors							
Polynomial	**1**	**2**	**3**	**4**	**5**	**8**	**10**	
Degree 16	16	32	48	64	80	128	160	
Degree 8	8	16	24	32	40	64	80	
Degree 4	4	8	12	16	20	32	40	(Bytes)

(Total # of bytes to be transferred)
= CRC Residue (4) + Syndrome Bytes + Status Bytes (2)

During the write operation, no syndrome bytes are generated, but two bytes of final status are reported through this FIFO at the end of each block.

Regardless of FIFO threshold option, SDRQ will be set high (true) at the end of the block.

29

The syndrome FIFO is cleared of its contents at the end of the data field of every block. So the external host has until the end of the next data field to finish reading the syndrome bytes, as long as there is no FIFO overflow.

The host can read them out as fast as one fifth of the clock frequency, but care must be taken to insure the $\overline{CS}$ $\overline{RE}$ pulse width (PIO mode) or SDACK width (DMA mode) to be more than 2.0 clock cycles. The supported DMA protocol is the slave side of demand driven burst transfer (i.e., SDRQ stays high (true) as long as there is a byte in the FIFO), and the external master DMA device can read them out in a burst, until SDRQ clears.

If, for any reason, the DMA device tries to read the syndrome FIFO when SDRQ is not set, not only it is likely to get a garbage byte, but that may also also upset the internal FIFO pointer, thereby making the next-to-be-read syndrome byte inaccessible. This situation is not reported in the status register, so one must be careful to insure sufficient setup and hold time for the DMA protocol.

DC ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings indicate where permanent damage to the device may occur if exceeded. Continuous operation at these limits is not intended and should be avoided.

Operating Temperature ..... 0°C (32°F) to 70°F (158°F)
Storage Temperature ..... −55°C (−67°F) to +125°C (257°F)
Minimum Voltage on any pin with respect to V_{SS} ..... −0.3V
Maximum Voltage on any pin with respect to V_{DD} ..... +0.3V
V_{DD} with respect to V_{SS} ..... +7.0V

DC OPERATING CHARACTERISTICS

The following characteristics apply to the WD60C80 device in the given conditions, in the ambient temperature between 0°C and 70°C.

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
V_{DD}	Power Supply Voltage	4.50	5.00	5.50	V	[1]
I_{DD}	Power Supply Current			25.0	mA	[1]

[1] Ta = 0°C, FCLK frequency = 25.0 MHz, all outputs open.

FOR ALL INPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{IL}	Input Leakage Current			10.0	μA	[2]
V_{IL}	Input Low Level Voltage			0.8	V	
V_{IH}	Input High Level Voltage	2.0			V	

[2] Input Voltage = V_{DD}

FOR ALL OUTPUTS:

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{OZ}	Output Leakage Current			10.0	μA	[3]
V_{OH}	Output High Level Voltage	2.8 2.8			V V	[4] [6]
V_{OL}	Output Low Level Voltage			0.4 0.4	V V	[5] [7]

[3] Output Voltage = V_{DD}
[4] Applies to AD0 through AD7 pins only. Io = −2.5 mA
[5] Applies to AD0 through AD7 pins only. Is = +6.0 mA
[6] Applies to all other output/bidirectional pins. Io = −1.0 mA
[7] Applies to all other output/bidirectional pins. Is = +2.0 mA

DC OPERATING CHARACTERISTICS (continued)

SYMBOL	CHARACTERISTIC	MIN	NOM	MAX	UNIT	COND.
I_{LU}	Latch Up Current	±40			mA	

AC TIMING CHARACTERISTICS

REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING

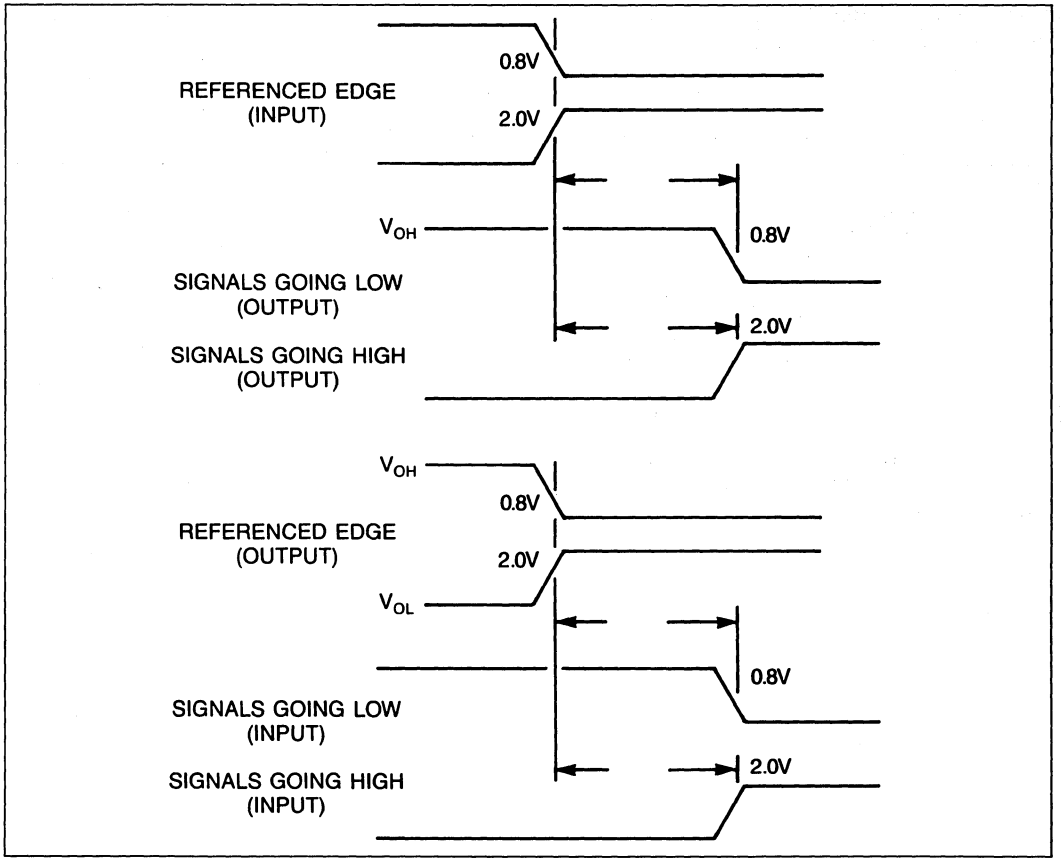
* Reference Number on the Timing Waveform Diagram.

* Abbreviated Symbol the Timing is Referred.

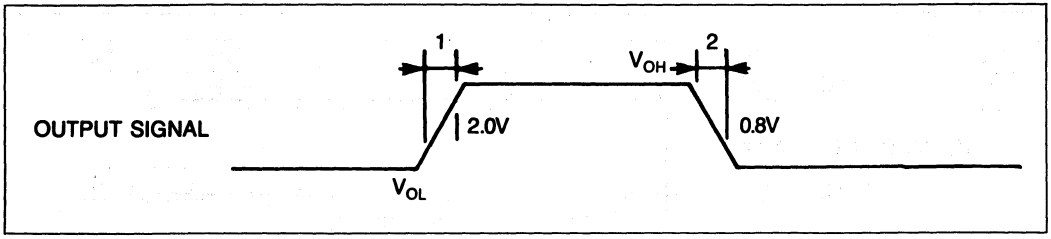
* The Reference Edge to which the Timing is Specified.
  L.E. = Leading Edge
  T.E. = Trailing Edge
  I.C. = Initial Condition

* Classification of Requirement/Specification
  R = Requirement on the External Interface
  S = WD60C80 Output Timing Specification

All the timing specifications assume the voltage levels shown below.
Capacitive loading on AD0-AD7 pins are 100 pF, and all other outputs are 50 pF.

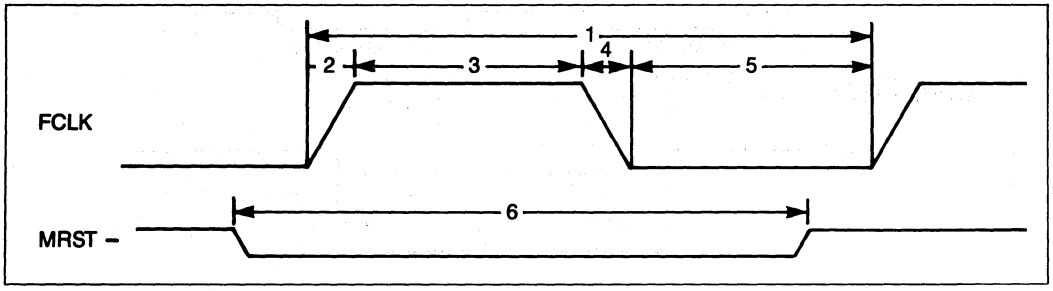


29



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	TR	Output Rise Time	From V_{OL} to 2.0V	S	25 nsec Max
2	TF	Output Fall Time	From V_{OH} to 0.8V	S	25 nsec Max

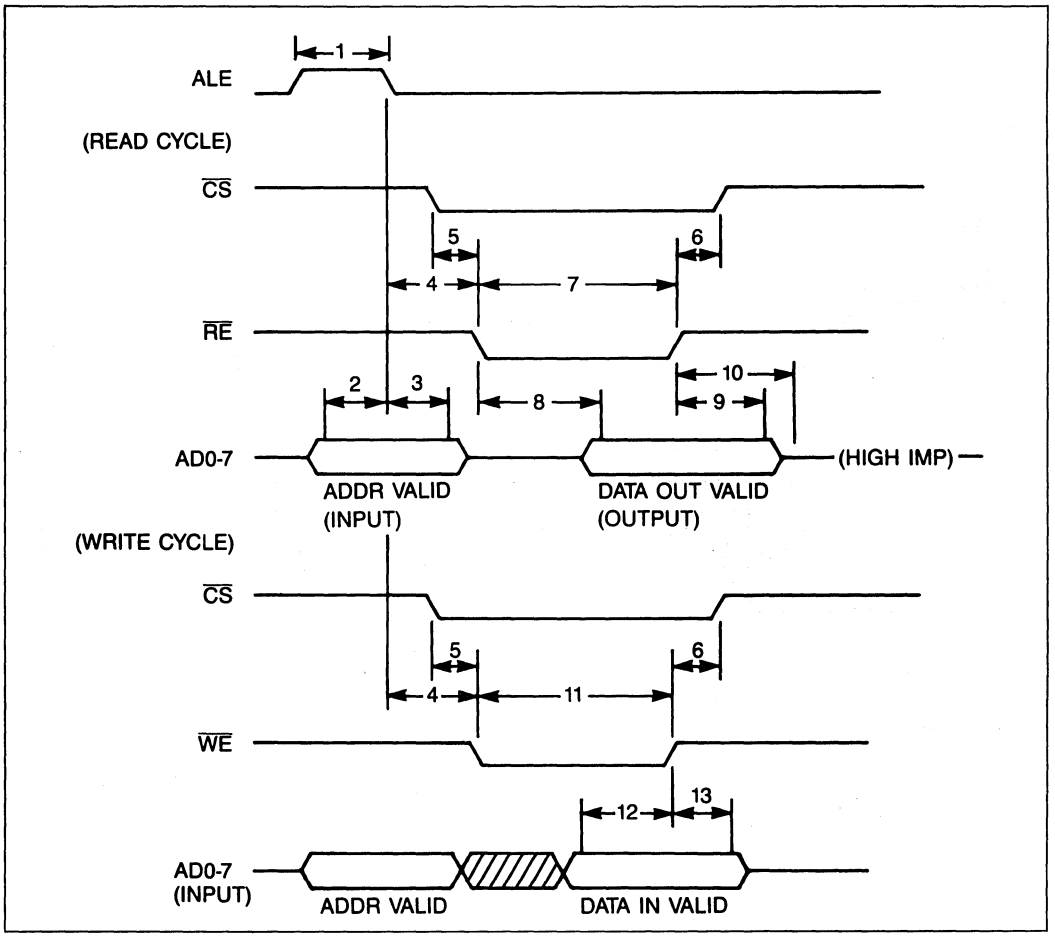
OUTPUT RISE/FALL TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	CLK	FCLK Cycle Time*		R	40 nsec Min [1]
				R	60 nsec Min [2]
2	TCR	FCLK Rise Time		R	10 nsec Max
3	TCH	FCLK High Time		R	.4 CLK Min
4	TCF	FCLK Fall Time		R	10 nsec Max
5	TCL	FCLK Low Time		R	.4 CLK Min
6	TMR	$\overline{MR}$ Pulse Width		R	80 CLK Min

* This specification is used to define several other timings.
[1] The maximum clock frequency is 25 MHz if Degree 4 or Degree 8 polynomial is selected.
[2] If the Degree 16 polynomial is selected, the maximum clock frequency is 16.7 MHz.

CLOCK/RESET TIMING



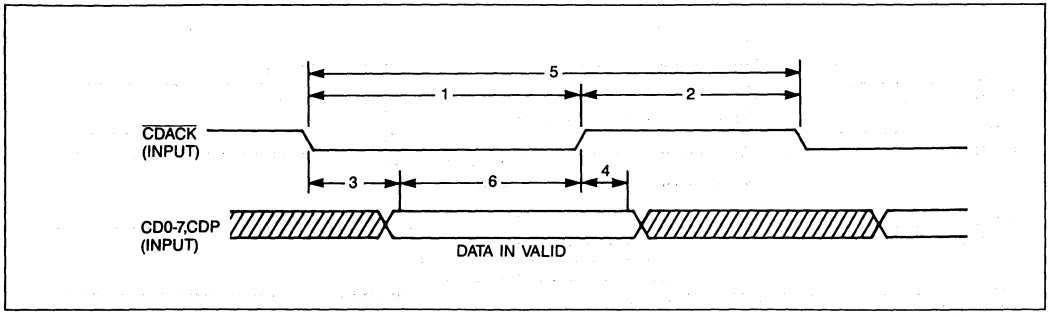
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TALW	ALE Pulse Width		R	50 nsec	Min
2	TADS	Address Setup Time	Before T.E., ALE	R	15 nsec	Min
3	TADH	Address Hold Time	After T.E., ALE	R	15 nsec	Min
4	TRWD	RE/We Setup Time	After T.E., ALE	R	15 nsec	Min
5	TCSE	$\overline{CS}$ Setup Time	Before L.E., RE/WE	R	0 nsec	Min
6	THLD	$\overline{CS}$ Hold Time	After T.E., RE/WE	R	0 nsec	Min
7	TRE	$\overline{RE}$ Pulse Width		R	120 nsec	Min
					2.0 CLK	Min [1]
8	TDAC	Data Output Delay	After L.E., $\overline{RE}$	S	95 nsec	Max
9	TDOH	Data Hold Time	After T.E., $\overline{RE}$	S	20 nsec	Min
10	TDOT	Data Bus High imp.	After T.E., $\overline{RE}$	S	75 nsec	Max
11	TWE	$\overline{WE}$ Pulse Width		R	130 nsec	Min
12	TDS	Data Setup Time	Before T.E., $\overline{WE}$	R	50 nsec	Min
13	TDH	Data Hold Time	After T.E., $\overline{WE}$	R	10 nsec	Min

[1] This restriction applies only when reading the syndrome FIFO.

TASKFILE ACCESS TIMING
(Including PIO mode Syndrome Transfer)

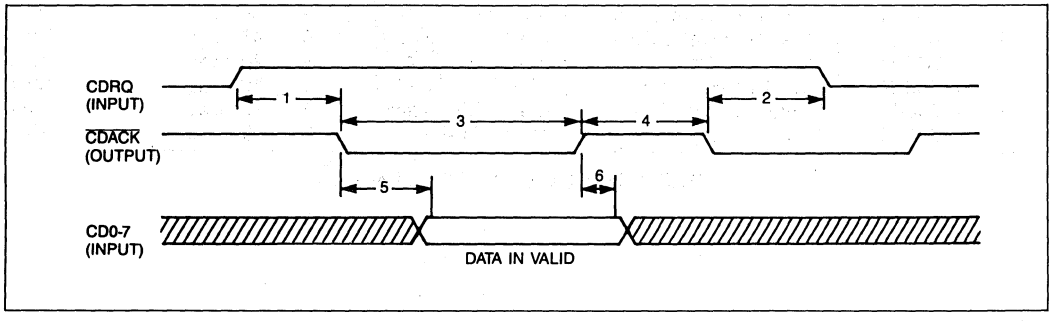
29

CONTROLLER BUS TIMING



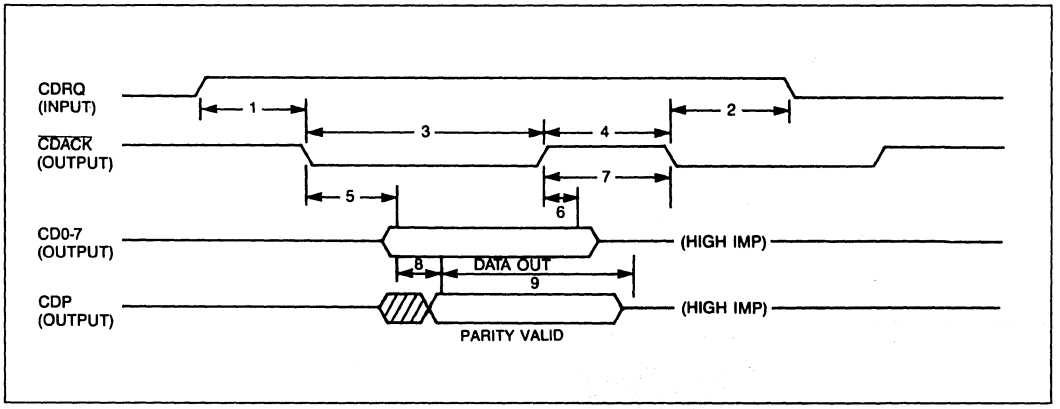
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDK1	CDACK INP Pulse Width		R	2.0 CLK + 10nsec	Min
					100 μsec	Max
2	TCDC1	Transfer Recovery Time	After T.E. CDACK	R	2.0 CLK + 20 nsec	Min
3	TACC1	Data Access Time	After L.E. CDACK	R	4.0 CLK – 80 nsec	Max
4	TCDH1	Data Hold Time	After T.E. CDACK	R	10 nsec	Min
5	TCCDK	Transfer/Cycle Time	Between L.E. CDACK	R	5.0 CLK	Min
6	TCDS1	Data Setup Time	Before T.E. CDACK	R	40 nsec	Min

REDUNDANCY READ TIMING



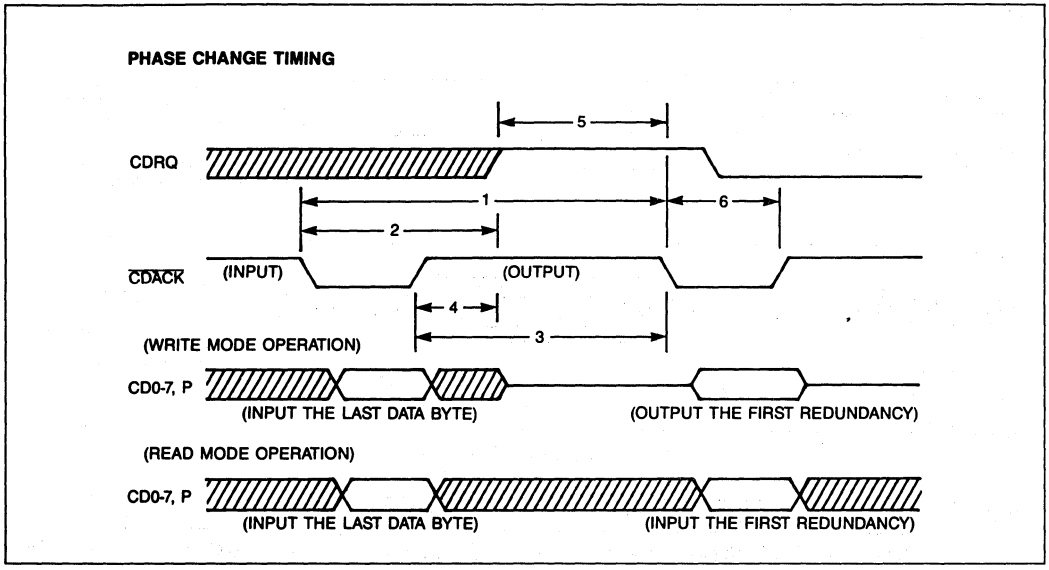
REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., DRQ	S	2.0 CLK	Min
					4.0 CLK + 20 nsec	Max
2	TDRR	CDRQ Reset Timing	After L.E., CDACK	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TDCD2	CDACK Recovery Time	After T.E., CDACK	S	2.0 CLK	Min
5	TACC2	Data Valid Delay Time	After L.E., CDACK	S	4.0 CLK – 80 nsec	Max
6	TCDH2	Data Hold Time	After T.E., CDACK	S	10 nsec	Min

DATA READ TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TCDD	CDACK Synchro Delay	After L.E., CDRQ	S	2.0 CLK	Min
					4.0 CLK + 20 nsec	Max
2	TDRR	CDRQ Reset Timing	After L.E., $\overline{\text{CDACK}}$	R	2.0 CLK – 15 nsec	Max
3	TCDK2	CDACK Out Pulse Width		S	4.0 CLK – 40 nsec	Min
4	TCDC2	CDACK Recovery Time	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK	Min
5	TCDD	Data Valid Delay Time	After L.E., $\overline{\text{CDACK}}$	S	45 nsec	Max
6	TCDH2	Data Hold Time	After T.E., $\overline{\text{CDACK}}$	S	20 nsec	Min
7	TCDOT	Data Bus High Imp.	After T.E., $\overline{\text{CDACK}}$	S	50 nsec	Max
8	TCDPD	Parity Bit Delay Time	After CD0-7 Valid	S	20 nsec	Max
9	TCDPT	Parity Bit High Imp.	After CD0-7 H.I.	S	10 nsec	Max

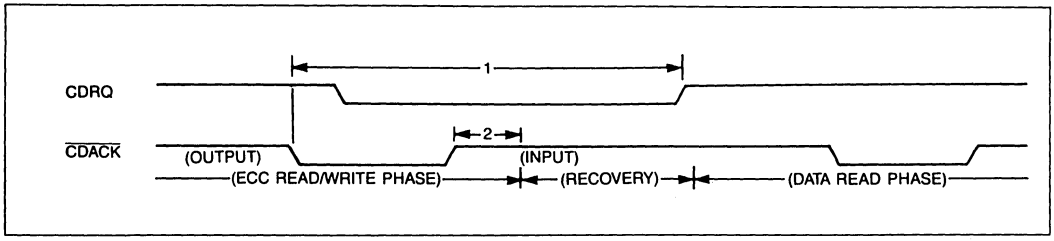
REDUNDANCY OUTPUT TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
***WRITE Mode Operation (Assumes FIFO empty prior to receiving the last data)**					
1	TSOLW	Switch Over Cycle Time	After L.E., $\overline{\text{CDACK}}$	S	10.0 CLK Min [1] 12.0 CLK + 25 nsec Max [1]
2	TCDLW	$\overline{\text{CDACK}}$ Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	4.0 CLK Min [2] 6.0 CLK + 25 nsec Max [2]
3	TSOTW	Switch Over Delay	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK Min
4	TCDTW	$\overline{\text{CDACK}}$ Direc. Reversal	After T.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min
***READ Mode Operation (Assumes FIFO not full after receiving the last data)**					
1	TSOLR	Switch Over Cycle Time	After L.E., $\overline{\text{CDACK}}$	S	6.0 CLK Min [1] 8.0 CLK + 24 nsec Max [1]
2	TCDLR	$\overline{\text{CDACK}}$ Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	4.0 CLK Min [2] 6.0 CLK + 25 nsec Max [2]
3	TSOTR	Switch over Delay	After T.E., $\overline{\text{CDACK}}$	S	2.0 CLK Min
4	TCDTR	$\overline{\text{CDACK}}$ Direc. Reversal	After T.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min
***WRITE/READ Operations**					
5	TCDD	$\overline{\text{CDACK}}$ Synchro Delay	After L.E., CDRQ	S	4.0 CLK + 20 nsec Min [3]
6	TCDK2	$\overline{\text{CDACK}}$ Out Pulse Width		S	4.0 CLK − 40 nsec Min

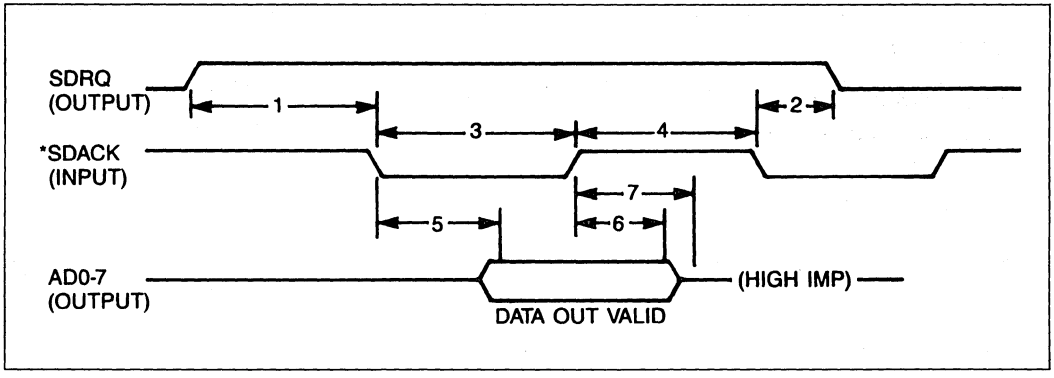
[1] This specification applies if TSOTR/W is met.
[2] This specification applies if TCDTR/W is met.
[3] This specification supercedes TSOLR/W and TCDLR/W.

PHASE CHANGE TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING
1	TSWI	Interblock Gap Time	After L.E., $\overline{\text{CDACK}}$	R	15.0 CLK Min (Write OP) 47.0 CLK Min (Read OP)
2	TCDI	CDACK Direc. Reversal	After L.E., $\overline{\text{CDACK}}$	S	1.0 CLK Min

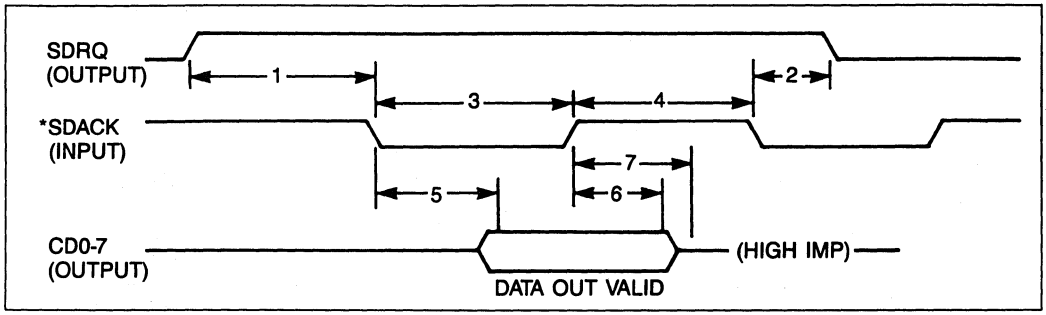
INTER-BLOCK GAP TIMING



REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD1	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S	80 nsec	Max
3	TSDK1	SDACK Pulse Width		R	3.0 CLK	Min
4	TSDC1	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA1	Data Output Delay	After L.E., SDACK	S	85 nsec	Max
6	TSDH1	Data Hold time	After T.E., SDACK	S	40 nsec	Min
7	TSDT1	Data Bus High Imp.	After T.E., SDACK	S	85 nsec	Max

DMA TRANSFER TIMING (SYNDROME ON PROCESSOR BUS)

29

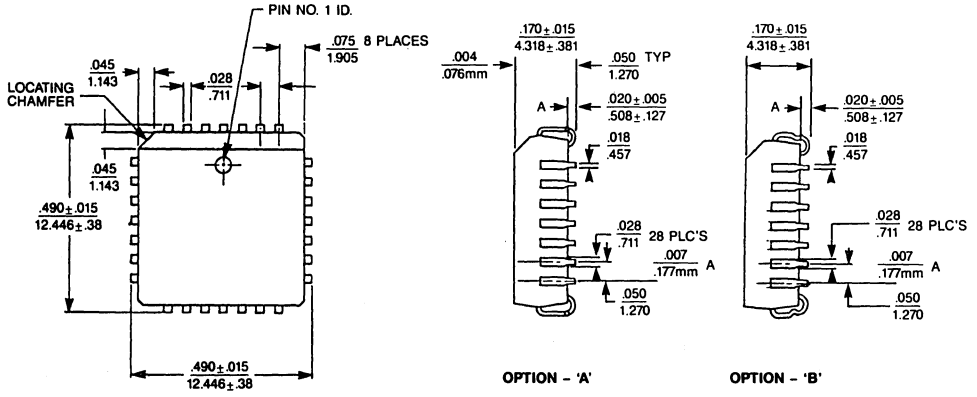


REF	NAME	DESCRIPTION	REFERENCE	R/S	TIMING	
1	TSDD2	SDACK Setup Time	After L.E., SDRQ	R	0 nsec	Min
2	TSDR	SDACK Reset Timing	After L.E., SDACK	S		
3	TSDK2	SDACK Pulse Width		R	4.0 CLK	Min
4	TSDC2	Transfer Recovery Time	After T.E., SDACK	R	2.0 CLK + 10 nsec	Min
5	TSDA2	Data Output Delay	After L.E., SDACK	S	110 nsec	Max
6	TSDH2	Data Hold Time	After T.E., SDACK	S	40 nsec	Max
7	TSDT2	Data Bus High Imp.	After T.E., SDACK	S	120 nsec	Max

* SDACK low active option is shown.

SYNDROME TRANSFER TIMING (SYNDROME ON CONTROLLER BUS)

PACKAGE INFORMATION



28 LEAD PLASTIC "JH"

29