DATABOOK

US74HCT High Speed CMOS
Logic Products

UNIVERSAL SEMICONDUCTOR INC.

US74HCT LOGIC PRODUCTS ⚡ CMOS

INDEX OF INTERIM DATA SHEETS

US74HCT LOGIC PRODUCTS cmos

Product Availability

DEVICE	AVAILABILITY	DEVICE	AVAILABILITY
US74HCT00	NOW	US74HCT158	NOW
US74HCT02	NOW	US74HCT161	OCT
US74HCT03	NOW	US74HCT163	JAN
US74HCT04	NOW	US74HCT164	OCT
US74HCT05	NOW	US74HCT173	JAN
US74HCT08	NOW	US74HCT174	OCT
US74HCT10	NOW	US74HCT175	OCT
US74HCT11	NOW	US74HCT191	JAN
US74HCT14	NOW	US74HCT193	OCT
US74HCT20	NOW	US74HCT194	OCT
US74HCT21	NOW	US74HCT221	OCT
US74HCT27	NOW	US74HCT240	OCT
US74HCT30	NOW	US74HCT241	OCT
US74HCT32	NOW	US74HCT244	OCT
US74HCT44	NOW	US74HCT245	OCT
US74HCT51	NOW	US74HCT251	JAN
US74HCT58	JAN	US74HCT257	NOW
US74HCT73	NOW	US74HCT258	NOW
US74HCT74	NOW	US74HCT266	NOW
US74HCT75	NOW	US74HCT273	OCT
US74HCT76	NOW	US74HCT299	OCT
US74HCT86	NOW	US74HCT365	JAN
US74HCT107	NOW	US74HCT373	OCT
US74HCT109	JAN	US74HCT374	OCT
US74HCT112	JAN	US74HCT375	NOW
US74HCT123	OCT	US74HCT377	OCT
US74HCT125	NOW	US74HCT390	JAN
US74HCT126	NOW	US74HCT533	JAN
US74HCT133	NOW	US74HCT534	JAN
US74HCT138	NOW	US74HCT640	JAN
US74HCT139	NOW	US74HCT643	JAN
US74HCT145	NOW	US74HCT648	JAN
US74HCT151	NOW	US74HCT4002	NOW
US74HCT153	NOW	US74HCT4075	NOW
US74HCT157	NOW	US74HCT4078	NOW

US74HCT00

⚡ CMOS
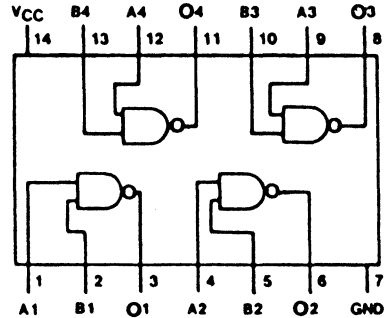
QUAD 2-INPUT NAND GATE

Preliminary

Features

- Wide Power Supply Range   5V±10% For 74HCT
- Typical Propagation Delay   10ns
- Low Quiescent Current   20μA Maximum
- Low Input Current   1μA Maximum
- Fanout of 10 LS-TTL Loads
- HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

Logic Diagram

UNIVERSAL SEMICONDUCTOR INC.

🔷 *CMOS*

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

UNIVERSAL SEMICONDUCTOR INC.

US74HCT02

⟨⟩ CMOS

QUAD 2-INPUT NOR GATE

Preliminary

Features

■ Wide Power Supply Range   5V±10% For 74HCT

■ Typical Propagation Delay   10ns
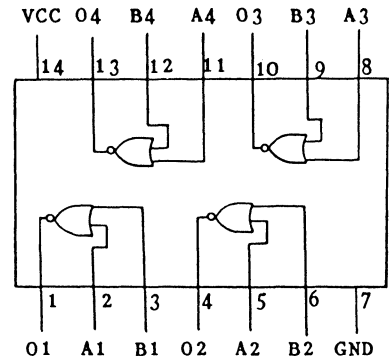
■ Low Quiescent Current   20μA Maximum

■ Low Input Current   1μA Maximum

■ Fanout of 10 LS-TTL Loads

■ HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

VCC O4 B4 A4 O3 B3 A3

14 13 12 11 10 9 8

1 2 3 4 5 6 7

O1 A1 B1 O2 A2 B2 GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1:   Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2:   Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

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Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

Switching Time Waveforms and AC Test Circuit

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

UNIVERSAL SEMICONDUCTOR INC.

US74HCT04

⊕ CMOS

HEX INVERTER (TRIPLE BUFFERED)

Preliminary

Features

■ Wide Power Supply Range   5V±10% For 74HCT

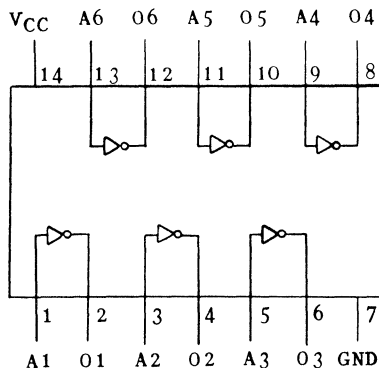■ Typical Propagation Delay   10ns

■ Low Quiescent Current   20μA Maximum

■ Low Input Current   1μA Maximum

■ Fanout of 10 LS-TTL Loads

■ HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1:   Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2:   Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max. limits apply across the whole operating temperature range unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

UNIVERSAL SEMICONDUCTOR INC.

US74HCT08 ⚡ CMOS

QUAD 2-INPUT AND GATE

Preliminary

Features

- Wide Power Supply Range   5V±10% For 74HCT
- Typical Propagation Delay   15ns
- Low Quiescent Current   20μA Maximum
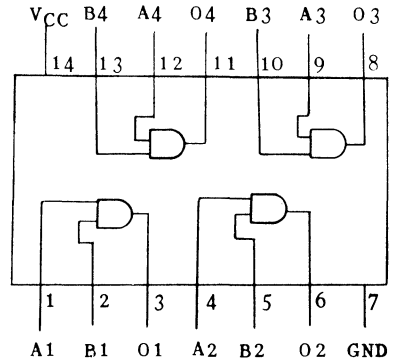- Low Input Current   1μA Maximum
- Fanout of 10 LS-TTL Loads
- HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

V_{CC}	B4	A4	O4	B3	A3	O3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	O1	A2	B2	O2	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

CMOS

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	15	20	ns
		C_L = 50pF	18	23	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	35		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption. $I_S = C_{PD} V_{CC} f + I_{CC}$.

Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

C_L = 15pF, 50 pF

UNIVERSAL SEMICONDUCTOR INC.

US74HCT10

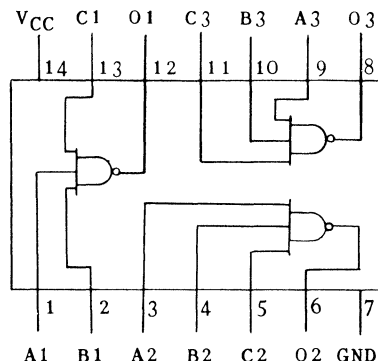# TRIPLE 3-INPUT NAND GATE

Preliminary

Features

■ Wide Power Supply Range   5V±10% For 74HCT

■ Typical Propagation Delay   10ns

■ Low Quiescent Current   20μA Maximum

■ Low Input Current   1μA Maximum

■ Fanout of 10 LS-TTL Loads

■ HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

V_CC	C1	O1	C3	B3	A3	O3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	A2	B2	C2	O2	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $|I_{OUT}| \leq 20\mu A$	V_{CC} = 4.5V	2	V
			V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $|I_{OUT}| \leq 20\mu A$	V_{CC} = 4.5V	0.8	V
			V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

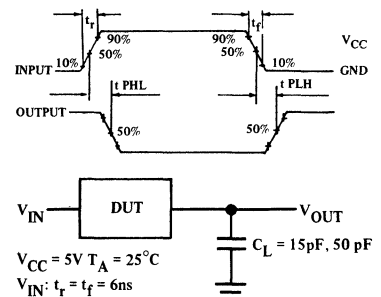## AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption. $I_S = C_{PD} V_{CC} f + I_{CC}$.

Switching Time Waveforms and AC Test Circuit

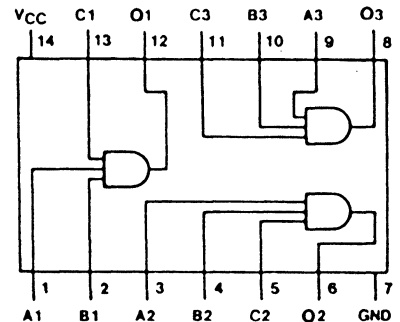V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns
C_L = 15pF, 50 pF

UNIVERSAL SEMICONDUCTOR INC.

US74HCT11

⚡ CMOS

TRIPLE 3-INPUT AND GATE

Preliminary

Features

- ■ Wide Power Supply Range — 5V±10% For 74HCT
- ■ Typical Propagation Delay — 15ns
- ■ Low Quiescent Current — 20µA Maximum
- ■ Low Input Current — 1µA Maximum
- ■ Fanout of 10 LS-TTL Loads
- ■ HCT Compatible With LS-TTL Outputs — No pull up resistor required

Pin Configuration

Vcc	C1	O1	C3	B3	A3	O3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	A2	B2	C2	O2	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.
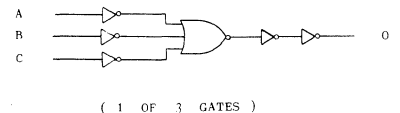
Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

Logic Diagram

(1 OF 3 GATES)

UNIVERSAL SEMICONDUCTOR INC.

⏚ CMOS

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time	C_L = 15pF	15	20	ns
	Output High to Low/ Output Low to High	C_L = 50pF	18	22	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	35		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = $C_{PD} V_{CC}^2 f$ + $I_{CC} V_{CC}$, and the no load dynamic current consumption. I_S = $C_{PD} V_{CC} f$ + I_{CC}.
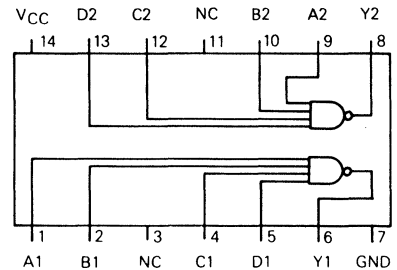
Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

UNIVERSAL SEMICONDUCTOR INC.
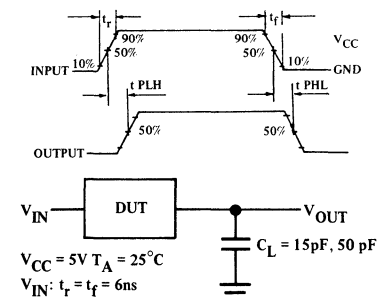
US74HCT20

DUAL 4-INPUT NAND GATE

Preliminary

Features

- **Wide Power Supply Range**
- **Typical Propagation Delay**
- **Low Quiescent Current**
- **Low Input Current**
- **Fanout of 10 LS-TTL Loads**
- **HCT Compatible With LS-TTL Outputs**

5V±10% For 74HCT

10ns

20μA Maximum

1μA Maximum

Normal Driving

No pull up resistor required

Pin Configuration

V_{CC}	D2	C2	NC	B2	A2	Y2
14	13	12	11	10	9	8
1	2	3	4	5	6	7
A1	B1	NC	C1	D1	Y1	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.
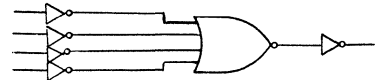
Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

Logic Diagram

UNIVERSAL SEMICONDUCTOR INC.

⌬ CMOS

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

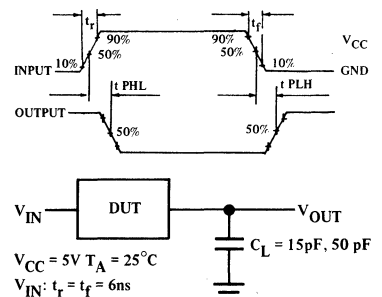| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 4.5V	2	V
			V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 4.5V	0.8	V
			V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = $C_{PD} V_{CC}^2$ f + $I_{CC} V_{CC}$, and the no load dynamic current consumption. I_S = $C_{PD} V_{CC}$ f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

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US74HCT27

@ CMOS

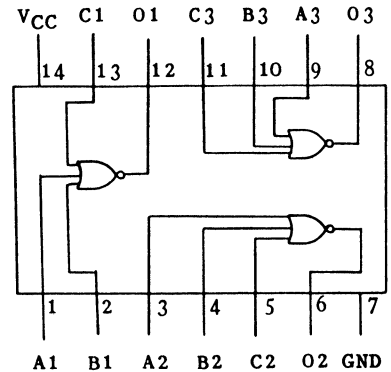# TRIPLE 3-INPUT NOR GATE

Preliminary

Features

- Wide Power Supply Range — 5V±10% For 74HCT
- Typical Propagation Delay — 10ns
- Low Quiescent Current — 20μA Maximum
- Low Input Current — 1μA Maximum
- Fanout of 10 LS-TTL Loads
- HCT Compatible With LS-TTL Outputs — No pull up resistor required

Pin Configuration

V_{CC}	C1	O1	C3	B3	A3	O3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	A2	B2	C2	O2	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

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Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

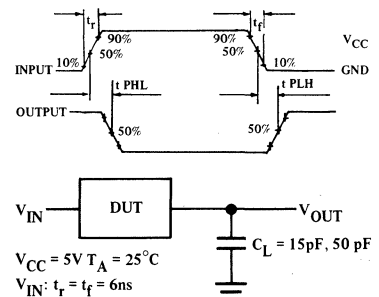| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 4.5V	2	V
			V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 4.5V	0.8	V
			V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	10	15	ns
		C_L = 50pF	13	18	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

C_L = 15pF, 50 pF
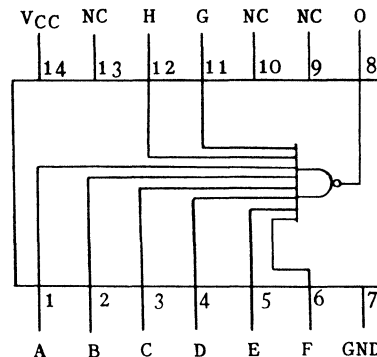
UNIVERSAL SEMICONDUCTOR INC.

US74HCT30

CMOS

8-INPUT NAND GATE

Preliminary

Features

- Wide Power Supply Range — 5V±10% For 74HCT
- Typical Propagation Delay — 18ns
- Low Quiescent Current — 20µA Maximum
- Low Input Current — 1µA Maximum
- Fanout of 10 LS-TTL Loads
- HCT Compatible With LS-TTL Outputs — No pull up resistor required

Pin Configuration

Vcc	NC	H	G	NC	NC	O
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A	B	C	D	E	F	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

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Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

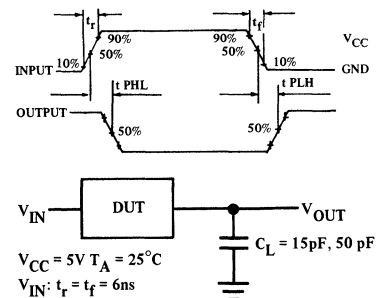| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL}	Maximum Propagation Delay Time	C_L = 15pF	18	25	ns
/ t_{PLH}	Output High to Low/ Output Low to High	C_L = 50pF	21	28	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	40		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption. $I_S = C_{PD} V_{CC} f + I_{CC}$.
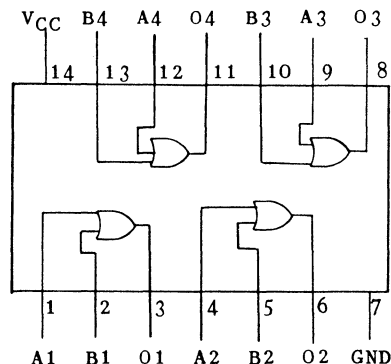
Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

UNIVERSAL SEMICONDUCTOR INC.

US74HCT32

CMOS

QUAD 2-INPUT OR GATE

Preliminary

Features

■ Wide Power Supply Range   5V±10% For 74HCT

■ Typical Propagation Delay   15ns

■ Low Quiescent Current   20μA Maximum

■ Low Input Current   1μA Maximum

■ Fanout of 10 LS-TTL Loads

■ HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

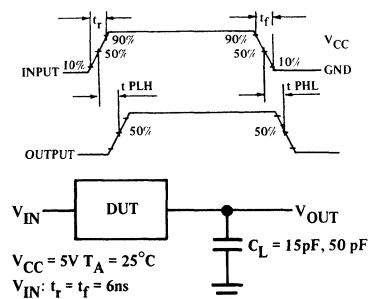| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	15	20	ns
		C_L = 50pF	18	23	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	50		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.
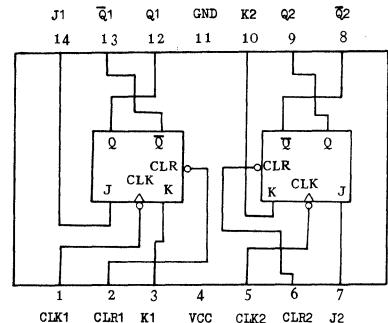
Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

UNIVERSAL SEMICONDUCTOR INC.

US74HCT73

$\oplus$ CMOS

DUAL J-K FLIP-FLOPS WITH CLEAR

Preliminary

Features

- **Wide Power Supply Range** — 5V±10% For 74HCT
- **Typical Propagation Delay** — 24ns
- **Low Quiescent Current** — 40μA Maximum
- **Low Input Current** — 1μA Maximum
- **Fanout of 10 LS-TTL Loads** — Normal Driving
- **HCT Compatible With LS-TTL Outputs** — No pull up resistor required

Pin Configuration

J1	$\overline{Q}$1	Q1	GND	K2	Q2	$\overline{Q}$2
14	13	12	11	10	9	8

CLK1	CLR1	K1	VCC	CLK2	CLR2	J2
1	2	3	4	5	6	7

Description

These high speed J-K Flip-Flops are fabricated with Oxide Isolated Silicon Gate CMOS Process. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads, and are functionally as well as pinout compatible with the standard LS-TTL type. HCT has level conversion which features LS-TTL input voltage level compatibility.

These Flip-Flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and is accomplished by a low level on the input.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V$_{CC}$)	-0.5 to +7.0V
DC Input or Output Voltage (V$_{IN}$, V$_{OUT}$)	-0.5 to V$_{CC}$+0.5V
DC Current Drain, per pin, any output (I$_{OUT}$)	±25mA
DC Current Drain, per pin, V$_{CC}$ or GND (I$_{CC}$)	±50mA
Storage Temperature (T$_{STG}$)	-65°C to +150°C
Power Dissipation (P$_D$) (NOTE 2)	500mW
Lead Temperature (T$_L$) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

⊕CMOS

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

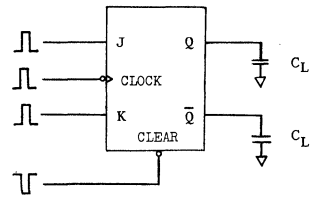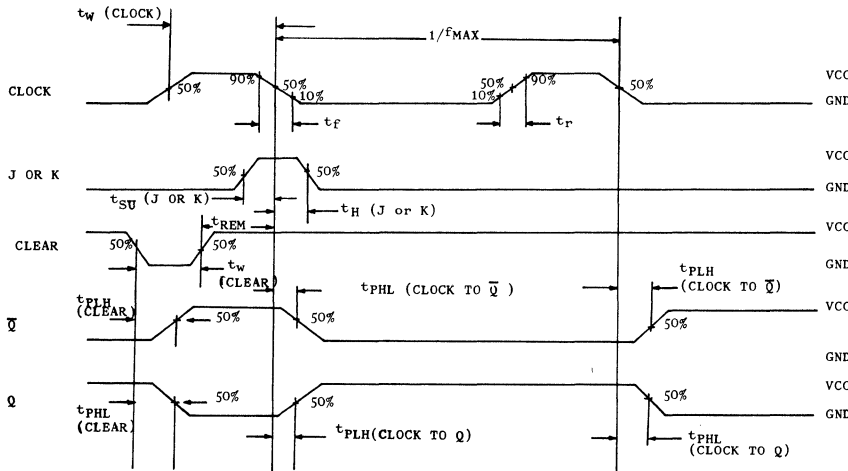| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	4.0	μA
			T_A = 85°C	40.0	μA
			T_A = 125°C	80.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

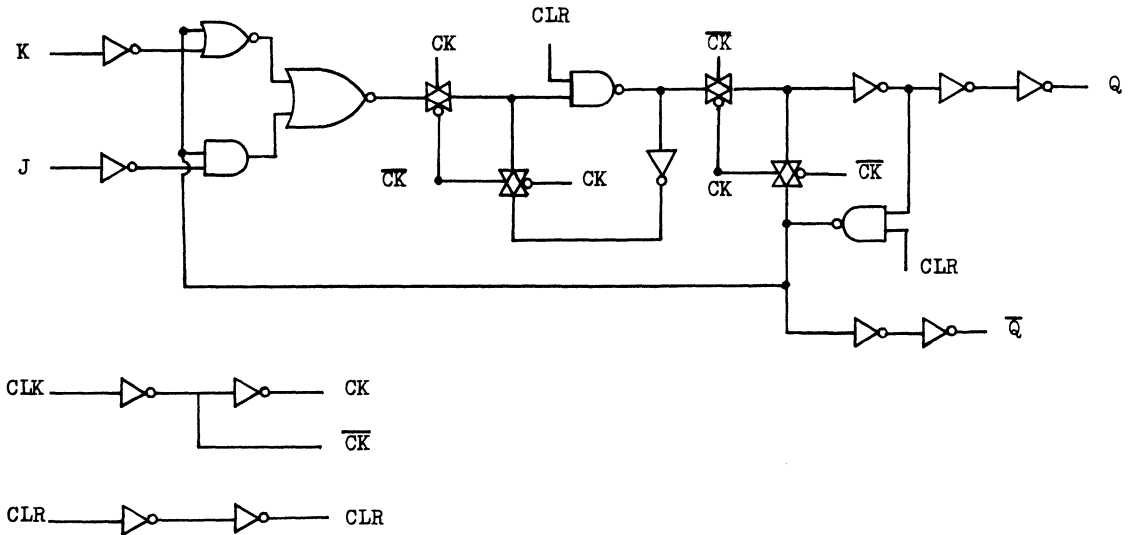$V_{CC} = 5.0V$, $T_A = 25°C$, $t_r = t_f = 6ns$, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
f_{MAX}	Maximum Clock Frequency	C_L = 15pF C_L = 50pF	50 50	30 30	MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$	C_L = 15pF C_L = 50pF	18 20	24 26	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Output Q or $\overline{Q}$	C_L = 15pF C_L = 50pF	24 28	29 31	ns ns
t_S	Time Prior to Clock Pulse that J or K must be present		16	20	ns
t_H	Time After Clock Pulse that J or K must be held			0	ns
t_W	Minimum Clock Pulse Width		6	16	ns
t_W	Minimum Clear Pulse Width		6	16	ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per Flip-Flop)	80		pF
t_{REM}	Minimum Clear Removed Time		10	20	ns

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Switching Time Waveforms and AC Test Circuit

⟨⟩ CMOS

Logic Diagram

Truth Table

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_o	$\overline{Q_o}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_o	$\overline{Q_o}$

US74HCT74

⚡CMOS

DUAL D FLIP-FLOPS WITH PRESET AND CLEAR

Preliminary

Features

- Wide Power Supply Range
- Typical Propagation Delay
- Low Quiescent Current
- Low Input Current
- Fanout of 10 LS-TTL Loads
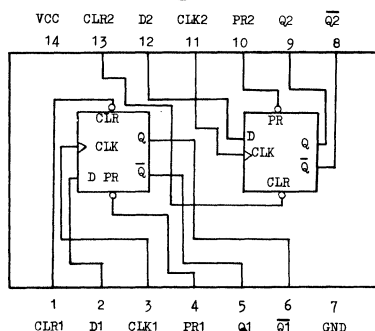- HCT Compatible With LS-TTL Outputs

5V±10% For 74HCT

22ns

40μA Maximum

1μA Maximum

Normal Driving

No pull up resistor required

Pin Configuration

VCC	CLR2	D2	CLK2	PR2	Q2	$\overline{Q2}$
14	13	12	11	10	9	8

1	2	3	4	5	6	7
CLR1	D1	CLK1	PR1	Q1	$\overline{Q1}$	GND

Description

The 74HCT74 utilizes Oxide Isolated Silicon Gate CMOS Process. They possess the high noise immunity, LS-TTL compatible operating speeds and low power consumption of standard CMOS integrated circuits. The 74HCT family is functionally and pinout compatible with the standard 74LS logic family, and has level conversion which features LS-TTL input voltage level compatibility.

Each Flip-Flop has independent DATA, PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and are accomplished by a low level at the appropriate input.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V$_{CC}$)	-0.5 to +7.0V
DC Input or Output Voltage (V$_{IN}$, V$_{OUT}$)	-0.5 to V$_{CC}$+0.5V
DC Current Drain, per pin, any output (I$_{OUT}$)	±25mA
DC Current Drain, per pin, V$_{CC}$ or GND (I$_{CC}$)	±50mA
Storage Temperature (T$_{STG}$)	-65°C to +150°C
Power Dissipation (P$_D$) (NOTE 2)	500mW
Lead Temperature (T$_L$) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

⊕ CMOS

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC})　74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	4.0	μA
			T_A = 85°C	40.0	μA
			T_A = 125°C	80.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

$V_{CC} = 5.0V$, $T_A = 25°C$, $t_r = t_f = 6ns$, (unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
f_{MAX}	Maximum Clock Frequency	$C_L = 15pF$	40	30	MHz
		$C_L = 50pF$	35	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$	$C_L = 15pF$	22	33	ns
		$C_L = 50pF$	24	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$	$C_L = 15pF$	28	44	ns
		$C_L = 50pF$	30	46	ns
t_{SU}	Minimum Set-Up Time, D to CLK		10	20	ns
t_H	Minimum Hold Time, CLK to D			0	ns
t_{REM}	Minimum Preset or Clear Removal Time			5	ns
t_W	Minimum Clock, Preset or Clear Pulse Width			16	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per Flip-Flop)	60		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.
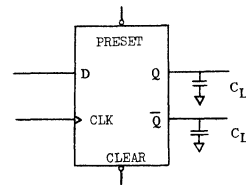
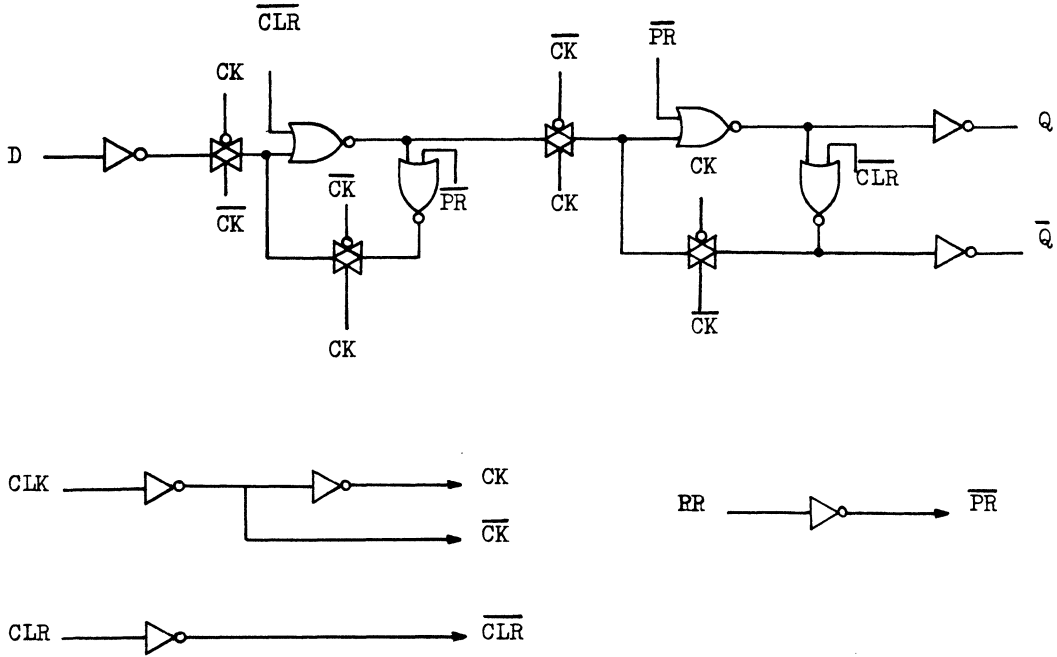## Switching Time Waveforms and AC Test Circuit
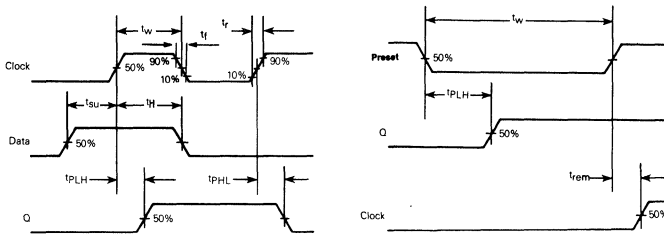
CLOCK AND DATA TIMING

PRESET TIMING

CLEAR TIMING

UNIVERSAL SEMICONDUCTOR INC.

🔲 CMOS
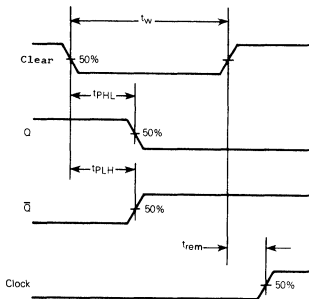
Logic Diagram

Truth Table

INPUTS				OUTPUTS	
PR	**CLR**	**CLK**	**D**	**Q**	**$\overline{Q}$**
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q_0}$

NOTE: Q_0 = the level of Q before the indicated input conditions were established.

*   This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

US74HCT76　　　　　　　　　⚡ CMOS

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR
Preliminary

Features

■ Wide Power Supply Range　　　　5V±10% For 74HCT

■ Typical Propagation Delay　　　　18ns

■ Low Quiescent Current　　　　　40μA Maximum

■ Low Input Current　　　　　　　1μA Maximum

■ Fanout of 10 LS-TTL Loads　　　Normal Driving

■ HCT Compatible With LS-TTL Outputs　　No pull up resistor required

Pin Configuration

K1	Q1	Q̄1	GND	K2	Q2	Q̄2	J2
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
CLK1	PR1	CLR1	J1	VCC	CLK2	PR2	CLR2

Description

These high speed J-K Flip-Flops are fabricated with Oxide Isolated Silicon Gate CMOS Process. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads, and are functionally as well as pinout compatible with the standard LS-TTL type. HCT has level conversion which features LS-TTL input voltage level compatibility.

Each Flip-Flop has independent J, K, PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and are accomplished by a low level on the corresponding input.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1:　Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2:　Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	4.0	μA
		I_{OUT} = 0μA	T_A = 85°C	40.0	μA
			T_A = 125°C	80.0	μA

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AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$	C_L = 15pF C_L = 50pF	18 22	23 28	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$	C_L = 15pF C_L = 50pF	23 28	29 34	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset to Q or $\overline{Q}$	C_L = 15pF C_L = 50pF	25 30	31 36	ns ns
t_{REM}	Mimimum Removal Time Preset to Clear to Clock		10	20	ns
t_{SU}	Minimum Set-Up Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock			0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		10	16	ns
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per Flip-Flop)	80		pF
C_{IN}	Maximum Input Capacitance		5	10	pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Switching Time Waveforms and AC Test Circuit
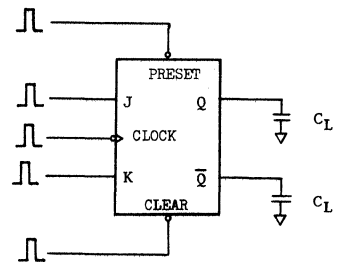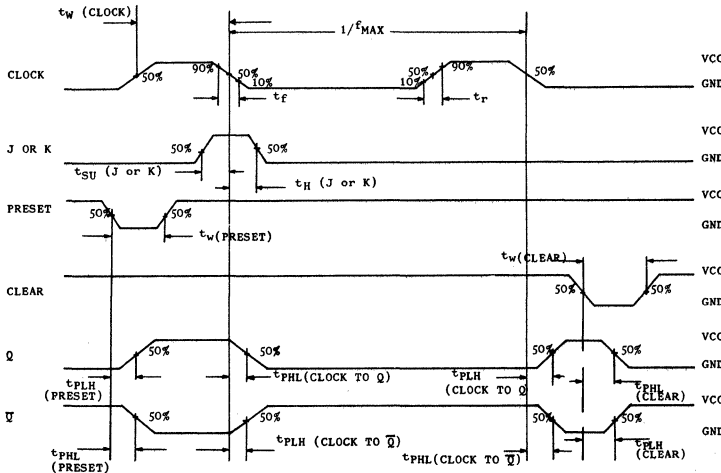
Logic Diagram
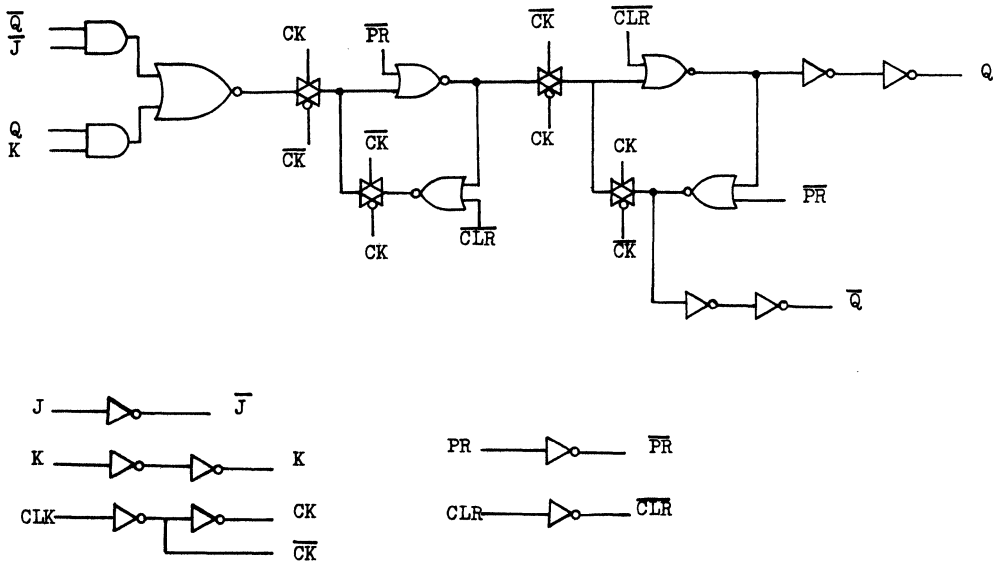
Truth Table

INPUTS					OUTPUTS	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q_0	Q_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q_0}$

* This is an unstable condition, and is not guaranteed.
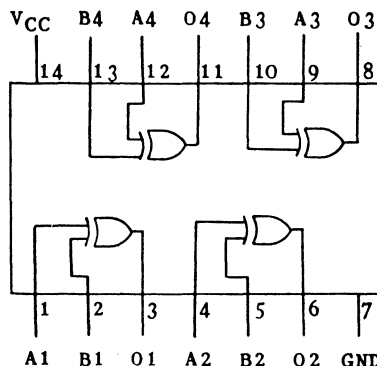
UNIVERSAL SEMICONDUCTOR INC.

US74HCT86 ⚡CMOS

QUAD 2-INPUT EXCLUSIVE OR GATE

Preliminary

Features

- Wide Power Supply Range   5V±10% For 74HCT
- Typical Propagation Delay   12ns
- Low Quiescent Current   20μA Maximum
- Low Input Current   1μA Maximum
- Fanout of 10 LS-TTL Loads
- HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

V_{CC}	B4	A4	O4	B3	A3	O3
14	13	12	11	10	9	8

1	2	3	4	5	6	7
A1	B1	O1	A2	B2	O2	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

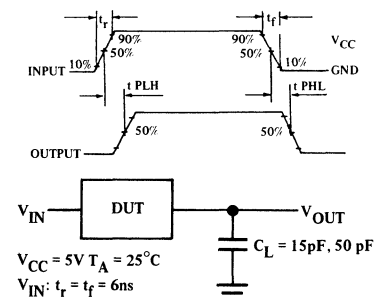| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	12	20	ns
		C_L = 50pF	15	23	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	20		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.
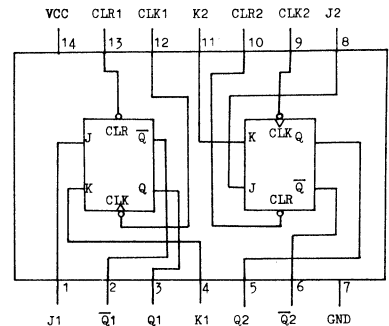
Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

C_L = 15pF, 50 pF

UNIVERSAL SEMICONDUCTOR INC.

US74HCT107 $\quad$ CMOS

DUAL J-K FLIP-FLOPS WITH CLEAR

Preliminary

Features

■ Wide Power Supply Range $\qquad$ 5V±10% For 74HCT

■ Typical Propagation Delay $\qquad$ 24ns

■ Low Quiescent Current $\qquad$ 40μA Maximum

■ Low Input Current $\qquad$ 1μA Maximum

■ Fanout of 10 LS-TTL Loads $\qquad$ Normal Driving

■ HCT Compatible With LS-TTL Outputs $\qquad$ No pull up resistor required

Pin Configuration

Description

These high speed J-K Flip-Flops are fabricated with Oxide Isolated Silicon Gate CMOS Process. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads, and are functionally as well as pinout compatible with the standard LS-TTL type. HCT has level conversion which features LS-TTL input voltage level compatibility.

These Flip-Flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and is accomplished by a low level on the input.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V$_{CC}$)	-0.5 to +7.0V
DC Input or Output Voltage (V$_{IN}$, V$_{OUT}$)	-0.5 to V$_{CC}$+0.5V
DC Current Drain, per pin, any output (I$_{OUT}$)	±25mA
DC Current Drain, per pin, V$_{CC}$ or GND (I$_{CC}$)	±50mA
Storage Temperature (T$_{STG}$)	-65°C to +150°C
Power Dissipation (P$_D$) (NOTE 2)	500mW
Lead Temperature (T$_L$) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
		$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	4.0	μA
			T_A = 85°C	40.0	μA
			T_A = 125°C	80.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

$V_{CC} = 5.0V$, $T_A = 25°C$, $t_r = t_f = 6ns$, (unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
f_{MAX}	Maximum Clock Frequency	$C_L = 15pF$ $C_L = 50pF$	50 50	30 30	MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}_o$	$C_L = 15pF$ $C_L = 50pF$	18 20	24 26	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Output Q or $\overline{Q}$	$C_L = 15pF$ $C_L = 50pF$	24 26	29 32	ns ns
t_S	Time prior to Clock Pulse that J or K must be present		16	20	ns
t_H	Time After Clock Pulse that J or K must be held			0	ns
t_W	Minimum Clock Pulse Width		6	16	ns
t_W	Minimum Clear Pulse Width		6	16	ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE)	(per Flip-Flop)	80		pF
t_{REM}	Minimum Clear Removed Time		10	20	ns

NOTE: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Switching Time Waveforms and AC Test Circuit
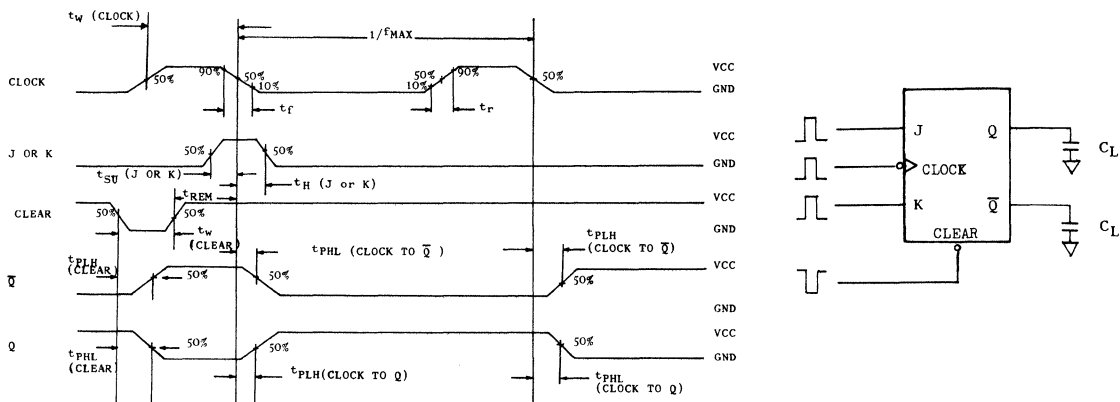
Logic Diagram
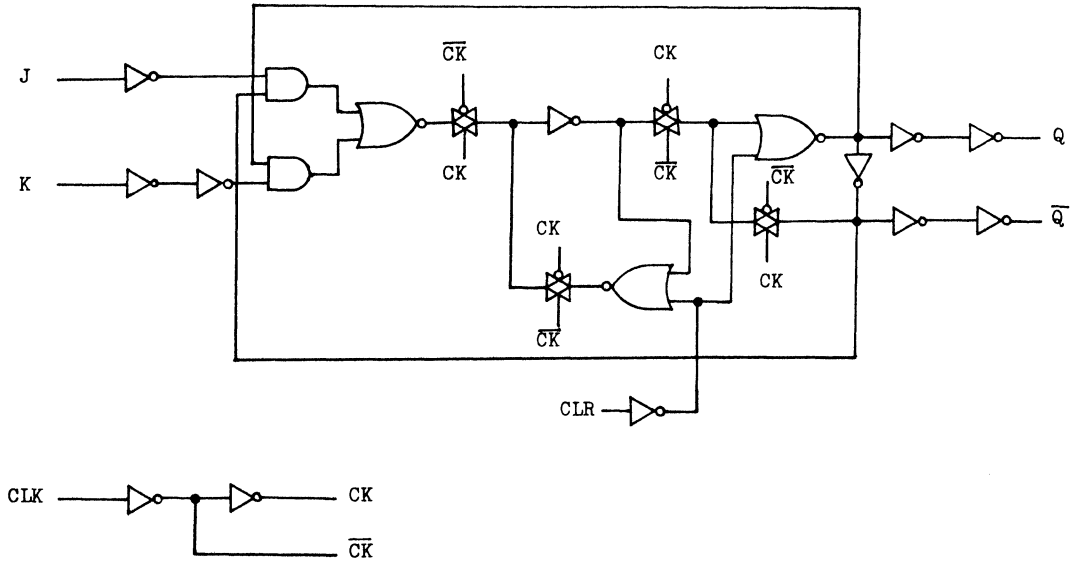
Truth Table

	INPUTS			OUTPUTS	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\overline{Q}_0$

US74HCT133　　　⚡CMOS
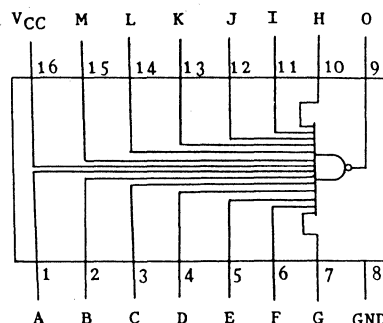
13-INPUT NAND GATE

<div align="center">Preliminary</div>

Features

- ■ Wide Power Supply Range　　5V±10% For 74HCT
- ■ Typical Propagation Delay　　18ns
- ■ Low Quiescent Current　　20μA Maximum
- ■ Low Input Current　　1μA Maximum
- ■ Fanout of 10 LS-TTL Loads
- ■ HCT Compatible With LS-TTL Outputs　　No pull up resistor required

Pin Configuration

Vcc	M	L	K	J	I	H	O
16	15	14	13	12	11	10	9

1	2	3	4	5	6	7	8
A	B	C	D	E	F	G	GND

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1:　Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2:　Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

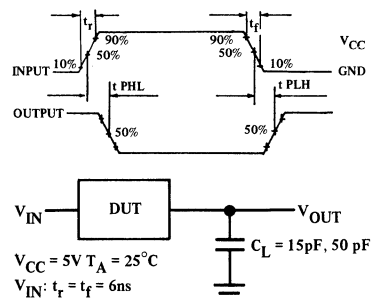| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL}	Maximum Propagation Delay Time	C_L = 15pF	18	25	ns
/ t_{PLH}	Output High to Low/ Output Low to High	C_L = 50pF	21	28	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	40		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.
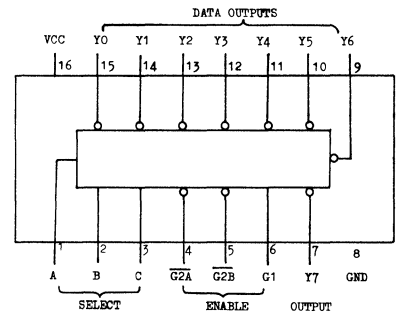
Switching Time Waveforms and AC Test Circuit

UNIVERSAL SEMICONDUCTOR INC.

US74HCT138   ⚡CMOS

3-TO-8 LINE DECODER

Preliminary

Features

- Wide Power Supply Range   **5V±10% For 74HCT**
- Typical Propagation Delay   **20ns**
- Low Quiescent Current   **40μA Maximum**
- Low Input Current   **1μA Maximum**
- Fanout of 10 LS-TTL Loads   **Normal Driving**
- HCT Compatible With LS-TTL Outputs   **No pull up resistor required**

Pin Configuration

DATA OUTPUTS

| VCC | YO | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 |
| 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| A | B | C | $\overline{G2A}$ | $\overline{G2B}$ | G1 | Y7 | GND |

SELECT   ENABLE   OUTPUT

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1:   Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2:   Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

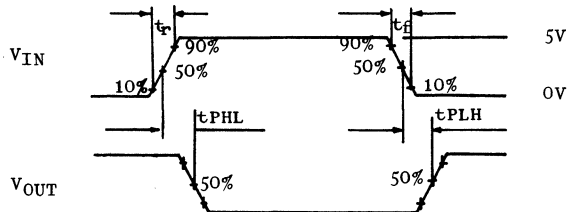| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$\|I_{OUT}\| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $\|I_{OUT}\| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	4	μA
			T_A = 85°C	40	μA
			T_A = 125°C	80	μA

AC Electrical Characteristics

V_{CC} = 5.0V 5V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Output	C_L = 15pF C_L = 50pF	21 25	35 40	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1, $\overline{G2A}$, $\overline{G2B}$ to Output	C_L = 15pF C_L = 50pF	25 27	40 40	ns ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE)		20		pF

NOTE: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.
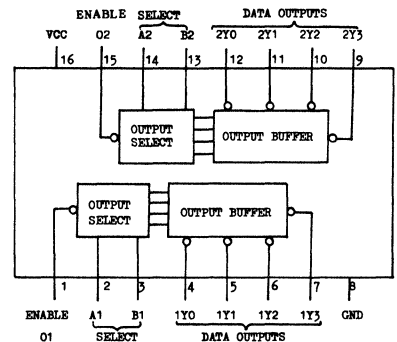
Switching Time Waveforms

⊕ CMOS

Logic Diagram

Truth Table

INPUT					OUTPUT							
Enable		Select										
G	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level,   L = Low Level,   *$\overline{G2}$ = $\overline{G2A}$ + $\overline{G2B}$

UNIVERSAL SEMICONDUCTOR INC.

US74HCT139 ⚡ CMOS

DUAL 2 TO 4 LINE DECODER

Preliminary

Features

- **Wide Power Supply Range**   5V±10% For 74HCT
- **Typical Propagation Delay**   20ns
- **Low Quiescent Current**   40μA Maximum
- **Low Input Current**   1μA Maximum
- **Fanout of 10 LS-TTL Loads**   Normal Driving
- **HCT Compatible With LS-TTL Outputs**   No pull up resistor required

Pin Configuration

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B To Output	C_L = 15pF C_L = 50pF	20		ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G To Output	C_L = 15pF C_L = 50pF	22		ns ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)		75		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.

Switching Time Waveforms
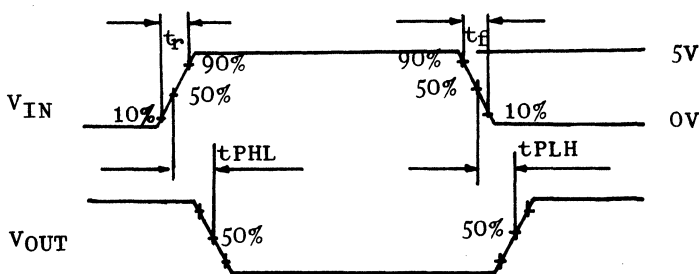
Logic Diagram
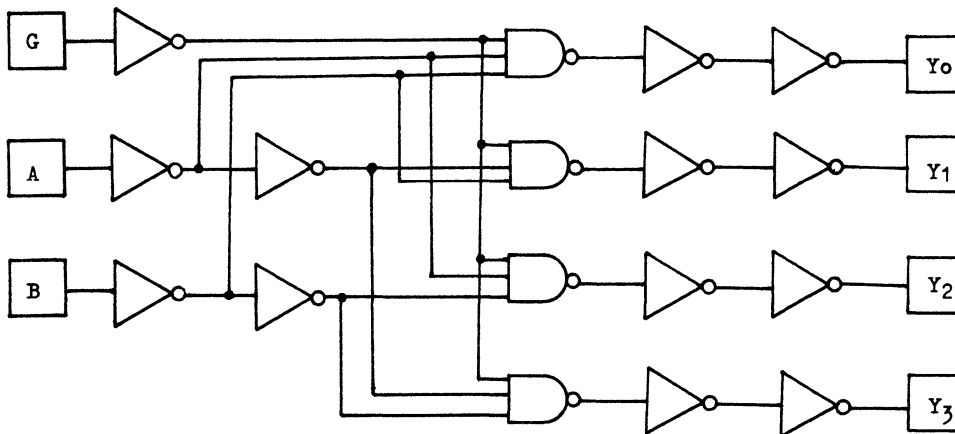
Truth Table

INPUTS			OUTPUTS			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level,   L = Low Level,   X = Don't Care

US74HCT151   ⚡ CMOS

8-CHANNEL DIGITAL MULTIPLEXER

Preliminary

Features

- Wide Power Supply Range   5V±10% For 74HCT
- Typical Propagation Delay   29ns
- Low Quiescent Current   80μA Maximum
- Low Input Current   1μA Maximum
- Fanout of 10 LS-TTL Loads   Normal Driving
- HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

VCC	D4	D5	D6	D7	A0	A1	A2
16	15	14	13	12	11	10	9
1	2	3	4	5	6	7	8
D3	D2	D1	D0	Y	$\overline{Y}$	$\overline{OE}$	GND
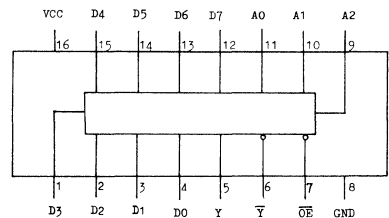
Description

This high speed DIGITAL MULTIPLEXER is fabricated with Oxide Isolated Silicon Gate CMOS Process. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, drive 10 LS-TTL loads, and are functionally as well as pinout compatible with the standard LS-TTL type. HCT has level conversion which features LS-TTL input voltage level compatibility.

This multiplexer selects one of the 8 data sources, depending on the address presented on the A0, A1, and A2 inputs. It features both true (Y) and complement ($\overline{Y}$) outputs. The $\overline{OE}$ input must be at a low logic level to enable this multiplexer. A high logic level at the $\overline{OE}$ forces the $\overline{Y}$ output high and the Y output low.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	8.0	μA
		I_{OUT} = 0μA	T_A = 85°C	80.0	μA
			T_A = 125°C	160.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNIT
t_{PHL}, t_{PLH}	Maximum Propagation Delay A0, A1, A2 to Y	C_L = 15pF C_L = 50pF	29 31	47 50	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A0, A1, A2, to $\overline{Y}$	C_L = 15pF C_L = 50pF	30 32	39 41	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{OE}$ to Y	C_L = 15pF C_L = 50pF	19 21	25 28	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{OE}$ to $\overline{Y}$	C_L = 15pF C_L = 50pF	18 20	23 25	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0-D7 to Y	C_L = 15pF C_L = 50pF	24 26	35 39	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0-D7 to $\overline{Y}$	C_L = 15pF C_L = 50pF	26 29	35 37	ns ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE)		110		pF

NOTE: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit
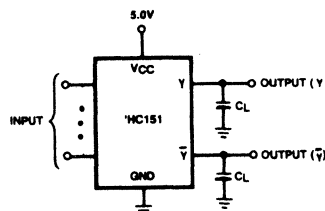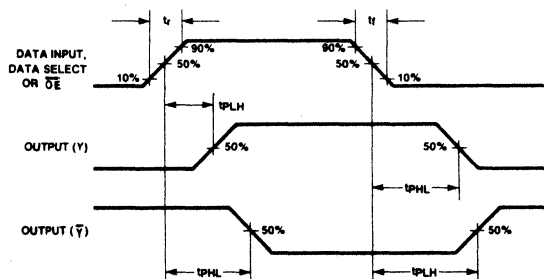
Logic Diagram
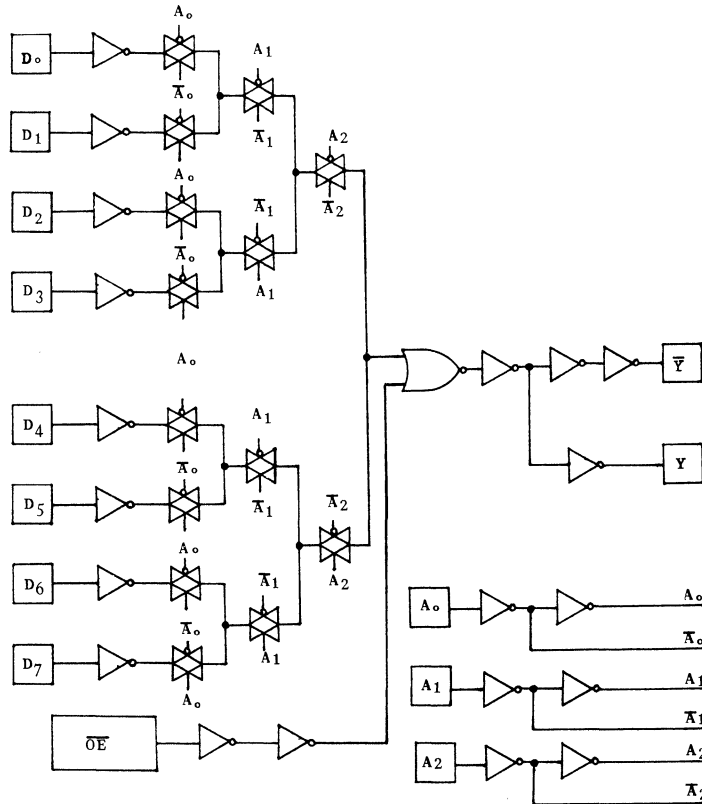
Truth Table

INPUTS				OUTPUTS	
SELECT			$\overline{OE}$	Y	$\overline{Y}$
A2	A1	A0			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level,   L = Low Level,   X = Don't Care
D0, D1,.....D7 = The Level of the Respective D Input

US74HCT153 ⚡ CMOS

DUAL 4-INPUT MULTIPLEXER

Preliminary

Features

- ■ **Wide Power Supply Range**   5V±10% For 74HCT
- ■ **Typical Propagation Delay**   27ns
- ■ **Low Quiescent Current**   80μA Maximum
- ■ **Low Input Current**   1μA Maximum
- ■ **Fanout of 10 LS-TTL Loads**   Normal Driving
- ■ **HCT Compatible With LS-TTL Outputs**   No pull up resistor required

Pin Configuration
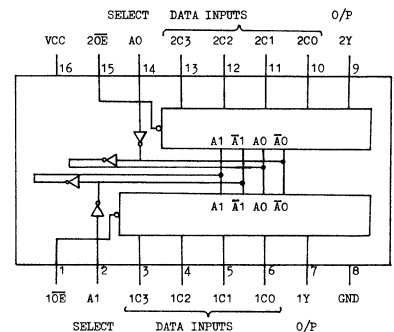
Description

This 4-to-1 line multiplexer is fabricated with Oxide Isolated Silicon Gate CMOS Process. It has the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads, and is functionally as well as pinout compatible with the standard LS-TTL type. HCT has level conversion which features LS-TTL input voltage level compatibility.

Information on the data inputs of each multiplexer is selected by the A0 and A1 inputs, and is presented on the Y ouputs. Each multiplexer possesses a $\overline{OE}$ inputs which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $|I_{OUT}| \leq 20\mu A$	V_{CC} = 4.5V	2	V
			V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level Input Voltage	V_{OUT} = 0.1V or V_{CC}-0.1V $|I_{OUT}| \leq 20\mu A$	V_{CC} = 4.5V	0.8	V
			V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	8.0	μA
			T_A = 85°C	80.0	μA
			T_A = 125°C	160.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

V_{CC} + 5.0V, T_A = 25°C, t_r =t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNIT
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select A0 or A1 to Y	C_L = 15pF C_L = 50pF	26 29	33 35	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{OE}$ to Y	C_L = 15pF C_L = 50pF	19 21	24 27	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Data to Y	C_L = 15pF C_L = 15pF	20 22	25 28	ns ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE)	(per package)	90		pF

NOTE: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit
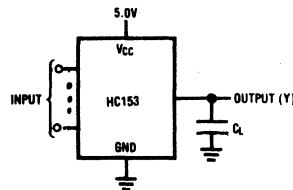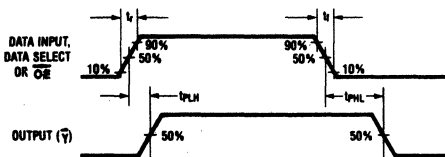
Logic Diagram
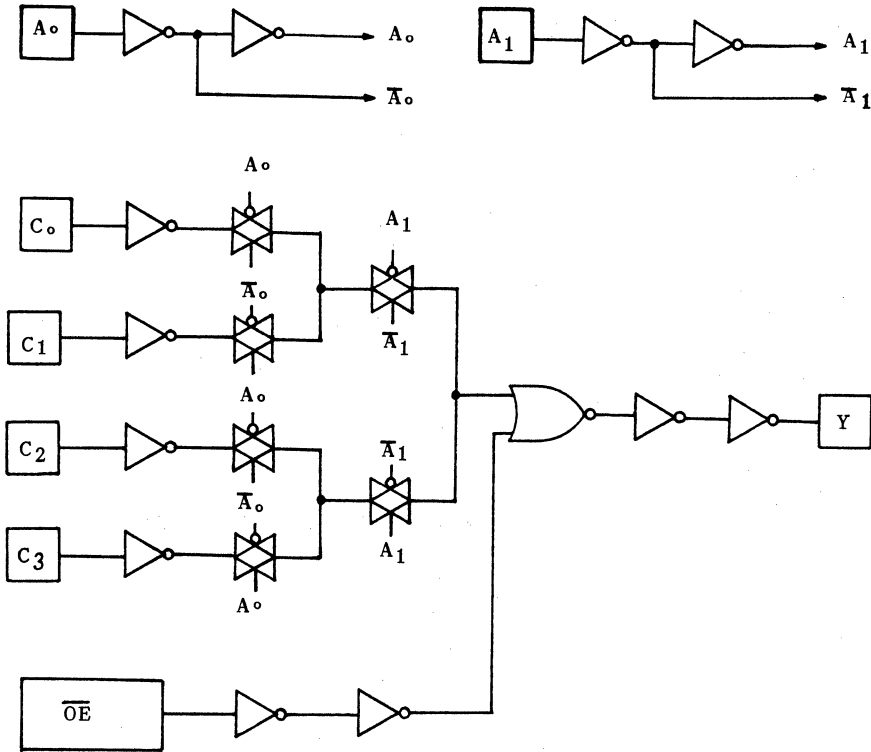
Truth Table

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
A0	A1	C0	C1	C2	C3	$\overline{OE}$	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = High Level,   L = Low Level,   X = Don't Care

UNIVERSAL SEMICONDUCTOR INC.

US74HCT157/158 ⊘ CMOS

QUAD 2-INPUT MULTIPLEXER

Preliminary

Features

- Wide Power Supply Range — 5V±10% For 74HCT
- Typical Propagation Delay — 18ns Data to Output
- Low Quiescent Current — 80μA Maximum
- Low Input Current — 1μA Maximum
- Fanout of 10 LS-TTL Loads — Normal Driving
- HCT Compatible With LS-TTL Outputs — No pull up resistor required

Pin Configuration

Description

These high speed QUAD 2-to-1 LINE DATA SELECTOR/MULTIPLEXER utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. All inputs are buffered and have static discharge protection by internal diodes clamped to V_{CC} and ground. These devices are functionally as well as pinout compatible with the standard 74LS logic family, and feature LS-TTL input voltage levels.

These devices each consist of four 2-input digital multiplexer with common select and Output Enable inputs. On the US74HCT157, when the OE input is at logical '0' the four outputs assume the values as selected from the inputs. When the OE is at a logical '1' outputs assume logical '0'. The US74HCT158 operates in the same manner, except that its ouput are inverted. Select decoding is done internally resulting in a single select only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	8.0	μA
			T_A = 85°C	80.0	μA
			T_A = 125°C	160.0	μA

UNIVERSAL SEMICONDUCTOR INC.

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	TYP	GUARANTEED LIMIT	UNITS
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 15pF C_L = 50pF	16 18	24 28	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output	C_L = 15pF C_L = 50pF	16 18	24 28	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{OE}$ to Output	C_L = 15pF C_L = 50pF	14 16	20 25	ns ns
C_{IN}	Maximum Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE)	(per multiplexer)	35		pF

NOTE: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

⑦CMOS
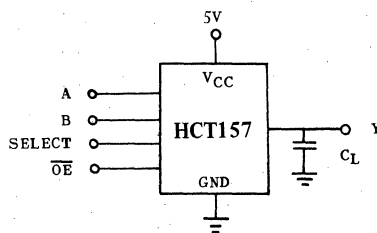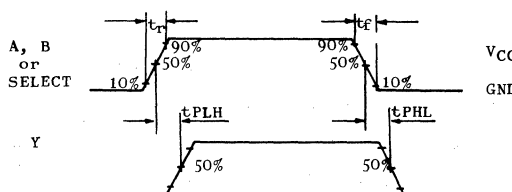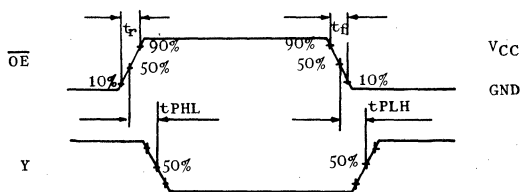
Logic Diagram
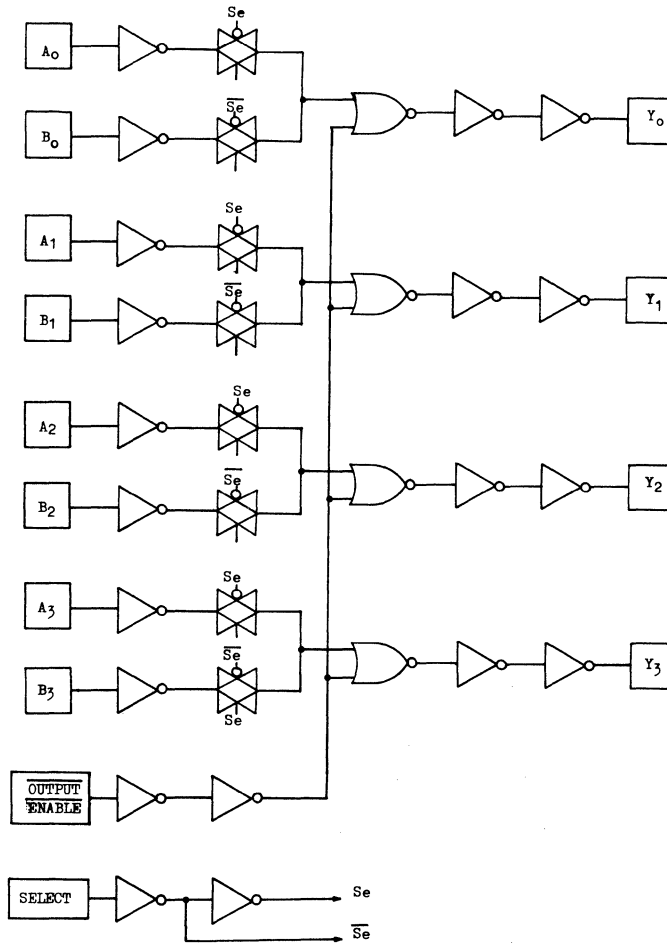
US74HCT158 has the same circuit as HCT157 except that the outputs are inverted.

Truth Table

INPUT				OUTPUT	
OE	SELECT	A	B	157	158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level,   L = Low Level,   X = Don't Care

UNIVERSAL SEMICONDUCTOR INC.

US74HCT266 ⚡CMOS

QUAD 2-INPUT EXCLUSIVE NOR GATE

Preliminary

Features

■ Wide Power Supply Range ... 5V±10% For 74HCT

■ Typical Propagation Delay ... 12ns

■ Low Quiescent Current ... 20µA Maximum

■ Low Input Current ... 1µA Maximum

■ Fanout of 10 LS-TTL Loads ... Normal Driving

■ HCT Compatible With LS-TTL Outputs ... No pull up resistor required

Pin Configuration and Truth Table
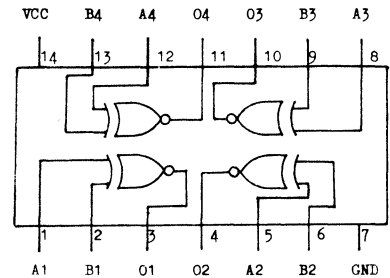
INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$$Y = \overline{A + B} = AB + \overline{A}\,\overline{B}$$

Description

Universal US74HCT High Speed CMOS series utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. HCT components have buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT features both LS-TTL input voltage levels, CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

UNIVERSAL SEMICONDUCTOR INC.

Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max limits apply across the whole operating temperature range unless otherwise specified)

| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND	T_A = 25°C	2	μA
		I_{OUT} = 0μA	T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL}	Maximum Propagation Delay Time	C_L = 15pF	12	20	ns
/ t_{PLH}	Output High to Low/ Output Low to High	C_L = 50pF	15	23	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	20		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns

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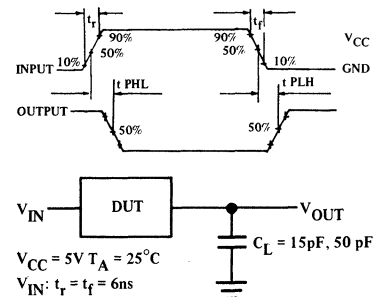
US74HCT4002 ⚡ CMOS

DUAL 4-INPUT NOR GATE

Preliminary

Features

- Wide Power Supply Range   5V±10% For 74HCT
- Typical Propagation Delay   10ns
- Low Quiescent Current   20μA Maximum
- Low Input Current   1μA Maximum
- Fanout of 10 LS-TTL Loads   Normal Driving
- HCT Compatible With LS-TTL Outputs   No pull up resistor required

Pin Configuration

TOP VIEW
$Y = A + B + C + D$

Description

Universal US74HCT4002 Nor Gates Utilize Oxide Isolated Silicon Gate CMOS Process to achieve operating speeds similar to LS-TTL gates with low power consumption of standard CMOS integrated circuits. All gates have the ability to drive 10 LS-TTL loads, as well as buffered inputs with discrete inverters that eliminate the dependence of the switching characteristic on the level of other inputs. All inputs have also static discharge protection by internal diodes clamped to V_{CC} and ground. HCT components feature both LS-TTL input voltage level and CMOS input compatibility, and are functionally as well as pinout compatible with the standard TTL (LS) logic family. HCT may be used as a level converter for interfacing LS-TTL to High Speed CMOS.

Absolute Maximum Ratings (Note 1)

DC Supply Voltage (V_{CC})	-0.5 to +7.0V
DC Input or Output Voltage (V_{IN}, V_{OUT})	-0.5 to V_{CC}+0.5V
DC Current Drain, per pin, any output (I_{OUT})	±25mA
DC Current Drain, per pin, V_{CC} or GND (I_{CC})	±50mA
Storage Temperature (T_{STG})	-65°C to +150°C
Power Dissipation (P_D) (NOTE 2)	500mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

NOTE 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

NOTE 2: Power Dissipation Temperature Derating Plastic "N" Package: -12mW/°C from 65 to 85°C

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Operating Conditions

OPERATING CONDITIONS	MIN	MAX	UNITS
DC Supply Voltage (V_{CC}) 74HCT	4.5	5.5	V
DC Input or Output (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature (T_A)	-40	+85	°C
Input Rise & Fall Times (t_r, t_f) at 4.5V	0	500	ns

DC Electrical Characteristics

V_{CC} + 5.0V 5V ± 10% (Min./Max. limits apply across the whole operating temperature range unless otherwise specified)

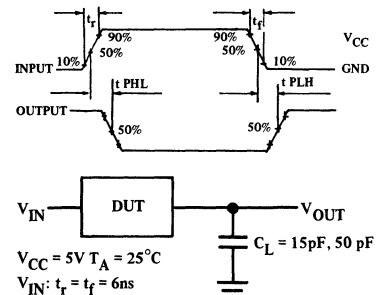| SYMBOL	PARAMETER	CONDITIONS		GUARANTEED LIMIT	UNITS
V_{IH}	Minimum High Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	2	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	2	V
V_{IL}	Maximum Low Level	V_{OUT} = 0.1V or V_{CC}-0.1V	V_{CC} = 4.5V	0.8	V
	Input Voltage	$|I_{OUT}| \leq 20\mu A$	V_{CC} = 5.5V	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		V_{CC}-0.05	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{CC} or GND $|I_{OUT}| \leq 20\mu A$		0.05	V
I_{OH}	Minimum High Level Output Current	V_{IN} = V_{CC} or GND V_{OUT} = V_{CC}-0.8V		-4.0	mA
I_{OL}	Minimum Low Level Output Current	V_{IN} or GND V_{OUT} = 0.4V		4.0	mA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±1.0	μA
I_{CC}	Maximum Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA	T_A = 25°C	2	μA
			T_A = 85°C	20	μA
			T_A = 125°C	40	μA

AC Electrical Characteristics

V_{CC} = 5.0V, T_A = 25°C, t_r = t_f = 6ns, (unless otherwise specified)

SYM-BOL	PARAMETER	CONDITIONS	TYP.	GUARANTEED LIMIT	UNITS
t_{PHL} / t_{PLH}	Maximum Propagation Delay Time Output High to Low/ Output Low to High	C_L = 15pF	14	20	ns
		C_L = 50pF	16	24	ns
C_{IN}	Input Capacitance		5	10	pF
C_{PD}	Power Dissipation Capacitance (NOTE 3)	(per gate)	25		pF

NOTE 3: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}, and the no load dynamic current consumption. I_S = C_{PD} V_{CC} f + I_{CC}.

Switching Time Waveforms and AC Test Circuit

V_{CC} = 5V T_A = 25°C
V_{IN}: t_r = t_f = 6ns
C_L = 15pF, 50 pF

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