SMC®
STANDARD
MICROSYSTEMS
CORPORATION

FDC37C78

Floppy Disk Controller

FEATURES

- 3.3/5 Volt Operation
- Intelligent Auto Power Management
- 2.88MB FDC37C78 Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMC's Proprietary 82077AA Compatible Core
  - Supports Two Floppy Drives Directly
  - Supports Vertical Recording Format
  - 16 Byte Data FIFO
  - 100% IBM® Compatibility
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA option
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
- Enhanced Digital Data Separator
  - 2 Mbps (Only Available When V_{CC} = 5V), 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- 48 pin TQFP Package

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GENERAL DESCRIPTION

The SMC FDC37C78 Floppy Disk Controller utilizes SMC's proven SuperCell technology for increased product reliability and functionality. The FDC37C78 is optimized for motherboard applications. The FDC37C78 supports both 1 Mbps and 2 Mbps data rates and vertical vertical recording operation at 1 Mbps Data Rate.

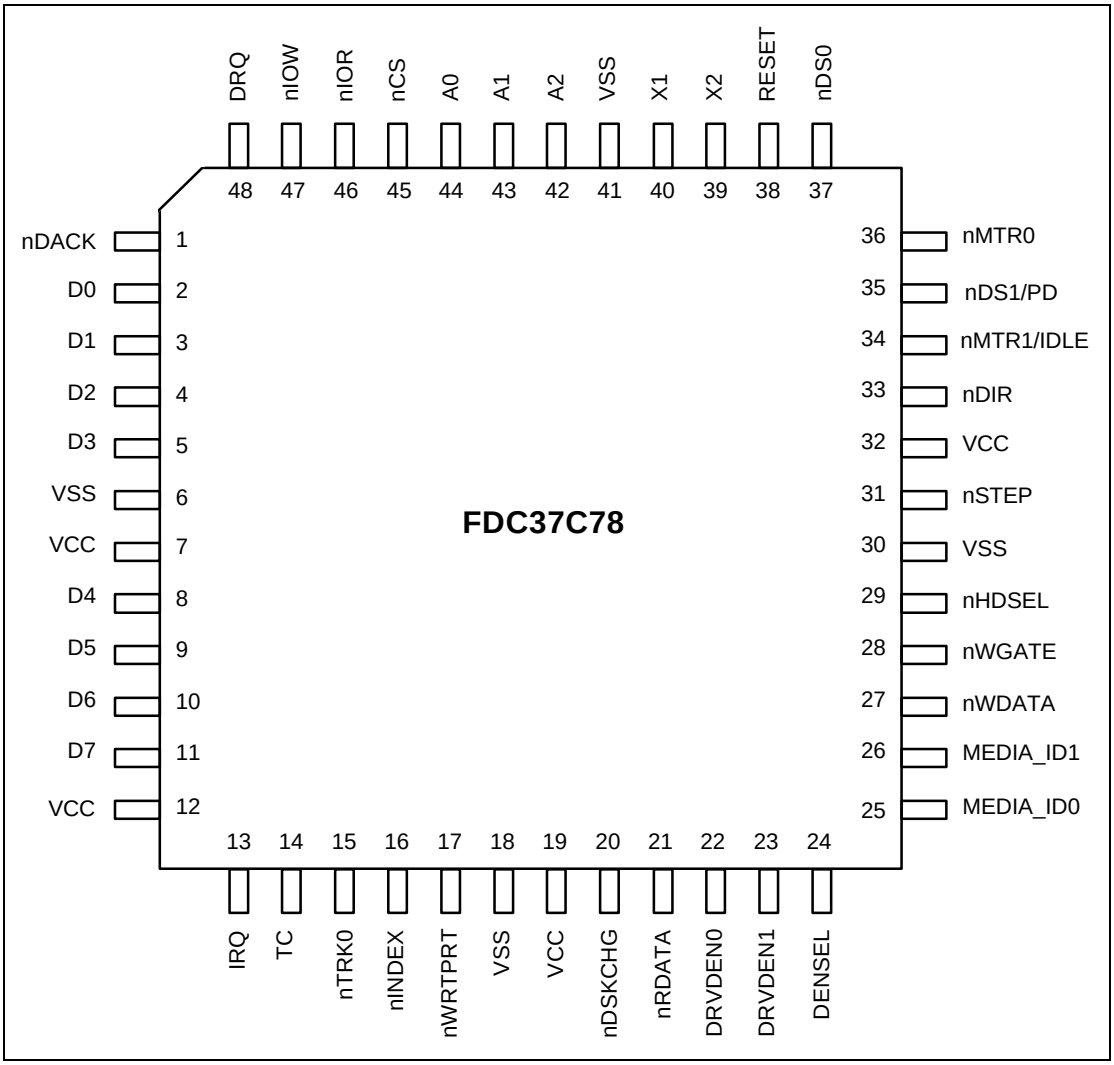
The FDC37C78 incorporates SMC's true CMOS 765B floppy disk controller, advanced digital data separator, 16 byte data FIFO, on-chip 12 mA bus drivers and two floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology, allowing for ease of testing and use.

The FDC37C78 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C78 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of the key floppy disk controller functions.

The FDC37C78 does not require any external filter components, and is, therefore easy to use and offers lower system cost and reduced board area. The FDC37C78 is software and register compatible with SMC's proprietary 82077AA core.

PIN CONFIGURATION



FDC37C78 PIN OUT

FDC37C78 48 Pin FDC

PIN #	NAME	PIN #	NAME
1	nDACK	25	MEDIA_ID0
2	D0	26	MEDIA_ID1
3	D1	27	nWDATA
4	D2	28	nWGATE
5	D3	29	nHDSEL
6	VSS	30	VSS
7	VCC	31	nSTEP
8	D4	32	VCC
9	D5	33	nDIR
10	D6	34	nMTR1/IDLE
11	D7	35	nDS1/PD
12	VCC	36	nMTR0
13	IRQ	37	nDS0
14	TC	38	RESET
15	nTRK0	39	X2
16	nINDEX	40	X1
17	nWRTPRT	41	VSS
18	VSS	42	A2
19	VCC	43	A1
20	nDSKCHG	44	A0
21	nRDATA	45	nCS
22	DRVDEN0	46	nIOR
23	DRVDEN1	47	nIOW
24	DENSEL	48	DRQ

Note: “n” denotes active low signal.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
HOST PROCESSOR INTERFACE				
2-5, 8-11	Data Bus 0-7	D0-D7	I/O12	The data bus connection used by the host microprocessor to transmit data to and from the chip. These pins are in a high-impedance state when not in the output mode.
46	I/O Read	nIOR	I	This active low signal is issued by the host microprocessor to indicate a read operation.
47	I/O Write	nIOW	I	This active low signal is issued by the host microprocessor to indicate a write operation.
44-42	I/O Address	A0-A2	I	These host address bits determine the I/O address to be accessed during nIOR and nIOW cycles. These bits are latched internally by the leading edge of nIOR and nIOW.
48	DMA Request	DRQ	O12	This active high output is the DMA request for byte transfers of data between the host and the chip. This signal is cleared on the last byte of the data transfer by the nDACK signal going low (or by nIOR going low if nDACK was already low as in demand mode).
1	n DMA Acknowledge	nDACK	I	An active low input acknowledging the request for a DMA transfer of data between the host and the chip. This input enables the DMA read or write internally.
14	Terminal Count	TC	I	This signal indicates to the chip that DMA data transfer is complete. TC is only accepted when nDACK is low. TC is active high.
13	Interrupt Request	IRQ	O12	The interrupt request from the logical device is output on the IRQ signal. Refer to the configuration registers for more information.
45	Chip Select Input	nCS	I	When enabled, this active low pin serves as an input for an external decoder circuit which is used to qualify address lines above A2.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
38	Reset	RESET	IS	This active high signal resets the chip and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset.
FLOPPY DISK INTERFACE				
21	Read Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
27	Write Data	nWDATA	OD20	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
29	Head Select	nHDSEL	OD20	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
33	Direction Control	nDIR	OD20	This high current low active output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
31	Step Pulse	nSTEP	OD20	This active low high current driver issues a low pulse for each track-to-track movement of the head.
20	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
22, 23	DRVDEN 0, DRVDEN 1	DRVDEN0, DRVDEN1	OD20	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
24	Density Select	DENSEL	OD20	Indicates whether a low (250/300 Kb/s) or high (500 Kb/s) data rate has been selected. This is determined by the IDENT bit in Configuration Register 3.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
25, 26	Media ID0, Media ID1	MEDIA_ID0, MEDIA_ID1	I	In Floppy Enhanced Mode 2 - These bits are the Media ID 0,1 inputs. The value of these bits can be read as bits 6 and 7 of the Floppy Tape Register.
28	Write Gate	nWGATE	OD20	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
15	Track 0	nTRK0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
16	Index	nINDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
17	nWrite Protected	nWRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
36	nMotor On 0	nMTR0	OD20	This active low open drain output selects motor drive 0.
37	nDrive Select 0	nDS0	OD20	This active low open drain output selects drive 0.
34	nMotor On 1 Idle	nMTR1 IDLE	OD20 OD20	This active low open drain output select motor drive 0. This pin indicates that the part is in the IDLE state and can be powered down. Whenever the part is in this state, IDLE pin is active high. If the part is powered down by the Auto Powerdown Mode, IDLE pin is set high and if the part is powered down by setting the DSR POWERDOWN bit (direct), IDLE pin is set low.
35	nDrive Select 1 Powerdown	nDS1 PD	OD20 OD20	This active low open drain output selects drive 0. This pin is active high whenever the part is in powerdown state, either via DSR POWERDOWN bit (direct) or via the Auto Powerdown Mode. This pin can be used to disable an external oscillator's output.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
MISCELLANEOUS				
40	CLOCK 1	X1	ICLK	The external connection for a parallel resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
39	CLOCK 2	X2	OCLK	24 MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
7, 12, 19, 32	Power	V_{CC}		Positive Supply Voltage.
6, 18, 30, 41	Ground	GND		Ground Supply.

BUFFER TYPE DESCRIPTIONS

Note: These values are for 3.3V operation. See Operational Description for 3.3V/5V values.

BUFFER TYPE	DESCRIPTION
I/O12	Input/output. 12 mA sink; 6 mA source
O12	Output. 12 mA sink; 6 mA source
OD20	Open drain. 20 mA sink
OCLK	Output to external crystal
ICLK	Input to Crystal Oscillator Circuit (CMOS levels)
I	Input TTL compatible.
IS	Input with Schmitt Trigger

FUNCTIONAL DESCRIPTION

FDC37C78 REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the FDC37C78 immediately after power up. Some addresses are used to access more than one register.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C78 through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide.

Table 1 - FDC37C78 Block Addresses

ADDRESS	BLOCK NAME	NOTES
+0, +1	Configuration	Write only; Note 1, 2
Base +0,1	Floppy Disk	Read only; Disabled at power up; Note 2
Base +[2:5, 7]	Floppy Disk	Disabled at power up; Note 2

Note 1: Configuration registers can only be modified in configuration mode, refer to the configuration register description for more information. Access to status registers A and B of the floppy disk is disabled in configuration mode.

Note 2: The FDC must be enabled in the configuration registers before accessing the registers.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC37C78 is compatible to the 82077AA using SMC's proprietary floppy disk controller core.

FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The Floppy Disk Controller contains eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the FDC description assumes the Base I/O Address is 3F0.

Table 2 - Status, Data and Control Registers

BASE I/O ADDRESS		REGISTER	
+0		Reserved	
+1		Reserved	
+2	R/W	Digital Output Register	DOR
+3	R/W	Tape Drive Register	TSR
+4	R	Main Status Register	MSR
+4	W	Data Rate Select Register	DSR
+5	R/W	Data (FIFO)	FIFO
+6		Reserved	
+7	R	Digital Input Register	DIR
+7	W	Configuration Control Register	CCR

DIGITAL OUTPUT REGISTER (DOR)

Address 3F2 READ/WRITE

The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and contains a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT

These two bit a are binary encoded for the four drive selects DS0-DS3, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET

A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

Writing this bit to logic "1" will enable the DRQ, nDACK, TC and IRQ outputs. This bit being a logic "0" will disable the nDACK and TC inputs, and hold the DRQ and IRQ outputs in a high impedance state. This bit is a logic "0" after a reset and in these modes.

BIT 4 MOTOR ENABLE 0

This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1

This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2

This bit controls the MTR2 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 7 MOTOR ENABLE 3

This bit controls the MTR3 disk interface output. A logic "1" in this bit causes the output to go active.

Table 3 - Drive Activation Values

DRIVE	DOR VALUE
0	1CH
1	2DH
2	4EH
3	8FH

TAPE DRIVE REGISTER (TDR)

Address 3F3 READ/WRITE

This register is included for 82077 software compatability. The robust digital data separator used in the FDC37C78 does not require its characteristics modified for tape support. The contents of this register are not used internal to the device. The TDR is unaffected by a software reset. Bits 2-7 are tri-stated when read in this mode.

Table 4- Tape Select Bits

TAPE SEL1	TAPE SEL2	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Table 5 - Internal 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR 3	nMTR 2	nMTR 1	nMTR 0
X	X	X	1	0	0	1	1	1	0	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	X	1	X	0	1	1	1	0	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 5	nBIT 4

Table 6 - Internal 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)				MOTOR ON OUTPUTS (ACTIVE LOW)			
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS3	nDS2	nDS1	nDS0	nMTR 3	nMTR 2	nMTR 1	nMTR 0
X	X	X	1	0	0	1	1	0	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	X	1	X	0	1	1	1	1	0	nBIT 7	nBIT 6	nBIT 4	nBIT 5
X	1	X	X	1	0	1	0	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
1	X	X	X	1	1	0	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5
0	0	0	0	X	X	1	1	1	1	nBIT 7	nBIT 6	nBIT 4	nBIT 5

Table 7 - External 2 to 4 Drive Decode - Normal

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	0	1	0
X	X	1	X	0	1	0	1	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	0	1	1
X	X	0	X	0	1	0	1	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1

Table 8 - External 2 to 4 Drive Decode - Drives 0 and 1 Swapped

DIGITAL OUTPUT REGISTER						DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 7	Bit 6	Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	X	X	1	0	0	0	1	1	0
X	X	1	X	0	1	0	0	1	0
X	1	X	X	1	0	1	0	1	0
1	X	X	X	1	1	1	1	1	0
X	X	X	0	0	0	0	1	1	1
X	X	0	X	0	1	0	0	1	1
X	0	X	X	1	0	1	0	1	1
0	X	X	X	1	1	1	1	1	1

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are a high impedance.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	Tri-state	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Media ID1	Media ID0	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

For this mode, DRATE0 and DRATE1 pins are inputs, and these inputs are gated into bits 6 and 7 of the 3F3 register. These two bits are not affected by a hard or soft reset.

BIT 7 Media ID 1; Read Only (See Table 9a)

BIT 6 Media ID 0; Read Only (See Table 9b)

BITS 5 and 4 Drive Type ID - These Bits reflect two of the bits of configuration register 6; which two bits depends on the last drive selected in the Digital Output Register (3F2). (See Table 11)

BITS 3 and 2 Floppy Boot Drive - These bits reflect the value of configuration register 7 bits 1, 0. Bit 3 = CR7 Bit DB1. Bit 2 = CR7 Bit DB0.

Bits 1 and 0 - Tape Drive Select (READ/WRITE). Same as in Normal and Enhanced Floppy Mode. 1.

Table 9a

	Media ID1	
Pin 26	Bit 7	
	CR7-DB3=0	CR7-DB3=1
0	0	1
1	1	0

Table 9b

	Media ID0	
Pin 25	Bit 6	
	CR7-DB2=0	CR7-DB2=1
0	0	1
1	1	0

Table 9c - Drive Type ID

Digital Output Register		**Register 3F3 - Drive Type ID**	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	CR6 - Bit 1	CR6 - Bit 0
0	1	CR6 - Bit 3	CR6 - Bit 2
1	0	CR6 - Bit 5	CR6 - Bit 4
1	1	CR6 - Bit 7	CR6 - Bit 6

DATA RATE SELECT REGISTER (DSR)

Address 3F4 WRITE ONLY
This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and Microchannel applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 13 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 12 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. this starting track number can be changed by the configure command.

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into Manual Low Power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.

Table 10 - Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY
111	0.00 ns-DISABLED
001	41.67 ns
010	83.34 ns
011	125.00 ns
100	166.67 ns
101	208.33 ns
110	250.00 ns
000	Default (See Table 14)

Table 11 - Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL (1)		DRATE (2)	
DRT1	DRT0	SEL1	SEL0	MFM	FM	IDENT=1	IDENT=0	1	2
0	0	1	1	1Meg	---	1	0	1	1
0	0	0	0	500	250	1	0	0	0
0	0	0	1	300	150	0	1	0	1
0	0	1	0	250	125	0	1	1	0
0	1	1	1	1Meg	---	1	0	1	1
0	1	0	0	500	250	1	0	0	0
0	1	0	1	500	250	0	1	0	1
0	1	1	0	250	125	0	1	1	0
1	0	1	1	1Meg	---	1	0	1	1
1	0	0	0	500	250	1	0	0	0
1	0	0	1	2Meg	---	0	1	0	1
1	0	1	0	250	125	0	1	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: This is for DENSEL in normal mode.
Note 2: This is for DRATE0, DRATE1 when Drive Opt are 00.

Table 12 - Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps*	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

*The 2 Mbps data rate is only available if V_{CC} = 5V.
*The 2 Mbps data rate is only available if V_{CC} = 5V.

MAIN STATUS REGISTER

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. NO delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	DRV3 BUSY	DRV2 BUSY	DRV1 BUSY	DRV0 BUSY

BIT 0 - 3 DRVx BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM

Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

DATA REGISTER (FIFO)

Address 3F5 READ/WRITE

All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 13 gives several examples of the delays with a FIFO. The data is based upon the following formula:

$$\text{Threshold \# } x \left| \frac{1}{\text{DATA RATE}} \text{ x } 8 \right| - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters must be sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 13- FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps* DATA RATE
1 byte	1 x 4 µs - 1.5 µs = 2.5 µs
2 bytes	2 x 4 µs - 1.5 µs = 6.5 µs
8 bytes	8 x 4 µs - 1.5 µs = 30.5 µs
15 bytes	15 x 4 µs - 1.5 µs = 58.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 µs - 1.5 µs = 6.5 µs
2 bytes	2 x 8 µs - 1.5 µs = 14.5 µs
8 bytes	8 x 8 µs - 1.5 µs = 62.5 µs
15 bytes	15 x 8 µs - 1.5 µs = 118.5 µs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 µs - 1.5 µs = 14.5 µs
2 bytes	2 x 16 µs - 1.5 µs = 30.5 µs
8 bytes	8 x 16 µs - 1.5 µs = 126.5 µs
15 bytes	15 x 16 µs - 1.5 µs = 238.5 µs

*The 2 Mbps data rate is only available if V_{CC} = 5V.

DIGITAL INPUT REGISTER (DIR)

Address 3F7 READ ONLY
This register is read-only.

	7	6	5	4	3	2	1	0
	DSK CHG							
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 will remain in a high impedance state during a read of this register.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable.

CONFIGURATION CONTROL REGISTER (CCR)

Address 3F7 WRITE ONLY

	7	6	5	4	3	2	1	0
							DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 13 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0" by the DOR and the DSR resets.

STATUS REGISTER ENCODING

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 14 - Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 15 - Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D*). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the IDX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

* D= Decimal

Table 16 - Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: 1. Read Data command - the FDC encountered a deleted data address mark. 2. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 17 - Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WP pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the RESET pin of the FDC37C78, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

RESET Pin (Hardware Reset)

The RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)

These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODE OF OPERATION

PC/AT mode - (IDENT high, MFM a "don't care")

The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (IRQ and DRQ can be hi Z), and TC and DENSEL become active high signals.

DMA TRANSFERS

DMA transfers are enabled with the Specify command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting nDACK and addresses need not be valid.

Note that if the DMA controller (i.e. 8237A) is programmed to function in verify mode, a pseudo read is performed by the FDC based only on nDACK. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled, the FDC can perform the above operation by using the new Verify command; no DMA operation is needed.

CONTROLLER PHASES

For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase

After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 18 for the command set descriptions.) These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase

All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by an IRQ or DRQ depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The IRQ pin and RQM bits in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The IRQ pin can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the IRQ pin and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The IRQ pin and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The IRQ pin and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The IRQ pin will also be deactivated if TC and nDACK both go inactive. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC activates the DDRQ pin when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller must respond to the request by reading data from the FIFO. The FDC will deactivate the DDRQ pin when the FIFO becomes empty. DRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOR, on the last byte, if no edge is present on nDACK). A data underrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

DMA Mode - Transfers from the Host to the FIFO

The FDC activates the DRQ pin when entering the execution phase of the data transfer commands. The DMA controller must respond by activating the nDACK and nIOW pins and placing data in the FIFO. DRQ remains active until the FIFO becomes full. DRQ is again set true when the FIFO has <threshold> bytes remaining in the FIFO. The FDC will also deactivate the DRQ pin when TC becomes true (qualified by nDACK), indicating that no more data is required. DRQ goes inactive after nDACK goes active for the last byte of a data transfer (or on the active edge of nIOW of the last byte, if no edge is present on nDACK). A data overrun may occur if DRQ is not removed in time to prevent an unwanted cycle.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC pin and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a hardware TC was received. The only difference between these implicit functions and TC is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of IRQ determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

COMMAND SET/DESCRIPTIONS

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 18 for explanations of the various symbols used. Table 19 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 18 - Description of Command Symbols

<table>
<tr><th>SYMBOL</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>C</td><td>Cylinder Address</td><td>The currently selected address; 0 to 255.</td></tr>
<tr><td>D</td><td>Data Pattern</td><td>The pattern to be written in each sector data field during formatting.</td></tr>
<tr><td>D0, D1, D2, D3</td><td>Drive Select 0-3</td><td>Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.</td></tr>
<tr><td>DIR</td><td>Direction Control</td><td>If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.</td></tr>
<tr><td>DS0, DS1</td><td>Disk Drive Select</td><td><table><tr><th>DS1</th><th>DS0</th><th>DRIVE</th></tr><tr><td>0</td><td>0</td><td>drive 0</td></tr><tr><td>0</td><td>1</td><td>drive 1</td></tr><tr><td>1</td><td>0</td><td>drive 2</td></tr><tr><td>1</td><td>1</td><td>drive 3</td></tr></table></td></tr>
<tr><td>DTL</td><td>Special Sector Size</td><td>By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.</td></tr>
<tr><td>EC</td><td>Enable Count</td><td>When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).</td></tr>
<tr><td>EFIFO</td><td>Enable FIFO</td><td>This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).</td></tr>
<tr><td>EIS</td><td>Enable Implied Seek</td><td>When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.</td></tr>
</table>

Table 18 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either tha DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is “00”, then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the “N’th” power) times 128. All values up to “07” hes are allowable. “07”H would equal a sector size of 16k. It is the user’s resposibility to not select combinations that are not possible with the drive.

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

Table 18 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode, interfacing to a DMA controller by means of the DRQ and nDACK signals.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

INSTRUCTION SET

Table 19 - Instruction Set

READ DATA										
PHASE	**R/W**	**DATA BUS**								**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERIFY									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

VERSION									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution for Each Sector Repeat:	W	C								Input Sector Parameters
	W	H								
	W	R								
	W	N								
										FDC formats an entire cylinder
Result	R	ST0								Status information after Command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

RECALIBRATE										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	——— ST0 ———								Status information at the end of each seek operation.
	R	——— PCN ———								

SPECIFY										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	—— SRT ——				—— HUT ——				
	W	——— HLT ———							ND	

SENSE DRIVE STATUS									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	——— ST3 ———								Status information about FDD

SEEK									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— NCN ———								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	— FIFOTHR —				
Execution	W	——— PRETRK ———								

RELATIVE SEEK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	RCN								

DUMPREG										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT					HUT			
	R	HLT							ND	
	R	SC/EOT								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	FIFOTHR				
	R	PRETRK								

READ ID									
PHASE	**R/W**	**DATA BUS**							**REMARKS**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution.
										Disk status after the Command has completed
	R	ST1								
	R	ST2								
	R	C								
	R	H								
	R	R								
	R	N								

PERPENDICULAR MODE									
PHASE	R/W	DATA BUS							REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - fdc goes into Stand-by State)
Result	R	———— ST0 ————								ST0 = 80H

LOCK										
PHASE	R/W	DATA BUS								REMARKS
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

NOTE: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

DATA TRANSFER COMMANDS

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it will be reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data

A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of TC, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 20 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 20 - Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/ sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 21.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 22 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 22, the C or R value of the sector address is automatically incremented (see Table 24).

Table 21 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 22 - Skip Bit vs Read Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 23 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 23, the C or R value of the sector address is automatically incremented (see Table 26).

Table 23 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a "1" if there is no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the IDX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 24 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented .

Write Data

After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.

The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) bit
- ND (No Data) bit
- Head Load, Unload Time Interval
- ID information when the host terminates the command
- Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data

This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, TC (pin 25) cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 24 and Table 25 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 25 - Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT ≤ # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

NOTE: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the IDX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the IDX pin again and it terminates the command.

Table 26 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						22x 4E	12x 00	3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM	DATA	CRC	GAP3	GAP 4b
40x FF	6x 00	FC	26x FF	6x 00	FE						11x FF	6x 00	FB or F8				

PERPENDICULAR FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		CYL	HD	SEC	NO	CRC	GAP2	SYNC	DATA AM		DATA	CRC	GAP3	GAP 4b
80x 4E	12x 00	3x C2	FC	50x 4E	12x 00	3x A1	FE						41x 4E	12x 00	3x A1	FB F8				

Table 26 - Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
NOTE: All values except sector size are in hex.

CONTROL COMMANDS

Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID

The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate

This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTR0 pin from the FDD. As long as the nTR0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTR0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once.

Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek

The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.

PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated.

During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.

Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command
3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command be issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero.

Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status

An interrupt signal on IRQ pin is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command
2. End of Seek, Relative Seek, or Recalibrate command
3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

Table 27 - Interrupt Identification

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status

Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify

The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 28. The values are the same for MFM and FM.

Table 28 - Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signalled by the FDRQ pin. Non-DMA mode uses the RQM bit and the FINT pin to signal data transfers.

Configure

The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version

The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek

The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

DIR	ACTION
0	Step Head Out
1	Step Head In

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult

to keep track of with software without the Read ID command.

Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 31 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The format field shown on page 61 illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC as shown in Figure 4. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commnds between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive wil be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".

If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits (GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 29 - Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

ENHANCED DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

COMPATIBILITY

The FDC37C78 was designed with software compatibility in mind. It is a fully backwards-compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with PC/AT and PC/XT floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT compatible operating mode.

AUTO POWER MANAGEMENT

Power management capabilities are provided for the floppy disk. Two types of power management are provided; direct powerdown and auto powerdown.

Direct powerdown is controlled by the powerdown bit in the configuration registers. Auto Powerdown can be enabled by setting the Auto Powerdown Enable bit in the configluation registers.

FDC Power Management

Direct power management is controlled by bit 3 of Configuration Register 0(CR0). Refer to CR0 bit 3 for more information.

Auto Power Management is enabled by CR7 bit 7. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1. The motor enable pins of register DOR are inactive (zero).

2. The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).

3. The internal head unload timer must have expired.

4. The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met. During the countdown of the powerdown timer, any operation of read MSR or read/write data (FIFO) will reinitiate the timer.

Disabling the auto powerdown mode cancels the timer and holds the FDC37C78 out of auto powerdown.

DSR From Powerdown

If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

Wake Up From Auto Powerdown

If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC37C78 resumes operation as though it was never in powerdown. Besides activating the RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).

2. A read from the MSR register.

3. A read or write to the Data register.

Once awake, the FDC37C78 will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

Register Behavior

Table 30 reiterates the AT registers available. It also shows the type of access permitted. In order to maintain software transparency, access to all the registers must be maintained. As Table 30 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

Pin Behavior

The FDC37C78 is specifically designed for portable PC systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the FDC37C78 can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

System Interface Pins

Table 31 gives the state of the system interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged". Input pins are "Disabled" to prevent them from causing currents internal to the FDC37C78 when they have indeterminate input values.

Table 30 - PC/AT Available Registers

Base + Address	Available Registers	Access Permitted
	PC-AT	
Access to these registers DOES NOT wake up the part		
00H	----	R
01H	----	R
02H	DOR (1)	R/W
03H	---	---
04H	DSR (1)	W
06H	---	---
07H	DIR	R
07H	CCR	W
Access to these registers wakes up the part		
04H	MSR	R
05H	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part

Table 31 - State of System Pins in Auto Powerdown

System Pins	State in Auto Powerdown
Input Pins	
IOR	Unchanged
IOW	Unchanged
A[0:9]	Unchanged
D[0:7]	Unchanged
RESET	Unchanged
IDENT	Unchanged
DACK	Unchanged
TC	Unchanged
Output Pins	
IRQ	Unchanged (low)
DB[0:7]	Unchanged
FDRQ	Unchanged (low)

FDD Interface Pins

All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED. Pins used for local logic control or part programming are unaffected. Table 32 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 32 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD Pins	State in Auto Powerdown
Input Pins	
RDATA	Input
WP	Input
TRK0	Input
INDX	Input
DRV2	Input
DSKCHG	Input
Output Pins	
MOTEN[0:3]	Tristated
DS[0:3]	Tristated
DIR	Active
STEP	Active
WRDATA	Tristated
WE	Tristated
HDSEL	Active
DENSEL	Active
DRATE[0:1]	Active

CONFIGURATION

The configuration of the chip is programmable through software selectable configuration registers.

CONFIGURATION REGISTER ADDRESS
The Configuration Registers are located at address offset +0 and +1 with nCS active.

CONFIGURATION REGISTERS
The configuration registers are used to select programmable options of the chip. After power up, the chip is in the default mode. The default modes are identified in the Configuration Mode Register Description. To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode.
2. Configure the Configuration Registers.
3. Exit Configuration Mode.

Enter Configuration Mode
To enter the configuration mode, two writes in succession to port +0 with 55H data are required. If a write to another address or port occurs between these two writes, the chip does not enter the configuration mode. It is strongly recommended that interrupts be disabled for the duration of these two writes.

Configuration Mode
The chip contains configuration registers CR00-CR1F. These registers are accessed by first writing the number (0-1FH) of the desired register to port +0 and then writing or reading the configuration register through port +1.

Exit Configuration Mode
The configuration mode is exited by writing an AAH to port +0.

Programming Example
The following is an example of a configuration program in Intel 8086 assembly language and assumes that the base address is set to 3F0H.

```
;------------------------------.
; ENTER CONFIGURATION MODE    |
;------------------------------'
MOV   DX,3F0H
MOV   AX,055H      ;
CLI                ; disable interrupts
OUT   DX,AL
OUT   DX,AL
STI                ; enable i nterrupts
;------------------------------.
; CONFIGURE REGISTERS CR0-CRx |
;------------------------------'
MOV   DX,3F0H
MOV   AL,00H
OUT   DX,AL ; Point to CR0
MOV   DX,3F1H
MOV   AL,3FH
OUT   DX,AL ; Update CR0
;
MOV   DX,3F0H      ;
MOV   AL,01H
OUT   DX,AL ; Point to CR1
MOV   DX,3F1H
MOV   AL,9FH
OUT   DX,AL ; Update CR1
;
; Repeat for all CRx registers
;
;------------------------------.
; EXIT CONFIGURATION MODE     |
;------------------------------'
MOV   DX,3F0H
MOV   AX,0AAH
OUT   DX,AL
```

Table 33 - Configuration Registers

Default		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
28H	CR00	Valid	Reserved	OSC	Reserved	FDC PWR	PDEN	Reserved	
90H	CR01	Lock CRx	Reserved			Reserved	Reserved	Reserved	
00H	CR02	Reserved	Reserved			Reserved	Reserved		
70H	CR03	Reserved	IDENT	MFM	DRVDEN 1	Reserved	Reserved	Enhanced FDC Mode 2	Reserved
00H	CR04	Reserved							
00H	CR05	Reserved	EXTx4	DRV 0X1	DEN SEL		DMA Mode	Reserved	
FFH	CR06	Floppy Drive D		Floppy Drive C		Floppy Drive B		Floppy Drive A	
00H	CR07	Auto Power Management				Media ID Polarity		Floppy Boot Drive	
00H	CR08	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
00H	CR09	Reserved		Reserved			Reserved	Reserved	Reserved
00H	CR0A	Reserved				Reserved			
00H	CR0B	FDD3-DRTx		FDD2-DRTx		FDD1-DRTx		FDD0-DRTx	
00H	CR0C	Reserved							
78H	CR0D	Device ID/ 78H							
00H	CR0E	Device Revision/00							
00H	CR0F	Test	Test	Test	Test	Test	Test	Test	Test
00H	CR10	Test	Test	Test	Test	Test	Test	Test	Test
00H	CR11	Test	Test	Test	Test	Test	Test	Test	Test
00H	CR12-CR1E	Reserved							
00H	CR1F	**FDD3-DTx**		**FDD2-DTx**		**FDD1-DTx**		**FDD0-DTx**	

Configuration Register Description

The configuration registers consist of the Configuration Select Register (CSR) and Configuration Registers CR00 -CR1F The configuration select register is written to by writing to port +0. The Configuration Registers CR00; CR1F are accessed by reading or writing to port +1.

Configuration Select Register (CSR)

This register can only be accessed when the chip is in the Configuration Mode. This register, located at port +0, must be initialized upon entering the Configuration Mode before the configuration registers can be accessed and is used to select which of the Configuration Registers are to be accessed at port +1.

Configuration Registers CR00 -CR1F

These registers are set to their default values at power up and are not affected by RESET (except where explicitly defined that a hardware reset causes that bit to be reset to default). They are accessed at port +1. Refer to the following descriptions for the function of each configuration register.

CR00
This register can only be accessed when the chip is in the Configuration Mode and after the CSR has been initialized to 00H. The default value of this register after power up is 28H.

Table 34 - CR00

BIT NO.	BIT NAME	DESCRIPTION
0:1	Reserved	Read only. Read as 0
2	PDEN	Power Down and Idle enable. 0 nDS1pin=nDS1, nMTR1pin=nMTR1 1 nDS1pin=Power Down, nMTR1pin=Idle
3	FDC Power	A high level on this bit, supplies power to the FDC (default). A low level on this bit puts the FDC in low power mode.
4, 6	Reserved	Read only. A read returns bits 4 and 6 as a 0.
5	OSC	Oscillator Control. 0 = Oscillator OFF 1 = Oscillator ON (default)
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

CR01
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 01H. The default value of this register after power up is 90H.

Table 35 - CR01

BIT NO.	BIT NAME	DESCRIPTION
0,1,2,3	Reserved	Read Only. A read returns a 0.
4	Reserved	Read Only. A read returns a 1.
5,6	Reserved	Read Only. A read returns a 0.
7	Lock CRx	A high level on this bit enables the reading and writing of CRxx registers (Default). A low level on this bit disables the reading and writing of all CRxx registers. Once set to 0, this bit can only be set to 1 by a hard reset or power-up reset.

CR02
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 02H. The default value of this register after power up is 00H.

Table 36 - CR02

BIT NO.	BIT NAME	DESCRIPTION
0:7	Reserved	Read Only. A read returns a 0.

CR03
This register can only be accessed in the Configuration Mode and the CSR has been initialized to 03H. The default value after power up is 70H.

Table 37 - CR03

BIT NO.	BIT NAME	DESCRIPTION		
0	Reserved	Reserved - Read as zero		
1	Enhanced Floppy Mode 2	Bit 1	Floppy Mode - Refer to the description of the TAPE DRIVE REGISTER (TDR) for more information on these modes.	
		0	NORMAL Floppy Mode (Default)	
		1	Enhanced Floppy Mode 2 (OS2)	
2	Reserved	Reserved - Read as zero		
3	Reserved	Reserved - Read as zero		
4	DRVDEN1	0 DRVDEN 1 output as per DRVDEN table 1 DRVDEN 1 pin is tri-state (default)		
5	MFM	IDENT is used in conjunction with MFM to define the interface mode of operation.		
6	IDENT	**IDENT** 1 1 0 0	**MFM** 1 0 1 0	**MODE** AT Mode (Default) Reserved Reserved Reserved
7	Reserved	Reserved - Read as zero		

CR04
This register can only be accessed in the Configuration Mode and the CSR has been initialized to 04H. The default value after power up is 00H.

Table 38 - CR04

BIT NO.	BIT NAME	DESCRIPTION
0:7	Reserved	Reserved - Read as zero

CR05
This register can only be accessed in the Configuration Mode and the CSR has been initialized to 05H. The default value after power up is 00H.

Table 39 - CR05- Floppy Disk Extended Setup Register

BIT NO.	BIT NAME	DESCRIPTION		
0,1	Reserved	Read Only. A read returns a 0.		
2	FDC DMA Mode	0=(default) Burst mode is enabled for the FDC FIFO execution phase data transfers. 1=Non-Burst mode enabled. The FDRQ and FIRQ pins are strobed once for each byte transferred while the FIFO is enabled.		
4,3	DenSel	Bit 4	Bit 3	Densel output
		0	0	Normal (Default)
		0	1	Reserved
		1	0	1
		1	1	0
5	Swap Drv 0,1	A high level on this bit, swaps drives and motor sel 0 and 1 of the FDC. A low level on this bit does not (Default).		
6	EXTx4	External 4 drive support: 0=Internal 2 drive decoder (default). 1=External 4 drive decoder (External 2 to 4 decoder required).		
7	Reserved	Read Only. A read of this bit returns a 0		

CR06
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 06H. The default value of this register after power up is FFH. This register holds the floppy disk drive types for up to four floppy disk drives.

CR07
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 07H. The default value of this register after power up is 00H. This register holds the value for the auto power management, polarity of the media ID bits and floppy boot drive information.

Table 40 - CR07

BIT NO.	BIT NAME	DESCRIPTION
0,1	Floppy Boot	This bit is used to define the boot floppy. 0 = Drive A (default) 1 = Drive B
2	Media ID0 Polarity	0 = Non-invert 1 = Invert
3	Media ID1 Polarity	0 = Non-invert 1 = Invert
4:6	Reserved	Read as 0.
7	Floppy Disk Enable	This bit controls the AUTOPOWER DOWN feature of the Floppy Disk. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.

CR08
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 08H. The default value of this register after power up is 00H. This register is read only.

CR09
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 09H. The default value of this register after power up is 00H. This register is read only.

CR0A
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 0AH. The default value of this register after power up is 00H. This register is read only.

CR0B
This register can only be ac1cessed in the Configuration Mode and after the CSR has been initialized to 0BH. The default value of this register after power up is 00H. This register indicates the data rate table used for each drive. Refer to CR1F for Drive Type register.

Table 41 - CR0B

FDD3		FDD2		FDD1		FDD0	
D7	D6	D5	D4	D3	D2	D1	D0
DRT1	DRT0	DRT1	DRT0	DRT1	DRT0	DRT1	DRT0

CR0C
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 0CH. The default value of this register after power up is 00H. This register is reserved.

CR0D
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 0DH. This register is read only. This is the Device ID. The default value of this register after power up is 78H.

CR0E
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 0EH. This register is read only. The default value of this register after power up is 00H. This is used to identify the chip revision level.

CR0F
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 0FH. The default value of this register after power up is 00H. This is a test register and must be left as 00H.

Table 42 - CR0F

BIT NO.	BIT NAME	DESCRIPTION
0:7	Reserved	Reserved For Test

CR10
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 10H. The default value of this register after power up is 00H. This is a test register and must be left as 00H.

Table 43 - CR10

BIT NO.	BIT NAME	DESCRIPTION
0:7	Reserved	Reserved For Test

CR11
This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 11H. The default value of this register after power up is 00H. This is a test register and must be left as 00H.

Table 44 - CR11

BIT NO.	BIT NAME	DESCRIPTION
0:7	Reserved	Reserved For Test

CR12-CR1E
These registers are reserved. The default value of these registers after power up is 00H.

CR1F

This register can only be accessed in the Configuration Mode and after the CSR has been initialized to 1FH. The default value of this register after power up is 00H. This register indicates the Drive Type used for each drive. Refer to CR0B for Data Rate Table register.

FDD3		**FDD2**		**FDD1**		**FDD0**	
D7	D6	D5	D4	D3	D2	D1	D0
DT0	DT1	DT0	DT1	DT0	DT1	DT0	DT1

DTx = Drive Type select

DT0	DT1	DRVDEN0 (Note)	DRVDEN1 (Note)	Drive Type
0	0	DENSEL	DRATE0	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	
1	1	DRATE0	DRATE1	

Note: DENSEL, DRATE1 and DRATE0 map onto two output pins DRVDEN0 and DRVDEN1.

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0^{o}C to $+70^{o}$C
Storage Temperature Range ..... -55^{o} to $+150^{o}$C
Lead Temperature Range (soldering, 10 seconds)..... $+325^{o}$C
Positive Voltage on any pin, with respect to Ground ..... V_{IO}+0.3V
Negative Voltage on any pin, with respect to Ground..... -0.3V
Maximum V_{IO}..... +7V
Maximum V_{CC}..... V_{IO}

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{IO}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{IO} (Note 1)
O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 12 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{IO} (Note 1)
OD20 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 20 mA
Output Leakage	I_{OH}	-10		+10	µA	V_{OH} = 0 to V_{IO} (Note 2)
Supply Current Active	I_{CC}			TBD	mA	All outputs open.
Supply Current Standby	I_{CSBY}			TBD	mA	(Note 3)

Note 1: All output leakages are measured with the current pins in high impedance.
Note 2: Output leakage is measured with the low driving output off.
Note 3: Defined by the device configuration.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{cc} = +5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger

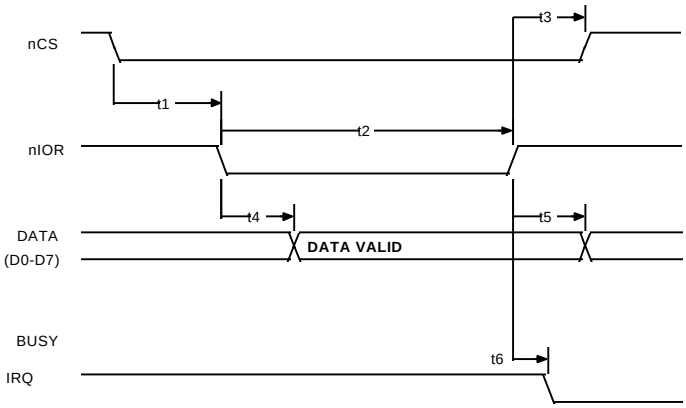
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	3.0			V	
Input Leakage						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	V_{IN} = V_{IO}
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{IO} (Note 1)
O12 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{IO} (Note 1)
OD20 Type Buffer						
Low Output Level	V_{OL}			0.5	V	I_{OL} = 48 mA
Output Leakage	I_{OH}	-10		+10	µA	V_{OH} = 0 to V_{IO} (Note 2)
Supply Current Active	I_{CC}			TBD	mA	All outputs open.
Supply Current Standby	I_{CSBY}			TBD	mA	(Note 3)

Note 1: All output leakages are measured with the current pins in high impedance.
Note 2: Output leakage is measured with the low driving output off.
Note 3: Defined by the device configuration.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 3.3V, 5V

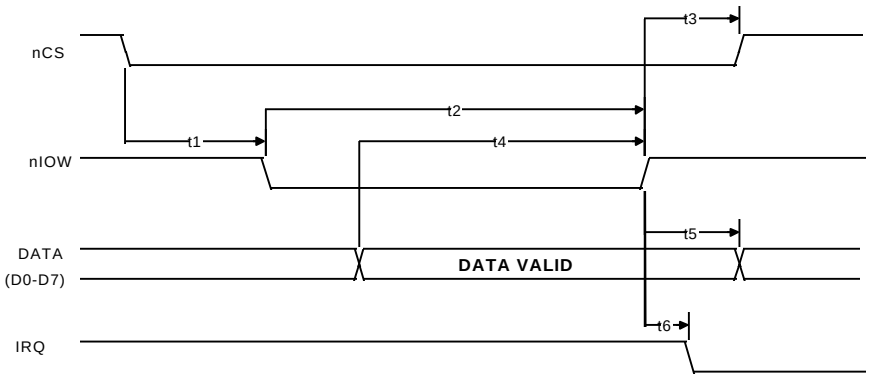
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS



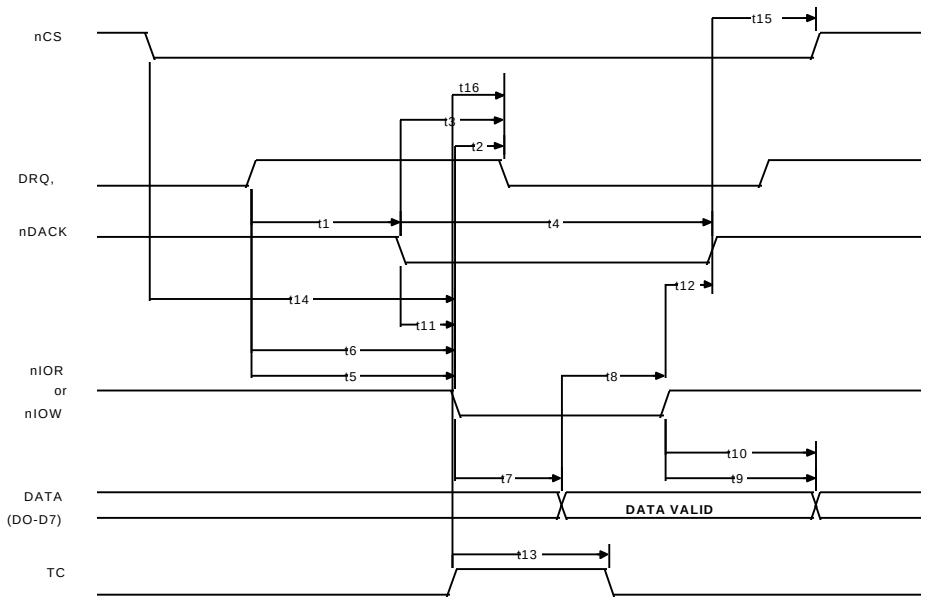
	Parameter	min	typ	max	units
t1	nCS Set Up to nIOR Low	40			ns
t2	nIOR Width	150			ns
t3	nCS Hold from nIOR High	10			ns
t4	Data Access Time from nIOR Low			100	ns
t5	Data to Float Delay from nIOR High	10		60	ns
t6	Read Strobe to Clear IRQ		40	55	ns

FIGURE 3 - MICROPROCESSOR READ TIMING



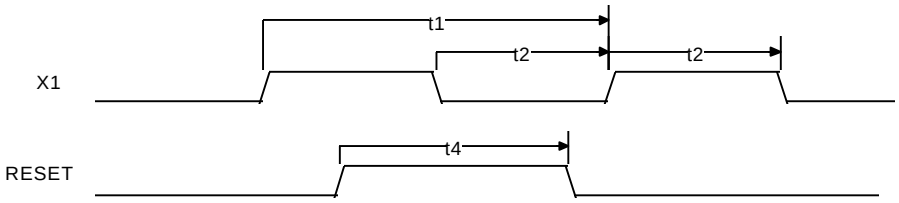
	Parameter	min	typ	max	units
t1	nCS Set Up to nIOW Low	40			ns
t2	nIOW Width	150			ns
t3	nCS Hold from nIOW High	10			ns
t4	Data Set Up Time to nIOW High	40			ns
t5	Data Hold Time from nIOW High	10			ns
t6	Write Strobe to Clear IRQ		40	55	ns

FIGURE 4 - MICROPROCESSOR WRITE TIMING



	Parameter	min	typ	max	units
t1	nDACK Delay Time from DRQ High	0		100	ns
t2	DRQ Reset Delay from nIOR or nIOW			100	ns
t3	DRQ Reset Delay from nDACK Low				ns
t4	nDACK Width	150			ns
t5	nIOR Delay from DRQ High	0			ns
t6	nIOW Delay from DRQ High	0		100	ns
t7	Data Access Time from nIOR Low				ns
t8	Data Set Up Time to nIOW High	40		60	ns
t9	Data to Float Delay from nIOR High	10			ns
t10	Data Hold Time from nIOW High	10			ns
t11	nDACK Set Up to nIOW/nIOR Low	5			ns
t12	nDACK Hold After nIOW/nIOR High	10			ns
t13	TC Pulse Width	60			ns
t14	nCS Set Up to nIOR/nIOW	40			ns
t15	nCS Hold from nDACK	10		100	ns
t16	TC Active to DRQ Inactive				ns

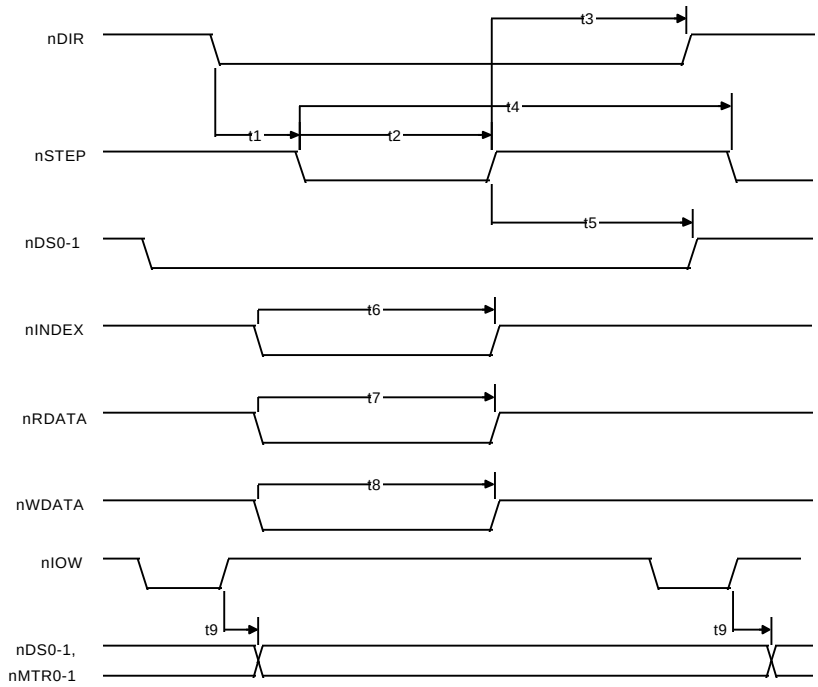
FIGURE 5 - DMA TIMING



Name	Description	min	typ	max	Units
t1	Clock CycleTime for 24MHZ	40		43.33	ns
t2	Clock High Time/Low Time	14			ns
	Clock Rise Time/Fall Time (not shown)			5	ns
t4	RESET width	1.5			us

NOTE 1:
The RESET width is dependent upon the processor clock.
RESET must be active while the clock is running and stable.

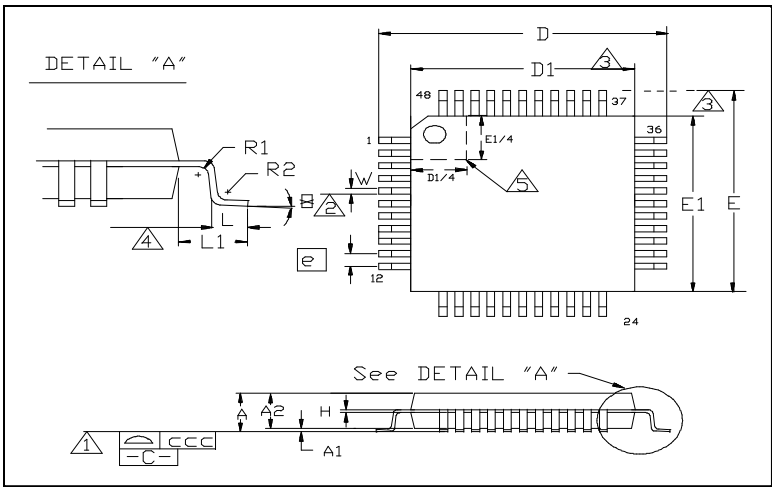
FIGURE 6 - CLOCK TIMING



	Parameter	min	typ	max	units
t1	nDIR Set Up to nSTEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time After nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-1, MTR0-1 from End of nIOW		25		ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16 x Data Rate (@500 kb/s MCLK = 8 MHz)
WCLK = 2 x Data Rate (@ 500 kb/s WCLK = 1 MHz)

FIGURE 7 - DISK DRIVE TIMING



	MIN	NOM	MAX		MIN	NOM	MAX
A			1.6	L	0.45	0.60	0.75
A1	0.05	0.10	0.15	L1		1.00	
A2	1.35	1.40	1.45	e	0.50 BSC		
D		9.00		~~θ~~	0^o		7^o
D1		7.00		W	0.17		0.27
E		9.00		R1	0.08		
E1		7.00		R2	0.08		0.20
H	0.09		0.20	ccc			0.08

Notes:

1 Coplanarity is 0.08 mm or 3.2 mils maximum

2 Tolerance on the position of the leads is 0.08 mm maximum

3 Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm

4 Dimension for foot length L is measured at the gauge plane 0.25 mm above the seating plane

5 Details of pin 1 identifier are optional but must be located within the zone indicated

6 Controlling dimension: millimeter

FIGURE 8 - 48 PIN TQFP PACKAGE DIMENSIONS

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FDC37C78 Rev. 4/9/96