Solid State Micro Technology for Music

SSM 2015

SSM 2015 MICROPHONE PREAMPLIFIER

DESCRIPTION

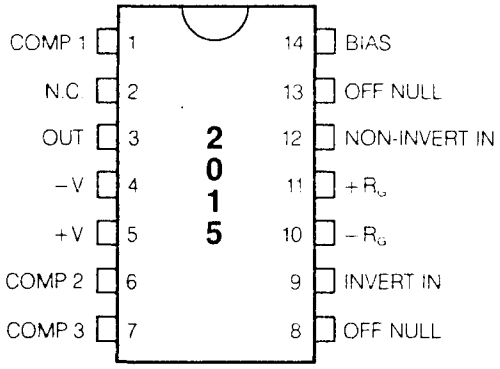
The SSM 2015 is an ultra low noise audio preamplifier particularly suited to microphone preamplification. Gains from 10 to over 2000 can be selected with wide bandwidth and low distortion over the full gain range.

True differential inputs with high common mode rejection provide easy interfacing to floatation transducers such as balanced microphone outputs, as well as single ended devices.

The very low voltage noise performance ($1.3nV/\sqrt{Hz}$) is enhanced by a programmable input stage which allows overall noise to be optimized for source impedances up to $4k\Omega$.

FEATURES

- Ultra Low Voltage Noise ($1.3nV/\sqrt{Hz}$)
- Wide Bandwidth (700kHz @ G = 100)
- High Slew Rate ($6V/\mu S$)
- Very Low Distortion (0.007% @ G = 100)
- Full D.C. Coupling
- True Differential Inputs
- High Common Mode Rejection (100dB)
- Programmable Input Stage
- No Crossover Distortion
- Symmetric Slew Rates



PIN OUT (TOP VIEW)

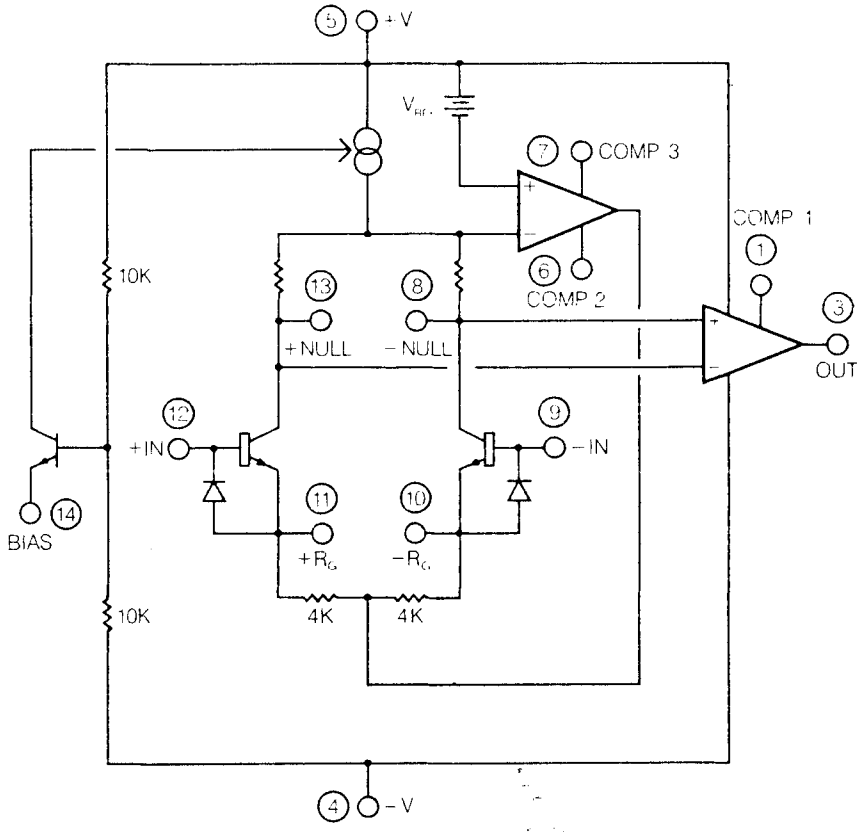


FIGURE 1. BLOCK DIAGRAM

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SPECIFICATIONS*

OPERATING TEMPERATURE
−10°C to +55°C

STORAGE TEMPERATURE
−55°C to +125°C

The following specifications apply for $V_S = \pm 15V$, $T_A = 25°C$, $R_{BIAS} = 33k\Omega$, unless otherwise noted.

PARAMETER (SYMBOL)	MIN	TYP	MAX	UNITS	CONDITIONS
Total Harmonic Distortion (THD) (Note 1)					
G = 1000					
@ 1kHz		0.007	0.01	%	V_{OUT} = 7V RMS
@ 10kHz		0.015	0.02	%	V_{OUT} = 7V RMS
G = 100					
@ 1kHz		0.007	0.01	%	V_{OUT} = 7V RMS
@ 10kHz		0.007	0.01	%	V_{OUT} = 7V RMS
G = 10					
@ 1kHz		0.01	0.015	%	V_{OUT} = 7V RMS
@ 10kHz		0.01	0.015	%	V_{OUT} = 7V RMS
Input Referred Voltage Noise (E_n) (Note 1)					
R_{BIAS} = 33kΩ					Inputs Shorted to GND
G = 1000		0.2	0.3	μV RMS	20kHz Bandwidth
G = 100		0.31	0.5	μV RMS	20kHz Bandwidth
G = 10		1.1	1.7	μV RMS	20kHz Bandwidth
R_{BIAS} = 150kΩ					
G = 1000		0.28	0.45	μV RMS	20kHz Bandwidth
G = 100		0.41	0.65	μV RMS	20kHz Bandwidth
G = 10		1.1	1.7	μV RMS	20kHz Bandwidth
Input Current Noise (I_n) (Note 1)					
R_{BIAS} = 33kΩ		250	380	pA RMS	20kHz Bandwidth
R_{BIAS} = 68kΩ		200	300	pA RMS	20kHz Bandwidth
R_{BIAS} = 150kΩ		130	200	pA RMS	20kHz Bandwidth
Gain Equation (G)		$G = \frac{20k\Omega}{R_G} + 3.5$			$R_1 = R_2 = 10k\Omega$
Error From Gain Equation (ΔG)					
G = 1000		0.1	0.3	dB	$R_1 = R_2 = 10k\Omega$
G = 100		0.1	0.3	dB	$R_1 = R_2 = 10k\Omega$
G = 10		0.2	0.8	dB	$R_1 = R_2 = 10k\Omega$
Input Offset Voltage (V_{OS})					
G = 1000		0.25	1.5	mV	$R_1 = R_2 = 10k\Omega$
G = 100		0.3	1.5	mV	$R_1 = R_2 = 10k\Omega$
G = 10		3	15	mV	$R_1 = R_2 = 10k\Omega$
Input Bias Current (I_b)					
R_{BIAS} = 33kΩ		4.5	12	μA	V_{CM} = 0V
R_{BIAS} = 150kΩ		1	3	μA	V_{CM} = 0V
Input Offset Current (I_{OS})					
R_{BIAS} = 33kΩ		0.5	1.5	μA	V_{CM} = 0V
R_{BIAS} = 150kΩ		0.15	0.4	μA	V_{CM} = 0V
Common Mode Rejection Ratio (CMRR)					
G = 1000	90	100		dB	$R_1 = R_2 = 10k\Omega$
G = 100	70	95		dB	$R_1 = R_2 = 10k\Omega$
G = 10	60	75		dB	$R_1 = R_2 = 10k\Omega$
Power Supply Rejection Ratio (PSRR)		100		dB	$V_S = \pm 12$ to $\pm 17V$
Common Mode Voltage Range (CMVR)	±4	±5.5		V	
Common Mode Input Impedance		50		MΩ	
Differential Mode Input Impedance					
G = 1000		0.5		MΩ	
G = 100		5		MΩ	
G = 10		20		MΩ	
Output Voltage Swing	±10.5	±12.5		V	$R_L = 2k\Omega$
Output Current (I_{OUT}) (Note 2)					
Source	15	25		mA	
Sink	8	14		mA	
−3dB Bandwidth (GBW)					
G = 1000		150		kHz	
G = 100		700		kHz	
G = 10		1000		kHz	
Slew Rate (SR)		6		V/μS	
Supply Current (I_{SY})		12	16	mA	

Note 1. Parameter is sample tested to maximum limits.
Note 2. Output is protected from short circuits to ground or either supply.
*Final specifications may be subject to change.

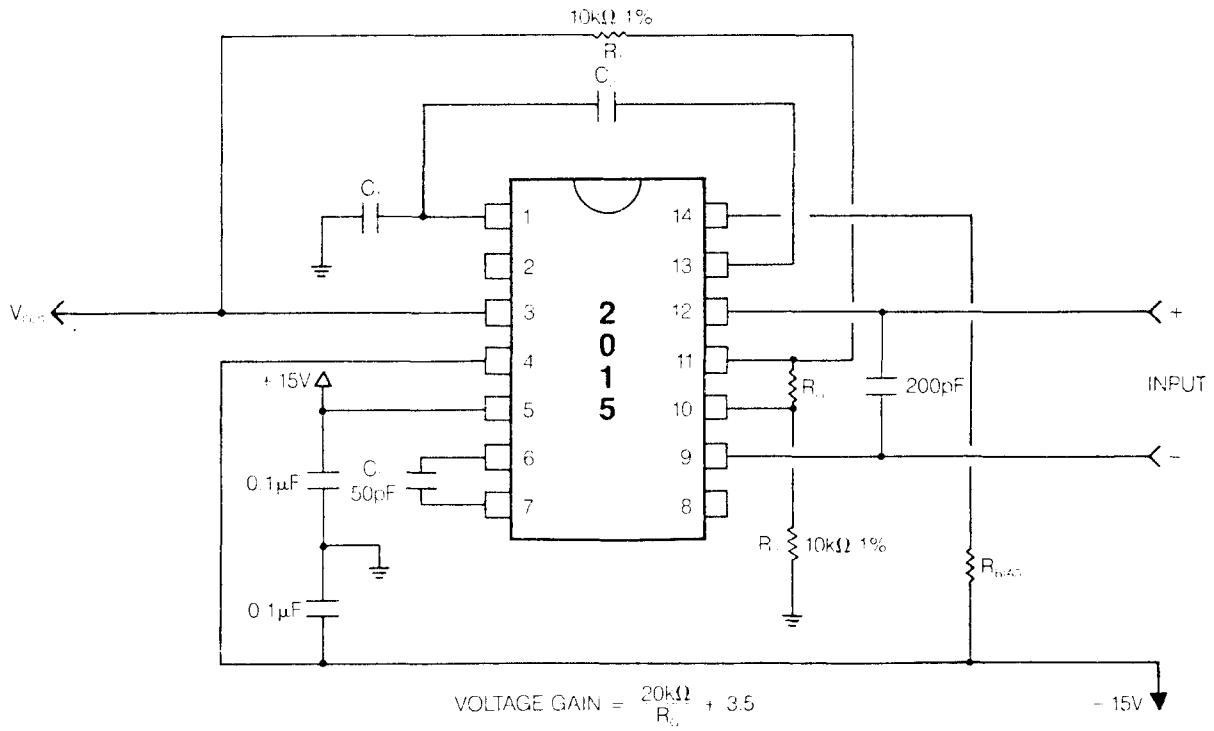

FIGURE 2. TYPICAL APPLICATION

Principle of Operation

The 2015 operates as a true differential amplifier with feedback returned directly to the emitters of the input stage transistors by R_1. This system produces both optimum noise and common mode rejection while retaining a very high input impedance.

An internal feedback loop maintains the input stage current at a value controlled by R_{BIAS}. This provides a programmability function which allows noise to be optimized for a wide range of source impedances.

Gain Setting

The nominal gain of the 2015 is given by:

$$G \cong \frac{R_1 + R_2}{R_G} + \frac{R_1 + R_2}{8k\Omega} + 1 \quad \text{or} \quad G = \frac{20k\Omega}{R_G} + 3.5 \text{ for } R_1, R_2 = 10k\Omega$$

R_1 and R_2 should be equal to 10kΩ for best results. It is vital that good quality resistors be used in the gain setting network, since low quality types (notably carbon composition) can generate significant amounts of distortion and, under some conditions, low frequency noise. The 2015 will function at gains down to 3.5, but will yield a degraded performance at gains below 10. The table below gives convenient R_G values for commonly used gains.

GAIN	R_G	ERROR
10	3kΩ	+0.14dB
50	430Ω	+0.002dB
100	200Ω	+0.3dB
500	39Ω	+0.28dB
1000	20Ω	+0.03dB

Frequency Compensation

Referring to figure 2, C_3 (50pf) provides compensation for the input stage current regulator, while C_1 and C_2 compensate the overall amplifier. The latter two depend on the value of R_{BIAS} chosen, and the following table gives recommended values which are valid for all gains:

R_{BIAS}	C_1	C_2
27kΩ–47kΩ	15pF	15pF
47kΩ–68kΩ	15pF	10pF
68kΩ–150kΩ	30pF	5pF

The 2015 has a bandwidth of more than 70kHz under worst case conditions (G = 1000, R_{BIAS} = 150kΩ) and considerably greater at higher set currents and lower gains. This excellent performance is supplemented by a highly symmetric slew rate for optimum large signal audio performance.

The output of the 2015 is not intended to drive long lines: capacitive loads greater than 150pf should be decoupled with 100Ω in series with the output (R_1 in Figure 2 should remain connected to pin 3).

Noise

Unfortunately, low noise amplifier design is always a trade-off between noise voltage and noise current. Normally, a compromise is chosen which produces optimum performance over a limited range of source impedances.

The programmability of the 2015 provides close to optimum performance for source impedances up to 4kΩ, and is within 1dB of the theoretical minimum value between 500Ω and 2.5kΩ.

Figure 3 shows the recommended bias resistor versus source impedance. Note that single ended sources have a different value from balanced ones. This is due to the uncorrelated nature of the input noise currents of the 2015.

2015 Inputs

Although the 2015 inputs are fully floating, care must be exercised to ensure that both inputs have a DC bias connection capable of maintaining them within the input common mode range. The usual method of achieving this is to ground one side of a transducer as in figure 4(a), but an alternative way is to float the transducer and use two resistors to set the bias point as in figure 4(b). The value of these resistors can be up to 10k or so, but they should be kept as small as possible to limit common mode noise. Noise generated in the resistors themselves is negligible since it is attenuated by the transducer impedance. Balanced transducers give the best noise immunity, and interface directly as in figure 4(c).

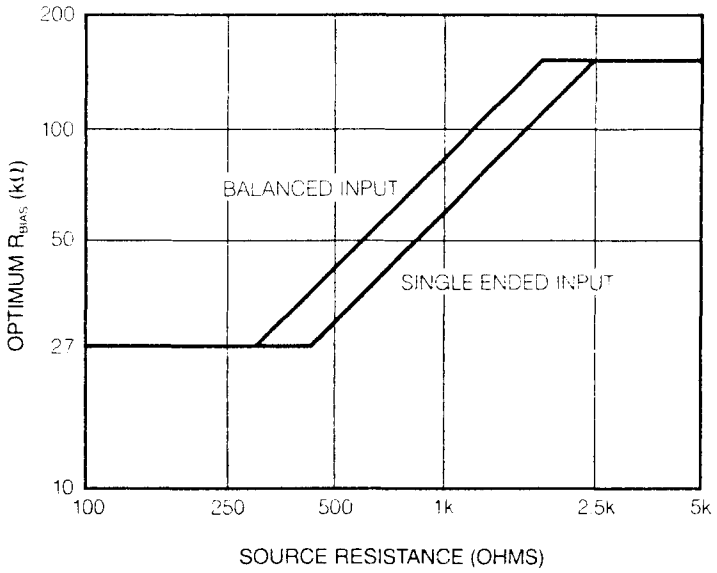

FIGURE 3. OPTIMUM R_{BIAS} vs SOURCE RESISTANCE

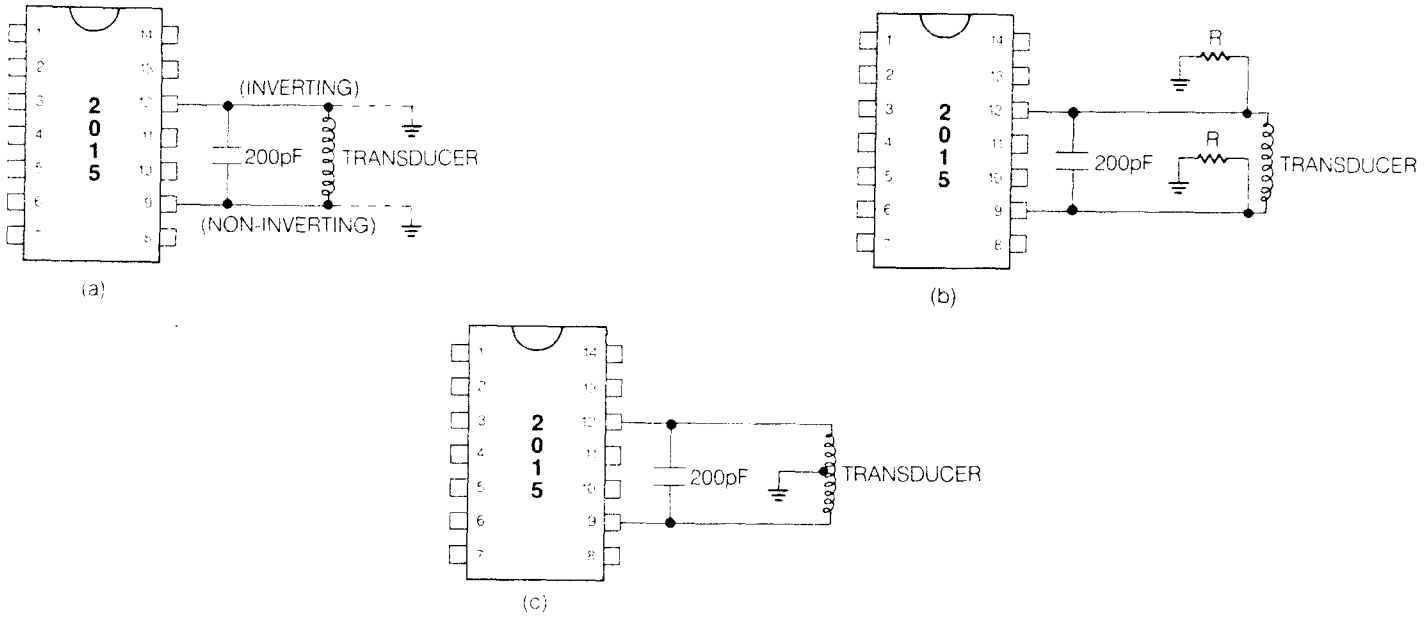

FIGURE 4. THREE WAYS OF INTERFACING TRANSDUCERS FOR HIGH NOISE IMMUNITY

(a)Single ended. (b)Pseudo differential. (c)True differential.

Phantom Power

A recommended circuit for phantom microphone powering is shown in figure 5. Z1 through Z4 provide transient overvoltage protection for the 2015 whenever microphones are plugged in and out.

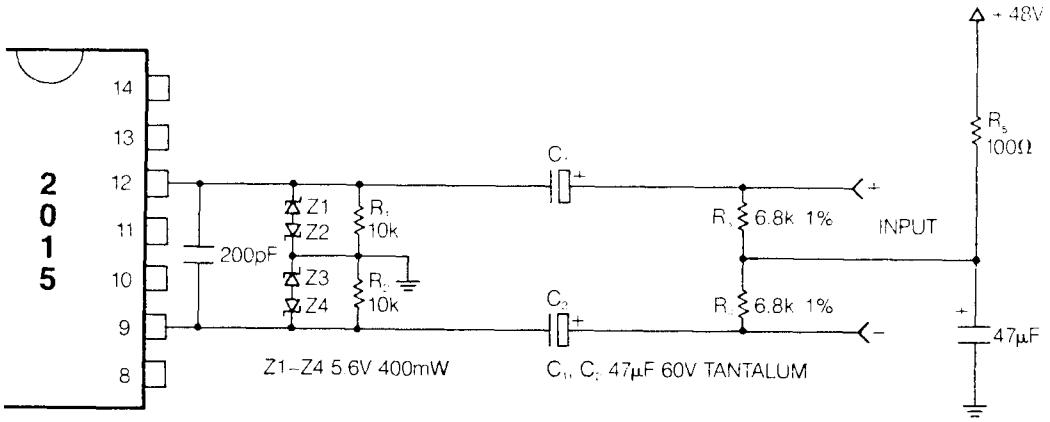

FIGURE 5. 2015 WITH PHANTOM POWER

Trimming the 2015

The gain of the 2015 can be easily trimmed by adjustment of R_G. However, two further trims may be desirable: offset voltage and common mode rejection; although the 2015 provides excellent untrimmed performance in both respects.

Figure 6 shows a method of trimming both these parameters.

VR_1 is the CMRR trim, and should be adjusted for minimum output with an 8Vp-p amplitude 60Hz sine wave common to both inputs.

VR_2 is the offset voltage trim, and should be selected from the following table:

	R_{BIAS}		
V_{R2}	27k–47kΩ	47k–68kΩ	68k–150kΩ
G = 10	500kΩ	250kΩ	250kΩ
G = 100	500kΩ	100kΩ	100kΩ
G = 1000	250kΩ	100kΩ	50kΩ

The offset trim should follow the CMRR trim, since there is a small (non-reciprocal) interaction.

The offset trim can also be used to null out the gain control feedthrough. The output offset at low gains is determined by the matching of the feedback resistors while at high gain it is determined by the matching of the input transistors. If the gain setting is changed rapidly, the output shift can cause an (audible) click or thump. To reduce or eliminate this, the offset at high gains is adjusted to be equal to the offset at low gains.

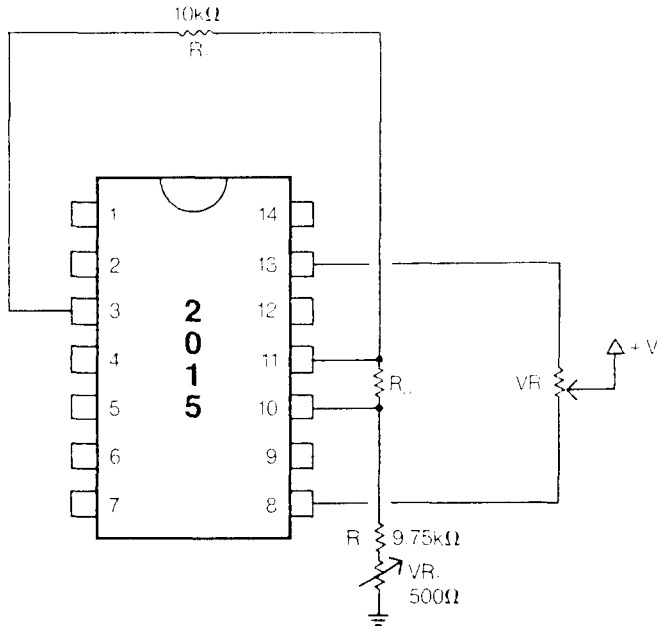

FIGURE 6. TRIMMING THE 2015

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