Ordering number : EN※4853A

CMOS LSI

SANYO

No. ※ 4853A

LC89513K

CD-ROM/CD-I Error Correction LSI for Integrated Host CPU Systems

Preliminary

Overview

The LC89513K is an error correction LSI appropriate for systems in which a single CPU handles both system control and data readout. The LC89513K consists of the three major blocks described below.

- CD Player Interface/Data Input Block

  The LC89513K supports three serial input formats, with the format used selected by setting internal register. That is, an application system can compensate for CD player serial data format differences by setting the LC89513K CDIF0 and CDIF1 registers.

  The LC89513K uses an internal synchronization detection circuit to synchronize internal operations with the input data in block (sector) units. LC89513K synchronization uses not only input data pattern detection, but also uses a synchronization signal interpolation circuit for synchronization protection. These two synchronization systems can be turned on and off under program control. Input data is stored in buffer RAM in 8-bit units after being processed by a descrambling circuit. All of the 2,352 bytes of the input data, including the synchronization, header and parity data, is stored in RAM in the order received from the CD player without exception.

- Error Correction Block

  This block corrects the errors in the CD-ROM data output from the CD player block.

  CD-ROM data output from the CD player is temporarily stored in the LC89513K's external buffer RAM. After one sector is buffered, the LC89513K automatically performs error correction. (Error detection and correction are only performed once.) After the correction procedure completes, the LC89513K issues an interrupt to the control CPU, and the control CPU reads the data through the LC89513K.

  Since the buffering, error correction, and data read operations are pipelined, as they are in the LC8951, these operations are performed in real time.

- CPU Interface Block

  In the LC8951, the CPU interface was divided into a microcontroller interface block (the LC8951 control bus) and a host interface block (data output bus). However, in the LC89513K, these functions are combined in a single block so that a single CPU can both control the CD player and read data from the LC89513K. The LC89513K outputs CD-ROM data from a separate port (pin), as did the earlier LC8951. The LC89513K CPU interface uses the same indirect addressing scheme used in the LC8951 interface, and programs written for the LC8951 can be used without modification.

Features

- Supports both double- and quad-speed playback, selectable by internal register settings.

  Operating frequencies: double-speed: 16.9344 MHz, quad speed: 33.8688 MHz

- Can be operated at 3.5 V.

  In normal operation SRAM with an access time of 300 ns or shorter must be used.

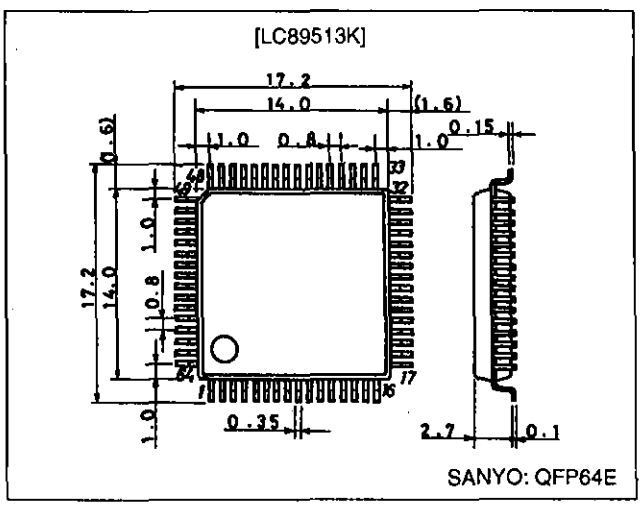
  In double-speed operation SRAM with an access time of 120 ns or shorter must be used.

- Supports CD-ROM drive systems in which a single CPU performs both control and data readout functions.

Package Dimensions

unit: mm

3159-QFP64E



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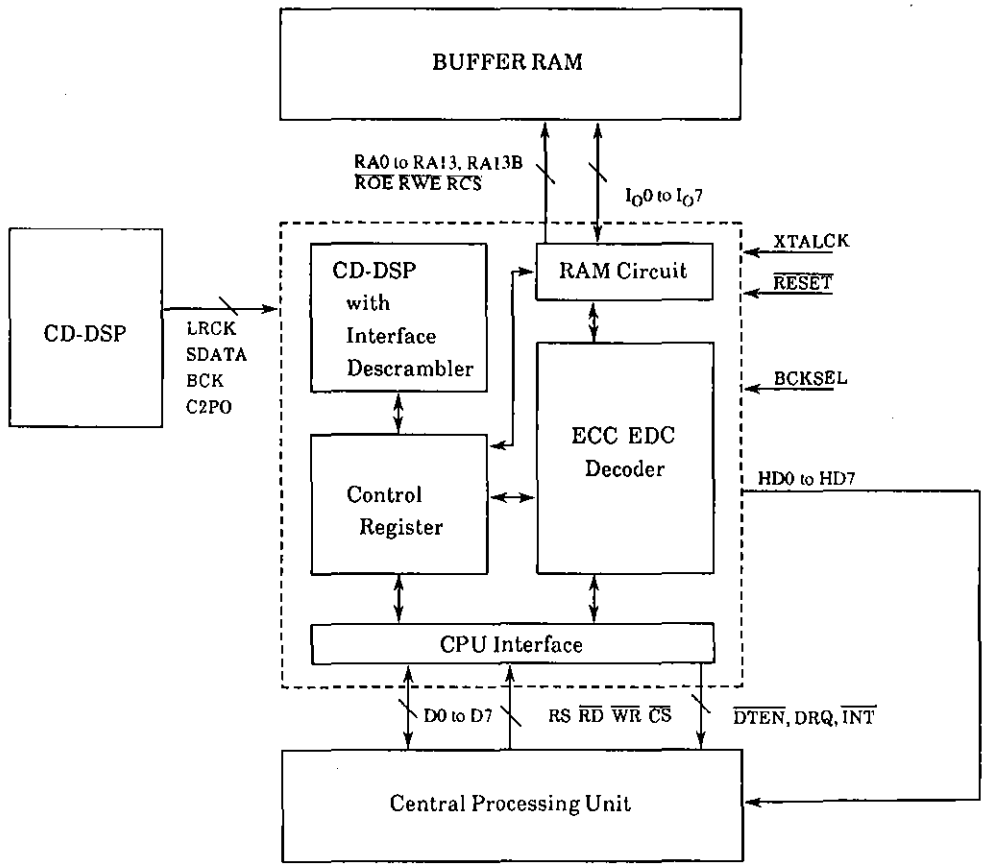
Block Diagram



Pin Functions

Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Pin	Type	Function
1	V_{SS}	P	
2	RA0	O	Data buffer RAM address signal outputs
3	RA1	O	
4	RA2	O	
5	RA3	O	
6	RA4	O	
7	RA5	O	
8	RA6	O	
9	V_{SS}	P	
10	RA7	O	Data buffer RAM data signals
11	RA8	O	
12	RA9	O	
13	RA10	O	
14	RA11	O	
15	RA12	O	
16	RA13	O	
17	V_{SS}	P	
18	RA13B	O	Data buffer RAM address signal output
19	$\overline{RCS}$	O	RAM chip select
20	$\overline{RWE}$	O	RAM data write signal output
21	$\overline{ROE}$	O	RAM data write signal output
22	$\overline{RESET}$	I	Chip select signal input
23	XTALCK	I	Crystal oscillator circuit input
24	V_{DD}	P	
25	C2PO	I	C2 pointer input
26	BCK	I	Serial data input clock
27	SDATA	I	Serial data input
28	LRCK	I	44.1 kHz strobe signal input
29	RS	I	Register selection signal input
30	$\overline{RD}$	I	CPU data read signal input
31	$\overline{WR}$	I	CPU data write signal input
32	$\overline{CS}$	I	Chip select signal input (from the CPU)
33	V_{SS}	P	
34	D0	B	CPU data signal pins These pins have built-in pull-up resistors.
35	D1	B	
36	D2	B	
37	D3	B	
38	D4	B	
39	D5	B	
40	D6	B	
41	D7	B	
42	GSRAM	I	Pseudo-SRAM selection
43	$\overline{INT}$	O	CPU interrupt request signal output
44	DRQ	O	DRQ signal output
45	HD0	O	Data outputs to the CPU
46	HD1	O	
47	HD2	O	
48	HD3	O	
49	V_{SS}	P	
50	HD4	O	Data outputs to the CPU
51	HD5	O	
52	HD6	O	
53	HD7	O	

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Type: I: Input pin, O: Output pin, B: Bidirectional pin, P: Power supply pin, NC: No connection pin

Pin No.	Pin	Type	Function
54	$\overline{HRD}$	I	Data read signal input
55	$\overline{DTEN}$	O	Data enable signal output
56	V_{DD}	P	
57	I_O0	B	Data buffer RAM data signals These pins have built-in pull-up resistors.
58	I_O1	B	
59	I_O2	B	
60	I_O3	B	
61	I_O4	B	
62	I_O5	B	
63	I_O6	B	
64	I_O7	B	

Specifications

Absolute Maximum Ratings at V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	Ta = 25°C	–0.3 to +7.0	V
I/O voltages	V_I V_O	Ta = 25°C	–0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	Ta ≤ 70°C	350	mW
Operating temperature	**Topr**		–30 to +70	°C
Storage temperature	Tstg		–55 to +125	°C
Soldering thermal stress limit		10 seconds	260	°C

Allowable Operating Ranges at Ta = –30 to +70°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{DD}		3.5	5.0	5.5	V
Input voltage range	V_{IN}		0		V_{DD}	V

DC Characteristics at Ta = –30 to +70°C, V_{SS} = 0 V, V_{DD} = 3.5 to 5.5 V

Parameter	Symbol	Conditions	min	typ	max	Unit
Input high level voltage	$V_{IH}1$	All input pins other than (1) and XTALCK	2.2			V
Input low level voltage	$V_{IL}1$				0.8	V
Input high level voltage	$V_{IH}2$	RS, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{RESET}$, $\overline{HRD}$ and I_O0 to I_O7 (1)	2.5			V
Input low level voltage	$V_{IL}2$				0.6	V
Output high level voltage	$V_{OH}1$	$I_{OH}1$ = –3 mA: All output pins (including bus pins) other than (2) and XTALCK	2.4			V
Output low level voltage	$V_{OL}1$	$I_{OL}1$ = 3 mA: All output pins (including bus pins) other than (2) and XTALCK			0.4	V
Output low level voltage	$V_{OL}2$	$I_{OL}2$ = 3 mA: $\overline{INT}$ (pull-up resistor open drain) (2)			0.4	V
Input leakage current	I_L	V_I = V_{SS}, V_{DD}: All input pins	–25		+25	μA
Pull-up resistance	R_{UP}	All bus pins and $\overline{INT}$	10	20	40	kΩ