Sonic/AD

Sonic

MULTIMEDIA ACCELERATION

Cooperative Accelerator Architecture

S3 Sonic/AD

Audio DAC

July 1995

S3 Incorporated
2770 San Tomas Expressway
Santa Clara, CA 95051-0968

NOTATIONAL CONVENTIONS

The following notational conventions are used in this data book:

Signal names are shown in all uppercase letters. For example, XD.

A bar over a signal name indicates an active low signal. For example, $\overline{OE}$.

n-m indicates a bit field from bit n to bit m. For example, 7-0 specifies bits 7 through 0, inclusive.

n:m indicates a signal (pin) range from n to m. For example D[7:0] specifies data lines 7 through 0, inclusive

Use of a trailing letter H indicates a hexadecimal number. For example, 7AH is a hexadecimal number.

Use of a trailing letter b indicates a binary number. For example, 010b is a binary number.

When K or M are used, they refer to binary rather than decimal form. Thus, for example, 1 KByte would be equivalent to 1024, not 1,000 bytes.

When k is used, it refers to the decimal form. For example, 1 kbit means 1000 bits.

NOTICES

Additional information may be obtained from:

S3 Incorporated, Literature Department, 2770 San Tomas Expressway, Santa Clara, CA 95051-0968.

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Section 1: Introduction

The S3® Sonic/AD™ high performance audio DAC (hereinafter referred to as Sonic/AD) accepts digital audio input from an audio controller and outputs stereo CD quality analog audio. It is optimized for interfacing to S3's Scenic/MX1™ PCI MPEG-1 audio/video decoder and Scenic/MX2™ MPEG-1 audio/video decoder. This section describes its major features.

1.1 HIGH QUALITY AUDIO

Sonic/AD provides 16-bit resolution and uses a 4x interpolation filter, a 64x Sigma-Delta DAC and linear phase filtering to provide a 90 dB dynamic range with more than 85 dB Signal-to-Noise Ratio.

1.2 GLUELESS INTERFACE

Sonic/AD provides a glueless interface to S3's Scenic/MX1 PCI and Scenic/MX2 MPEG-1 audio/video decoders. This interface is an industry standard I^2S serial bus and includes clocks, data and frequency select signals.

Figure 1-1 shows how the Sonic/AD integrates into a Scenic/MX2-based multimedia subsystem. The interface to a Scenic/MX1 is exactly the same.

1.3 CLOCK GENERATION

Sonic/AD contains a phase-locked-loop (PLL) frequency generator that allows it to provide a master clock signal (DACCLK) for driving the interface to the MPEG-1 decoder. The decoder uses DACCLK to generate a clock with its sampling rate frequency, usually 32, 44.1 or 48 kHz. The DACCLK frequency required to generate these frequencies can be selected via hardware (FS[1:0] lines) or by programming of Sonic/AD registers via the serial interface. S3's Scenic/MX1 PCI and Scenic/MX2 MPEG-1 audio/video decoders provide the FS[1:0] lines, allowing on-the-fly changes in the sampling rate.

A major benefit of the integrated PLL is that it supports .WAV file requirements for sampling rates other than those of the MPEG standard.

1.4 LOW COST DESIGN

Sonic/AD comes in a 28-pin PLCC package. The integration of the audio DAC and PLL in this small package results in a very cost effective solution. The Sonic/AD operates at 5V.

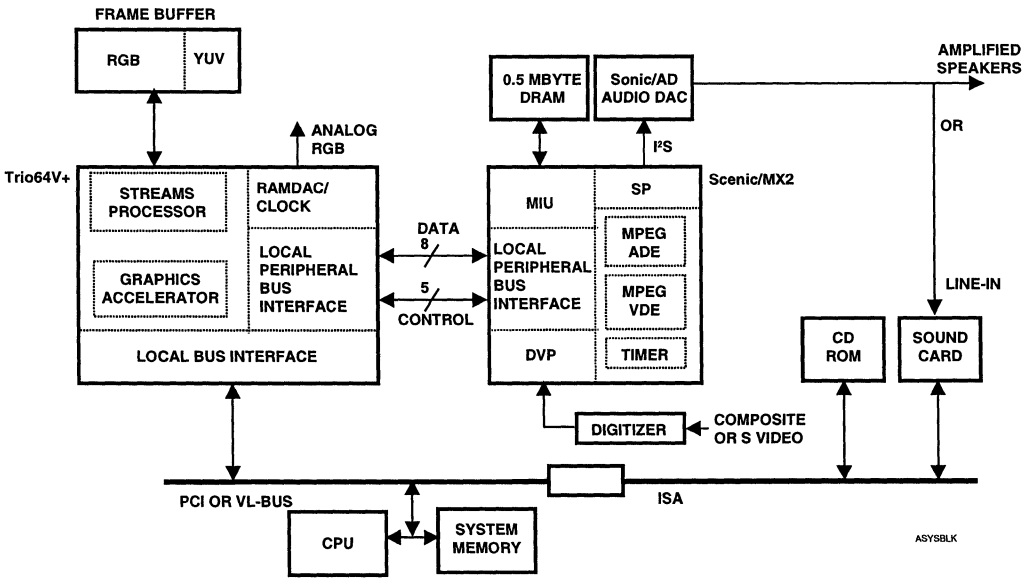


Figure 1-1. System Architecture

Section 2: Mechanical Data

2.1 THERMAL SPECIFICATIONS

Parameter	Min	Typ	Max	Unit
Thermal Resistance Θ_{JA} (200 ft/min air flow)		41		°C/W
Thermal Resistance Θ_{JA} (Still Air)		52		°C/W
Power Dissipation			1.3	W
Junction Temperature			125	°C
Ambient Temperature	0		70	°C

2.2 MECHANICAL DIMENSIONS

The Sonic/AD comes in a 28-pin PLCC package. The mechanical dimensions are given in Figure 2-1.

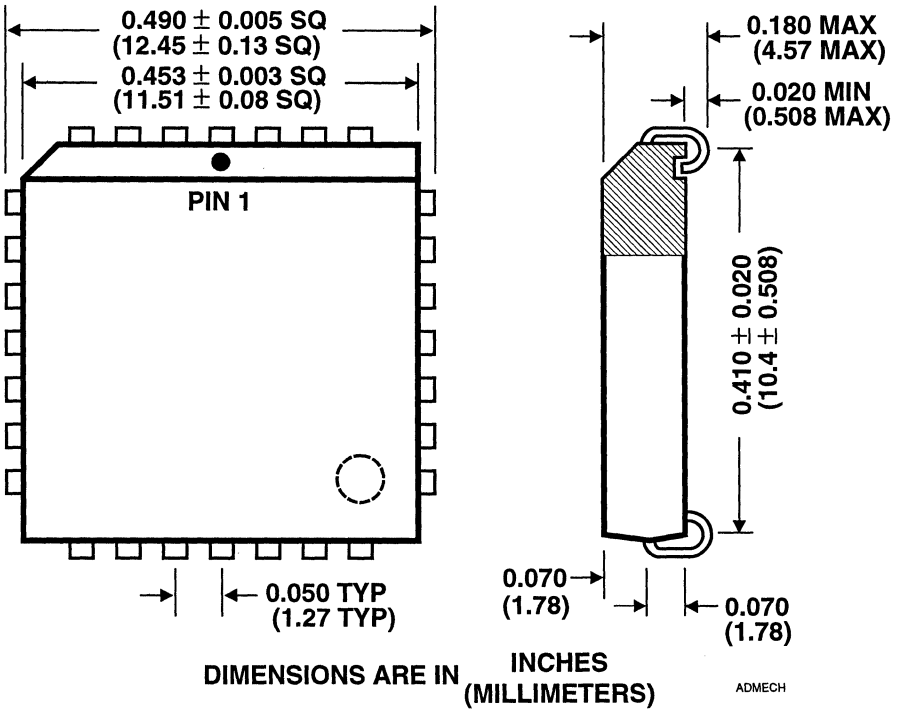


Figure 2-1. 28-pin PLCC Mechanical Dimensions

Section 3: Pins

3.1 PINOUT DIAGRAM

Sonic/AD comes in a 28-pin PLCC package. Figure 3-1 shows the pinout.

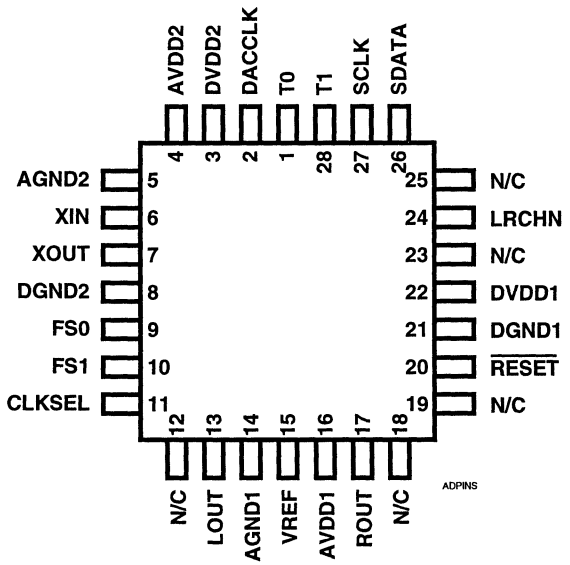


Figure 3-1. Sonic/AD Pinout

3.2 PIN DESCRIPTIONS

The following table describes each pin. The following definitions are used in these descriptions:

I - Input signal
O - Output signal
B - Bidirectional signal

Table 3-1. Sonic/AD Pin Descriptions

Symbol	Type	Pin Number(s)	Description
XIN	I	6	Crystal Oscillator Input. If the CLKSEL pin is pulled low, a 14.31818 MHz crystal must be connected between XIN and XOUT. This provides the base frequency for generation of the internal master clock, which is also buffered and output as DACCLK. If the CLKSEL pin is pulled high, an external CMOS level clock input must be connected to XIN to provide the internal master clock and (buffered) DACCLK output. The external clock source must be 256x the sampling frequency. XOUT is left floating.
XOUT	O	7	Crystal Oscillator Output. See description for XIN.
CLKSEL	I	11	Clock Select. See description for XIN.
DACCLK	O	2	DAC Clock. Buffered clock output to the audio decoder. The frequency is 256x the sampling frequency. This is used by the decoder to generate LRCHN (= sampling frequency) and SCLK, which must be 64x or 128x the sampling frequency.
SCLK	I	27	Serial Clock. This input is used to latch the serial input data on SDATA. It can be 64x or 128x the sampling frequency.
SDATA	I	26	Serial Data. This input provides the digital audio data and, optionally, PLL programming, frequency select and mute data.
LRCHN	I	24	Left/Right Channel. The rising edge of this input signals the beginning of left channel data. The falling edge signals the beginning of right channel data.
$\overline{\text{RESET}}$	I	20	Reset. Returns the chip to its power-on reset state.
FS[1:0]	I	10, 9	Frequency Select. When bit 21 of the left channel cycle is 0, these pins select the internal master clock value.
LOUT	O	13	Left Channel Analog Output.
ROUT	O	17	Right Channel Analog Output.
VREF	B	15	Voltage Reference. Common voltage for the analog circuitry. Connect this pin to ground through a 0.1 µF capacitor. The nominal voltage level is 2.2 V.

Table 3-1. Sonic/AD Pin Descriptions (Continued)

T[1:0]	I	1, 28	Test. These pins are used for chip testing and must be grounded for normal operation.
AVDD1	I	16	Analog Power Supply for the DAC
AGND1	I	14	Analog Ground
DVDD1	I	22	Digital Power Supply for the DAC
DGND1	I	21	Digital Ground
AVDD2	I	4	Analog Power Supply for the PLL
AGND2	I	5	Analog Ground
DVDD2	I	3	Digital Power Supply for the PLL
DGND2	I	8	Digital Ground

3.3 PIN LISTS

Table 3-2 lists all pins alphabetically. Table 3-3 lists all pins in numerical order.

Table 3-2. Alphabetical Pin List

Name	Pins
AGND1	14
AGND2	5
AVDD1	16
AVDD2	4
CLKSEL	11
DACCLK	2
DGND1	21
DGND2	8
DVDD1	3
DVDD2	22
FS[1:0]	10, 9
LOUT	13
LRCHN	24
N/C*	12, 18, 19, 23, 25
$\overline{\text{RESET}}$	20
ROUT	17
T[1:0]	1, 28
VREF	15
XIN	6
XOUT	7

* N/C means No Connect

Table 3-3. Numerical Pin Listing

Number	Name
1	T0
2	DACCLK
3	**DVDD2**
4	**AVDD2**
5	**AGND2**
6	XIN
7	XOUT
8	**DGND2**
9	FS0
10	FS1
11	CLKSEL
12	N/C*
13	LOUT
14	**AGND1**
15	VREF
16	**AVDD1**
17	ROUT
18	N/C*
19	N/C*
20	$\overline{\text{RESET}}$
21	**DGND1**
22	**DVDD1**
23	N/C
24	LRCHN
25	N/C*
26	SDATA
27	SCLK
28	T1

* N/C means No Connect

Section 4: Functional Description

4.1 OVERVIEW

Sonic/AD accepts serialized audio data and commands from the audio source and generates high quality analog stereo output. It also provides the basic clock used to control the interface with the digital audio source.

4.2 FREQUENCY SELECTION

The key parameter for determining the required clock frequencies is the audio sampling frequency f_S. The three standard MPEG frequencies are:

- 32 kHz
- 44.1 kHz
- 48 kHz

The audio source is programmed to select one of these frequencies (or a custom-specified frequency). This can be done externally via the FS[1:0] inputs or internally by setting certain bits in the serial input data stream. The appropriate values are shown in Table 4-1.

Table 4-1. Frequency Selection

FS1, IFS1	FS0, IFS0	f_S	DACCLK
0	0	32 kHz	8.192 MHz
0	1	44.1 kHz	11.2896 MHz
1	0	48 kHz	12.288 MHz
1	1	CUSTOM	CUSTOM

For example, if a sampling frequency of 44.1 kHz is desired, the audio source is programmed to output 1, 0 on FS[1:0]. This generates an internal master clock frequency of 11.2896 MHz (256x f_S). This frequency is also output as the DACCLK signal to the audio source. The method of selecting the frequency internally (IFS[1:0]) is explained in the Serial Input section below.

In a standard design, a 14.31818 MHz crystal is connected between the XIN and XOUT pins and the CLKSEL pin is pulled low. This generates the frequencies listed in Table 4-1. For a non-standard design, CLKSEL can be pulled high and an external CMOS-level clock source connected to XIN with XOUT left floating. This external clock input must be 256x the desired f_S. It is buffered and output as DACCLK.

4.3 SERIAL INPUT

The audio source sends audio data and some control information to Sonic/AD via the serial interface SCLK and SDATA. The format of this input is described in Figure 4-1.

The audio source takes the DACCLK input and generates SCLK and LRCHN. SCLK (serial clock) is output to Sonic/AD and is used to latch the serial data on SDATA. The first 32 bits of data after a LRCHN transition are latched. The functional timing for this is shown in Figure 4-2.

LRCHN (Left/Right Channel) must be the same frequency as the sampling frequency f_S. SCLK must be at least 64x f_S. If it is faster, all data after 32 bits is ignored until the next LRCHN transition.

As long as the PLL bit (bit 21 of the right channel cycle) is 0, all bits other than the data and mute

Left Channel (LRCHN = 1)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
LEFT CHANNEL AUDIO DATA [15:0]															
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	0	0	0	PLL	Mute	0	ISEL	M[7:0]							

Right Channel (LRCHN = 0)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
RIGHT CHANNEL AUDIO DATA [15:0]															
17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
0	0	0	0	0	Mute	IFS1	IFS0	N2[2:0]			N1[4:0]				

Figure 4-1. Serial Data Input Format

bits are ignored and frequency selection must be performed via the FS[1:0] pins.

If the PLL and ISEL bits are both set to 1, the frequency is selected by the settings of the IFS1 and IFS0 bits in the serial stream as shown in Table 4-1 and Figure 4-1.

4.4 CUSTOM FREQUENCY PROGRAMMING

If the PLL and ISEL bits are both set to 1 and the IFS[1:0] bits are 1,1, the PLL generates a frequency determined by the M[7:0], N1[4:0] and N2[2:0] field values shown in Figure 4-1.

The M byte can be programmed with any integer value from 1 to 127. The PLL feedback loop frequency from the voltage controlled oscillator stage is scaled by dividing that frequency by (M+2). See Figure 4-3.

The N byte of each PLL parameter register contains two parameters. N1 is a 5-bit value that can be programmed with any integer value from 1 to 31. The reference frequency is divided by (N1+2) before being fed to the phase detector stage of the PLL.

The second N byte parameter is N2. This is a 3-bit value that can be programmed with any integer value from 0 to 7. This value codes the selection of a frequency divider for the PLL output. This is shown in the following table.

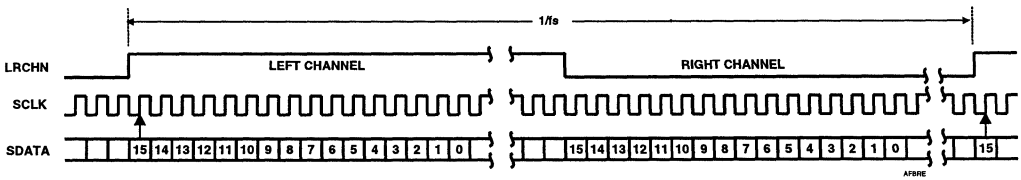


Figure 4-2. First Audio Bits Latched on Rising Edge

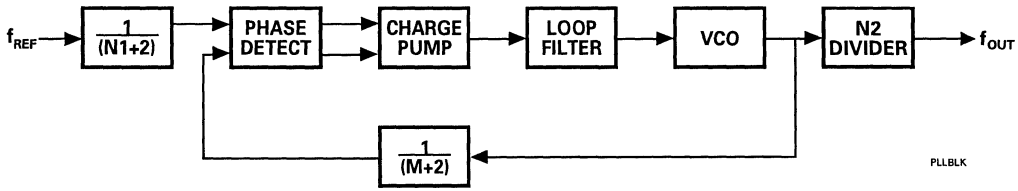


Figure 4-3. PLL Block Diagram

Table 4-2. PLL N2 Parameter Decoding

N2-Divider Code	Frequency Divider
000	8
001	16
010	32
011	64
100	128
101	256
110	512
111	1024

The output frequency resulting from a given set of parameters is specified by the following formula:

$$f_{OUT} = \frac{(M+2)}{(N1+2)\times 2^{N2}\times 8} \times f_{REF}$$

Programmed M and N values should be consistent with the following two constraints:

$$1.\ 65MHz < \frac{(M+2)f_{REF}}{(N1+2)} \leq 130MHz$$

2. min N1 ≥ 1

The following sequence may be followed to arrive at M and N values for any frequency.

1. Calculate the highest possible N2 which does not violate the following constraint:

   $$65MHz < 2^{N2}\times f_{OUT}\times 8 \leq 130MHz$$

2. Start with N1 = 1 and calculate:

   $$M = [\frac{f_{OUT}\times (N1+2)\times 2^{N2}\times 8}{f_{REF}}] - 2$$

3. Using the calculated M and N values, determine if the resulting frequency is within 0.5% of the desired frequency.
4. If the constraint in step 3 is not met, repeat steps 2 and 3 with N1 increased by 1 each time until the constraint in step 3 is met. Note that multiple combinations of M and N are possible for a given output frequency.

If the PLL bit is set to one and one of the three hardwired frequencies is selected (IFS[1:0] not 1,1), the M and N values in the current serial stream are internally latched. A subsequent external frequency selection with FS[1:0] = 1,1 will generate a DACCLK output determined by this most recent M and N value update.

4.5 MUTING

To avoid audible clicks, the Mute bit should be set to 1 before changing the frequency and cleared to 0 after the frequency has been changed.

There are two ways to mute the output:

1.- Set the Mute bit (bit 22 of the left and right data words) to 1. When this is done, Sonic/AD will gradually reduce the sound volume and then (after 4096 LRCHN clock cycles), turn off the sound output com-

pletely. Muting is removed when the mute bit is cleared to 0.

2. Program SDATA to all '0's for more than 4096 LRCHN clock cycles. The muting effect is the same as described above for setting the Mute bit. In this case, muting is removed when any of the SDATA bits is programmed to 1.

Section 5: Layout Recommendations

5.1 POWER AND GROUND PLANES

Figure 5-1 shows the recommended ground plane layout. The analog ground plane is separate from the digital ground plane and the two connect through a single connection.

Figure 5-2 shows the recommended power plane layout. This is the same as for the ground planes except the two power planes are connected by a ferrite bead.

One exception is that the PLL analog supply may require a regulated supply as shown in Figure 5-3. The Zener diode is adequate because the PLL VCO current requirement is small.

Depending on the system design complexity, the DAC +5V supply may need to be regulated. If a voltage regulator is available for other circuits, it could be shared. Otherwise, use an LM78L05.

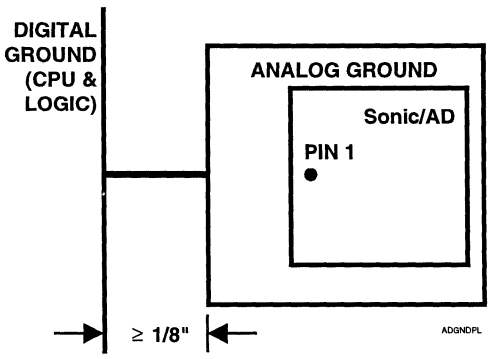


Figure 5-1. Ground Planes

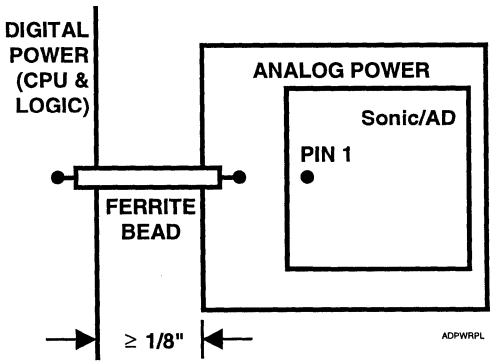
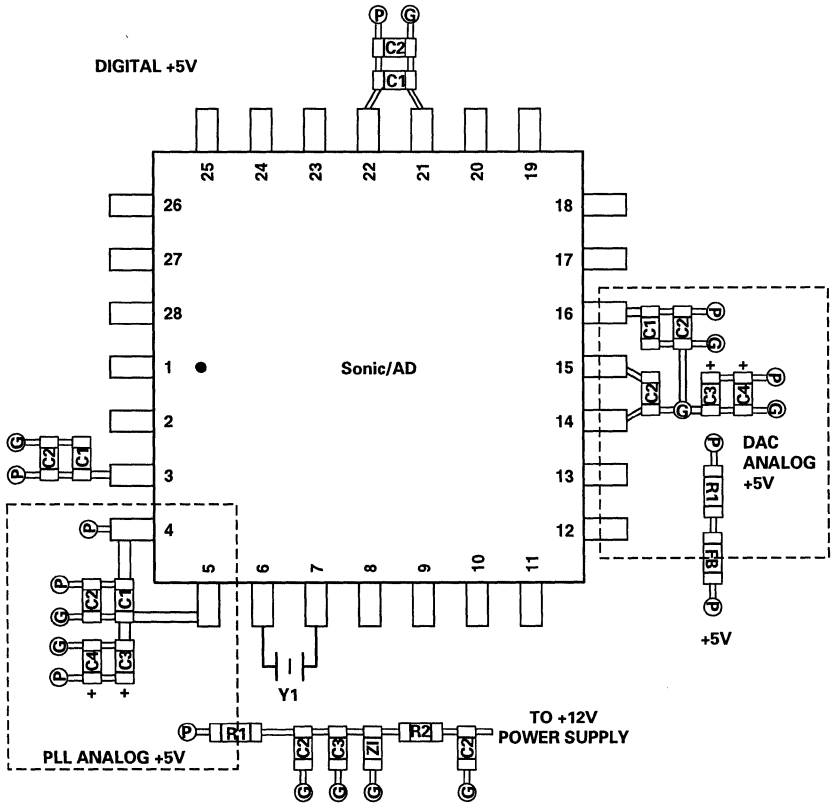


Figure 5-2. Power Planes

5.2 POWER AND GROUND CONNECTIONS

Figure 5-3 shows the recommended power and ground connections.



C1 = 0.01 µF CERAMIC CHIP CAPACITOR
C2 = 0.1 µF CERAMIC CHIP CAPACITOR
C3 = 1.0 µF TANTALUM CAPACITOR
C4 = 10 µF TANTALUM CAPACITOR
R1 = 10Ω RESISTOR
R2 = 68Ω RESISTOR
Y1 = 14.318 MHz PARALLEL CRYSTAL CUT FOR CL = 12 pF
Z1 = 1N4733 ZENER DIODE
FB = FERRITE BEAD

ADLOUT

Figure 5-3. Recommended Power Connections

Section 6: Electrical Characteristics

6.1 MAXIMUM RATINGS

Table 6-1. Maximum Ratings

Ambient Temperature	-40° C to 85° C
Storage Temperature	-65° C to 150° C
Operating Temperature	0° C to 70° C
DC Supply Voltage (analog and digital)	7.0 V
I/O Pin Voltage	GND - 0.5 V to VDD + 0.5 V
Power Dissipation	0.375 W

Warning: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

6.2 POWER DISSIPATION

Table 6-2. Operational Power Dissipation

Parameter	Typ	Unit	Note
Power dissipation (analog and digital)	.26	W	fs = 48 kHz, 500 Hz sine wave

6.3 DC CHARACTERISTICS

Conditions: 5V ± 5%, full-scale output sine wave at 1 kHz, resistive loading = 10 kΩ

Table 6-3. Analog DC Characteristics

Parameter	Min	Typ	Max	Unit
DAC Information				
Resolution		16 bits		
Maximum Accuracy				
Integral Linearity Error		± 1 LSB		
Differential Linearity Error		± 1 LSB		
Monotonicity		Guaranteed		
Coding		Binary (2's complement)		
Power Supply Current (measured at pin)		10		mA
VREF	2.0	2.2	2.4	V
Output Offset Voltage		10		mV
Power Supply Rejection Ratio on AVDD		40		dB

Table 6-4. Digital DC Characteristics (Operating at RoomTemperature)

Symbol	Parameter	Min	Typ.	Max	Unit	Notes
VIL	Supply Low Voltage	- 0.5		0.8	V	
VIH	Supply High Voltage	2.0		VDD+0.5	V	
IIN	Supply Leakage Current	-10		10	µA	@ VI = VDD or VSS
VOL	Output Low Voltage (DACCLK)			0.4	V	@ rated output current
VOH	Output High Voltage (DACCLK)	2.4			V	@ rated output current
IOL	Output Low Current (DACCLK)	3.2			mA	@ rated output voltage
IOH	Output High Current (DACCLK)			-400	µA	@ rated output voltage
IDD	Digital Power Supply Current		42		mA	fs = 48 kHz, 500 Hz sine wave
CIN	Input Capacitance			7	pF	

6.4 AC CHARACTERISTICS

Conditions: 5V ± 5%, full-scale output sine wave at 1 kHz, resistive loading = 10 kΩ, bandwidth 20 Hz to 20 kHz.

Table 6-5. Analog AC Characteristics

Parameter	Min	Typ	Max	Unit
Signal to Noise Ratio		86		dB
Dynamic Range		90		dB
Total Harmonic Distortion (THD)		0.04		%
Frequency Response		± 0.5		dB
Full-scale Output Voltage	2.5	2.8		VPP
Out of Band Energy (22 kHz to 100 kHz)		-60		dB
Capacitive Load			100	pF

Table 6-6. Digital AC Characteristics

Parameter	Min	Typ	Max	Unit
Crystal Frequency (Default = 14.31818 MHz)	-0.01		0.01	%
Input Clock Frequency (XIN)	14	14.318	15	MHz
Input Clock Duty Cycle (XIN)	40	50	60	%
Custom Sampling Frequency (f_S)	4		50	kHz
Internal Clock Out Duty Cycle	40	50	60	%
Frequency Change Lock Time			500	µs
Cycle to Cycle Jitter (DACCLK) 1σ		80	250	ps
Group Delay		30/fs		s

6.5 AC TIMING

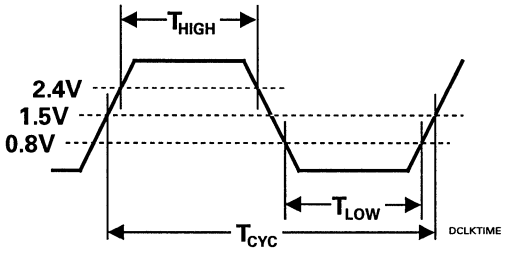


Figure 6-1. Clock Waveform Timing

Table 6-7. Clock Waveform Timing

Symbol	Parameter	Min	Typ	Max	Units	Notes
T_{CYC}	SCLK Cycle Time		1/(64xf_S)		s	
	DACCLK Cycle Time		1/(256xf_S)		s	
	LRCHN Cycle Time		1/f_S		s	
T_{HIGH}	SCLK High Time	312			ns	1
	DACCLK High Time	78			ns	1
	LRCHN High Time	20			µs	1
T_{LOW}	SCLK Low Time	312			ns	1
	DACCLK Low Time	78			ns	1
	LRCHN Low Time	20			µs	1
	SCLK Slew Rate		2		V/ns	
	DACCLK Slew Rate		2		V/ns	
	LRCHN Slew Rate		2		V/ns	

Note:

1. 50 % duty cycle

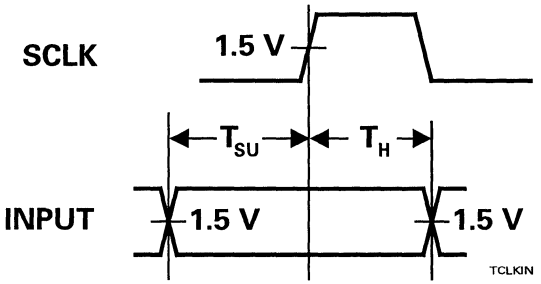


Figure 6-2. Input Timing

Table 6-8. SCLK-Referenced Input Timing

Symbol	Parameter	Min	Units
T_{SU}	SDATA, LRCHN setup	10	ns
T_H	SDATA, LRCHN hold	10	ns

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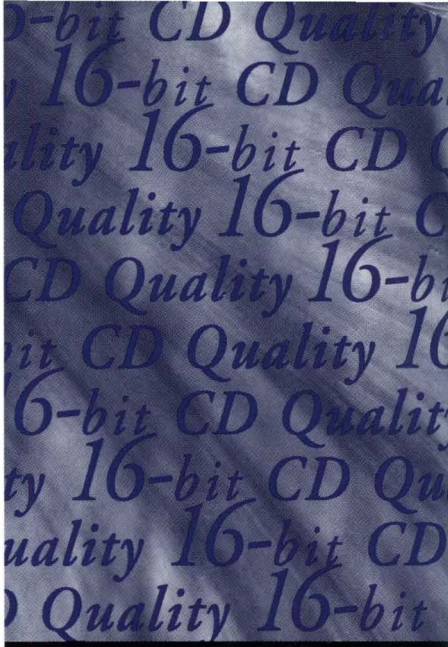

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