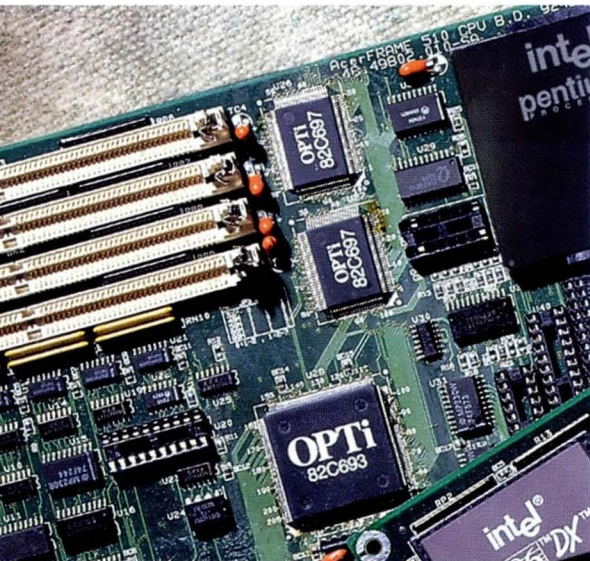
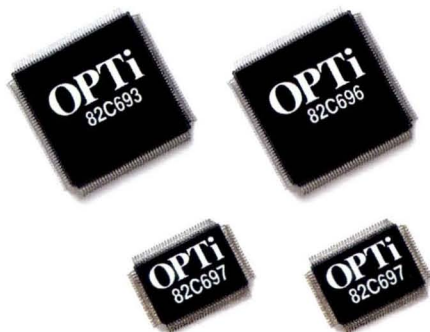


# PENTIUM

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## .....Pentium™ $\mu$ P Write Back Cache EISA .....

**E**ISA provides a high performance 32-bit migration path for PC/ATs based on the 32-bit microprocessor architecture from Intel. OPTi's EISA Pentium chipset provides unprecedented performance, features and cost advantages for discriminating OEMs. While the EISA Pentium chipset has been designed to support the full range of Pentium microprocessors, it is optimized especially for Pentium processors which are extremely sensitive to external wait states. This patented Write Back cache implementation makes this the fastest Pentium chipset available and clearly distinguishes itself from the competition. In addition to the WB cache, Systems Integrators finally have a chipset that directly supports both single and double density x36 SIMMs resulting in remarkable DRAM integration. The EISA Pentium is targeted at OEMs who must provide a low cost, small-footprint EISA/PC yet still provide the performance and rich feature set necessary to differentiate themselves from the rest of the pack.

The OPTi chipset craftsman, with their proven track record in high performance PC/AT chipsets are proud to offer the EISA Pentium - and help PC OEMs extend their AT product lines with top-of-the-line EISA PCs.

### Features/Benefits

- Fastest 100% EISA compatible 60/66 MHz Pentium write back chipset
- Patented write back controller
  - Flexible cache sizes - 128K to 1 MB
- High performance, closely coupled, 8 bank DRAM controller
  - Direct connections for both single and double density x36 SIMMs
  - 2MB - 256MB main memory with just 8 SIMMs
- Total system performance tuning features
  - Hidden refresh
  - Programmable holes in memory
  - CPU bus local device support
  - Fast GATEA20/transparent CPU reset
  - Synchronous EISA bus clock with relaxed skew requirements
  - Video/system BIOS shadowable and cacheable
- Complete EISA motherboard
- Low power, high speed CMOS technology



OPTi



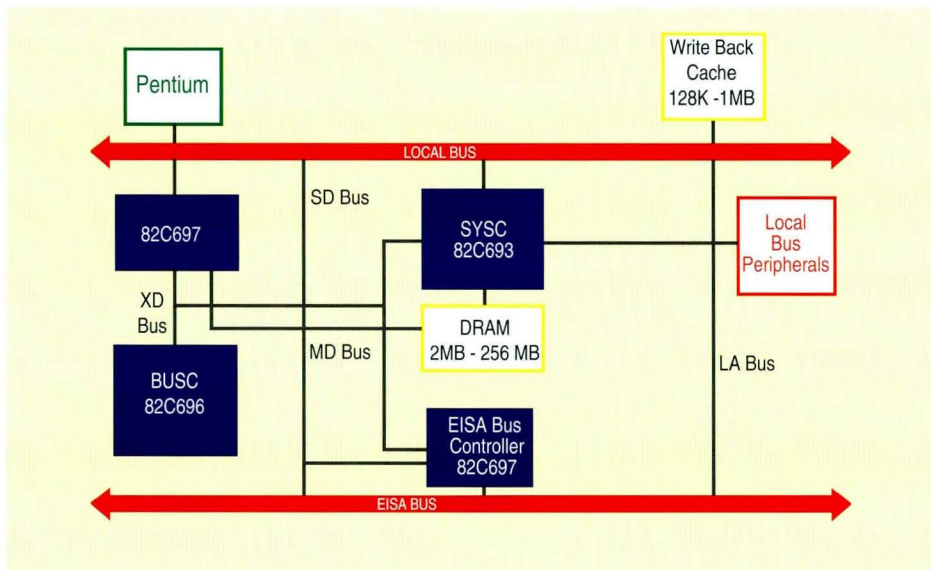
The OPTi EISA Pentium chipset consists of two 208-pin QFP devices: the SYSC, the BUSC and 2 100-pin DBC buffer chips.

The SYSC write back-memory cache controller - 82C693 - controls the memory subsystem for EISA bus controller accesses between the CPU, EISA/ISA masters and DMA devices. The memory subsystem consists of up to 8 banks of DRAM with hidden refresh and from 128K to 1MB of write back cache translates bus control signals and addresses between the CPU, EISA, ISA and DMA masters and slaves.

The BUSC - 82C696 - integrates the motherboard I/O logic defined by the EISA specification: two 8254 timers, EISA NMI/time-out logic, two EISA 8259 interrupt controllers, a 32-bit DMA controller and the EISA system arbiter.

The Data Bus Controller - 82C697 - integrates data buffers and provides control for synchronous data pipelining. It also provides control for bus conversion, Parity generation and checking and an EISA ID register.

The high levels of integration and performance provided by these 4 devices enable OEMs to plan the evolution of their Pentium PC/ATs to EISA/PCs. This chipset enables OEMs to move ahead aggressively with high performance EISA platforms in order to participate successfully in the migration of 32-bit PCs to EISA.



**OPTi Baby  
EISA 486  
Pentium -  
robust, high  
performance  
design for  
high volume  
EISA PCs.**

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