

Description

The VRC4171A™ is a companion chip to NEC's 64-bit VR41xx™ family of MIPS® RISC microprocessors. Together, these two devices form the essential engine for most Windows® CE-based handheld products.

Features

- **Processor Interface**
 - LCD module: *RD, *WR, *LCDCS and LCDRDY signals from the VR41xx
 - Other modules: mini-ISA-like 16-bit bus interface (as defined in the VR41xx)
 - 256 x 18-bit on-chip color palette RAM for STN, DSTN, and TFT color panels
 - On-chip hardware cursor control (32 x 32 x 2)

- **LCD Panel Support**
 - 240- and 480-line single scans
 - 480-line dual scans
 - STN, DSTN, and TFT color panels
 - Nonindexed, true color (R, G, B): 15-bit (5-5-5) and 16-bit (5-6-5)
 - Controller functions (320 x 240, 480 x 240, 640 x 240, and 640 x 480)
 - Monochrome: up to 16 gray-scale levels (1, 2, or 4 bits/pixel)
 - Color depth: 1, 2, 4, 5, 6, 8, or 16 bits/pixel

- **Frame Buffer Memory**
 - One or two 3.3-volt 256K x 16-bit DRAMs (512K or 1 MB)
 - One 1 MB x 16-bit DRAM (2 MB)

- **PC Card™ Slots (up to two)**
 - PC Card or CompactFlash™ with adapter
 - PC Card or CompactFlash or Miniature Card™
 - PC Card controller: compliant with ExCA and PCMCIA release 2.1
 - CompactFlash controller: compliant with release 1.1
 - Miniature Card controller: compliant with release 1 (flash/ROM only)

- **Other Features**
 - Up to four general-purpose I/O (GPIO) pins *or* up to two GPIO pins and two PCS pins
 - 5-volt tolerance for LCD panel, frame buffer, and PC Card interface signals
 - 208-pin LQFP package
 - 3.3-volt ±5% operation

Figure 1. Internal Block Diagram

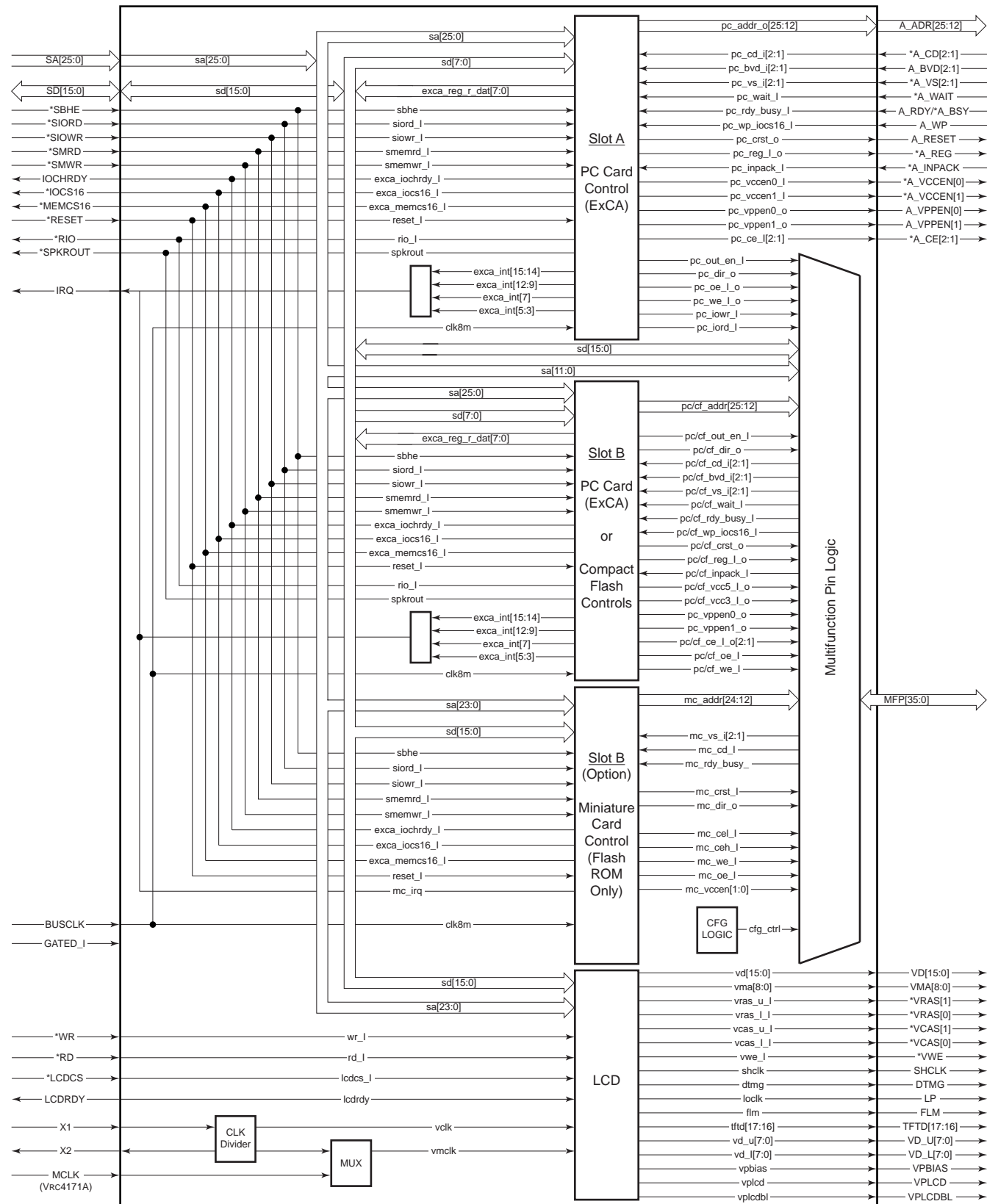
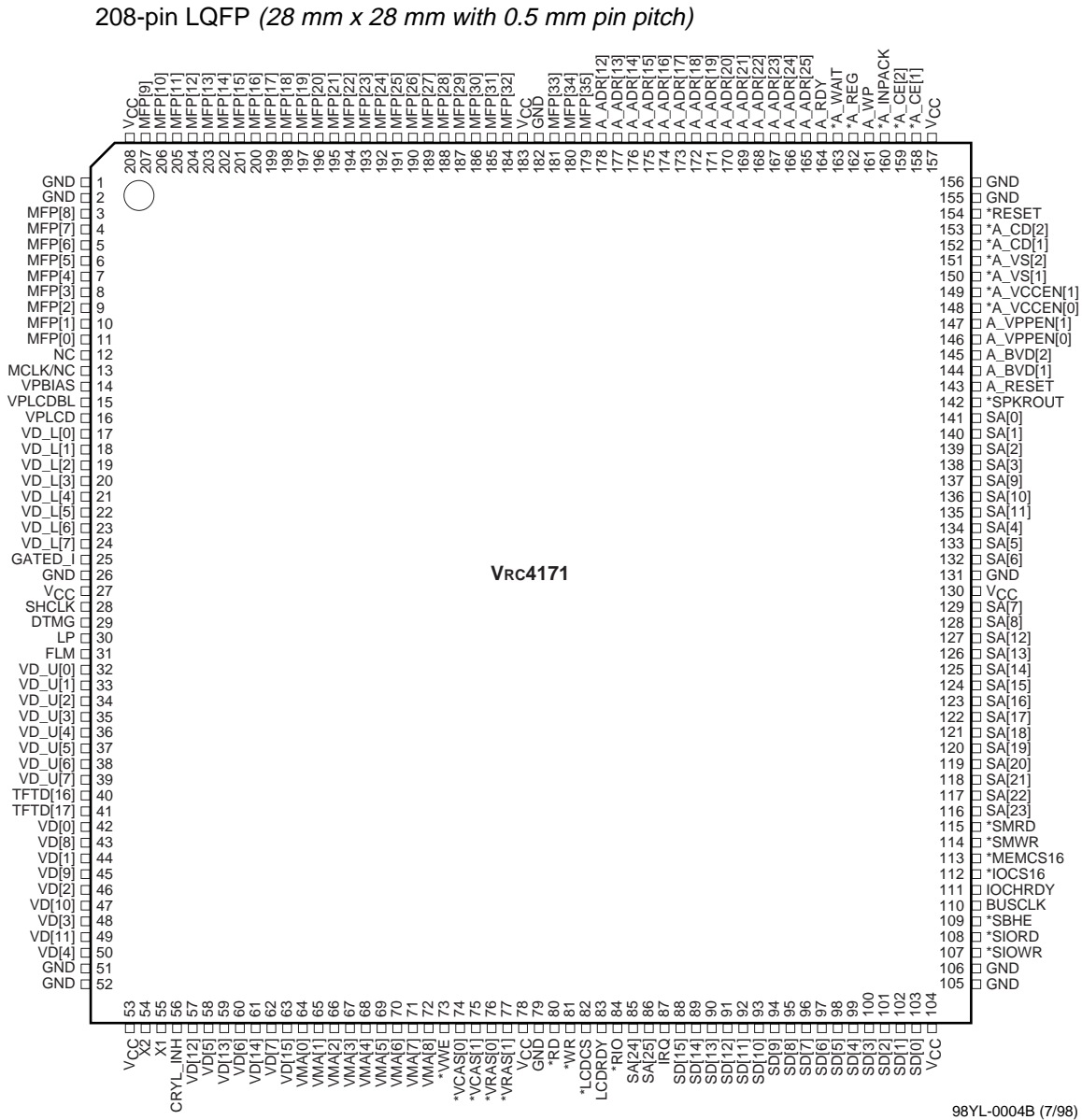


Figure 2. Pin Configuration



Refer to the *Vrc4171A Companion Chip User's Manual* (document no. U13275EU1V0UM00) for a detailed description of pin functions.

Table 1. Absolute Maximum Ratings

Parameter	Specification
Power supply voltage, V_{DD}	-0.5 to +4.6 volts
Input voltage, V_I	
3.3-volt input buffer (at $V_I < V_{DD} + 0.5$ volt)	-0.5 to +4.6 volts
3.3-volt fail-safe buffer (at $V_I < V_{DD} + 0.5$ volt)	-0.5 to +4.6 volts
5-volt tolerant (at $V_I < V_{DD} + 3.0$ volts)	-0.5 to +6.6 volts
Output voltage, V_O	
3.3-volt output buffer (at $V_O < V_{DD} + 0.5$ volt)	-0.5 to +4.6 volts
5-volt tolerant buffer (at $V_O < V_{DD} + 3.0$ volts)	-0.5 to +6.6 volts
5-volt open-drain output buffer (at $V_O < V_{DD} + 3.0$ volts)	-0.5 to +6.6 volts
Latch-up current, I_{LATCH}	>1 A (typical)
Operating temperature, T_{OPT}	-40 to +85°C
Storage temperature, T_{STG}	-65 to +125°C

Caution: Exposure to absolute maximum ratings for extended periods may affect device reliability; exceeding the rating could cause permanent damage. Do not operate the device outside the recommended operating conditions.

Table 2. Recommended Operating Conditions ($V_{DD} = 3.3 V \pm 0.165 V$; $T_A = 0$ to +70°C)

Parameter	Symbol	3.3-Volt Interface Block			5-Volt Interface Block		Unit
		Min.	Typ.	Max.	Min.	Max.	
I/O power supply voltage	V_{DD}	3.135	3.3	3.465			V
Junction temperature	T_j	0		+100	0	+100	°C
High-level input voltage	V_{IH}	2.0		V_{DD}	2.0	5.5	V
Low-level input voltage	V_{IL}	0		0.8	0	0.8	V
Positive trigger voltage	V_P	1.50		2.70	2.20	2.55	V
Negative trigger voltage	V_N	0.60		1.4	0.84	1.01	V
Hysteresis voltage	V_H	1.10		1.5	1.10	1.5	V
Input rise/fall time	t_r, t_f	0		200	0	200	ns
Input rise/fall time, Schmitt	t_r, t_f	0		10	0	10	ns
I/O power supply voltage	V_{DD}						

Table 3. Input/Output Capacitance ($V_{DD} = V_I = 0 V$; $f = 1 MHz$)

Terminal	Symbol	Typ.	Max.	Unit
Input	C_{IN}	10	20	pF
Output	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	10	20	pF

Note: Values include package capacitance.

Table 4. DC Characteristics ($V_{DD} = 3.3 V \pm 0.165 V$; $T_j = 0$ to $+70^\circ C$)

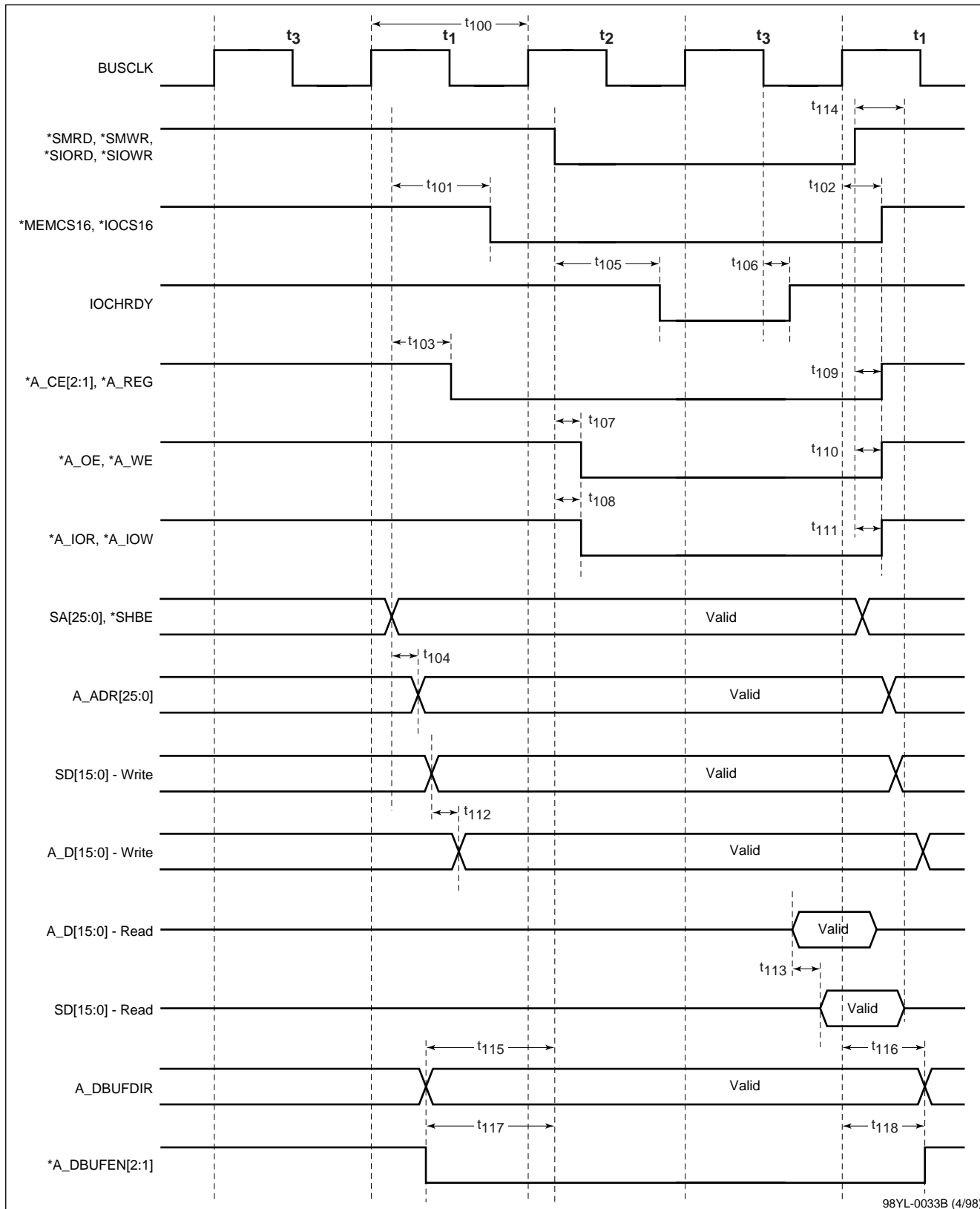
Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
All Buffer Types						
Output current, low (3 mA)	I_{OL}	3			mA	$V_{OL} = 0.4$ volt
Output current, low (6 mA)	I_{OL}	6			mA	$V_{OL} = 0.4$ volt
5-Volt-Tolerant Block						
Output current, high (3 mA)	I_{OH}	-3			mA	$V_{OH} = 2.4$ volts
Output current, high (6 mA)	I_{OH}	-3			mA	$V_{OH} = 2.4$ volts
3.3-Volt Interface Block						
Output current, high (3 mA)	I_{OH}	-3			mA	$V_{OH} = 2.4$ volts
Output current, high (6 mA)	I_{OH}	-6			mA	$V_{OH} = 2.4$ volts
Output voltage, high	V_{OH}	$0.9 V_{DD}$			V	$I_{OH} = -500 \mu A$
Output voltage, low	V_{OL}			$0.1 V_{DD}$	V	$I_{OL} = 1500 \mu A$
Vcc Current						
LCD only	I_{CC1}		60		mA	$V_{CC} = 3.3$ volts
						MCLK = 60 MHz
			VCLK = 20 MHz			
			PC Card off			
LCD plus PC Card active	I_{CC2}		90		mA	$V_{CC} = 3.3$ volts
						MCLK = 60 MHz
			VCLK = 20 MHz			
			BUSCLK = 8 MHz			
Hibernate mode	I_{CC3}		100		μA	Gated_I enable
						CRYL-INH enable
			LCD panel off			
			Frame buffer PC Card self-refresh off			
			95		mA	MCLK = 50 MHz
						VCLK = 25 MHz

Table 5. Clock Operation

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
X1, X2 crystal input	f_{xx}			50	MHz	Crystal oscillator
X2 clock input (Note)	F_x			66	MHz	External clock with 60 ns DRAMs
MCLK clock input	F_m			80	MHz	External clock with 50 ns DRAMs
				66.6	MHz	External clock with 60 ns DRAMs

Note: Leave X1 open with no MCLK input.

Figure 3. Preliminary Uncharacterized AC Timing



98YL-0033B (4/98)

Table 6. Uncharacterized AC Characteristics (refer to Figure 3)

Parameter	Symbol	Min.	Typ.	Max.	Unit
BUSCLK clock period	t100		125		ns
Slot A Only					
*MEMCS16, *IOCS16 ↓ delay from SA[23:0] address and *SBHE valid	t101		8	15	ns
*MEMCS16, *IOCS16 ↓ hold time from BUSCLK ↑	t102	3	4		ns
*A_CE[2:1], *A_REG ↓ delay from SA[23:0] address and *SBHE valid	t103		9	15	ns
A_ADR[25:0] address valid delay from SA[23:0] address and *SBHE valid	t104		5	9	ns
IOCHRDY valid delay from *SMRD, *SMWR, *SIORD, *SIOWR ↓	t105		4	7	ns
IOCHRDY hold time from BUSCLK ↓	t106	4	7		ns
*A_OE, *A_WE ↓ delay from *SMRD, *SMWR ↓	t107		6	10	ns
*A_IOR, *A_IOW ↓ delay from *SIORD, *SIOWR ↓	t108		7	12	ns
*A_CE[2:1], *A_REG ↑ delay from *SMRD, *SMWR, *SIORD, *SIOWR ↑	t109		9	15	ns
*A_OE, *A_WE ↑ delay from *SMRD, *SMWR ↑	t110		6	10	ns
*A_IOR, *A_IOW ↑ delay from *SIORD, *SIOWR ↑	t111		7	12	ns
SD[15:0] data valid to A_D[15:0] valid delay (write cycle)	t112		13	17	ns
SD[15:0] data valid delay from A_D[15:0] valid (read cycle)	t113		6	9	ns
SD[15:0] data hold time from *SMRD, *SMWR, *SIORD, *SIOWR ↑ (read cycle)	t114	4	6	9	ns
Slot A in Dual Slot Mode					
A_DBUFDIR delay from *SMRD, *SMWR, *SIORD, *SIOWR ↓	t115		6	9	ns
A_DBUFDIR hold time to *SMRD, *SMWR, *SIORD, *SIOWR ↑	t116	4	7		ns
A_DBUFEN[2:1] delay from *SMRD, *SMWR, *SIORD, *SIOWR ↓	t117		9	13	ns
A_DBUFEN[2:1] hold time to *SMRD, *SMWR, *SIORD, *SIOWR ↑	t118	5	8		ns

Note: All values are subject to change without notice.

Figure 4. DRAM Read Cycle

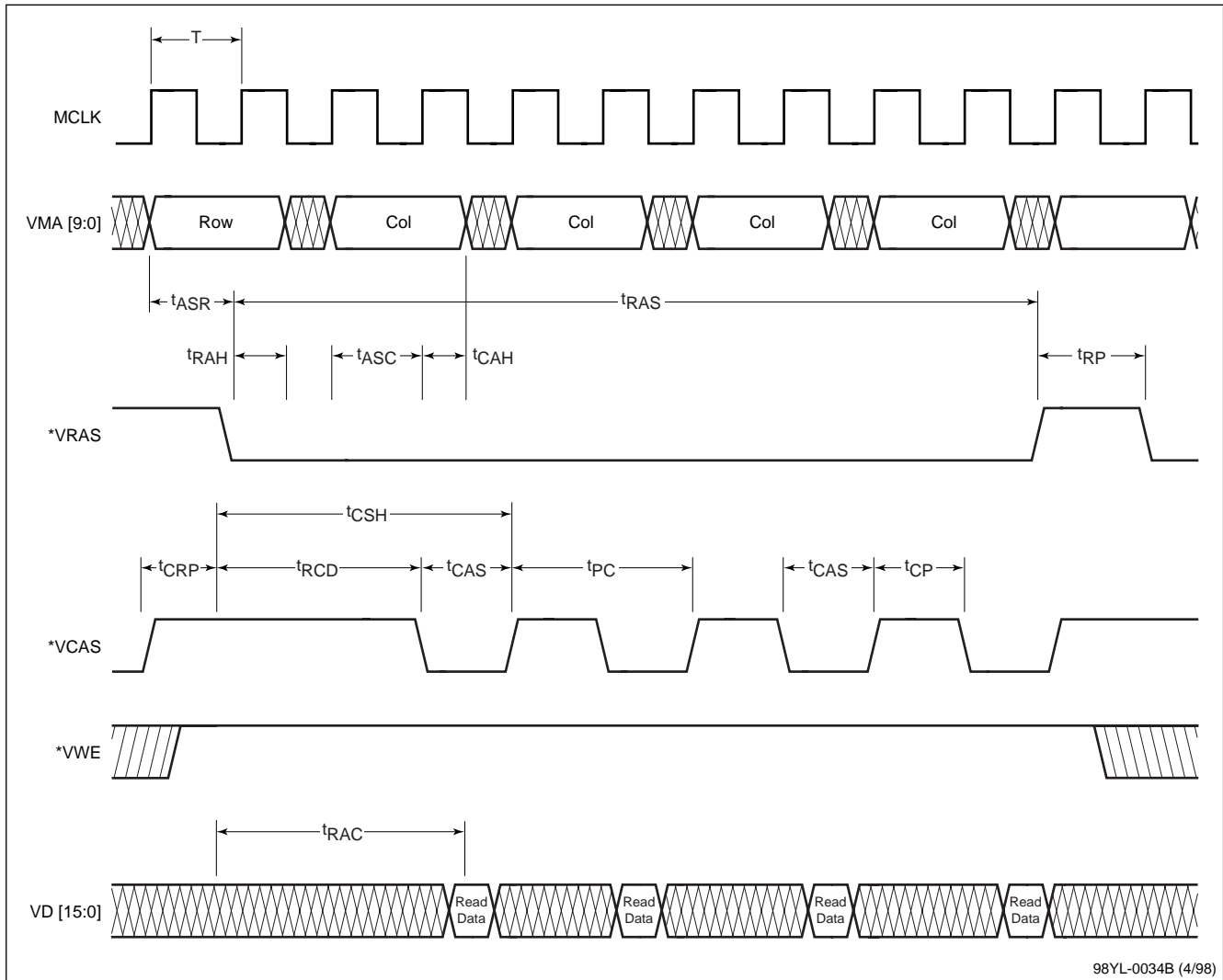


Figure 5. DRAM Write Cycle

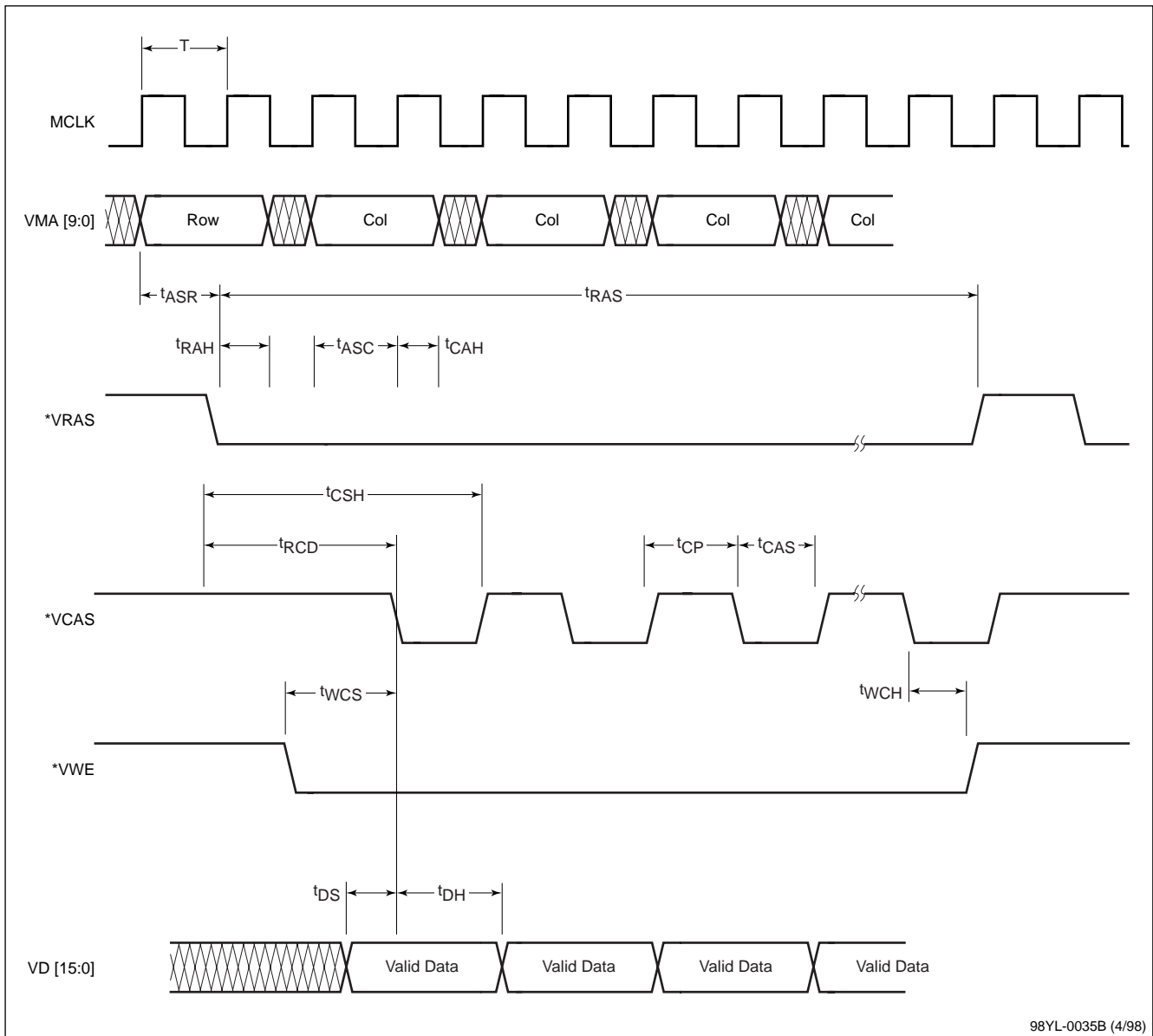


Table 7. DRAM Read Cycle Characteristics (refer to Figure 4)

Description	Symbol	Min.	Max.	Unit
Row address setup time	t _{ASR}	T		ns
Row address hold time	t _{RAH}	T-5		ns
Column address setup	t _{ASC}	T		ns
Column address hold time	t _{CAH}	T		ns
*VRAS pulse width	t _{RAS}	4.5T		ns
*VRAS precharge time	t _{RP}	3.5 T-3		ns
*VRAS to *VCAS delay time	t _{RCD}	3.5 T + 2		ns
*VCAS hold time	t _{CSH}	3 T + 2		ns
*VCAS pulse width	t _{CAS}	T - 1		ns
*VCAS precharge time	t _{CP}	T		ns
Data access time from *VRAS	t _{RAC}		4.5 T + 3	ns
Data access time from *VCAS	t _{CAC}		T + 3	ns

Note: MCLK is from either XTAL on X1 and X2 or from the external oscillator.

Table 8. DRAM Write Cycle Characteristics (refer to Figure 5)

Description	Symbol	Min.	Max.	Unit
Row address setup time	t _{ASR}	T		ns
Row address hold time	t _{RAH}	T-5		ns
Column address setup	t _{ASC}	T		ns
Column address hold time	t _{CAH}	T		ns
*VRAS pulse width	t _{RAS}	4.5 T		ns
*VRAS precharge time	t _{RP}	3.5 T-3		ns
*VCAS to *VRAS precharge time	t _{CRP}	3 T		ns
*VCAS hold time	t _{CSH}	3 T+2		ns
*VCAS pulse width	t _{CAS}	T- 1		ns
*VCAS precharge time	t _{CP}	T		ns
*VRAS to *VCAS delay time	t _{RCD}	3.5 T+2		ns
Write pulse setup time from *VCAS	t _{WCS}	2T		ns
Write pulse hold time from *VCAS	t _{WCH}	T		ns
Data setup time to *VCAS	t _{DS}	8		ns
Data hold time to *VCAS	t _{DH}	12		ns

Figure 6. System Bus Cycle

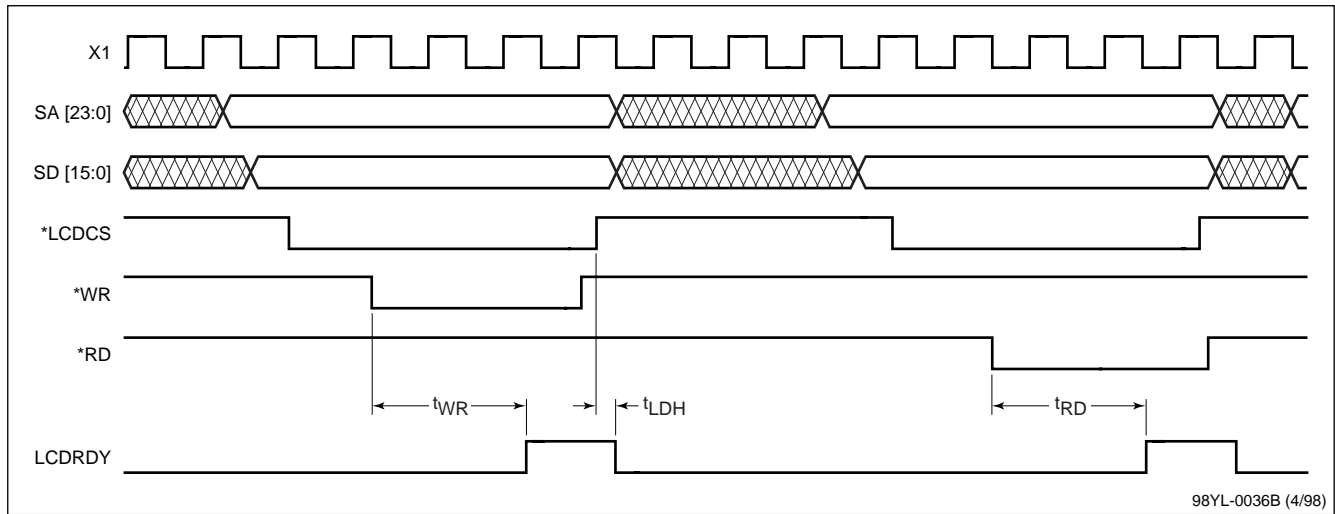


Table 9. System Bus Cycle Characteristics (refer to Figure 6)

Parameter	Symbol	Min	Max	Unit
LCDRDY to *LCDCS hold time	t_{LDH}	3	5	ns
*RD low to LCDRDY high time	t_{RD}	20	40	ns
*WR_L low to LCDRDY high time	t_{WR}	20	40	ns

Figure 7. *VCAS Before *VRAS Refresh Cycle

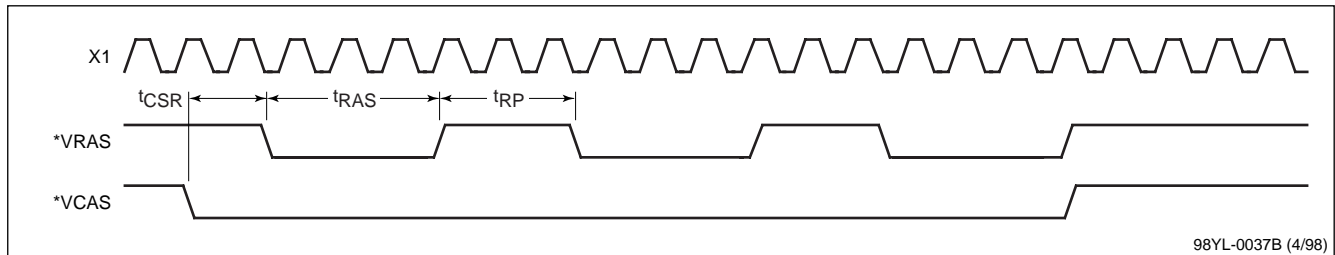


Table 10. *VCAS Before *VRAS Refresh Characteristics (refer to Figure 7)

Parameter	Symbol	Min	Max	Unit
*VCAS setup time	t_{CSR}	$1.5 T - 2$		ns
*VRAS pulse width	t_{RAS}	$3.5 T$		ns
*VRAS precharge time	t_{RP}	$3.5 T - 2$		ns

Figure 8. Video Display Timing for TFT Panel

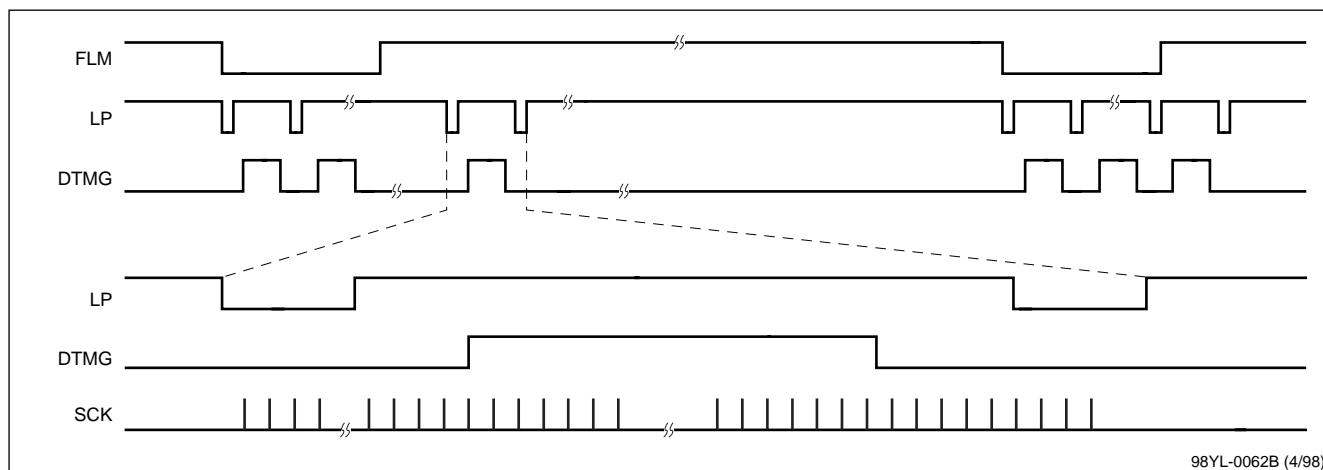
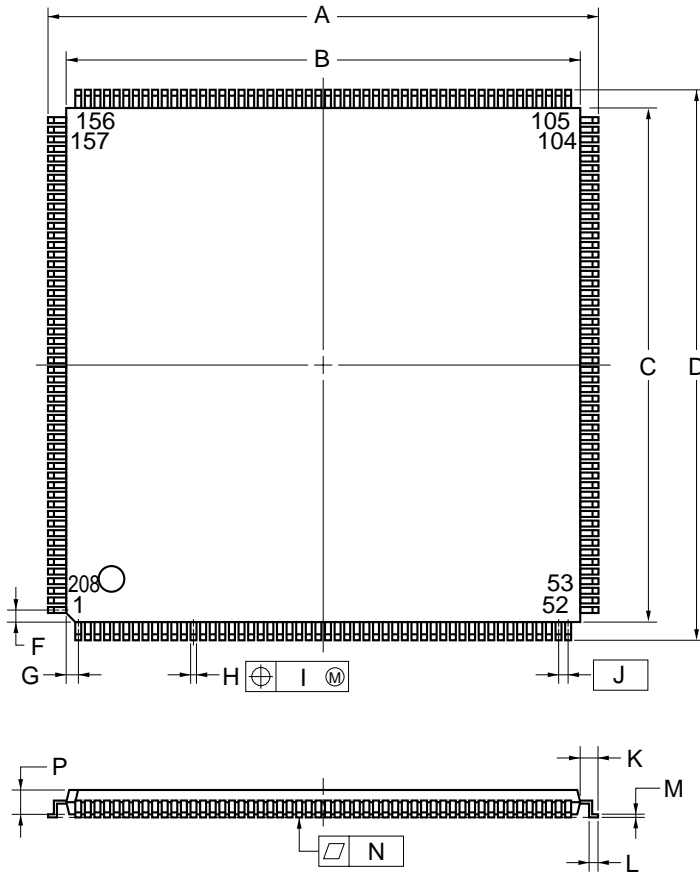


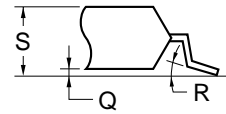
Figure 9. 208-Pin LQFP



ITEM	MILLIMETERS	INCHES
A	30.0±0.2	1.181±0.008
B	28.0±0.2	1.102 ^{+0.009} _{-0.008}
C	28.0±0.2	1.102 ^{+0.009} _{-0.008}
D	30.0±0.2	1.181±0.008
F	1.25	0.049
G	1.25	0.049
H	0.22 ^{+0.05} _{-0.04}	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	0.039 ^{+0.009} _{-0.008}
L	0.5±0.2	0.020 ^{+0.008} _{-0.009}
M	0.145 ^{+0.055} _{-0.045}	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	3° ^{+7°} _{-3°}	3° ^{+7°} _{-3°}
S	1.7 MAX.	0.067 MAX.

S208GD-50-8EU-2

detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

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