PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD30100

VR4100™
64-BIT MICROPROCESSOR

The μPD30100 (VR4100) is a high-performance, 64-bit RISC (Reduced Instruction Set Computer) type microprocessor employing the RISC architecture developed by MIPS.

The VR4100 is compact and consumes little power so that it can be used in battery-driven, high-performance portable systems. In addition, a multiplier circuit is provided to increase the speed.

Detailed functions are described in the following manual. Make sure to read this manual when you are designing systems.

- VR4100 User's Manual (U10050E)

FEATURES

- Employs MIPS 64-bit RISC architecture
- High-speed processing
  - 5-stage pipelining
  - Multiplier circuit
- Instruction set compatible with VR4000™ series (conforming to MIPS-I/II/III)
  - Sum-of-products operation instructions added
  - Floating-point operation instructions deleted
- Low power consumption
- Supports three power control modes in addition to normal operation modes
- Virtual memory management unit (MMU)
- 32-bit address/data multiplexed bus facilitating system designing
- Supply voltage: 2.2 to 3.6 V
- Package: 100-pin plastic TQFP

APPLICATIONS

- Battery-driven portable systems
- Embedded controller, etc.

ORDERING INFORMATION ★

Part Number	Package
μPD30100GC-40-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)

The information in this document is subject to change without notice.

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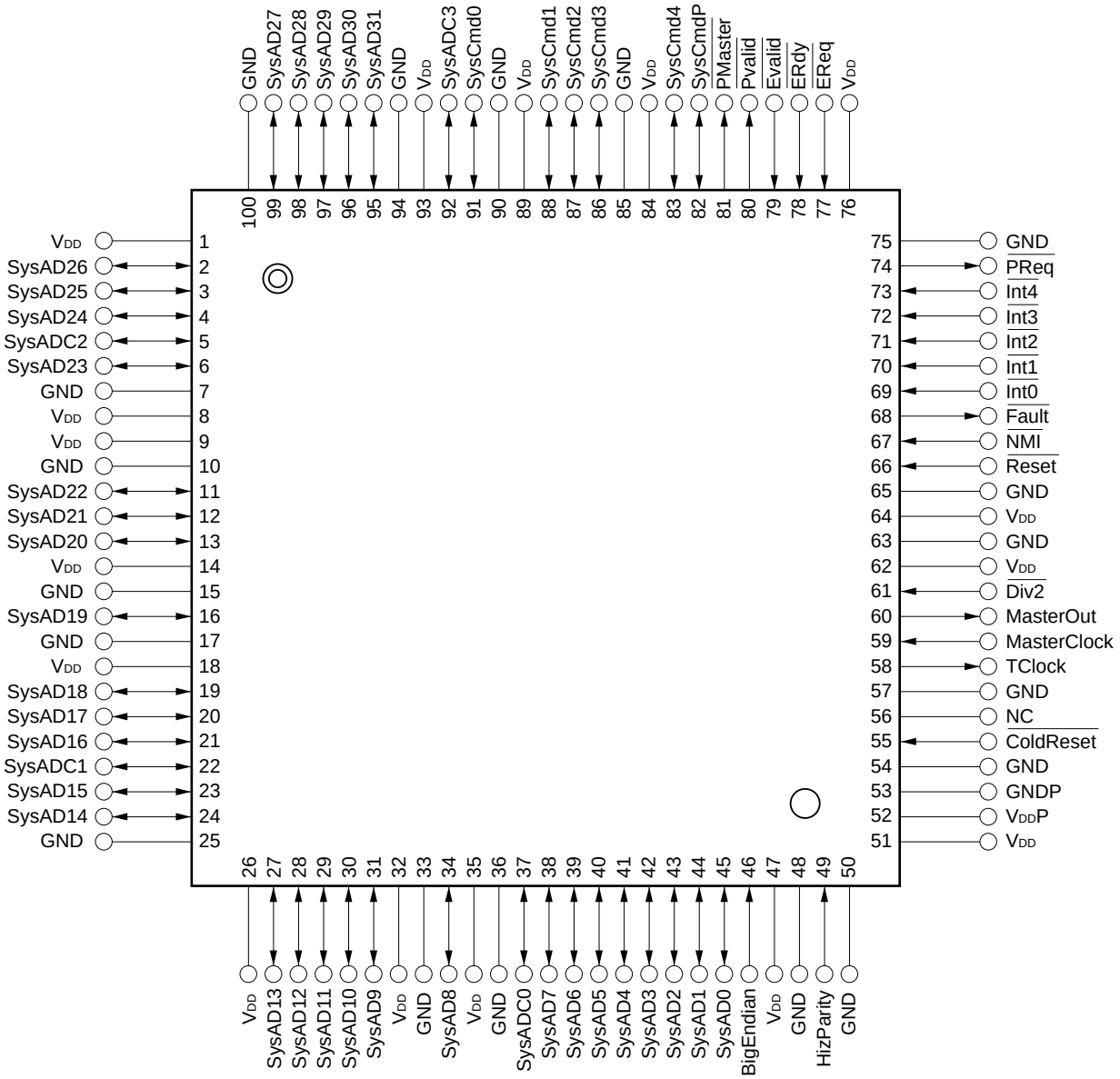
The mark ★ shows major revised points.

PIN CONFIGURATION

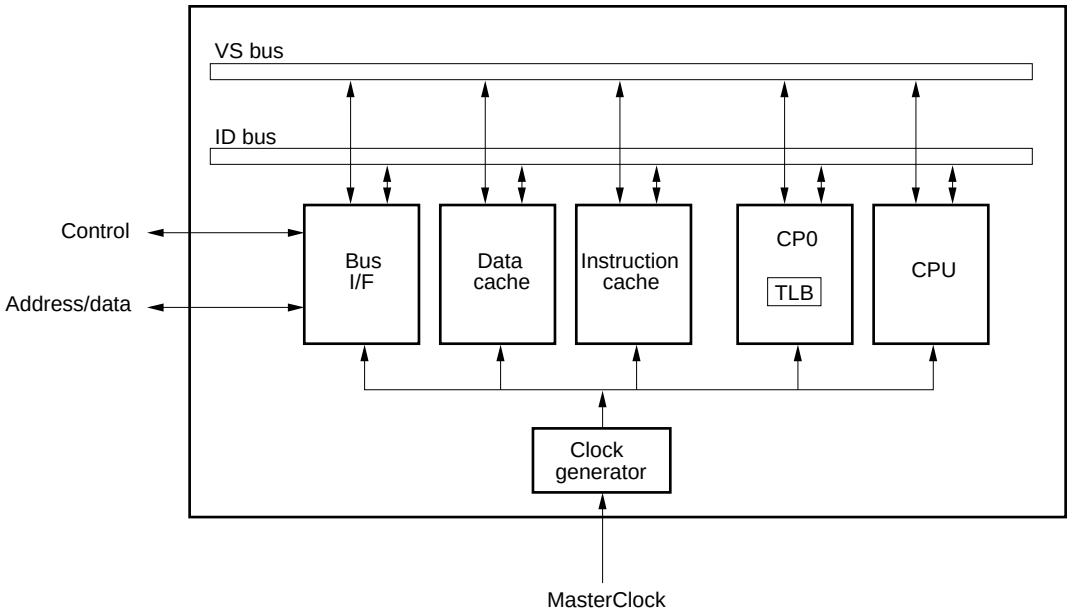
- **100-pin plastic QFP (fine pitch) (14 × 14 mm)**
- **μPD30100GC-40-7EA**



PIN NAMES

BigEndian	:	Big Endian
$\overline{\text{ColdReset}}$	:	Cold Reset
$\overline{\text{Div2}}$	:	Divide by 2
$\overline{\text{ERdy}}$	:	External Ready
$\overline{\text{EReq}}$	:	External Request
$\overline{\text{EValid}}$	:	External Valid
$\overline{\text{Fault}}$	:	Fault
HizParity	:	Hi Impedance Parity
$\overline{\text{Int}}$(4:0)	:	Interrupt Request
MasterClock	:	Master Clock
MasterOut	:	Master Clock Out
NC	:	No Connection
$\overline{\text{NMI}}$	:	Non-maskable Interrupt Request
$\overline{\text{PMaster}}$	:	Processor Master
$\overline{\text{PReq}}$	:	Processor Request
$\overline{\text{PValid}}$	:	Processor Valid
$\overline{\text{Reset}}$	:	Reset
SysAD(31:0)	:	System Address/Data Bus
SysADC(3:0)	:	System Address/Data Check
SysCmd (4:0)	:	System Command/Data ID Bus
SysCmdP	:	System Command Parity
TClock	:	Transmit Clock
V_{DD}	:	Power Supply
GND	:	Ground
V_{DD}P	:	V_{DD} for PLL
GNDP	:	GND for PLL

INTERNAL BLOCK DIAGRAM



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1. PIN FUNCTIONS

Pin Name	I/O	Function
SysAD (31:0)	I/O	System address/data bus. 32-bit bus for communication between processor and external agent.
SysADC (3:0)	I/O	System address/data check bus. 4-bit bus for checking SysAD bus.
SysCmd (4:0)	I/O	System command/data ID bus. 5-bit bus for communication of commands and data identifiers between processor and external agent.
SysCmdP	I/O	System command/data ID bus parity. 1-bit bus even number parity bit for SysCmd.
$\overline{\text{EValid}}$	Input	External valid. Signal indicating that external agent has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{PValid}}$	Output	Processor valid. Signal indicating that processor has transmitted valid address or data onto SysAD bus and valid command or data identifier onto SysCmd bus.
$\overline{\text{EReq}}$	Input	External request. Signal used by external agent to request for issuance by system interface.
$\overline{\text{PReq}}$	Output	Processor request. Signal used by processor to request for issuance by system interface.
$\overline{\text{PMaster}}$	Output	Processor master. Signal indicating that processor controls system interface.
$\overline{\text{ERdy}}$	Input	External ready. Signal indicating that external agent can accept processor request.
$\overline{\text{Fault}}$	Output	Fault. Signal indicating that a parity error has occurred in SysCmd bus.
$\overline{\text{Int}}$ (4:0)	Input	Interrupt. General-purpose processor interrupt requests whose input statuses can be confirmed by bits 14 through 10 of cause register.
$\overline{\text{NMI}}$	Input	Non-maskable interrupt. Interrupt request that cannot be masked.
$\overline{\text{ColdReset}}$	Input	Cold reset. Signal that initializes internal status of processor.
$\overline{\text{Reset}}$	Input	Reset. Signal that generates reset exception without initializing internal status of processor.
MasterClock	Input	Master clock. Clock input signal to processor.
MasterOut	Output	Master clock output. Output of master clock synchronized with master clock.
TClock	Output	Transmit clock. Transmit clock of system interface.

Pin Name	I/O	Function
BigEndian	Input	Big Endian. Switches endian mode of system interface. Sampled at cold reset. Do not change the level of this pin after cold reset. ★
$\overline{\text{Div2}}$	Input	Operation speed of system interface. Switches the frequency divisor for the pipeline clock for the system interface frequency. Fix the level of this pin on power application. ★
HizParity	Input	High impedance parity mode. Determines whether the output of the parity pins (SysADC (3:0), SysCmdP) is set to high impedance and the external bus parity check is stopped. Fix the level of this pin on power application. ★
$V_{DD}P$	–	PLL V_{DD}. Power supply for internal PLL.
GNDP	–	PLL GND. Ground for internal PLL.
V_{DD}	–	Positive power supply pin.
GND	–	Ground pin.

2. INTERNAL BLOCK

(1) Execution unit

Executes integer operation instructions. This unit is provided with the 64-bit register file and data path.

(2) Coprocessor 0 (CP0)

This coprocessor is provided with the following:

- Exception processing unit
- Memory management unit
  The memory management unit converts virtual addresses into physical addresses and checks memory access between different memory segments (kernel, supervisor, and user).

TLB (translation lookaside buffer) converts virtual addresses into physical addresses.
The VR4100 supports five types of page size, 1K byte, 4K bytes, 16K bytes, 64K bytes and 256K bytes, with VSIZE (virtual address) = 40 and PSIZE = (physical address) = 32. TLB has 32 entries. Each entry is mapped to an even/odd page of a page frame number.
The exception processing unit is provided with system control coprocessor registers. For the data format of each register, refer to **3.5 System Control Coprocessor (CP0)**.

(3) Pipeline control

The pipeline is controlled and appropriate processing is executed in the following cases:

- Occurrence of cache miss
- Multi-cycle instruction
- Occurrence of system exception, etc.

(4) Instruction address

The execution address of the next instruction to be fetched is calculated.
For this purpose, the following units are provided:

- PC incrementer
- Branch address adder
- Conditional branch address selector

(5) Instruction cache

The instruction cache employs the following methods:

- Direct map
- Virtual index address
- Physical tag cache

The capacity of the instruction cache is 2K bytes. Each cache line consists of 4-word data and its word parity, 22-bit tag and its parity bit, and a valid bit.
The instruction cache data interface is 32 bits wide.

(6) Data cache

The following methods are employed:

- Direct map
- Virtual index address
- Physical tag, write back cache

The capacity of the data cache is 1K byte.
Each cache line consists of 4-word data and its byte parity, 22-bit tag and its parity bit, valid bit, write back bit and its parity bit.

(7) System interface

This interface enables the processor to access external resources to satisfy internal requests.
The system interface consists of a 32-bit multiplexed address/data bus, clock signal, interrupt, and control signal.

(8) Clock generator

Generates the following four clocks from the input clock (MasterClock):

- PClock : Pipeline clock (internal)
- MasterOut : Clock output to external agent in synchronization with MasterClock
- SClock : System interface clock (internal). Two frequencies can be selected at cold reset
- TClock : Output clock as reference for external agent. Same frequency as SClock

The clocks internally generated by the processor can be temporarily stopped by a power mode.
The VR4100 uses a phase locked loop (PLL) to suppress skew between the input clock and internal clock.

3. INTERNAL ARCHITECTURE

3.1 Power Modes

The VR4100 supports three types of power modes, in addition to Fullspeed mode, to reduce the power dissipation:

- Fullspeed mode : Normal operation mode. All the clocks operate.
- Standby mode : The internal clocks except that related to the timer/interrupt are stopped.
- Suspend mode : The internal clocks except that related to the timer/interrupt, and TClock are stopped.
- Hibernate mode : All the clocks generated by the processor are stopped.

To change the mode from Fullspeed, a dedicated instruction is used. To change the mode from Standby or ★ Suspend to Fullspeed, generate a hardware interrupt, timer interrupt, or NMI; or execute a software reset or cold reset. To change from Hibernate to Fullspeed, execute a cold reset.

The mode cannot be directly changed from the Standby, Suspend, and Hibernate modes to a mode other than Fullspeed. Be sure to change the mode from these three modes to Fullspeed, and then change from Fullspeed to the desired operation mode.

Figure 3-1 and Table 3-1 show how the modes are changed.

Figure 3-2 shows the clock status in the Suspend mode and the sequence of mode transition as an example of the power mode.

Figure 3-1. Power Mode Status Transitions

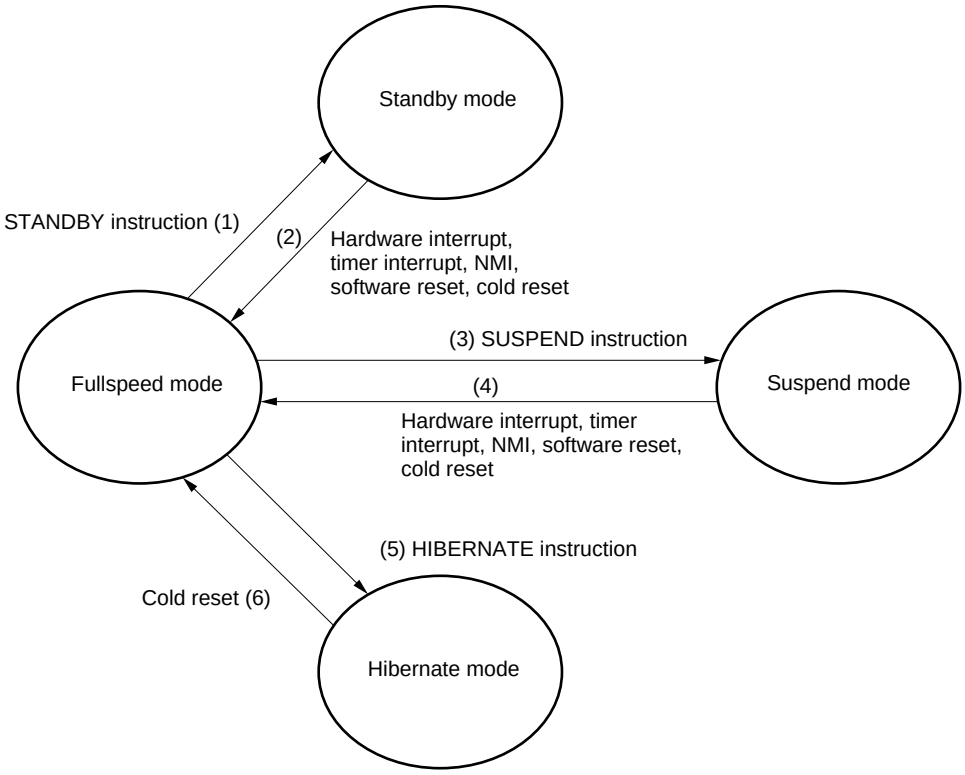


Table 3-1. Changing to Power Modes

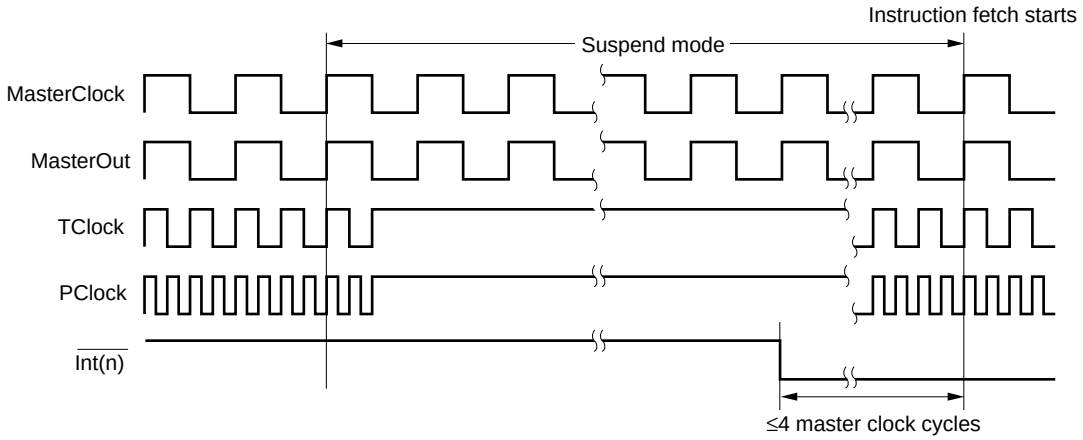
No. in Figure 3-1	How Changed	Maximum Time
(1)	STANDBY instruction	Time until SysAD bus idle + 4 master clock cycles
(2)	Hardware interrupt, timer interrupt, NMI, software reset	4 master clock cycles
	Cold reset	PLL lock time[Note] + 16 master clock cycles
(3)	SUSPEND instruction	Time until SysAD bus idle + 4 master clock cycles ★
(4)	Hardware interrupt, timer interrupt, NMI, software reset	4 master clock cycles
	Cold reset	PLL lock time[Note] + 16 master clock cycles
(5)	HIBERNATE instruction	Time until SysAD bus idle + 4 master clock cycles
(6)	Cold reset	PLL lock time[Note] + 16 master clock cycles

Note PLL lock time (where PClock is 33 MHz) is approximately 8 ms.

Table 3-2. Processor Status in Power Modes

Item / Mode	PLL	MasterOut	Timer/interrupt	TClock	PClock
Fullspeed	ON	ON	ON	ON	ON
Standby	ON	ON	ON	ON	OFF
Suspend	ON	ON	ON	OFF	OFF
Hibernate	OFF	OFF	OFF	OFF	OFF

Figure 3-2. Timing in Suspend Mode (when the $\overline{\text{Div2}}$ pin is set to low) ★



3.2 Pipeline

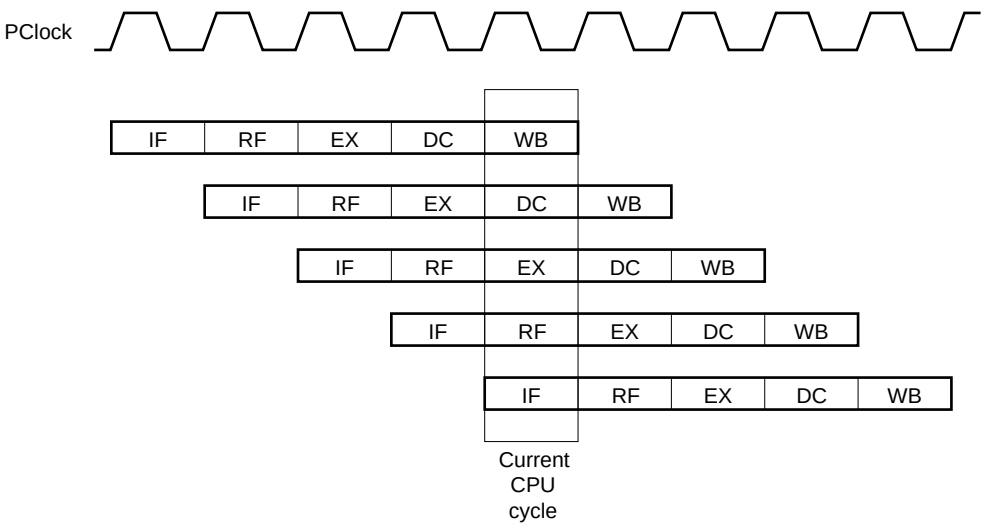
Each instruction is executed in the following five steps:

(1) IF instruction cache fetch
(2) RF register fetch
(3) EX execution
(4) DC data cache
(5) WB write back

The VR4100 is provided with a 5-stage pipeline. Although it takes five clocks to execute each instruction, paralleling is implemented at instruction level. PClock, which is the pipeline clock, operates at a frequency 4 times higher than that of the master clock input.

The following shows the pipeline outline.

Figure 3-3. Pipeline of VR4100 (5 stages)



3.3 CPU Register

3.3.1 Overview of register file

Figure 3-4 shows the CPU registers of the VR4100. The bit width of these registers is determined by the operation mode of the processor (in 32-bit mode: 32 bits, in 64-bit mode: 64 bits).

Of the thirty-two general-purpose registers of the VR4100, the following two registers have special meanings:

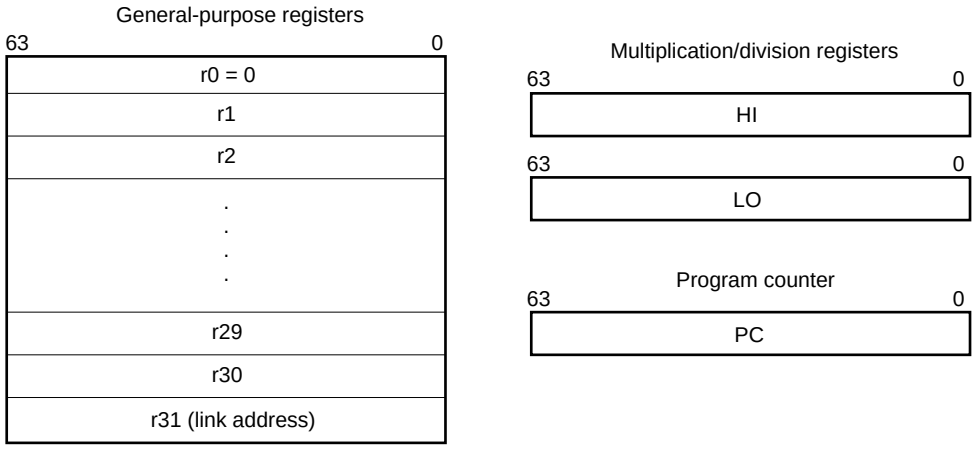
- Register r0 : The contents of this register are always 0. To discard the result of an operation, this register can be coded as the target of the instruction. If the value 0 is needed, this register can be used as a source register.
- Register r31 : This is a link register for the JAL and JALR instructions. Therefore, do not use this register with any other instructions.

The two multiplication/division registers (HI and LO) store the result of multiplication or sum-of-products operation, or quotient (LO) and remainder (HI) resulting from division.

However, because the VR4100 does not support floating-point operation instructions, the thirty-two floating-point general-purpose registers (FGRs), which are provided in the VR4200™ and VR4400™, are not provided in the VR4100.

Remark The load link bit (LL bit) used for the multi-processor system synchronization instructions (LL and SC) supported by the VR4200 and VR4400 is not provided in the VR4100 (refer to **3.4 (2) Deletion of multi-processor instructions**).

Figure 3-4. CPU Registers



No program status word (PSW) is provided. The function of the program status word is substituted by the status register and cause register of the system control coprocessor (CP0).

3.4 Overview of Instruction Set

The instruction set of the VR4100 conforms basically to the MIPS-I, -II, and -III instruction sets. However, it differs from the instructions set of the other processors in the VR series in the following four points:

(1) Deletion of floating-point (FPU) instructions

Because the VR4100 does not have a floating-point unit, it does not support FPU instructions. If an FPU instruction is executed, therefore, a reserved instruction exception occurs. If it is necessary to use an FPU instruction, emulate it by software in an exception handler.

(2) Deletion of multi-processor instructions

The VR4100 does not support the operating environment of a multi-processor system. If a synchronization support instruction (LL or SC instruction) defined by MIPS-II and -III ISA is executed, therefore, reserved instruction exception occurs. For the above reason, the VR4100 is not provided with a load link bit (LL bit).

The VR4100 executes all the load/store instructions in the sequence specified in the program. Therefore, the SYNC instruction is treated as a NOP instruction.

(3) Addition of sum-of-products instructions

The VR4100 has a dedicated sum-of-products core in the CPU and integer sum-of-products instructions to increase the speed of sum-of-products operations. These instructions are not correctly executed by the other processors in the VR series.

The operations of the sum-of-products instructions are given below.

(a) MADD16 (Multiply and Add 16-bit Integer)

Multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as 16-bit signed integers. The bits 62 through 15 of both the operands must be sign-extended values.

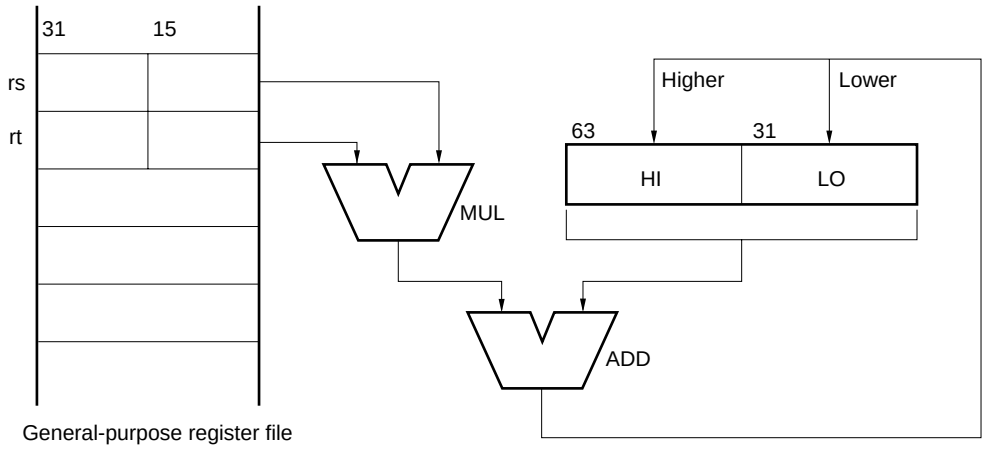
The result of the multiplication is added to the 64-bit value of the special registers HI and LO.

The lower word of the 64-bit result is loaded to special register LO, and the higher word is loaded to special register HI.

An integer overflow exception does not occur.

Figure 3-5 shows the MADD16 instruction operation outline.

★ **Figure 3-5. MADD16 Instruction Operation**



(b) DMADD16 (Doubleword Multiply and Add 16-bit Integer)

Multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as 16-bit signed integers. The bits 62 through 15 of both the operands must be sign-extended values.

The result of the multiplication is added to the value of the special register HI. The result of the addition is treated as a signed integer. The 64-bit result is loaded to the special register LO.

An integer overflow exception does not occur.

This operation is defined in the 64-bit mode and 32-bit kernel mode. If this instruction is executed in the 32-bit user or supervisor mode, a reserved instruction exception occurs.

(4) Additional instructions for power modes

The VR4100 supports three power modes to reduce the power dissipation, and has dedicated instructions to set these modes.

Note that these dedicated instructions are not correctly executed by the other processors in the VR series.

Here are the details of the operations for the power modes:

(a) STANDBY (Standby)

Changes the mode of the processor from Fullspeed to Standby.

When execution of the instruction proceeds to the WB stage, the processor waits for the SysAD bus to enter the idle status, then fixes the internal clock to the high level and stops pipeline operation.

In the Standby mode, the PLL, clock related to the timer/interrupt, and system interface clocks (TClock and MasterOut) operate normally.

To change the mode from Standby to Fullspeed, either generate a hardware interrupt, timer interrupt or NMI, or execute a software reset or cold reset. ★

(b) SUSPEND (Suspend)

Changes the mode of the processor from Fullspeed to Suspend.

When execution of the instruction proceeds to the WB stage, the processor waits for the SysAD bus to enter the idle status, then fixes the internal clock and TClock to the high level and stops the operation of the pipeline and the external bus interface.

In the Suspend mode, the PLL, clock related to the timer/interrupt, and MasterOut operate normally.

To change the mode from Suspend to Fullspeed, either generate a hardware interrupt, timer interrupt or NMI, or execute a software reset or cold reset. ★

(c) HIBERNATE (Hibernate)

Changes the mode of the processor from Fullspeed to Hibernate.

When execution of the instruction proceeds to the WB stage, the processor waits for the SysAD bus to enter the idle status, then fixes the all the clocks to the high level and stops pipeline operation.

To change the mode from Hibernate to Fullspeed, execute a cold reset.

3.5 System Control Coprocessor (CP0)

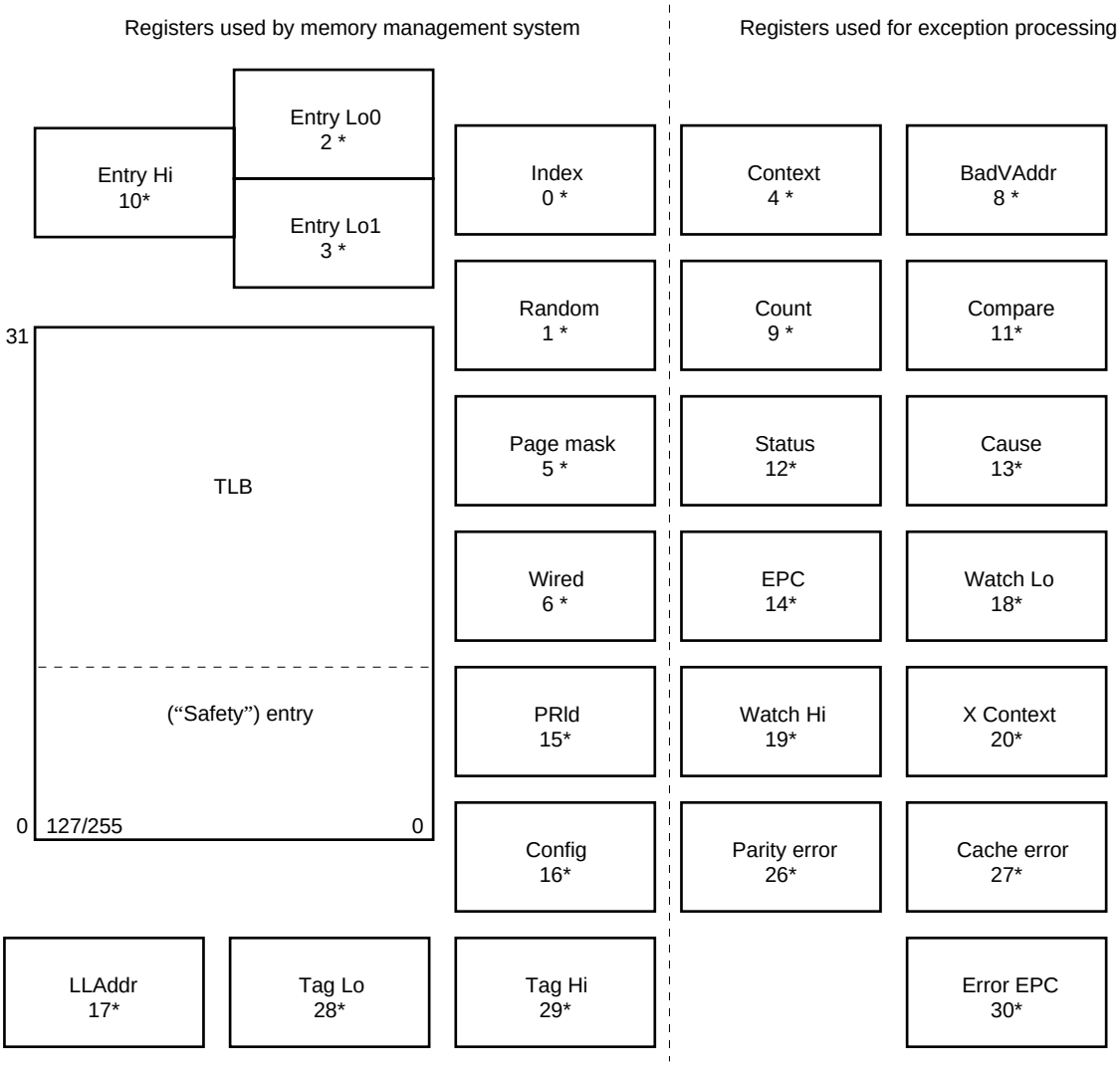
The CP0 supports memory management, address conversion, exception processing, and privileged operation. CP0 has the registers shown in Table 3-3 and a 32-entry TLB.

Although the basic configuration of the CP0 register of the VR4100 is the same as that of the VR4200 and VR4400, the bit configuration and the settings differ because the number of entries of the TLB, page size, cache size, physical address space, and system interface differ. For details, refer to **VR4100 User's Manual**.

3.5.1 CP0 registers

All the CP0 registers of the VR4100 that can be used are listed below. Writing or reading an unused register (RFU) is undefined. In the 32-bit mode, the higher 32 bits of the 64-bit registers are masked.

★ **Figure 3-6. CP0 Registers and TLB**



Remark "*" denotes a register number.

Table 3-3. CP0 Registers

Number	Register	Description
0	Index	Programmable pointer to TLB array
1	Random	Random pointer to TLB array (read-only)
2	Entry Lo0	Second half of TLB entry for even VPN
3	Entry Lo1	Second half of TLB entry for odd VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page mask	Specifies page size
6	Wired	Number of wired TLB entries
7	–	RFU (Reserved for Future Use)
8	BadVAddr	Displays virtual address at which error last occurred
9	Count	Timer count
10	Entry Hi	First half of TLB entry (includes ASID)
11	Compare	Timer comparison value
12	Status	Sets operation status
13	Cause	Displays cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision ID
16	Config	Sets memory system mode
17	LLAddr	Displays address of LL instruction
18	Watch Lo	Lower bits of memory reference trap address
19	Watch Hi	Higher bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21 to 25	–	RFU
26	Parity error	Parity bit of cache
27	Cache error	Cache error and status register
28	Tag Lo	Cache register, low
29	Tag Hi	Cache register, high (reserved register)
30	Error EPC	Error exception program counter
31	–	RFU

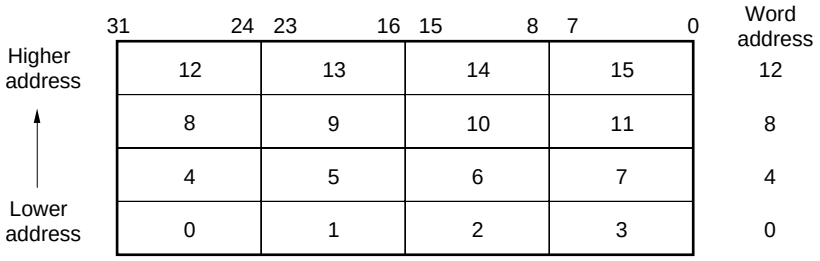
★ 3.6 Data Format and Addressing

The VR4100 uses the following four types of data formats.

Double word (64 bits)
Word (32 bits)
Half-word (16 bits)
Byte (8 bits)

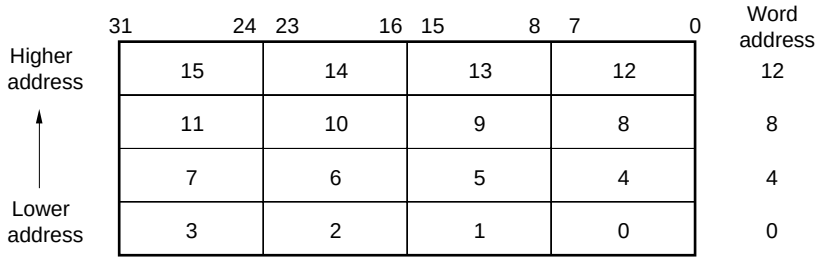
When the data format is double-word, word, or half-word, the alignment of bytes can be set to either big endian or little endian with the configuration register BE bit.

Figure 3-7. Byte Address in Word: Big Endian



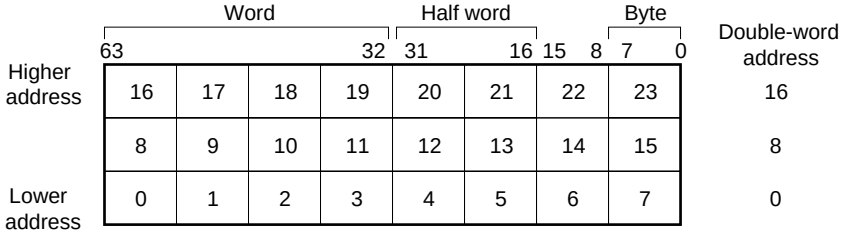
Remarks 1. The most significant byte is at the lowest address.
2. The word is addressed at the highest address.

Figure 3-8. Byte Address in Word: Little Endian



Remarks 1. The least significant byte is at the lowest address.
2. The word is addressed at the lowest address.

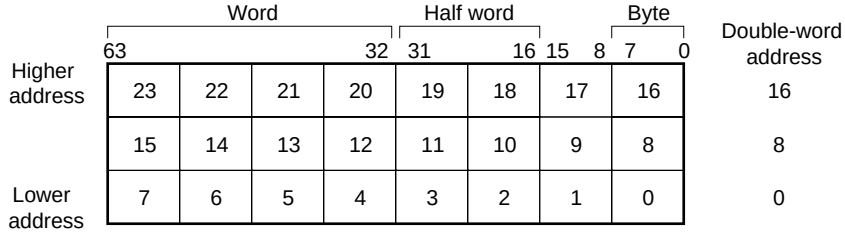
Figure 3-9. Byte Address in Double-Word: Big Endian



Remarks 1. The most significant byte is at the lowest address.

2. The word is addressed at the highest address.

Figure 3-10. Byte Address in Double-Word: Little Endian



Remarks 1. The least significant byte is at the lowest address.

2. The word is addressed at the lowest address.

3.7 Virtual Storage

The VR4100 has a virtual storage management mechanism using TLB.

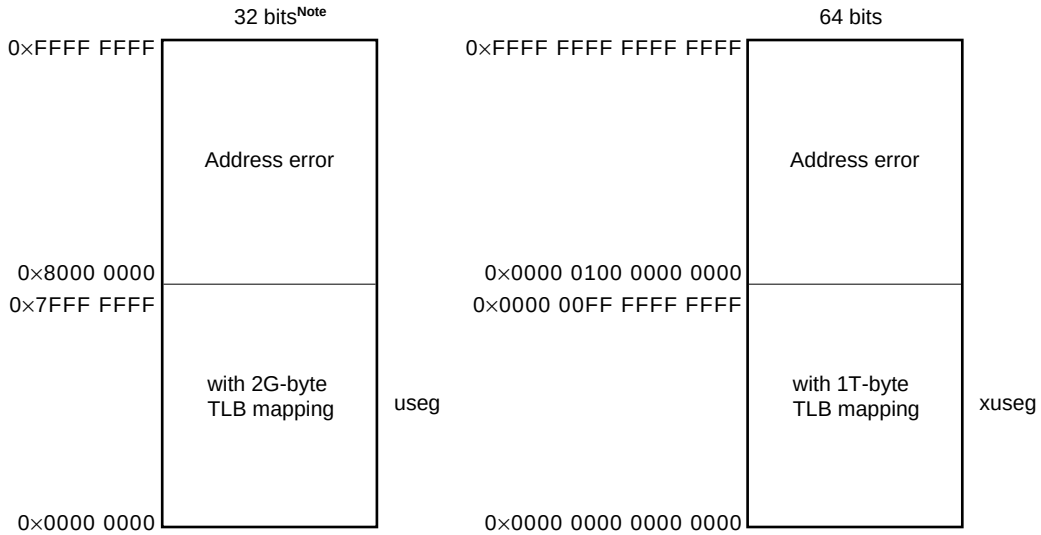
Virtual addresses are used for address management by the software or address calculation of the pipeline. To access the memory or I/O such as to fetch the program or access data, physical addresses converted from virtual addresses by the TLB are used.

Some addresses of the virtual address space are not converted into physical addresses by the TLB. Conversion to physical addresses is carried out by only changing specific addresses. If only this space is used, the processor can be used in the same manner as a CPU that operates with physical addresses.

3.7.1 Virtual address space

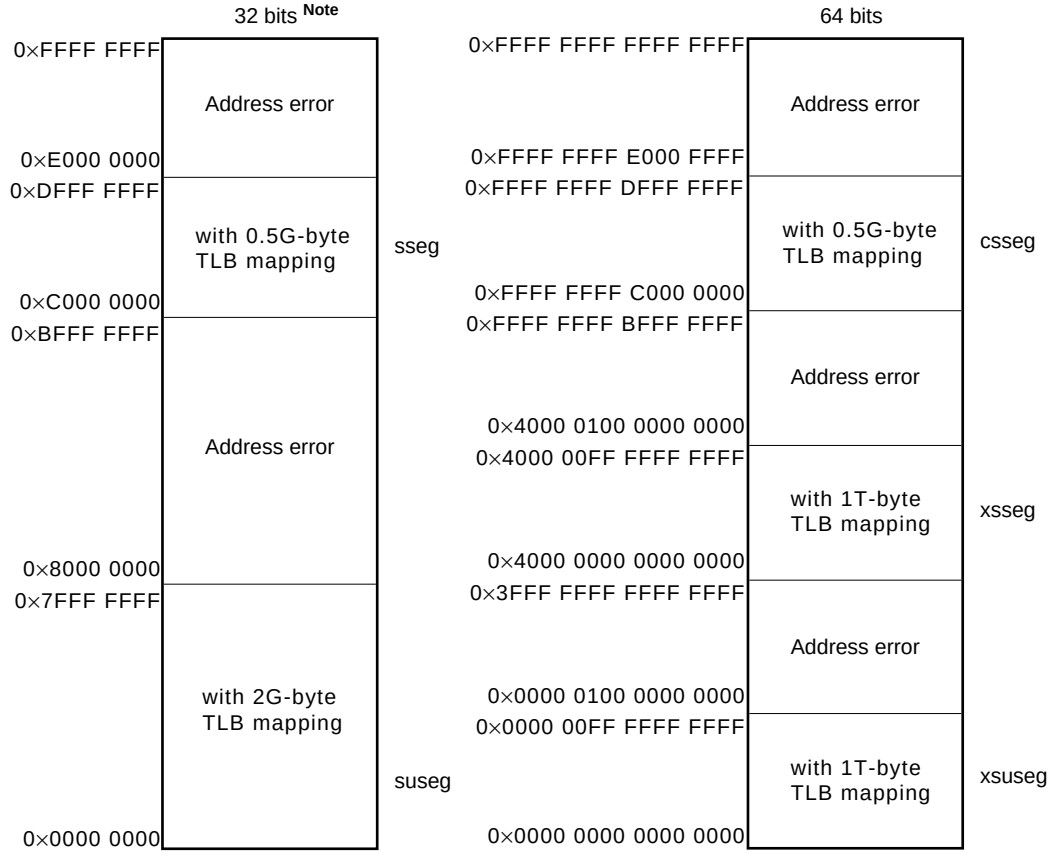
The VR4100 has two operation modes: 32-bit and 64-bit modes. It also has three operating modes: user, supervisor, and kernel. The figures below show the virtual address spaces in each operating mode.

Figure 3-11. User Mode Address Space



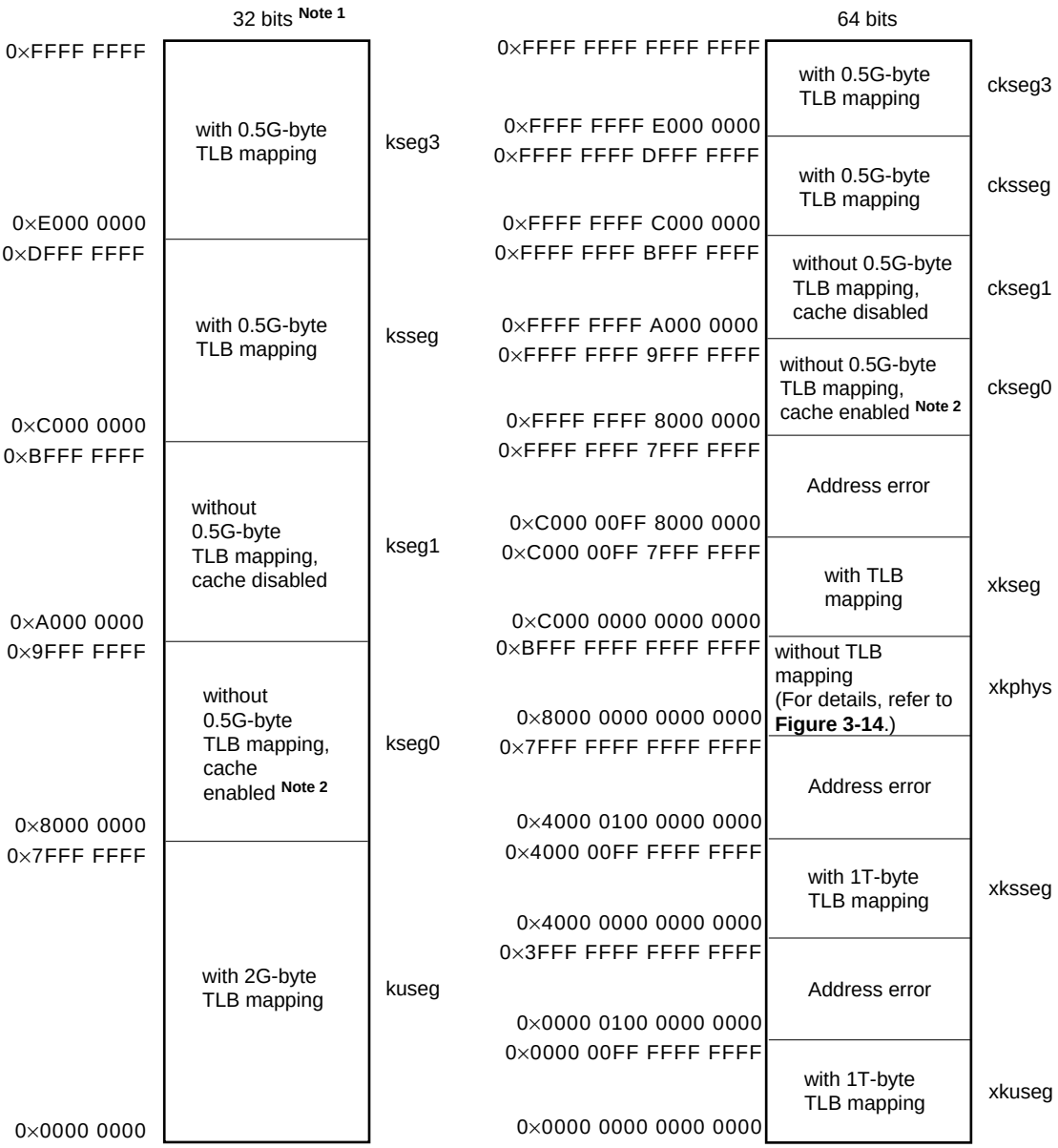
Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4100 User's Manual**.

Figure 3-12. Supervisor Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4100 User's Manual**.

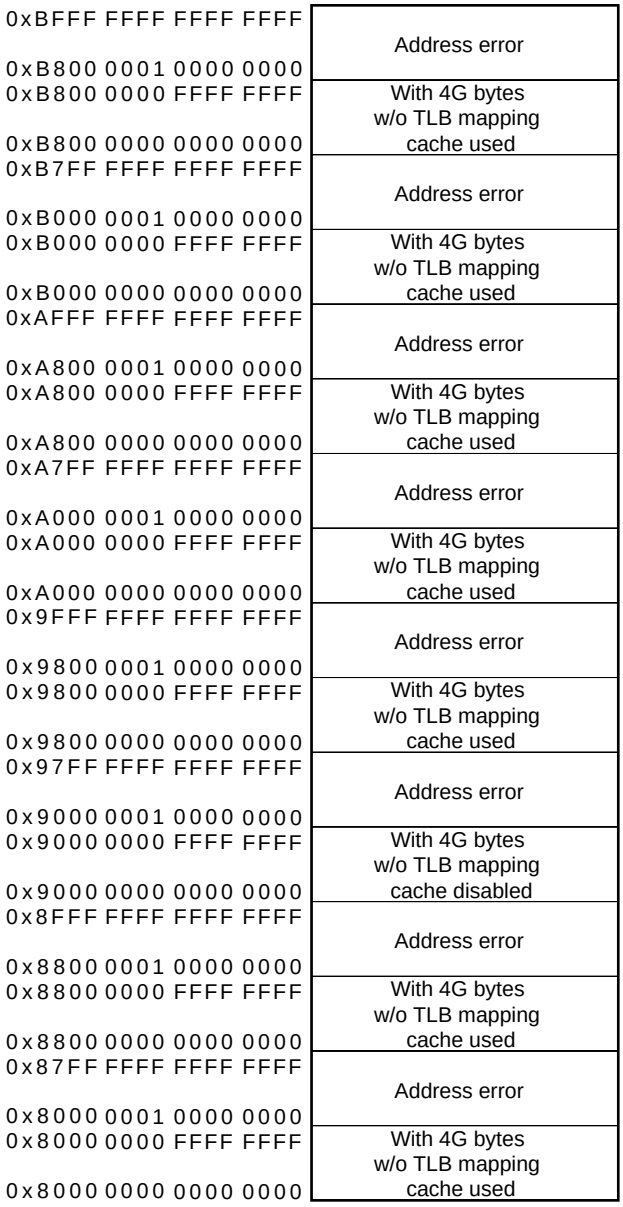
Figure 3-13. Kernel Mode Address Space ★



Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4100 User's Manual**.

2. The config register K0 area determines whether this is the cache area.

★ **Figure 3-14. Details of xkphys Area**



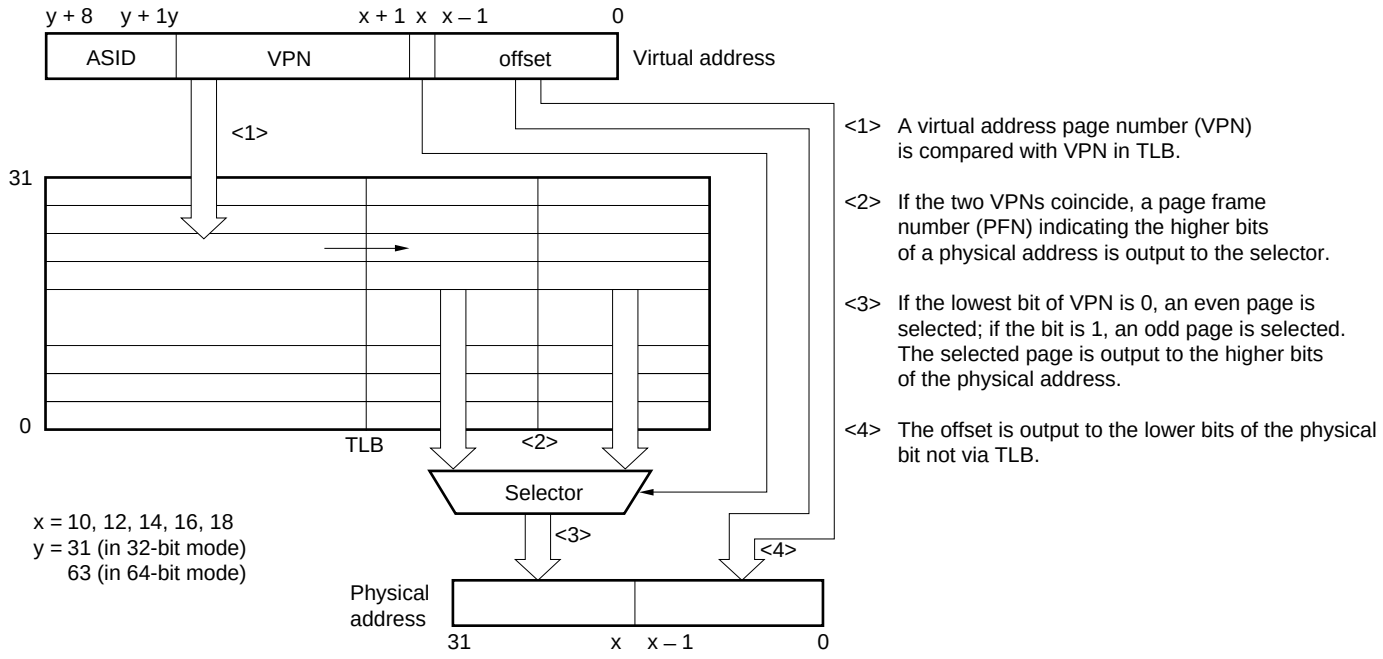
★ **3.7.2 Address conversion**

Conversion from virtual addresses to physical addresses is performed per page by the built-in TLB (Translation Lookaside Buffer). The TLB, which is based on a full-associative configuration, has 64 entries on the virtual address side and 32 entries on the physical address side. The page size can be varied between 4 KB and 16 MB.

In case no TLB entry is hit, a TLB mismatch exception occurs in 32-bit mode; and an XTLB mismatch exception in 64-bit mode. Use software to reshuffle the TLB contents.

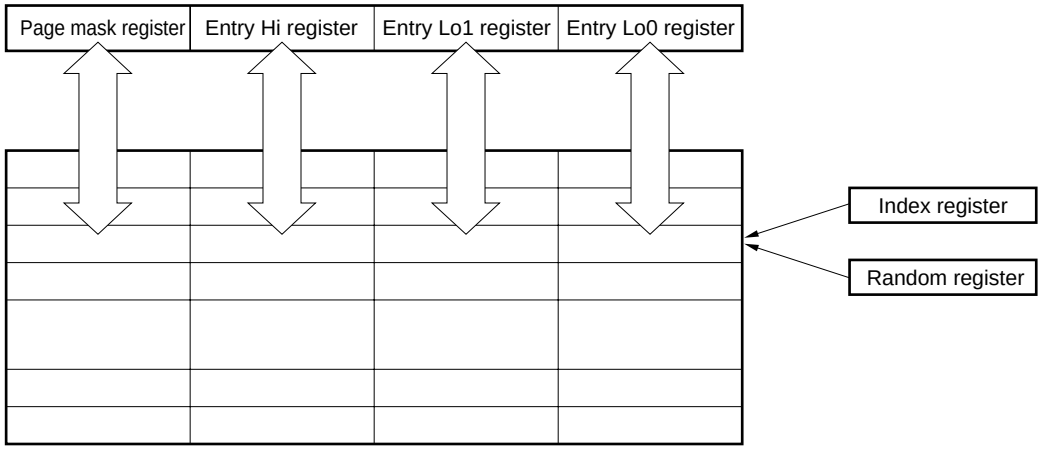
The address conversion is shown below diagramatically.

Figure 3-15. Overview of Address Conversion



Reading and writing of TLB entries is performed by loading/storing between the TLB entry specified by the index register or the random register, and the entry Hi, entry Lo1, entry Lo0, and page mask registers.

Figure 3-16. Overview of TLB Operation



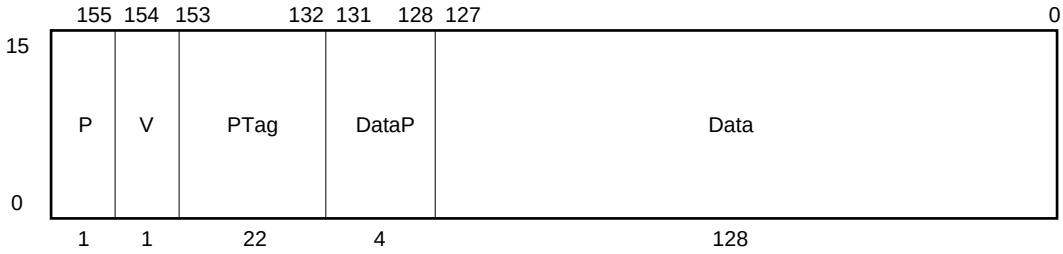
★ 3.8 Caches

(1) Instruction cache

The features of the instruction cache are listed below.

- Built-in cache memory
- Capacity: 2K bytes
- Direct mapping
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-17. Instruction Cache Format



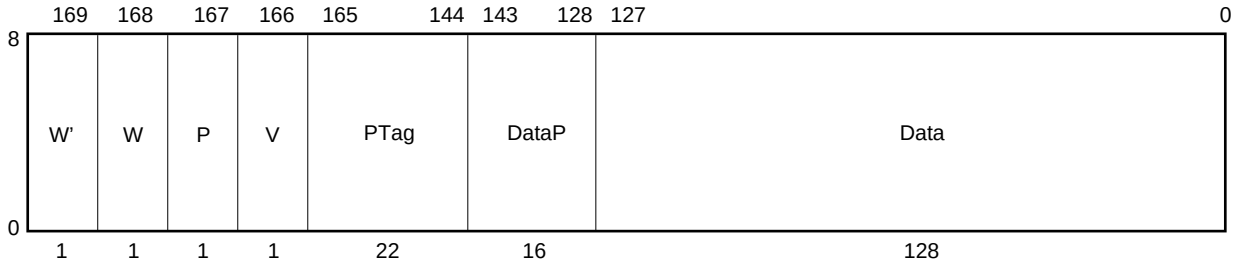
PTag : Physical tag (bits 31-12 of physical address)
V : Valid bit
Data : Cache data
P : Even parity for physical tag and V bit
DataP : Even parity for data (parity of 1 bit per 4-byte data)

(2) Data cache

The features of the data cache are listed below.

- Built-in cache memory
- Capacity: 1K bytes
- Write back
- Direct mapping
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-18. Format of Data Cache



W' : Even parity for write back bit
W : Write back bit
P : Even parity for physical tag and V bit
V : Valid bit
PTag : Physical tag (bits 31 through 10 of physical address)
DataP : Even parity for data (parity of 1 bit per 1-byte data)
Data : Cache data

3.9 Exception Processing

If an exception occurs, the VR4100 enters the kernel mode with interrupts disabled, and executes an exception handler from a fixed exception vector address. When execution returns from the exception handler, it is necessary to restore the original information on the program counter, operating mode, and enabling of interrupts. Therefore, save this information when an exception occurs.

When an exception occurs, the EPC register holds the address of the instruction that has generated the exception. If the exception occurs in the delay branch slot, the EPC register holds the address of the instruction immediately before the instruction that has generated the exception. In other words, the EPC register stores an address from which execution is to be started after exception processing has been completed. The VR4100 also has the following modes related to exception processing. At reset, the restart address is retained when the NMI is generated.

Table 3-4. Types of Exceptions

Exception	Abbreviation	Description
Cold reset	–	Occurs if $\overline{\text{ColdReset}}$ and $\overline{\text{Reset}}$ signals are simultaneously asserted active. Aborts instruction execution and executes a handler on the reset vector. The internal status is undefined, except some bits of the status register.
Soft reset	–	Occurs if $\overline{\text{Reset}}$ signal is asserted active. Aborts instruction execution and executes a handler on the reset vector. The internal status before soft reset is retained.
NMI	–	Non-maskable interrupt request by the external agent.
TLB unmatch	TLBL/TLBS	Occurs if the operating mode is the 32-bit mode and the number of TLB entries matching the referenced address runs short.
Expansion addressing TLB unmatch	TLBL/TLBS	Occurs if the operating mode is 64-bit mode and the number of TLB entries matching the referenced address runs short.
TLB invalid	TLBL/TLBS	Occurs if the TLB entry matching the referenced virtual address is invalid. (V bit = 0)
TLB change	Mod	Occurs if a TLB entry that coincides with virtual address to be accessed is valid but write is disabled (D bit = 0) when the store instruction is executed
Bus error	IBE/DBE	Occurs if an external agent indicates a data error on the SysCmd bus by an external interrupt to the bus interface (bus timeout, bus parity error, or invalid physical memory address or access type)
Address error	AdEL/AdES	Occurs if an attempt is made to execute the LH, SH/LW/SW, LD, or SD instruction to the half word/word/double word not at the half word/word/double word boundary, or to reference a virtual address that cannot be accessed.
Integer overflow	Ov	Occurs if 2's complement overflow occurs as a result of addition or subtraction.
Trap	Tr	Occurs if the condition is true at trap instruction execution.
System call	Sys	Occurs when the SYSCALL instruction is executed.
Breakpoint	Bp	Occurs when the BREAK instruction is executed.
Reserved instruction	RI	Occurs when an instruction whose op code (bits 31-26) is undefined, or the SPECIAL instruction whose op code (bits 5-0) is undefined is executed.
Coprocessor unusable	CpU	Occurs if the coprocessor instruction is executed when the corresponding coprocessor use enable bit is not set.
Interrupt	Int	Occurs when one of the eight interrupt sources becomes active.
Cache error	–	Occurs when a parity error is detected on the internal cache or system interface.
Watch	WATCH	Occurs when an attempt is made to reference the physical address in the watch Lo/Hi register with the load/store instruction.

Exception vectors and those offset values in the 64-bit mode and 32-bit mode are listed below.

Table 3-5. Base Address of Exception Vector in 64-Bit Mode

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xFFFF FFFF BFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xFFFF FFFF A000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0100
TLB unmatch, EXL = 0	0xFFFF FFFF 8000 0000 (BEV = 0)	0x0000
XTLB unmatch, EXL = 0	0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0080
Others		0x0180

Table 3-6. Base Address of Exception Vector in 32-Bit Mode

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xBFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xA000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0100
TLB unmatch, EXL = 0	0x8000 0000 (BEV = 0	0x0000
XTLB unmatch, EXL = 0	0xBFC0 0200 (BEV = 1)	0x0080
Others		0x0180

4. INTERFACES

4.1 System Interface

There are the following four system interface buses.

- SysAD (31:0) : Bus for address and data transfer.
- SysADC (3:0) : Even parity bus for SysAD bus.
- SysCmd (4:0) : Bus for command and data identifier transfer.
- SysCmdP : Even parity bit for SysCmd bus

The SysAD and SysCmd buses are bidirectional and driven by the processor or an external agent. Depending on the direction, they are placed in either of the following two statuses.

- Master status : The bus is driven by the processor, because a processor request is issued.
- Slave status : The bus is driven by an external agent, because an external request is issued.

The processor's input/output timings are as follows:

- The processor output starts to change at the rising edge of SClock.
- The processor input is latched at the trailing edge of SClock.

Depending on the information included in the SysAD bus, two cycles occur as follows.

- Address cycle : The SysAD bus contains a valid address.
- Data cycle : The SysAD bus contains valid data.

The interface control signals are briefly described below.

- $\overline{\text{EValid}}$: Activate this signal when an external agent is in the master status and the SysAD and SysCmd buses are valid.
- $\overline{\text{PValid}}$: This signal is activated when the processor is in the master status and the SysAD and SysCmd buses are valid.
- $\overline{\text{EReq}}$: Activate this signal when an external agent requests the right to use the interface.
- $\overline{\text{PReq}}$: This signal is activated when the processor requests the right to use the interface.
- $\overline{\text{PMaster}}$: This signal is activated when the processor is placed in the master status.
- $\overline{\text{ERdy}}$: Activate this signal when an external agent becomes capable of accepting the processor request.

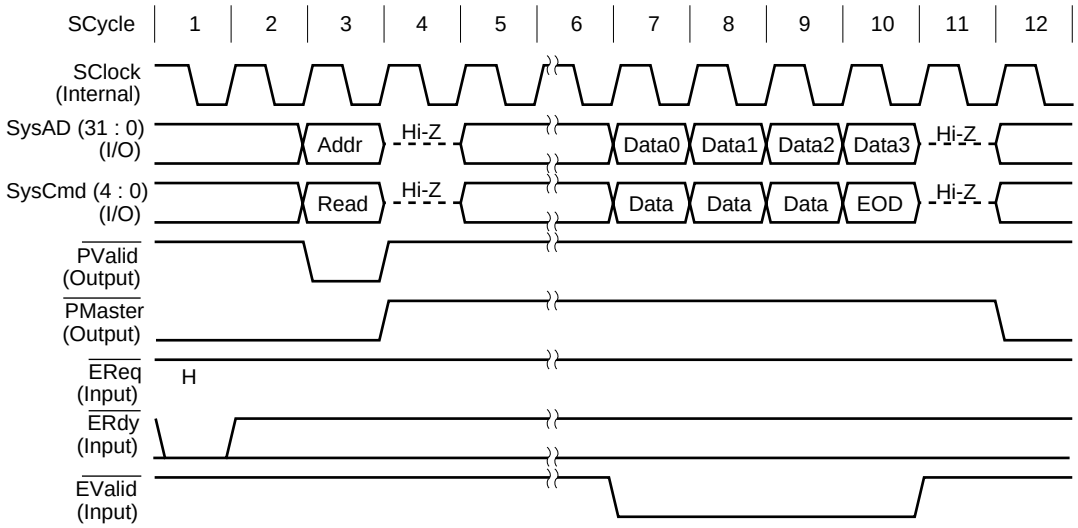
4.1.1 System interface requests

The following requests are supported by the system interface.

Request	Outline	Data Unit
Processor read request	Read request to main memory or I/O	1 to 4 bytes (single);
Processor write request	Write request to main memory or I/O	2/4 words (block)
External write request	Interrupt request from the system bus	1 word

As an example of the system interface request protocol, Figure 4-1. shows the timing between a processor block read request and the response.

Figure 4-1. Processor Block Read Request and the Following Read Response



4.1.2 Control of data transfer rate

The system interface of the VR4100 can transfer word data in one cycle.

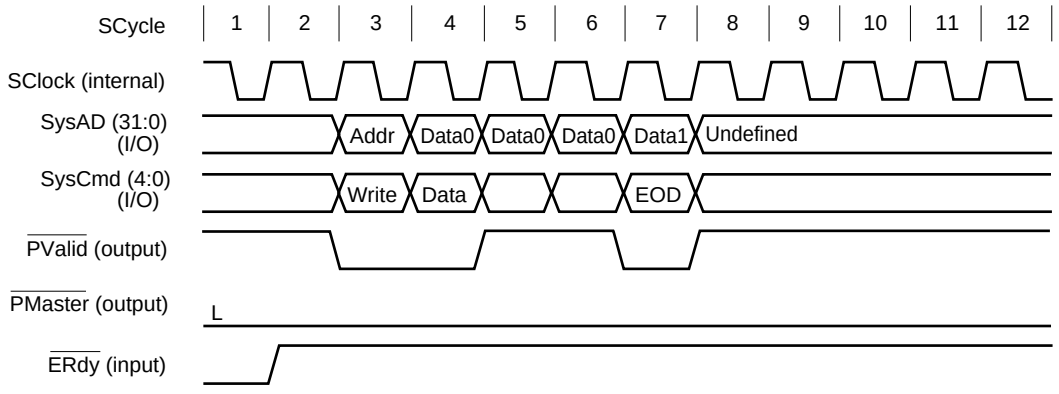
The external agent can transfer data to the processor at any transfer rate. The rate at which data is transferred from the processor to the external agent is set by the EP field of the config register. The VR4100 has four write data transfer rates: “D”, “DX”, “DXX”, and “DXXX”. The processor holds the data output during the period “D” immediately before, during the period of “X”, and continues output.

The pattern of the data transfer rate is expressed by a combination of symbols “D” and “X”, where “D” indicates the data transfer cycle, and “X” indicates an unused cycle. This transfer pattern indicates an appropriate data transfer rate by a data cycle and unused cycle.

Example DXX: Transfers 1-word data every 3 cycles

Figure 4-2 shows the timing of the processor block write request when the transfer pattern is DXX.

Figure 4-2. Processor Block Write Request When Transfer Pattern Is DXX ★



4.1.3 Clock interface

The internal clock of the VR4100 is controlled by an internal phase lock loop (PLL) circuit. This PLL circuit synchronizes the internal clock of the VR4100 with the MasterClock (input clock) signal.

Stopping the output of the clock can be controlled in the power mode. For details, refer to **3.1 POWER MODES**.

The clock signals used in the VR4100 are described below.

★ **(1) MasterClock (Input)**

All internal clocks and external clocks are generated based on the MasterClock.

(2) PClock (Internal)

PClock is the basis of the pipeline operation. The frequency of PClock is 4 times higher than that of the Master Clock.

(3) SClock (Internal)

SClock is the basis of the operation of the system interface. However, this clock does not output to the external agent.

SClock is generated by dividing PClock. The division ratio to generate the SClock from the PClock is set by the $\overline{\text{Div2}}$ pin at cold reset.

$\overline{\text{Div2}}$	PClock : SClock (Frequency Ratio)
0	2 : 1
1	1 : 1

(4) TClock (Output)

TClock is the clock on which the operation of external agents is based.

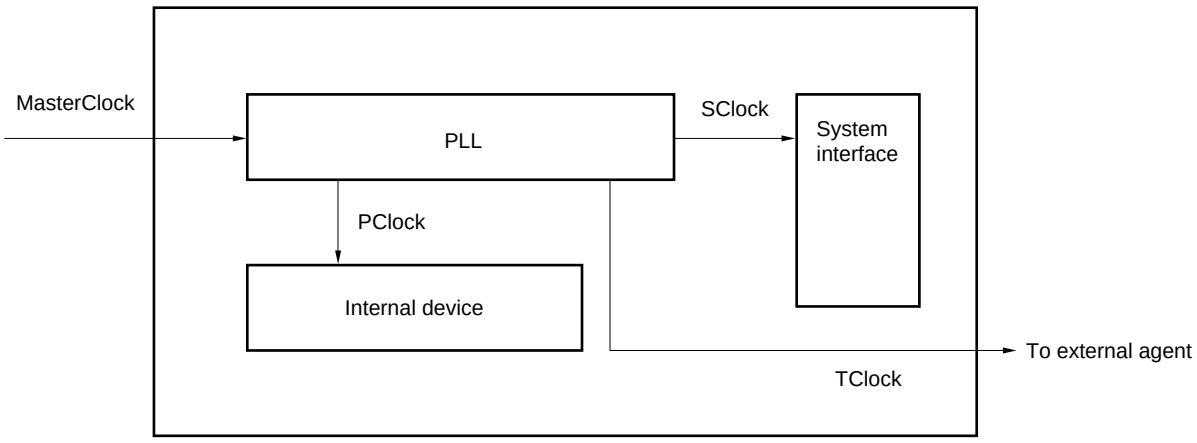
TClock is generated at the same frequency as that of SClock, and is synchronized with SClock.

(5) MasterOut (Output)

MasterOut is generated at the same frequency as MasterClock and is synchronized with MasterClock.

This clock is used for the external logic that controls resets or interrupts.

★ **Figure 4-3. Clock Interface**



5. INTERNAL/EXTERNAL FUNCTION

5.1 Reset Functions

The VR4100 has two reset signals: cold reset ($\overline{\text{ColdReset}}$) and soft reset ($\overline{\text{Reset}}$). Setting of the necessary mode is controlled directly by pins and the config register.

5.1.1 Cold reset

This reset operation initializes all the information of the CPU.

The following registers are set to the values shown at cold reset.

- TS and SR bits of status register ... 0
- ERL and BEV bits of status register ... 1
- Random register ... upper-limit value
- Wired register ... 0

Cold reset is executed when the $\overline{\text{ColdReset}}$ and $\overline{\text{Reset}}$ signals are made active.

5.1.2 Software reset

This reset operation can be executed when the $\overline{\text{Reset}}$ signal is asserted active. This reset does not perform initialization, and the status before reset is retained as much as possible. However, if a multi-cycle instruction is aborted by this reset, the result is undefined.

5.2 Interrupt Functions

There are two major categories of interrupt requests as follows:

- Maskable interrupt requests
- Non-maskable interrupt (NMI) requests

(1) Maskable interrupt requests

These interrupts undergo mask control. The mask processing is performed by the status register. (Each interrupt can be handled individually, or interrupts can be handled as a group.)

There is no priority among interrupts.

(a) Hardware interrupt request (5 causes)

Accepted by activating an external write request or $\overline{\text{Int}}$ (4:0) signal.

(b) Software interrupt request (2 causes)

Accepted by setting the cause register IP0 and IP1 bits.

(c) Timer interrupt request (1 cause)

If the value of the count register becomes equal to that of the compare register, the cause register IP7 bit is set and the interrupt is accepted.

(2) NMI request (1 cause)

This interrupt request does not undergo mask control. The interrupt can be accepted by activating the external write request or $\overline{\text{NMI}}$ signal.

Caution The NMI request is not accepted while the pipeline is stopped. Therefore, it cannot be used to return from a report of hang-up of the external bus.

6. INSTRUCTION SET ★

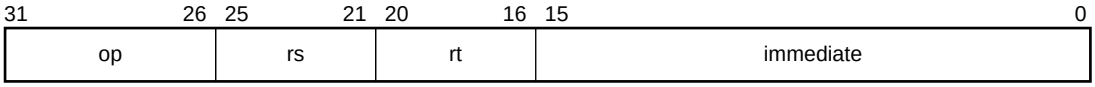
The VR4100's instructions consist of 1 word (32 bits) located on a word boundary. The instruction format has three types as shown in Figure 7-1. Decoding of instructions is simplified by having only three format types. Complicated and infrequently used operations and addressing modes are realized by compilers.

6.1 Instruction Format

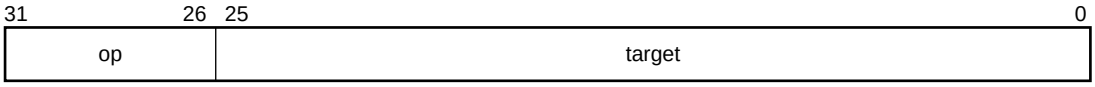
VR4100's instruction formats are as shown below.

Figure 6-1. CPU Instruction Formats

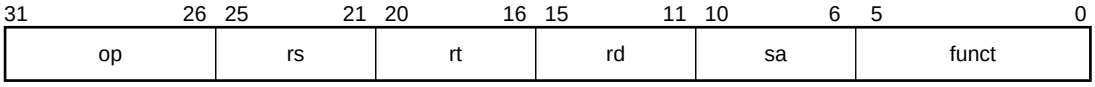
I-type (Immediate format)



J-type (Jump format)



R-type (Register format)



op	6-bit instruction code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register, or branch condition
immediate	16-bit immediate value, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register specifier
sa	5-bit shift quantity
funct	6-bit function field

6.2 List of CPU Instruction Set

The VR4100's CPU instructions are classified into three categories: the instruction set (ISA: Instruction Set Architecture) common to all VR series processors, the instruction set (extended ISA) executed on the VR4000 series, and the system control coprocessor instruction set. The instruction set is listed below.

Table 6-1. CPU Instruction Set: ISA (1/3)

Instructions	Description	Format
Load/store instruction	op | base | rt | offset	
LB	Load Byte	LB rt, offset (base)
LBU	Load Byte Unsigned	LBU rt, offset (base)
LH	Load Halfword	LH rt, offset (base)
LHU	Load Halfword Unsigned	LHU rt, offset (base)
LW	Load Word	LW rt, offset (base)
LWL	Load Word Left	LWL rt, offset (base)
LWR	Load Word Right	LWR rt, offset (base)
SB	Store Byte	SB rt, offset (base)
SH	Store Halfword	SH rt, offset (base)
SW	Store Word	SW rt, offset (base)
SWL	Store Word Left	SWL rt, offset (base)
SWR	Store Word Right	SWR rt, offset (base)
ALU immediate instruction	op | rs | rt | offset	
ADDI	Add Immediate	ADDI rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU rt, rs, immediate
ANDI	And Immediate	ANDI rt, rs, immediate
ORI	Or Immediate	ORI rt, rs, immediate
XORI	Exclusive Or Immediate	XORI rt, rs, immediate
LUI	Load Upper Immediate	LUI rt, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
ADD	Add	ADD rd, rs, rt
ADDU	Add Unsigned	ADDU rd, rs, rt
SUB	Subtract	SUB rd, rs, rt
SUBU	Subtract Unsigned	SUBU rd, rs, rt
SLT	Set On Less Than	SLT rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU rd, rs, rt
AND	And	AND rd, rs, rt
OR	Or	OR rd, rs, rt
XOR	Exclusive Or	XOR rd, rs, rt
NOR	Nor	NOR rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
SLL	Shift Left Logical	SLL rd, rt, sa
SRL	Shift Right Logical	SRL rd, rt, sa
SRA	Shift Right Arithmetic	SRA rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV rd, rt, rs

Table 6-1. CPU Instruction Set: ISA (2/3)

Instructions	Description	Format
Multiplication/division instruction	op | rs | rt | rd | sa | funct	
MULT	Multiply	MULT rs, rt
MULTU	Multiply Unsigned	MULTU rs, rt
DIV	Divide	DIV rs, rt
DIVU	Divide Unsigned	DIVU rs, rt
MFHI	Move From HI	MFHI rd
MFLO	Move From LO	MFLO rd
MTHI	Move To HI	MTHI rs
MTLO	Move To LO	MTLO rs
Jump instruction (1)	op | target	
J	Jump	J target
JAL	Jump And Link	JAL target
Jump instruction (2)	op | rs | rt | rd | sa | funct	
JR	Jump Register	JR rs
JALR	Jump And Link Register	JALR rs, rd
Branch instruction (1)	op | rs | rt | offset	
BEQ	Branch On Equal	BEQ rs, rt, offset
BNE	Branch On Not Equal	BNE rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZ	Branch On Less Than Zero	BLTZ rs, offset
BGEZ	Branch On Greater Than Or Equal to Zero	BGEZ rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL rs, offset
Special instruction	SPECIAL | rs | rt | rd | sa | funct	
SYNC	Synchronize	SYNC
SYSCALL	System Call	SYSCALL
BREAK	Breakpoint	BREAK
Coprocessor instruction (1)	op | base | rt | offset	
LWCz	Load Word To Coprocessor z	LWCz rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz rt, offset (base)
Coprocessor instruction (2)	COPz | sub | rt | rd | 0	
MTCz	Move To Coprocessor z	MTCz rt, rd
MFCz	Move From Coprocessor z	MFCz rt, rd
CTCz	Move Control To Coprocessor z	CTCz rt, rd
CFCz	Move Control From Coprocessor z	CFCz rt, rd

Table 6-1. CPU Instruction Set: ISA (3/3)

Instructions	Description	Format
Coprocessor instruction (3)	COPz | CO | cofun	
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instruction (4)	COPz | BC | br | offset	
BCzT	Branch On Coprocessor z True	BCzT offset
BCzF	Branch On Coprocessor z False	BCzF offset

Table 6-2. CPU Instruction Set: Expansion ISA (1/2)

Instructions	Description	Format
Load/store instruction	op | base | rt | offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
ALU immediate instruction	op | rs | rt | immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shift Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, rs
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, rs
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, rs
DSLL32	Doubleword Shift Left Logical +32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logiscal +32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic +32	DSRA32 rd, rt, sa

Table 6-2. CPU Instruction Set: Expansion ISA (2/2)

Instructions	Description	Format	
Multiplication/division instruction (1)	op | rs | rt | rd | sa | funct		
DMULT	Doubleword Multiply	DMULT	rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU	rs, rt
DDIV	Doubleword Divide	DDIV	rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU	rs, rt
Multiplication/division instruction (2)	op | rs | rt | rd | sa | funct		
MADD16	Multiply and Add 16-bit Integer	MADD16	rs, rt
DMADD16	Doubleword Multiply and Add 16-bit Integer	DMADD16	rs, rt
Branch instruction (1)	op | rs | rt | offset		
BEQL	Branch On Equal Likely	BEQL	rs, rt, offset
BNEL	Branch On Not Equal Likely	BNEL	rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely	BLEZL	rs, offset
BGTZL	Branch On Greatrer Than Zero Likely	BGTZL	rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset		
BLTZL	Branch On Less Than Zero Likely	BLTZL	rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely	BGEZL	rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely	BLTZALL	rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely	BGEZALL	rs, offset
Exception instruction	SPECIAL | rs | rt | rd | sa | funct		
TGE	Trap If Greater Than Or Equal	TGE	rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned	TGEU	rs, rt
TLT	Trap If Less Than	TLT	rs, rt
TLTU	Trap If Less Than Unsigned	TLTU	rs, rt
TEQ	Trap If Equal	TEQ	rs, rt
TNE	Trap If Not Equal	TNE	rs, rt
Exception immediate instruction	REGIMM | rs | sub | immediate		
TGEI	Trap If Greater Than Or Equal Immediate	TGEI	rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned	TGEIU	rs, immediate
TLTI	Trap If Less Than Immediate	TLTI	rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned	TLTIU	rs, immediate
TEQI	Trap If Equal Immediate	TEQI	rs, immediate
TNEI	Trap If Not Equal Immediate	TNEI	rs, immediate

Table 6-3. System Control Coprocessor (CP0) Instruction

Instructions	Description	Format
System control coprocessor instruction (1)	COP0 | sub | rt | rd | 0	
MFC0	Move From Coprocessor 0	MFC0 rt, rd
MTC0	Move To Coprocessor 0	MTC0 rt, rd
DMFC0	Doubleword Move From Coprocessor 0	DMFC0 rt, rd
DMTC0	Doubleword Move To Coprocessor 0	DMTC0 rt, rd
System control coprocessor instruction (2)	COP0 | CO | funct	
TLBR	Read Indexed TLB Entry	TLBR
TLBWI	Write Indexed TLB Entry	TLBWI
TLBWR	Write Random TLB Entry	TLBWR
TLBP	Probe TLB For Matching Entry	TLBP
ERET	Exception Return	ERET
System control coprocessor instruction (3)	COP0 | CO | funct	
STANDBY	Standby	STANDBY
SUSPEND	Suspend	SUSPEND
HIBERNATE	Hibernate	HIBERNATE
System control coprocessor instruction (4)	CACHE | base | sub | offset	
CACHE	Cache Operation	CACHE sub, offset (base)

6.3 Instruction Execution Times

The VR4100 in principle executes one instruction in one cycle. Some instructions, however, requires two or more cycles to execute.

(1) Data loaded by the load instruction cannot be used in the delay slot. If an instruction that uses the loaded data is located in the delay slot, the pipeline is stalled.

★ If a store instruction is executed followed by a load instruction or MFC0, the pipeline is stalled for the duration of the delay slot.

If the condition of a branch instruction is satisfied or if a jump instruction is executed, the instruction at the destination address is executed after the delay slot.

Table 6-4. Number of Delay Slot Cycles

Instruction Category	Required Number of Cycles (PCycle)
Load	1
Store	1
Jump	1
Branch	1

(2) To execute an integer multiplication, division, or sum-of-products instruction, the number of cycles shown in the table below is necessary.
These instructions can be executed in parallel with instructions other than those that access the HI/LO register which stores execution results, and multiplication, division, and sum-of-products instructions.

Table 6-5. Number of Execution Cycles for Integer Multiplication and Division Instructions

Instruction Category	Required Number of Cycles (PCycle)
MULT	1
MULTU	1
DIV	35
DIVU	35
DMULT	4
DMULTU	4
DDIV	67
DDIVU	67
MADD16	1
DMADD16	1

7. ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage	V_I	$V_{DD} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD} < 3.7$ V	–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{Stg}		–65 to +150	°C

Cautions 1. Do not short circuit two or more outputs at the same time.

2. The quality of the product may be degraded if the absolute maximum rating of even one of the above parameters is exceeded, even momentarily. Absolute maximum ratings, therefore, specify the values which if exceeded may physically damage the product. Use the product never exceeding these ratings.

The specifications and conditions shown in the following DC Characteristics and AC Characteristics are the range within which the product can normally operate and the quality can be guaranteed.

DC Characteristics (T_A = –10 to +70 °C, V_{DD} = 2.2 to 3.6 V) ★

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
High-level output voltage	V_{OH}	I_{OH} = –2 mA	0.8 V_{DD}			V	
		I_{OH} = –20 μA	V_{DD}–0.1				
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V	
		I_{OL} = 20 μA			0.1		
High-level output voltage[Note 1]	V_{OHC}	I_{OH} = –2 mA	0.8 V_{DD}			V	
		I_{OH} = –20 μA	V_{DD}–0.1				
Low-level output voltage[Note 1]	V_{OLC}	I_{OL} = 2 mA			0.4	V	
		I_{OL} = 20 μA			0.1		
High-level input voltage[Note 2]	V_{IH}	V_{DD} < 2.7 V	0.7 V_{DD}		V_{DD} + 0.3	V	★
		V_{DD} ≥ 2.7 V	2.0		V_{DD} + 0.3		
Low-level input voltage[Note 2]	V_{IL}	V_{DD} < 2.7 V	–0.3		0.3 V_{DD}	V	★
		V_{DD} ≥ 2.7 V	–0.3		0.8		
High-level input voltage[Note 3]	V_{KH}		0.8 V_{DD}		V_{DD} + 0.3	V	★
Low-level input voltage[Note 3]	V_{KL}		–0.3		0.2 V_{DD}	V	★
Supply current[Note 4]	I_{DD}	in Fullspeed mode		1.5f[Note 5]	2.7f	mA	★
		in Standby mode			0.3f		
		in Suspend mode			0.1f		
		in Hibernate mode			50[Note 5]	μA	
High-level input leakage current	I_{LIH}	V_{DD} = 3.6 V, V_I = 3.6 V			5	μA	
Low-level input leakage current	I_{LIL}	V_{DD} = 3.6 V, V_I = 0 V			–5	μA	
High-level output leakage current	I_{LOH}	V_{DD} = 3.6 V, V_O = 3.6 V			5	μA	
Low-level output leakage current	I_{LOL}	V_{DD} = 3.6 V, V_O = 0 V			–5	μA	

Notes **1.** Applied to the TClock pin and MasterOut pin.
2. Applied to the pins other than the MasterOut pin.
3. Applied to the MasterClock pin only.
4. The value when all output pins are open
5. Target value

Remark f: PClock frequency (MHz). For example, f = 40 at 40 MHz operation

★ **Capacitance (T_A = 25 °C, V_{DD} = 0 V)**

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
Input/Output capacitance	C_{IO}	Pins other than tested pin: 0 V		10	pF

★ **AC Characteristics (T_A = –10 to +70 °C, V_{DD} = 2.2 to 3.6 V)**

All the output timing is tested by the load capacity 40 pF.

★ **(1) When 2.2 ≤ V_{DD} < 2.7 V**

Master clock and clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Master clock high-level width	t_{KKH}		115		ns
Master clock low-level width	t_{KKL}		115		ns
Master clock frequency**Note**			1.5	4	MHz
Master clock cycle	t_{CYK}		250	666	ns
Clock jitter	t_{Jitter}			±0.5	ns
Master clock rise time	t_{KR}			10	ns
Master clock fall time	t_{KF}			10	ns

Note The operation of the V_R4100 is guaranteed only when the PLL is enable.
The frequency of the master clock is 0 MHz when the PLL is in the self-running mode.
To set the processor in the self-running mode, fix the master clock to the high or low level.

Remark The output of MasterOut is 500 kHz (TYP.) in the self-running mode.

System Interface Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time**Note 1**	t_{DO}		3	20	ns
Data setup delay time**Note 1**	t_{DS}		5		ns
Data hold delay time**Note 1**	t_{DH}		1**Note 2**		ns
MasterOut rise time	t_{MOR}			7	ns
MasterOut fall time	t_{MOF}			7	ns
MasterOut high-level width	t_{MOH}		118		ns
MasterOut low-level width	t_{MOL}		118		ns
TClock rise time	t_{TCR}			5	ns
TClock fall time	t_{TCF}			5	ns
TClock high-level width	t_{TCH}		26		ns
TClock low-level width	t_{TCL}		26		ns

Notes 1. Applied to all system interface pins
2. Target value

(2) When 2.7 ≤ V_{DD} ≤ 3.6 V

Master clock and clock parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit	
Master clock high-level width	t_{KKH}	2.7 ≤ V_{DD} < 3.0	56		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	45			
Master clock low-level width	t_{KKL}	2.7 ≤ V_{DD} < 3.0	56		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	45			
Master clock frequency**Note**		2.7 ≤ V_{DD} < 3.0	1.5	8.25	MHz	★
		3.0 ≤ V_{DD} ≤ 3.6	1.5	10		
Master clock cycle	t_{CYK}	2.7 ≤ V_{DD} < 3.0	121	666	ns	★
		3.0 ≤ V_{DD} ≤ 3.6	100	666		
Clock jitter	t_{Jitter}			±0.5	ns	★
Master clock rise time	t_{KR}			5	ns	
Master clock fall time	t_{KF}			5	ns	

Note The operation of the V_R4100 is guaranteed only when the PLL is enable.
The frequency of the master clock is 0 MHz when the PLL is in the self-running mode. ★
To set the processor in the self-running mode, fix the master clock to the high or low level.

Remark The output of MasterOut is 500 kHz (TYP.) in the self-running mode. ★

System Interface Parameter

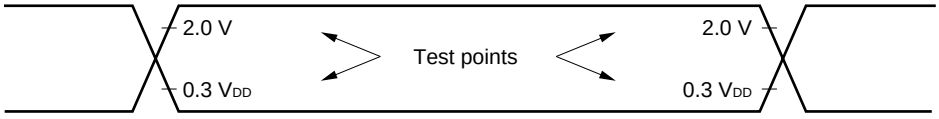
Parameter	Symbol	Condition	MIN.	MAX.	Unit	
Data output delay time**Note 1**	t_{DO}		3	15	ns	
Data setup delay time**Note 1**	t_{DS}		5		ns	★
Data hold delay time**Note 1**	t_{DH}		1**Note 2**		ns	
MasterOut rise time	t_{MOR}			6	ns	
MasterOut fall time	t_{MOF}			6	ns	
MasterOut high-level width	t_{MOH}	2.7 ≤ V_{DD} < 3.0	55		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	44			
MasterOut low-level width	t_{MOL}	2.7 ≤ V_{DD} < 3.0	55		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	44			
TClock rise time	t_{TCR}			3	ns	
TClock fall time	t_{TCF}			3	ns	
TClock high-level width	t_{TCH}	2.7 ≤ V_{DD} < 3.0	12		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	9			
TClock low-level width	t_{TCL}	2.7 ≤ V_{DD} < 3.0	12		ns	★
		3.0 ≤ V_{DD} ≤ 3.6	9			

Notes 1. Applied to all system interface pins
2. Target value

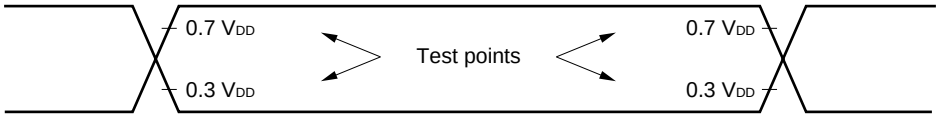
Load Coefficient

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

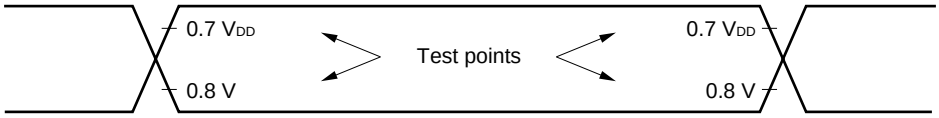
AC Test Input Points (except MasterClock)



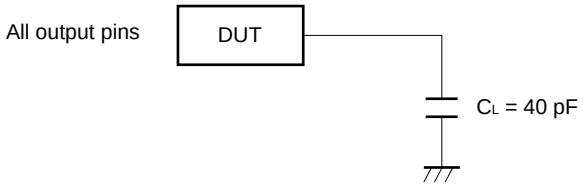
AC Test Input Points (MasterClock)



AC Test Output Points

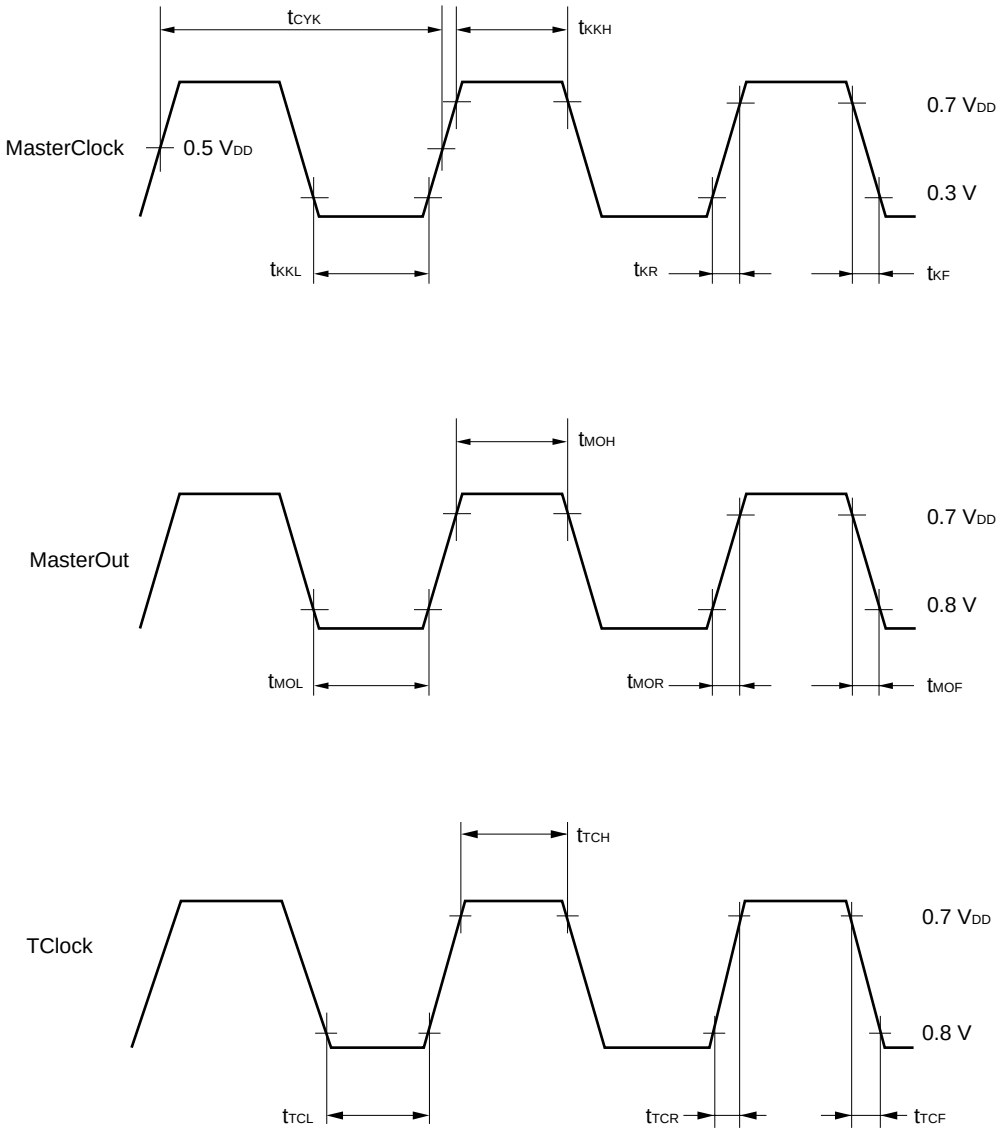


Test Load

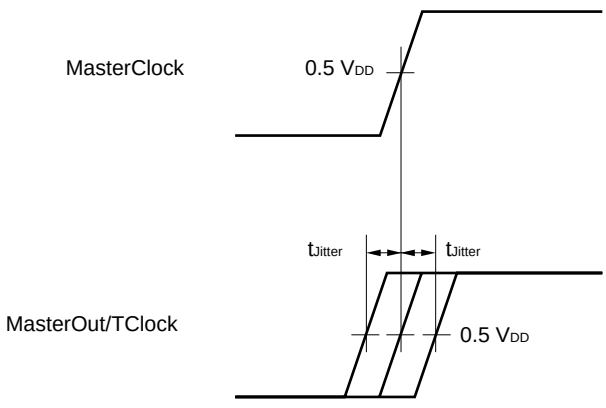


Timing Chart

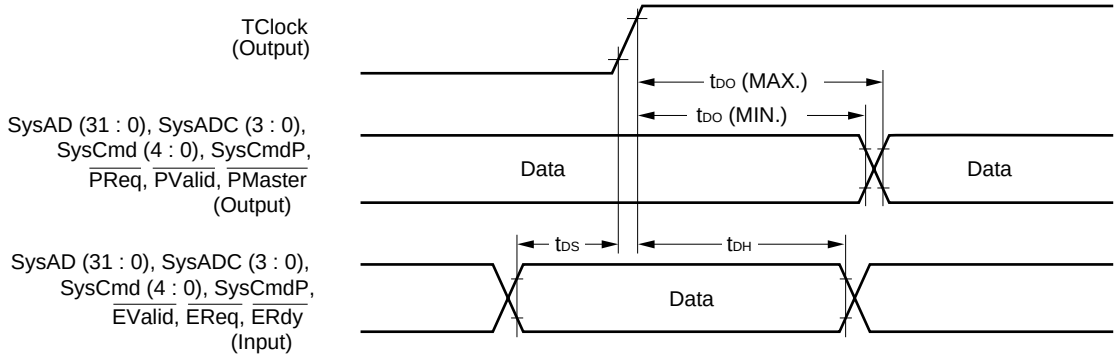
Clock timing



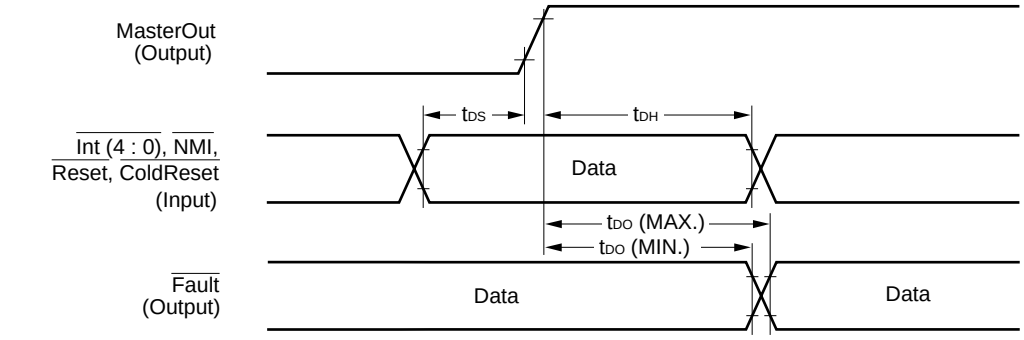
Clock jitter



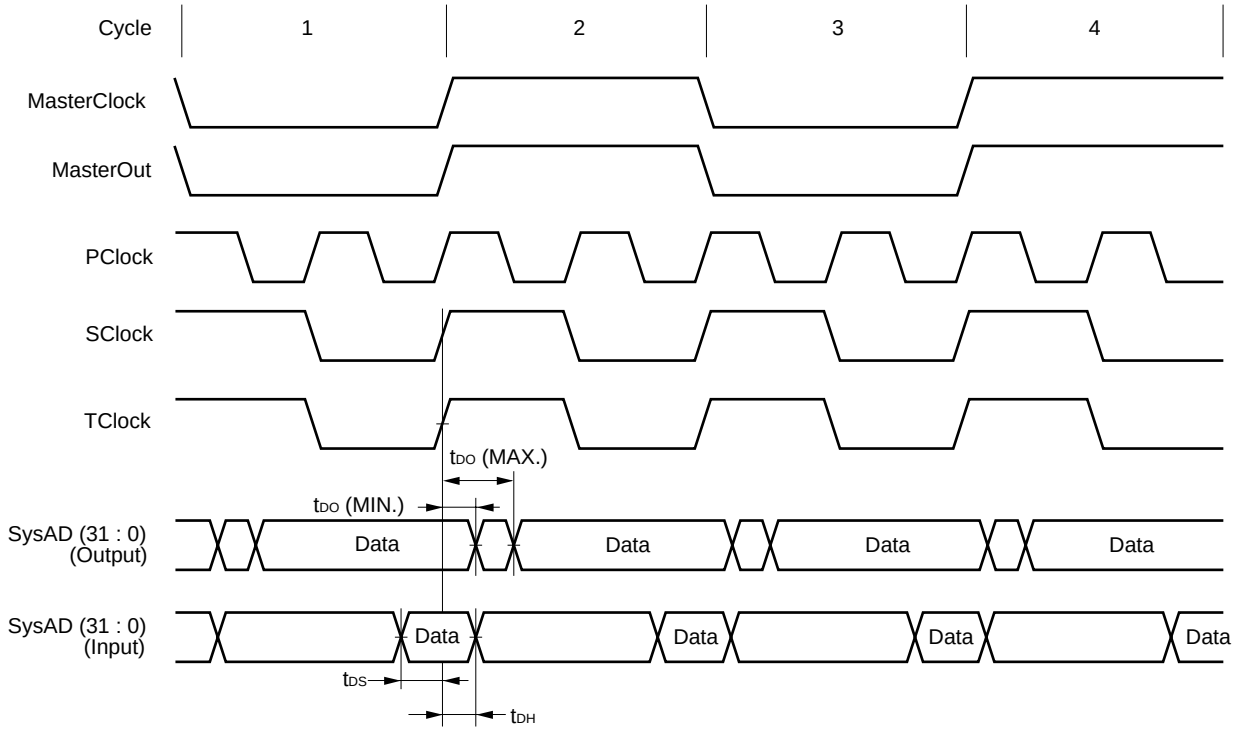
System interface edge timing



Interrupt/reset edge timing

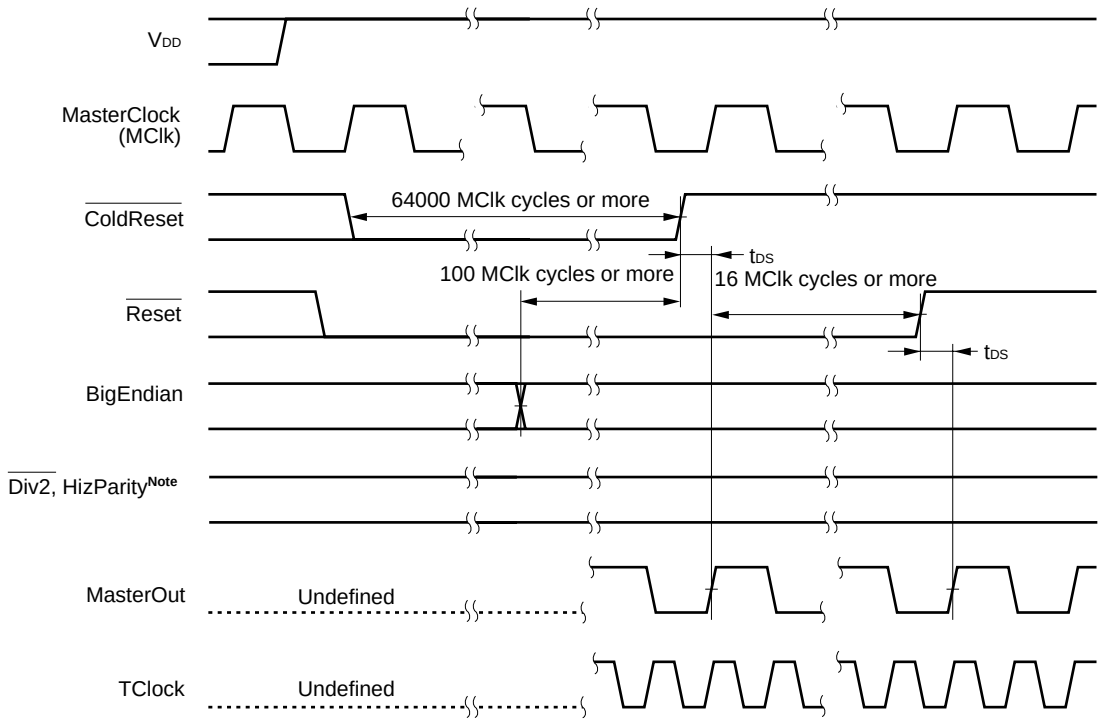


Relation between clock and system bus (when the Div2 pin is set to low)



Remark For the details or t_{DO}, t_{DS}, and t_{DH}, refer to **System interface edge timing**.

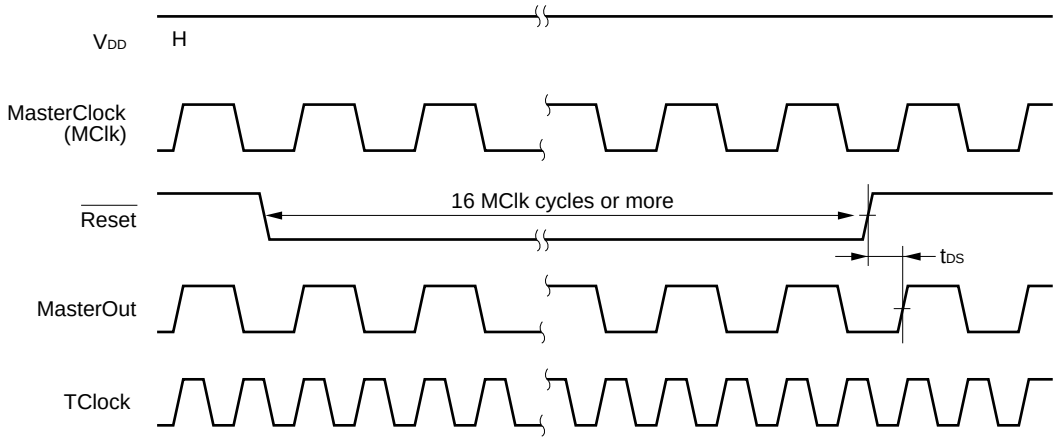
Cold reset timing



Note Fix the status of the $\overline{\text{Div2}}$ and HizParity pins on power application.

Remark For the datails on t_{DS}, refer to **Interrupt/reset edge timing**.

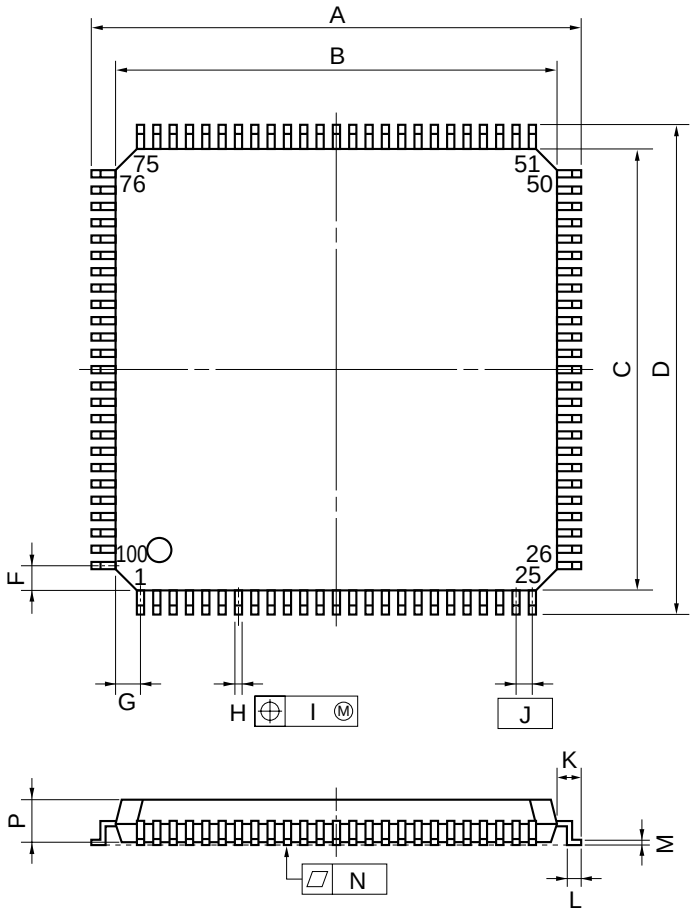
Soft reset timing

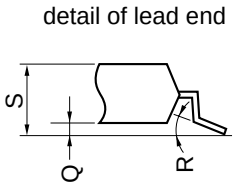


Remark For the datails on t_{DS}, refer to **Interrupt/reset edge timing**.

★ 8. PACKAGE DRAWING

100 PIN PLASTIC QFP (FINE PITCH) (□14)





NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

APPENDIX DIFFERENCES BETWEEN VR4100 AND VR4300™ ★

Item		VR4100	VR4300
Instruction set	Multi-processor synchronization (LL, LLD, SC, SCD) instructions	None	Supported
	Sum-of-products (MADD16, DMADD16) Instructions	Supported	None
	Standby mode transition instruction	Supported	None
	Floating-point instruction	None	Supported
PRId register		Imp = 0x0C	Imp = 0x0B
TLB	Page size	1 K, 4 K, 16 K, 64 K, 256 K	4 K, 16 K, 64 K, 256 K, 1 M, 4 M, 16 M
Cache	Size	Instruction: 2K bytes Data: 1K bytes	Instruction: 16K bytes Data: 8K bytes
	Line size	Instruction: 4 words Data: 4 words	Instruction: 8 words Data: 4 words
	Parity	Instruction: 1 bit per 1 word Data: 1 bit per 1 byte	None
System bus interface	Handshake signal	$\overline{\text{ERq}}$, $\overline{\text{PReq}}$, $\overline{\text{PMaster}}$, $\overline{\text{ERdy}}$	$\overline{\text{ERq}}$, $\overline{\text{PReq}}$, $\overline{\text{PMaster}}$, $\overline{\text{EOK}}$
	Write data transfer rate	D, Dx, Dxx, Dxxx	D, Dxx
	Address generation during block read	Subblock in word units for both instruction and data	Instruction: Sequential Data: Subblock in 2-word units
	Address generation during block write	Subblock in word units for both instruction and data	Sequential for both instruction and data
	Non-cache high-speed write	Supported (set by AD bit of config register)	Supported
	Address ready timing	2S cycles before issuance cycle ($\overline{\text{ERdy}}$ active)	From 1S cycle before issuance cycle to issuance cycle ($\overline{\text{EOK}}$ active)
	Re-execution of processor request	None	Supported
	Status after last data write	Ends access	Retains last data when transfer rate is set
	Parity check	1 bit per 1 byte	None
	SysCmd bus parity miss indication	$\overline{\text{Fault}}$ pin	None
Clock interface	Multiplication rate of input to internal	4	1.5, 2, 3
	Division rate of internal to bus	1, 2	1.5, 2, 3
	Clock output	TClock, MasterOut	TClock
	SyncOut-SyncIn bus	None	Supported
Manipulation at cold reset		Both $\overline{\text{ColdReset}}$ and $\overline{\text{Reset}}$ pins are asserted	$\overline{\text{ColdReset}}$ pin is asserted ($\overline{\text{Reset}}$ pin is don't care)
JTAG interface		None	Supported
Standby mode		3 types	None
Supply voltage		2.2 to 3.6 V	3.0 to 3.6 V

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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Note that this document is not designated as 'preliminary', while some of the related documents are preliminary versions.

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