NEC

MOS INTEGRATED CIRCUIT

μPD720404

PCI Express – PCI/PCI-X Bridge

(Ver 1.03)

μPD720404 is a PCI Express to PCI/PCI-X Bridge chip that supports the PCI Express Base Specification Revision1.1 and PCI Express to PCI/PCI-X Bridge Specification Revision1.0. μPD720404 contains a PCI Express Serdes circuit with an x4 Lane structure as a primary interface and single 64bits PCI/PCI-X bus interface circuit.

Ordering Information

Part number	Package	Chip Version	Remark
μPD720404F1-JN3	320-pin Plastic BGA (21x21)	Ver.1.1	
μPD720404F1-JN3-A	320-pin Plastic BGA (21x21)	Ver.1.1	Lead-free product

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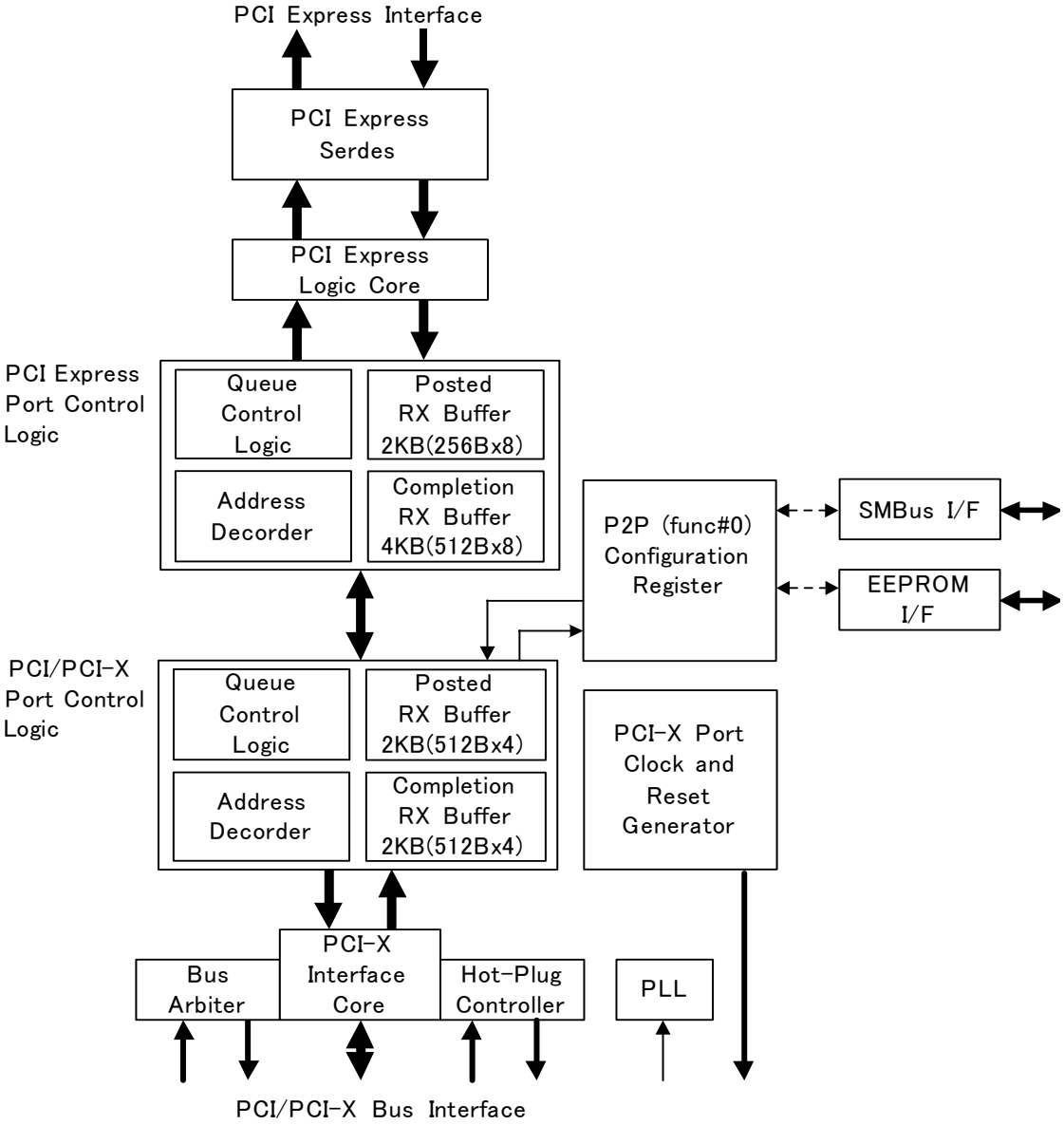
1. Features

- PCI Express Interface
  - Compliant with The PCI Express Base Specification Revision 1.1
  - Contains x4Lane 2.5Gbps full-duplex serial interface PCI Express Serdes
  - Supports 1 Virtual Channel
  - Supports 256 byte Max Payload Size
  - Supports PCI Express Advanced Error Logging
  - Supports Data Poisoning
  - Supports ECRC checking and generation
- PCI/PCI-X Interface
  - Compliant with the PCI Local Bus Specification Revision 3.0, PCI-X Protocol/Electrical and Mechanical Addendum to the PCI Local Bus Specification Revision 2.0a
  - Compliant with PCI-PCI Bridge Specification Revision 1.2 and PCI Express to PCI/PCI-X Bridge Specification Revision 1.0
  - Supports single PCI/PCI-X bus interface
  - Supports 133MHz Single Data Rate 64 bit PCI-X mode (PCI-X Mode1) and 66MHz 64 bit PCI mode
  - Supports 3.3V signaling (not supports 5V tolerant signaling)
  - Supports LOCK# transaction
  - Contains arbitration fucntions for up to 4 external agents at the PCI/PCI-X port
  - Supports PCI bus parking function
- SMBus Interface
  - Conforms to SMBus Specification Version 2.0
  - SMBus Slave interface
  - Supports Read/Write access to internal configuration and memory mapped registers
  - Supports Packet Error Checking (PEC)
  - Supports SMBus Alert
- EEPROM Interface
  - Parameter loading from Serial EEPROM (set in Configuration registers)
- Hot Plug Controller
  - Compliant with PCI SHPC and Subsystem Specification Revision 1.0
  - Supports Hot Plug Controller functions at the PCI/PCI-X port
  - Supports Hot Plug Slot controls in both parellel and serial modes
  - Supports interface for ACPI Hot Plug handling as well as OSHP (Operating System Hot Plug)
- Power Management
  - Compliant with to PCI Bus Power Management Interface Specification Revision1.1
  - Supports D0, D1 and D3 power states

  - Supports S3 wake-up by PME Messaging
  - Supports PCI Express Active State Power Management L0s and L1
- Package
  - 21mm x 21mm Plastic BGA
- Memory Buffer Architecture
  - Contains a 4K byte completion data reception buffer and a 2K byte Posted data reception buffer in the PCI Express interface port
  - Contains a 2K byte completion data reception buffer and a 2K byte Posted data reception buffer in the PCI/PCI-X interface port
  - 8 Posted Transactions managed by the PCI Express interface
  - 8 Non-posted Split Transactions managed by the PCI Express interface
  - 4 Posted Transactions managed by the PCI/PCI-X interface port
  - 4 Non-posted Split Transactions managed by the PCI/PCI-X interface port
  - 4 Delayed Transactions managed by the PCI/PCI-X interface
  - Supports Parity Protection of built-in SRAM data
- Testing
  - Supports IEEE® 1149.1 JTAG

2. Block Diagram

Figure 2-1 Block Diagram of μPD720404



PCI Express Serdes	x4 Lane Full duplex Serializer/Deserializer function
PCI Express Logic Core	PCI Express Logical Protocol (Logical Physical Layer, Data Link Layer, Transaction Layer (Flow Control Management)) function
PCI Express Port Control Logic	PCI Express port reception buffer control, address decoding process, transaction queue control function
PCI/PCI-X Port Control Logic	PCI/PCI-X port reception buffer control, address decoding process, transaction queue control function
PCI-X Interface Core	64bits PCI/PCI-X Master, Target processing function
Bus Arbiter	PCI/PCI-X bus arbitration function
Hot-Plug Controller	SHPC compatible Hot-Plug Controller processing function
P2P Configuration Register	Type 1 PCI-PCI Bridge Configuration Register
PCI-X Port Clock and Reset Generator	PCI/PCI-X Clock generation and Reset generation
PLL	Feedback PCI Cock Skew rectification PLL
SMBus I/F	SMBus Slave controller function
EEPROM I/F	Serial EEPROM Master controller function

3. Pin Connection

- **320-pin plastic BGA (21 x 21 mm)**

  μPD720404

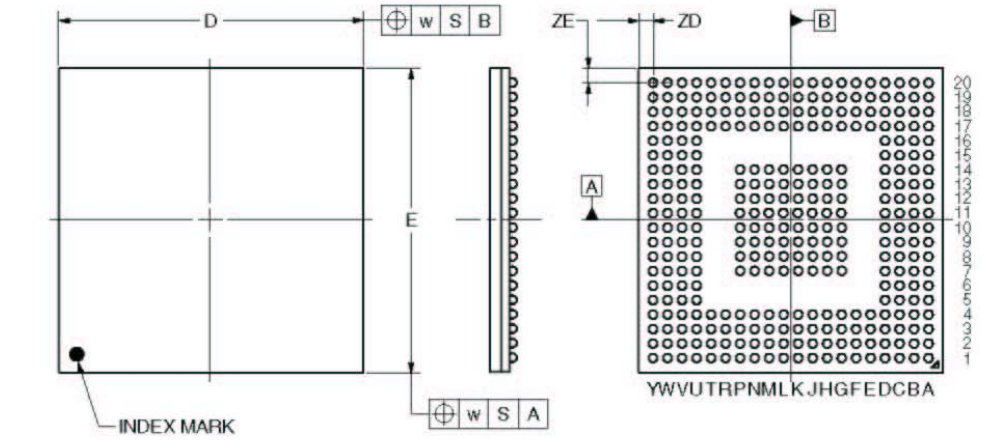
Bottom view (1/2)

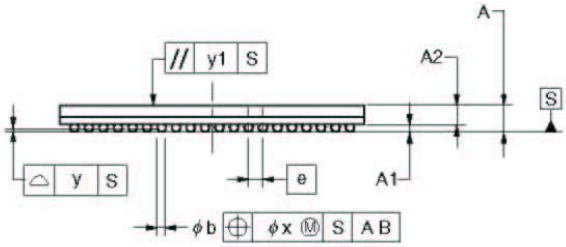
	A	B	C	D	E	F	G	H	J	K
1	VSS	VSS	S_PCIXCAP_P	S_PERRB	S_CBE1B	S_AD13	VSS	VDD3.3	EPR_EN	S_AD6
2	VDD3.3	S_PCIXCAP_I	S_STOPB	S_SERRB	S_AD15	S_AD12	S_AD9	S_HPCM1	S_CBE0B	S_AD5
3	S_TRDYB	S_DEVSELB	S_LOCKB	S_PAR	S_AD14	S_AD11	S_AD8	S_HPCM0	S_AD7	S_AD4
4	S_CBE2B	S_FRAMEB	S_IRDYB	VSS	VDD1.5	S_AD10	VDD3.3	S_CLKM	VSS	VDD1.5
5	S_AD18	S_AD17	S_AD16	VDD3.3						
6	S_AD22	S_AD21	S_AD20	S_AD19						
7	S_AD24	S_CBE3B	S_AD23	VDD1.5			VDD3.3	VDD1.5	VDD1.5	VSS
8	S_AD27	S_AD26	S_AD25	VSS			VDD3.3	VDD3.3	VDD3.3	VSS
9	S_AD30	S_AD29	S_AD28	VDD3.3			VDD1.5	VDD1.5	VDD1.5	VSS
10	VSS	NTEST5	CTRI	S_AD31			VSS	VSS	VSS	VSS
11	VDD3.3	SMB_ADD0	NTEST3	VDD1.5			VSS	VSS	VSS	VSS
12	SMB_ADD2	SMB_ADD4	NTEST2	VSS			VDD1.5	VDD1.5	VDD1.5	VSS
13	AVSS2	AVSS2	SMB_ADD1	VDD3.3			VDD3.3	VDD3.3	VDD3.3	VSS
14	AVDD2	AVDD2	SD_TESTEN	VDD1.5			VDD3.3	VDD1.5	VDD1.5	VSS
15	SMB_ADD3	DBT_MODE	NTEST4	NTEST1						
16	SB_PCLK_I	EPR_DAT	SB_PCLK	VDD1.5						
17	SMB_ALERTB	NTEST7	PWRGD	VSS	VDD3.3	VDD1.5	VDD1.5	AVDD1	VSS	AVSS1
18	NTEST8	S_SOL	SMB_CLK	VAUX_DET	VDD1.5	VSS	VSS	VSS	VDD1.5	AVSS1
19	VDD3.3	NTEST6	TCK	EPR_CLK	TMS	P_TX0P	P_TX1P	P_TX2P	P_TX3P	P_REF100P
20	VDD3.3	VSS	TRSTB	TDI	TDO	P_TX0N	P_TX1N	P_TX2N	P_TX3N	P_REF100N

Bottom view (2/2)

L	M	N	P	R	T	U	V	W	Y	
S_AD3	VDD3.3	VSS	S_CBE5B	S_AD63	S_AD59	S_AD56	S_SLOTM2	VSS	VDD3.3	1
S_AD2	S_AD0	S_CBE7B	S_CBE4B	S_AD62	S_AD58	S_SLOTM0	DC_TEST_MODE	TMC2	S_M66EN	2
S_AD1	S_REQ64B	S_CBE6B	S_PAR64	S_AD61	S_AD57	S_SLOTM1	TMC1	S_M66EN_O	VDD3.3	3
VDD1.5	S_ACK64B	VDD3.3	VDD1.5	S_AD60	VDD1.5	VDD3.3	S_AD53	S_AD54	S_AD55	4
						VSS	S_AD50	S_AD51	S_AD52	5
						S_AD46	S_AD47	S_AD48	S_AD49	6
VSS	VDD1.5	VDD1.5	VDD3.3			VDD1.5	S_AD44	S_AD45	VDD3.3	7
VSS	VDD3.3	VDD3.3	VDD3.3			VDD3.3	S_AD42	S_AD43	VSS	8
VSS	VDD1.5	VDD1.5	VDD1.5			S_AD38	S_AD39	S_AD40	S_AD41	9
VSS	VSS	VSS	VSS			VSS	S_AD35	S_AD36	S_AD37	10
VSS	VSS	VSS	VSS			VDD1.5	S_AD32	S_AD33	S_AD34	11
VSS	VDD1.5	VDD1.5	VDD1.5			S_GNT1B	S_GNT0B	S_GNT2B	VSS	12
VSS	VDD3.3	VDD3.3	VDD3.3			VDD3.3	S_PCLK2	S_GNT3B	VDD3.3	13
VSS	VDD1.5	VDD1.5	VDD3.3			VDD1.5	S_PCLK_I	S_PCLK4	S_PCLK1	14
						PX_REF133	S_INTBB	S_PCLK0	S_PCLK3	15
						S_PMEB	S_INTCB	AVSS2	AVSS2	16
VSS	VDD1.5	VDD1.5	VDD1.5	VDD1.5	VDD3.3	VSS	S_SIC	AVDD2	AVDD2	17
VDD1.5	VSS	VSS	VSS	S_SOD	VDD1.5	S_INTDB	S_REQ0B	S_REQ2B	S_REQ3B	18
P_RX0P	P_RX1P	P_RX2P	P_RX3P	P_WAKEB	S_SOC	S_SID	S_INTAB	S_REQ1B	VDD3.3	19
P_RX0N	P_RX1N	P_RX2N	P_RX3N	RSM_PWRGD	SMB_DAT	S_SORB	S_SILB	VDD1.5	VSS	20

320-PIN PLASTIC BGA (21x21)





(UNIT:mm)

ITEM	DIMENSIONS
D	21.00±0.10
E	21.00±0.10
w	0.30
e	1.00
A	1.83±0.17
A1	0.50±0.10
A2	1.33
b	0.60±0.10
x	0.15
y	0.15
y1	0.35
ZD	1.00
ZE	1.00

P320F1-100-JN3

3.1. Pin List (numerical order)

PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
A1	VSS	C11	NTEST3	G7	VDD3.3	K9	VSS
A2	VDD3.3	C12	NTEST2	G8	VDD3.3	K10	VSS
A3	S_TRDYB	C13	SMB_ADD1	G9	VDD1.5	K11	VSS
A4	S_CBE2B	C14	SD_TESTEN	G10	VSS	K12	VSS
A5	S_AD18	C15	NTEST4	G11	VSS	K13	VSS
A6	S_AD22	C16	SB_PCLK	G12	VDD1.5	K14	VSS
A7	S_AD24	C17	PWRGD	G13	VDD3.3	K17	AVSS1
A8	S_AD27	C18	SMB_CLK	G14	VDD3.3	K18	AVSS1
A9	S_AD30	C19	TCK	G17	VDD1.5	K19	P_REF100P
A10	VSS	C20	TRSTB	G18	VSS	K20	P_REF100N
A11	VDD3.3	D1	S_PERRB	G19	P_TX1P	L1	S_AD3
A12	SMB_ADD2	D2	S_SERRB	G20	P_TX1N	L2	S_AD2
A13	AVSS2	D3	S_PAR	H1	VDD3.3	L3	S_AD1
A14	AVDD2	D4	VSS	H2	S_HPCM1	L4	VDD1.5
A15	SMB_ADD3	D5	VDD3.3	H3	S_HPCM0	L7	VSS
A16	SB_PCLK_I	D6	S_AD19	H4	S_CLKM	L8	VSS
A17	SMB_ALERTB	D7	VDD1.5	H7	VDD1.5	L9	VSS
A18	NTEST8	D8	VSS	H8	VDD3.3	L10	VSS
A19	VDD3.3	D9	VDD3.3	H9	VDD1.5	L11	VSS
A20	VDD3.3	D10	S_AD31	H10	VSS	L12	VSS
B1	VSS	D11	VDD1.5	H11	VSS	L13	VSS
B2	S_PCIXCAP_I	D12	VSS	H12	VDD1.5	L14	VSS
B3	S_DEVSELB	D13	VDD3.3	H13	VDD3.3	L17	VSS
B4	S_FRAMEB	D14	VDD1.5	H14	VDD1.5	L18	VDD1.5
B5	S_AD17	D15	NTEST1	H17	AVDD1	L19	P_RX0P
B6	S_AD21	D16	VDD1.5	H18	VSS	L20	P_RX0N
B7	S_CBE3B	D17	VSS	H19	P_TX2P	M1	VDD3.3
B8	S_AD26	D18	VAUX_DET	H20	P_TX2N	M2	S_AD0
B9	S_AD29	D19	EPR_CLK	J1	EPR_EN	M3	S_REQ64B
B10	NTEST5	D20	TDI	J2	S_CBE0B	M4	S_ACK64B
B11	SMB_ADD0	E1	S_CBE1B	J3	S_AD7	M7	VDD1.5
B12	SMB_ADD4	E2	S_AD15	J4	VSS	M8	VDD3.3
B13	AVSS2	E3	S_AD14	J7	VDD1.5	M9	VDD1.5
B14	AVDD2	E4	VDD1.5	J8	VDD3.3	M10	VSS
B15	DBT_MODE	E17	VDD3.3	J9	VDD1.5	M11	VSS
B16	EPR_DAT	E18	VDD1.5	J10	VSS	M12	VDD1.5
B17	NTEST7	E19	TMS	J11	VSS	M13	VDD3.3
B18	S_SOL	E20	TDO	J12	VDD1.5	M14	VDD1.5
B19	NTEST6	F1	S_AD13	J13	VDD3.3	M17	VDD1.5
B20	VSS	F2	S_AD12	J14	VDD1.5	M18	VSS
C1	S_PCIXCAP_P	F3	S_AD11	J17	VSS	M19	P_RX1P
C2	S_STOPB	F4	S_AD10	J18	VDD1.5	M20	P_RX1N
C3	S_LOCKB	F17	VDD1.5	J19	P_TX3P	N1	VSS
C4	S_IRDYB	F18	VSS	J20	P_TX3N	N2	S_CBE7B
C5	S_AD16	F19	P_TX0P	K1	S_AD6	N3	S_CBE6B
C6	S_AD20	F20	P_TX0N	K2	S_AD5	N4	VDD3.3
C7	S_AD23	G1	VSS	K3	S_AD4	N7	VDD1.5
C8	S_AD25	G2	S_AD9	K4	VDD1.5	N8	VDD3.3
C9	S_AD28	G3	S_AD8	K7	VSS	N9	VDD1.5
C10	CTRI	G4	VDD3.3	K8	VSS	N10	VSS

PKG	NAME	PKG	NAME	PKG	NAME	PKG	NAME
N11	VSS	U11	VDD1.5	Y1	VDD3.3		
N12	VDD1.5	U12	S_GNT1B	Y2	S_M66EN		
N13	VDD3.3	U13	VDD3.3	Y3	VDD3.3		
N14	VDD1.5	U14	VDD1.5	Y4	S_AD55		
N17	VDD1.5	U15	PX_REF133	Y5	S_AD52		
N18	VSS	U16	S_PMEB	Y6	S_AD49		
N19	P_RX2P	U17	VSS	Y7	VDD3.3		
N20	P_RX2N	U18	S_INTDB	Y8	VSS		
P1	S_CBE5B	U19	S_SID	Y9	S_AD41		
P2	S_CBE4B	U20	S_SORB	Y10	S_AD37		
P3	S_PAR64	V1	S_SLOTM2	Y11	S_AD34		
P4	VDD1.5	V2	DC_TEST_MODE	Y12	VSS		
P7	VDD3.3	V3	TMC1	Y13	VDD3.3		
P8	VDD3.3	V4	S_AD53	Y14	S_PCLK1		
P9	VDD1.5	V5	S_AD50	Y15	S_PCLK3		
P10	VSS	V6	S_AD47	Y16	AVSS2		
P11	VSS	V7	S_AD44	Y17	AVDD2		
P12	VDD1.5	V8	S_AD42	Y18	S_REQ3B		
P13	VDD3.3	V9	S_AD39	Y19	VDD3.3		
P14	VDD3.3	V10	S_AD35	Y20	VSS		
P17	VDD1.5	V11	S_AD32				
P18	VSS	V12	S_GNT0B				
P19	P_RX3P	V13	S_PCLK2				
P20	P_RX3N	V14	S_PCLK_I				
R1	S_AD63	V15	S_INTBB				
R2	S_AD62	V16	S_INTCB				
R3	S_AD61	V17	S_SIC				
R4	S_AD60	V18	S_REQ0B				
R17	VDD1.5	V19	S_INTAB				
R18	S_SOD	V20	S_SILB				
R19	P_WAKEB	W1	VSS				
R20	RSM_PWRGD	W2	TMC2				
T1	S_AD59	W3	S_M66EN_O				
T2	S_AD58	W4	S_AD54				
T3	S_AD57	W5	S_AD51				
T4	VDD1.5	W6	S_AD48				
T17	VDD3.3	W7	S_AD45				
T18	VDD1.5	W8	S_AD43				
T19	S_SOC	W9	S_AD40				
T20	SMB_DAT	W10	S_AD36				
U1	S_AD56	W11	S_AD33				
U2	S_SLOTM0	W12	S_GNT2B				
U3	S_SLOTM1	W13	S_GNT3B				
U4	VDD3.3	W14	S_PCLK4				
U5	VSS	W15	S_PCLK0				
U6	S_AD46	W16	AVSS2				
U7	VDD1.5	W17	AVDD2				
U8	VDD3.3	W18	S_REQ2B				
U9	S_AD38	W19	S_REQ1B				
U10	VSS	W20	VDD1.5				

3.2. Pin List (alphabetical order)

NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
AVDD1	H17	S_AD2	L2	S_AD52	Y5	S_REQ1B	W19
AVDD2	A14	S_AD3	L1	S_AD53	V4	S_REQ2B	W18
AVDD2	B14	S_AD4	K3	S_AD54	W4	S_REQ3B	Y18
AVDD2	W17	S_AD5	K2	S_AD55	Y4	S_REQ64B	M3
AVDD2	Y17	S_AD6	K1	S_AD56	U1	S_SERRB	D2
AVSS1	K17	S_AD7	J3	S_AD57	T3	S_SIC	V17
AVSS1	K18	S_AD8	G3	S_AD58	T2	S_SID	U19
AVSS2	A13	S_AD9	G2	S_AD59	T1	S_SILB	V20
AVSS2	B13	S_AD10	F4	S_AD60	R4	S_SLOTM0	U2
AVSS2	W16	S_AD11	F3	S_AD61	R3	S_SLOTM1	U3
AVSS2	Y16	S_AD12	F2	S_AD62	R2	S_SLOTM2	V1
CTRI	C10	S_AD13	F1	S_AD63	R1	S_SOC	T19
DBT_MODE	B15	S_AD14	E3	S_CBE0B	J2	S_SOD	R18
DC_TEST_MODE	V2	S_AD15	E2	S_CBE1B	E1	S_SOL	B18
EPR_CLK	D19	S_AD16	C5	S_CBE2B	A4	S_SORB	U20
EPR_DAT	B16	S_AD17	B5	S_CBE3B	B7	S_STOPB	C2
EPR_EN	J1	S_AD18	A5	S_CBE4B	P2	S_TRDYB	A3
NTEST1	D15	S_AD19	D6	S_CBE5B	P1	SB_PCLK	C16
NTEST2	C12	S_AD20	C6	S_CBE6B	N3	SB_PCLK_I	A16
NTEST3	C11	S_AD21	B6	S_CBE7B	N2	SD_TESTEN	C14
NTEST4	C15	S_AD22	A6	S_CLKM	H4	SMB_ADD0	B11
NTEST5	B10	S_AD23	C7	S_DEVSELB	B3	SMB_ADD1	C13
NTEST6	B19	S_AD24	A7	S_FRAMEB	B4	SMB_ADD2	A12
NTEST7	B17	S_AD25	C8	S_GNT0B	V12	SMB_ADD3	A15
NTEST8	A18	S_AD26	B8	S_GNT1B	U12	SMB_ADD4	B12
P_REF100N	K20	S_AD27	A8	S_GNT2B	W12	SMB_ALERTB	A17
P_REF100P	K19	S_AD28	C9	S_GNT3B	W13	SMB_CLK	C18
P_RX0N	L20	S_AD29	B9	S_HPCM0	H3	SMB_DAT	T20
P_RX0P	L19	S_AD30	A9	S_HPCM1	H2	TCK	C19
P_RX1N	M20	S_AD31	D10	S_INTAB	V19	TDI	D20
P_RX1P	M19	S_AD32	V11	S_INTBB	V15	TDO	E20
P_RX2N	N20	S_AD33	W11	S_INTCB	V16	TMC1	V3
P_RX2P	N19	S_AD34	Y11	S_INTDB	U18	TMC2	W2
P_RX3N	P20	S_AD35	V10	S_IRDYB	C4	TMS	E19
P_RX3P	P19	S_AD36	W10	S_LOCKB	C3	TRSTB	C20
P_TX0N	F20	S_AD37	Y10	S_M66EN	Y2	VAUX_DET	D18
P_TX0P	F19	S_AD38	U9	S_M66EN_O	W3	VDD1.5	D7
P_TX1N	G20	S_AD39	V9	S_PAR	D3	VDD1.5	D11
P_TX1P	G19	S_AD40	W9	S_PAR64	P3	VDD1.5	D14
P_TX2N	H20	S_AD41	Y9	S_PCIXCAP_I	B2	VDD1.5	D16
P_TX2P	H19	S_AD42	V8	S_PCIXCAP_P	C1	VDD1.5	E4
P_TX3N	J20	S_AD43	W8	S_PCLK_I	V14	VDD1.5	E18
P_TX3P	J19	S_AD44	V7	S_PCLK0	W15	VDD1.5	F17
P_WAKEB	R19	S_AD45	W7	S_PCLK1	Y14	VDD1.5	G9
PWRGD	C17	S_AD46	U6	S_PCLK2	V13	VDD1.5	G12
PX_REF133	U15	S_AD47	V6	S_PCLK3	Y15	VDD1.5	G17
RSM_PWRGD	R20	S_AD48	W6	S_PCLK4	W14	VDD1.5	H7
S_ACK64B	M4	S_AD49	Y6	S_PERRB	D1	VDD1.5	H9
S_AD0	M2	S_AD50	V5	S_PMEB	U16	VDD1.5	H12
S_AD1	L3	S_AD51	W5	S_REQ0B	V18	VDD1.5	H14

NAME	PKG	NAME	PKG	NAME	PKG	NAME	PKG
VDD1.5	J7	VDD3.3	N4	VSS	L13		
VDD1.5	J9	VDD3.3	N8	VSS	L14		
VDD1.5	J12	VDD3.3	N13	VSS	L17		
VDD1.5	J14	VDD3.3	P7	VSS	M10		
VDD1.5	J18	VDD3.3	P8	VSS	M11		
VDD1.5	K4	VDD3.3	P13	VSS	M18		
VDD1.5	L4	VDD3.3	P14	VSS	N1		
VDD1.5	L18	VDD3.3	T17	VSS	N10		
VDD1.5	M7	VDD3.3	U4	VSS	N11		
VDD1.5	M9	VDD3.3	U8	VSS	N18		
VDD1.5	M12	VDD3.3	U13	VSS	P10		
VDD1.5	M14	VDD3.3	Y1	VSS	P11		
VDD1.5	M17	VDD3.3	Y3	VSS	P18		
VDD1.5	N7	VDD3.3	Y7	VSS	U5		
VDD1.5	N9	VDD3.3	Y13	VSS	U10		
VDD1.5	N12	VDD3.3	Y19	VSS	U17		
VDD1.5	N14	VSS	A1	VSS	W1		
VDD1.5	N17	VSS	A10	VSS	Y8		
VDD1.5	P4	VSS	B1	VSS	Y12		
VDD1.5	P9	VSS	B20	VSS	Y20		
VDD1.5	P12	VSS	D4				
VDD1.5	P17	VSS	D8				
VDD1.5	R17	VSS	D12				
VDD1.5	T4	VSS	D17				
VDD1.5	T18	VSS	F18				
VDD1.5	U7	VSS	G1				
VDD1.5	U11	VSS	G10				
VDD1.5	U14	VSS	G11				
VDD1.5	W20	VSS	G18				
VDD3.3	A2	VSS	H10				
VDD3.3	A11	VSS	H11				
VDD3.3	A19	VSS	H18				
VDD3.3	A20	VSS	J4				
VDD3.3	D5	VSS	J10				
VDD3.3	D9	VSS	J11				
VDD3.3	D13	VSS	J17				
VDD3.3	E17	VSS	K7				
VDD3.3	G4	VSS	K8				
VDD3.3	G7	VSS	K9				
VDD3.3	G8	VSS	K10				
VDD3.3	G13	VSS	K11				
VDD3.3	G14	VSS	K12				
VDD3.3	H1	VSS	K13				
VDD3.3	H8	VSS	K14				
VDD3.3	H13	VSS	L7				
VDD3.3	J8	VSS	L8				
VDD3.3	J13	VSS	L9				
VDD3.3	M1	VSS	L10				
VDD3.3	M8	VSS	L11				
VDD3.3	M13	VSS	L12				

4. Pin Functions

Pin functions are described below. Pin direction types are classified as power, I (Input), O (Output), O 3State (3State Type Output), OD (Nch Open Drain Type Output), I/O (bi-directional), and I/OD (bi-directional/Nch Open Drain Type Output).

4.1. Power supply

Pin	I/O	Buffer Type	Active Level	Function
VDD3.3	Power			+3.3 V power supply
VDD1.5	Power			+1.5 V power supply
AVDD1	Power			+1.5 V power supply for PCI Express PLL circuit
AVDD2	Power			+1.5 V power supply for PCI/PCI-X Skew Control PLL circuit
VSS	Power			Ground
AVSS1	Power			Ground for PCI Express PLL circuit
AVSS2	Power			Ground for PCI/PCI-X Skew Control PLL circuit

4.2. PCI Express Interface

Pin	I/O	Buffer Type	Active Level	Function
P_TX (0 : 3)P	O	PCI Express Driver		PCI Express Transmit Data (Positive polarity signal of differential pair)
P_TX (0 : 3)N	O	PCI Express Driver		PCI Express Transmit Data (Negative polarity signal of differential pair)
P_RX (0 : 3)P	I	PCI Express Receiver		PCI Express Receive Data (Positive polarity signal of differential pair)
P_RX (0 : 3)N	I	PCI Express Receiver		PCI Express Receive Data (Negative polarity signal of differential pair)
P_REF100P	I	PCI Express Reference Clock		PCI Express 100MHz Reference Clock (Positive polarity signal of differential pair)
P_REF100N	I	PCI Express Reference Clock		PCI Express 100MHz Reference Clock (Negative polarity signal of differential pair)
P_WAKEB	OD	Nch Open Drain Output	Low	PCI Express “WAKE#” signal

4.3. PCI/PCI-X Interface

Pin	I/O	Buffer Type	Active Level	Function
S_AD (63 : 0)	I/O	PCI-X I/O		PCI /PCI-X “AD [63 : 0]” signal
S_CBE (7 : 0)B	I/O	PCI-X I/O		PCI/PCI-X “C/BE [7 : 0]” signal
S_PAR	I/O	PCI-X I/O		PCI/PCI-X “PAR” signal
S_PAR64	I/O	PCI-X I/O		PCI/PCI-X “PAR64” signal
S_FRAMEB	I/O	PCI-X I/O	Low	PCI/PCI-X “FRAME#” signal

Pin	I/O	Buffer Type	Active Level	Function
S_IRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “IRDY#” signal
S_TRDYB	I/O	PCI-X I/O	Low	PCI/PCI-X “TRDY#” signal
S_STOPB	I/O	PCI-X I/O	Low	PCI/PCI-X “STOP#” signal
S_DEVSELB	I/O	PCI-X I/O	Low	PCI/PCI-X “DEVSEL#” signal
S_REQ (3 : 0)B	I	Input	Low	PCI/PCI-X “REQ#” signal (Note) S_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode. 0b: Attention Button depressed 1b: Attention Button not depressed
S_GNT (3 : 0)B	O 3State	3-State Output	Low	PCI/PCI-X “GNT#” signal (Note) S_GNT3B is used as Power LED Control output in SHPC Parallel mode. 0b: Power LED off 1b: Power LED on
S_PERRB	I/O	PCI-X I/O	Low	PCI/PCI-X “PERR#” signal
S_SERRB	I	Input	Low	PCI/PCI-X “SERR#” signal
S_LOCKB	I/O	PCI-X I/O	Low	PCI/PCI-X “LOCK#” signal
S_REQ64B	I/O	PCI-X I/O	Low	PCI/PCI-X “REQ64#” signal
S_ACK64B	I/O	PCI-X I/O	Low	PCI/PCI-X “ACK64#” signal
S_INTAB	I	Input	Low	PCI/PCI-X “INTA#” signal
S_INTBB	I	Input	Low	PCI/PCI-X “INTB#” signal
S_INTCB	I	Input	Low	PCI/PCI-X “INTC#” signal
S_INTDB	I	Input	Low	PCI/PCI-X “INTD#” signal
S_PMEB	I	Input	Low	PCI/PCI-X “PME#” signal
S_M66EN	I	Input		PCI/PCI-X “M66EN” signal
S_M66EN_O	O 3State	3-State Output		PCI/PCI-X M66EN Low Clamp
S_PCIXCAP_I	I	Input		PCI/PCI-X “PCIXCAP” signal
S_PCIXCAP_P	O 3State	3-State Output		PCI/PCI-X PCIXCAP Low-impedance High Drive
S_PCLK (4 : 0)	O	Output		PCI/PCI-X “CLK” signal S_PCLK4 must be connected to S_PCLK_I to make a feedback loop of PCI/PCI-X PLL.
S_PCLK_I	I	Input		PCI/PCI-X Feedback Clock
SB_PCLK	O	Output		SB_PCLK must be connected to SB_PCLK_I to make a feedback loop of PCI/PCI-X PLL.
SB_PCLK_I	I	Input		PCI/PCI-X Feedback Clock

4.4. System clock & Reset interface

Pin	I/O	Buffer Type	Active Level	Function
PX_REF133	I	Input with 50 kΩ Pull down R		133MHz PCI-X reference clock provided by system clock input or oscillator input
PWRGD	I	Schmitt Trigger Input	High	Power Good signal
RSM_PWRGD	I	Schmitt Trigger Input	High	Resume Well Power Good signal

4.5. Hot Plug Controller interface

(PCI/PCI-X Port)

Pin	I/O	Buffer Type	Active Level	Function
S_SIC	I/O	I/O		(SHPC Serial-mode) Shift-in Clock output signal (SHPC Parallel-mode) Power Fault Status input signal 0b: Power Fault happened 1b: Power Fault not happened (Non-SHPC mode) Not used
S_SID	I	Input		(SHPC Serial-mode) Shift-in Data input signal (SHPC Parallel-mode) MRL Sensor Status input signal 0b: MRL closed 1b: MRL opened (Non-SHPC mode) Not used
S_SILB	O	Output		(SHPC Serial-mode) Shift-in Load control output signal. Active Low. (SHPC Parallel-mode) PCI/PCI-X RST# output signal. Active Low. (Non-SHPC mode) PCI/PCI-X RST# output signal
S_SOC	I/O	I/O		(SHPC Serial-mode) Shift-out Clock output signal (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT1# input signal

Pin	I/O	Buffer Type	Active Level	Function
S_SOD	O	Output		(SHPC Serial-mode) Shift-out Data output signal (SHPC Parallel-mode) Power Enable Control output signal 0b: Power off 1b: Power on (Non-SHPC mode) Not used
S_SOL	O	Output		(SHPC Serial-mode) Shift-out Load Control output signal. Active Low. (SHPC Parallel-mode) Attention LED Control output signal 0b: Attention LED off 1b: Attention LED on (Non-SHPC mode) Not used
S_SORB	I/O	I/O		(SHPC Serial-mode) Shift-out Reset Control output signal 0b: Reset Shift-out Registers 1b: Not reset Shift-out Registers (SHPC Parallel-mode or Non-SHPC mode) PCI/PCI-X PRSNT2# input signal

(NOTE) S_REQ3B is used as Attention Button Depress Input in SHPC Parallel mode.

S_GNT3B is used as Power LED Control Output in SHPC Parallel mode.

4.6. System Interface

Pin	I/O	Buffer Type	Active Level	Function
VAUX_DET	I	Input	High	Vaux detect signal 0: Vaux not present 1: Vaux present
SMB_CLK	I	Schmitt Trigger Input with Failsafe		SMBus Clock signal
SMB_DAT	I/OD	I/O Nch Open Drain Output		SMBus Data signal
SMB_ALERTB	OD	Nch Open Drain Output		SMBus Alert# signal
EPR_CLK	O	Output		EEPROM Clock signal
EPR_DAT	I/OD	I/O Nch Open Drain Output		EEPROM Data signal

4.7. Strap-pin Signals

Pin	I/O	Buffer Type	Active Level	Function
SMB_ADD (4 : 0)	I	Input with 50 kΩ Pull down R		SMBus Slave Address (4:0)

Pin	I/O	Buffer Type	Active Level	Function
EPR_EN	I	Input with 50 kΩ Pull down R	High	EEPROM Enable mode 0: EEPROM data load disable 1: EEPROM data load enable
S_CLKM	I	Input with 50 kΩ Pull down R		PCI/PCI-X Port Clock 100/133MHz mode 0: Maximum frequency is 133MHz 1: Maximum frequency is 100MHz
S_SLOTM (2 : 0)	I	Input with 50 kΩ Pull down R		PCI/PCI-X Port Hot Plug Slot configuration 000: No Hot Plug Slot 001: One Hot Plug Slot 010: Two Hot Plug Slot 011: Three Hot Plug Slot 100: Four Hot Plug Slot Others: Reserved
S_HPCM (1 : 0)	I	Input with 50 kΩ Pull down R		PCI/PCI-X Port SHPC Option support Bit0 0: MRL Sensor not support 1: MRL Sensor support Bit1 0: Attention button not support 1: Attention button support

4.8. Test Signals

Pin	I/O	Buffer Type	Active Level	Function
TCK	I	Input with 50 kΩ Pull down R		JTAG Test Clock
TDI	I	Input with 50 kΩ Pull up R		JTAG Test Data Input
TDO	O	Output		JTAG Test Output
TMS	I	Input with 50 kΩ Pull up R		JTAG Test Mode Select
TRSTB	I	Input with 50 kΩ Pull up R	Low	JTAG Test Reset
CTRI	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
SD_TESTEN	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
DBT_MODE	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
DC_TEST_MODE	I	Input with 50 kΩ Pull down R	High	NEC Test. Should be left open on circuit board.
TMC1	I	Input with Pull down R	High	NEC Test. Should be left open on circuit board.
TMC2	I	Input with Pull down R	High	NEC Test. Should be left open on circuit board.
NTEST1	I	Input		NEC Test. Should be pulled up on circuit board.
NTEST2	I	Input with 50 kΩ Pull down R		NEC Test. Should be left open on circuit board.
NTEST3	I	Input with 50 kΩ Pull up R		NEC Test. Should be left open on circuit board.

Pin	I/O	Buffer Type	Active Level	Function
NTEST4	I	Input with 50 kΩ Pull down R		NEC Test. Should be left open on circuit board.
NTEST5	I	Input		NEC Test. Should be pulled up on circuit board.
NTEST6	O	Output		NEC Test. Should be left open on circuit board.
NTEST7	I	Input		NEC Test. Should be left open or pulled up on circuit board.
NTEST8	I	Input		NEC Test. Should be left open or pulled up on circuit board.

5. Electrical characteristics

This section describes the electrical characteristics of μPD720404.

5.1. I/O Buffer List

Table 5-1 I/O Buffer List

Buffer Type	Signal Name
3.3V Input Buffer with 50KΩ Pull-Down	SMB_ADD(4:0), S_CLKM, S_SLOTM(2:0), S_HPCM(1:0), EPR_EN, TCK
3.3V Input Buffer with 50KΩ Pull-Up	TDI, TMS, TRSTB
3.3V Input Buffer	S_SERRB, S_M66EN, S_PCIXCAP_I, S_INTAB, S_INTBB, S_INTCB, S_INTDB, S_PMEB, VAUX_DET, S_SID
3.3V Schmitt Trigger Input Buffer	PWRGD, RSM_PWRGD
3.3V Schmitt Trigger Input Buffer with Fail Safe	SMB_CLK
3.3V 3mA Output Buffer	EPR_CLK
3.3V 6mA Output Buffer	S_SOD, S_SOL
3.3V 9mA Output Buffer	S_SILB, TDO
3.3V 24mA 3State Output Buffer	S_M66EN_O, S_PCIXCAP_P
3.3V bi-directional Buffer 6mA Output	S_SIC, S_SOC, S_SORB
3.3V bi-directional Buffer 3mA Nch Open Drain Buffer	EPR_DAT
3.3V bi-directional Buffer 12mA Nch Open Drain Buffer	SMB_DAT
3.3V 3mA Nch Open Drain Buffer	P_WAKEB, SMB_ALERTB
PCI/PCI-X 3.3V 24mA bi-directional Buffer	S_AD(63:0), S_CBE(7:0)B, S_PAR, S_PAR64, S_FRAMEB, S_IRDYB, S_TRDYB, S_STOPB, S_DEVSELB, S_PERRB, S_LOCKB, S_REQ64B, S_ACK64B
PCI/PCI-X 3.3V 24mA 3State Output Buffer	S_GNT (3:0)B
PCI/PCI-X 3.3V Input Buffer	S_REQ (3:0)B
PCI/PCI-X 3.3V 24mA Clock Output	S_PCLK (4:0), SB_PCLK
PCI/PCI-X 3.3V Feedback Clock Input	S_PCLK_I, SB_PCLK_I
PCI-X 3.3V Reference Clock Input	PX_REF133
PCI Express Reference Clock Input	P_REF100P, P_REF100N
PCI Express Interface	P_TX (0:3) P, P_TX (0:3) N, P_RX (0:3) P, P_RX (0:3) N

5.2. Terminology

Table 5-2 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Table 5-3 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage.

Table 5-4 Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

5.3. Absolute Maximum Ratings

Table 5-5 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	1.5V Power Supply	-0.5 to +2.0	V
		3.3V Power Supply	-0.5 to +4.6	
Input voltage, 1.5V buffer	V_I	$1.425\ V \le V_{DD} \le 1.575\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +2.0	V
Input voltage, 3.3V buffer	V_I	$3.135\ V \le V_{DD} \le 3.465\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +4.6	V
Output voltage, 1.5V buffer	V_O	$1.425\ V \le V_{DD} \le 1.575\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +2.0	V
Output voltage, 3.3V buffer	V_O	$3.135\ V \le V_{DD} \le 3.465\ V$ $V_I < V_{DD} + 0.5\ V$	-0.5 to +4.6	V
Storage temperature	T_{stg}		-65 to +150	°C

5.4. Recommended Operating Ranges

Table 5-6 Recommended Operating Ranges

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operating voltage	V_{DD}	1.5V Power Supply	1.425	1.5	1.575	V
		3.3V Power Supply	3.135	3.3	3.465	
High-level input voltage	V_{IH}	3.3V input buffer	2.0		V_{DD}	V
Low-level input voltage	V_{IL}	3.3V input buffer	-0.5		0.8	V
Positive-Trigger input voltage	V_P	3.3V schmitt input	1.2		2.4	V
Negative-Trigger input voltage	V_N	3.3V schmitt input	0.6		1.8	V

5.5. DC Characteristics

Table 5-7 DC Characteristics (Pin Block other than PCI/PCI-X)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Off-state output current	I_{OZ}	$V_O = V_{DD}$ or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note1			-250	mA
Low-level outpt voltage 3.3V Low-level outpt voltage	V_{OL}	I_{OL} = 0 mA		0.1	V
High-level outpt voltage 3.3V High-level outpt voltage	V_{OH}	I_{OH} = 0 mA	V_{DD}-0.1		V
Low-level outpt current 3.3V Low-level outpt current	I_{OL}				
3mA output buffer		V_{OL} = 0.4 V	3.0		mA
6mA output buffer		V_{OL} = 0.4 V	6.0		mA
9mA output buffer		V_{OL} = 0.4 V	9.0		mA
12mA output buffer		V_{OL} = 0.4 V	12.0		mA
24mA output buffer		V_{OL} = 0.4 V	24.0		mA
High-level outpt current 3.3V High-level outpt current	I_{OH}				
6mA output buffer		V_{OH} = 2.4 V	6.0		mA
9mA output buffer		V_{OH} = 2.4 V	9.0		mA
24mA output buffer		V_{OH} = 2.4 V	24.0		mA
Input leakage current 3.3V buffer	I_I	$V_I = V_{DD}$ or V_{SS}		±10	μA
3.3V buffer with 50k ohm PD		$V_I = V_{DD}$		175	μA
3.3V buffer with 50k ohm PU		$V_I = V_{SS}$		253	μA

Note 1: The output short circuit time is one second or less and is only for one pin on the LSI.

Table 5-8 DC Characteristics (PCI/PCI-X Interface Block)

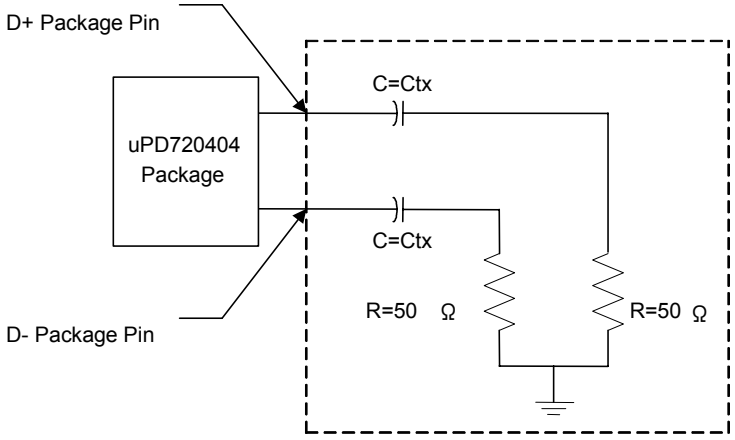
Parameter	Symbol	Condition	MIN.	MAX.	Unit
High-level input voltage	V_{IH}		2.0	3.6	V
Low-level input voltage	V_{IL}		0	0.9	V
Low-level output voltage	V_{OL}	I_{OL} = 0 mA		0.1	V
High-level output voltage	V_{OH}	I_{OH} = 0 mA	V_{DD} - 0.1		V
Low-level output current	I_{OL}	V_{OL} = 0.4 V	24.0		mA
High-level output current	I_{OH}	V_{OH} = 2.4 V	24.0		mA
Input low leakage current	I_{IL}	0 < Vin < 3.6 V		±10	μA

Table 5-9 DC Characteristics (PCI Express Interface Block)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Differential Transmitter (TX) Output					
Differential Peak to Peak Output Voltage	$V_{tx\text{-}diffpp}$		0.800	1.200	V

Parameter	Symbol	Condition	MIN.	MAX.	Unit
De-Emphasized Differential Output Voltage (Ratio)	$V_{tx\text{-}de\text{-}ratio}$		-3.0	-4.0	dB
Absolute Delta of DC Common Mode Voltage	$V_{tx\text{-}cm\text{-}dc\text{-}active\text{-}idle\text{-}delta}$	During L0 and Electrical Idle	0	100	mV
Absolute Delta of DC Common Mode Voltage between D+ and D-	$V_{tx\text{-}cm\text{-}dc\text{-}line\text{-}delta}$		0	25	mV
Electrical Idle Differential Peak Output Voltage	$V_{tx\text{-}idle\text{-}diffp}$		0	20	mV
The amount of voltage change during Receiver Detection	$V_{tx\text{-}rcv\text{-}detect}$			600	mV
The TX DC Common Mode Voltage	$V_{tx\text{-}dc\text{-}cm}$		0	1.575	V
TX Short Circuit Current	$I_{tx\text{-}short}$			90	mA
DC Differential TX Impedance	$Z_{tx\text{-}diff\text{-}dc}$		80	120	Ω
Transmitter DC Impedance	$Z_{tx\text{-}dc}$		40		Ω
Differential Receiver (RX) Input					
Differential Input Peak to Peak Voltage	$V_{rx\text{-}diffpp}$		0.175	1.200	V
DC Differential Input Impedance	$Z_{rx\text{-}diff\text{-}dc}$		80	120	Ω
DC Input Impedance	$Z_{rx\text{-}dc}$		40	60	Ω
Powered Down DC Input Impedance	$Z_{rx\text{-}high\text{-}imp\text{-}dc}$		200K		Ω
Electrical Idle Detect Threshold	$V_{rx\text{-}idle\text{-}det\text{-}diffpp}$		65	175	mV

Figure 5-1 Transmitter Measurement Load



5.6. Pin Capacitance

Table 5-10 Pin Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	V_{DD} = 0 V, T_A = 25°C	3.82	6.14	pF
Output capacitance	C_O	f_c = 1 MHz	6.14	8.14	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	6.14	8.14	pF

5.7. Power Consumption and Thermal Spec

Table 5-11 Power Consumption and Thermal Spec

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
VDD3.3 supply current	I_{DD} (3.3V)	PCIe x4 / PCI-X 1 port		0.2	0.3	A
VDD1.5 supply current	I_{DD} (1.5V)			1.3	1.5	A
Junction Temperature	T_j		0		115	°C
Thermal Resistance of case	θ_{jc}			3.90		°C/W
Thermal Resistance total	θ_{ja}	wv = 0 m/s *		23.27		°C/W
		wv = 1.0 m/s *		17.78		
		wv = 2.0 m/s *		16.29		
		wv = 3.0 m/s *		15.30		

(Note1) wv : wind velocity

(Note2) Recommended heat-sinks for uPD720404 are below.

ALPHA UB19-10B (http://www.micforg.co.jp/en/c_ub19e.html)

ALPHA UB25-10B (http://www.micforg.co.jp/en/c_ub25e.html)

(Note3) The formulas of the Tj calculation are below.

(1) Without heat-sink

$Tj = Power \times \theta_{ja} + Ta$

(2) With heat-sink

$Tj = Power \times (\theta_{jc} + \theta_{ch} + \theta_{ha}) + Ta$

Where

θ_{ch} is thermal resistance of adhesive. (like 0.5 °C /W)

θ_{ha} is thermal resistance of heat-sink.

5.8. System Clock Ratings

The characteristics for the PCI/PCI-X Reference Clock are described in Table 5-12. Regarding the characteristics for the PCI Express Reference Clock, μPD720404 is based on the PCI EXPRESS CARD ELECTROMECHANICAL SPECIFICATION. Please refer to the Section 2.1. of that specification.

Table 5-12 PCI/PCI-X Reference Clock

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock frequency	f_{CLK}		-500 ppm	133	+500 ppm	MHz
Clock Duty cycle	t_{DUTY}		45		55	%
Input rise time	T_r				2	ns
Input fall time	T_f				2	ns

5.9. AC Characteristics

Table 5-13 AC Characteristics (PCI/PCI-X Interface Block) 1/2

Parameter	Symbol	Conditions	MIN	MAX	Unit
PCI clock cycle time	t_{cyc}	PCI-X 133	7.5		ns
		PCI-X 66	15		
		Conventional PCI 66	15		
		Conventional PCI 33	30		
PCI clock pulse, high-level width	t_{high}	PCI-X 133	3		ns
		PCI-X 66	6		
		Conventional PCI 66	6		
		Conventional PCI 33	11		
PCI clock pulse, low-level width	t_{low}	PCI-X 133	3		ns
		PCI-X 66	6		
		Conventional PCI 66	6		
		Conventional PCI 33	11		
PCI clock, rise slew rate	S_{cr}	0.2 V_{DD} to 0.6 V_{DD}			V/ns
		PCI-X 133	1.5	4	
		PCI-X 66	1.5	4	
		Conventional PCI 66	1.5	4	
		Conventional PCI 33	1	4	
PCI clock, fall slew rate	S_{cf}	0.2 V_{DD} to 0.6 V_{DD}			V/ns
		PCI-X 133	1.5	4	
		PCI-X 66	1.5	4	
		Conventional PCI 66	1.5	4	
		Conventional PCI 33	1	4	
Delay from RSTB Low to CLK Frequency Change	T_{rlcx}		0		V/ns

Table 5-14 AC Characteristics (PCI/PCI-X Interface Block) 2/2

Parameter	Symbol	Conditions	MIN	MAX	Unit
PCI reset active time (vs. power supply stability)	t_{rst}		1		ms
PCI reset active time (vs. CLK Start)	$t_{rst-clk}$		100		μs
Output float delay time (vs. RSTB↓)	$t_{rst-off}$			40	ns
PCI reset rise slew rate	S_{rr}		50		mV/ns
PCI bus signal output time (vs. PCLK↑)	t_{val}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0.7	3.8	ns
PCI point-to-point signal output time (vs. PCLK↑)	t_{val} (ptp)	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0.7	3.8	ns
Output delay time (vs. PCLK↑)	t_{on}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	2		ns
Output float delay time (vs. PCLK↑)	t_{off}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33		7	ns
Input setup time (vs. PCLK↑)	t_{su}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	1.2		ns
Point-to-point input setup time (vs. PCLK↑)	t_{su} (ptp)	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	1.2		ns
Input hold time	t_h	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0		ns
REQ64B to RSTB Setup Time	t_{rrsu}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	10		Clock
RSTB to REQ64B Hold Time	t_{rrh}	PCI-X 133, PCI-X 66, Conventional PCI 66, Conventional PCI 33	0	50	ns
PCI-X Initialization Pattern to RSTB Setup Time	t_{prsu}		10		Clocks
RSTB to PCI Initialization Pattern Hold Time	t_{prh}		0	50	ns

Table 5-15 AC Characteristics (PCI Express Interface Block)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Differential Transmitter (TX) Output					
Unit Interval	UI		399.88	400.12	ps
Minimum TX Eye Width	T_{rx-eye}		0.70		UI
Maximum time between the jitter median and maximum deviation from the median	$T_{tx-eye-median-to-max-jitter}$			0.15	UI
D+/D- TX Output Rise/Fall Time	$T_{rx-rise}$, $T_{rx-fall}$		0.125		UI
AC Peak Common Mode Output Voltage	$V_{tx-cm-acp}$			20	mV
Minimum time spent in Electrical Idle	$T_{tx-idle-min}$		50		UI
Maximum time to transition to a valid Electrical Idle after sending an Electrical Idle Ordered set	$T_{tx-idle-set-to-idle}$			20	UI
Lane-to-Lane Output Skew	$L_{tx-skew}$			500+2UI	ps
Differential Receiver (RX) Input					
Unit Interval	UI		399.88	400.12	ps
Minimum Receiver Eye Width	T_{rx-eye}		0.4		UI
Maximum time between the jitter median and maximum deviation from the median	$T_{rx-eye-median-to-max-jitter}$			0.3	UI
AC Peak Common Mode Input Voltage	$V_{rx-cm-acp}$			150	mV
Total Skew	$L_{rx-skew}$			20	ns

Figure 5-2 Minimum Transmitter Timing and Voltage

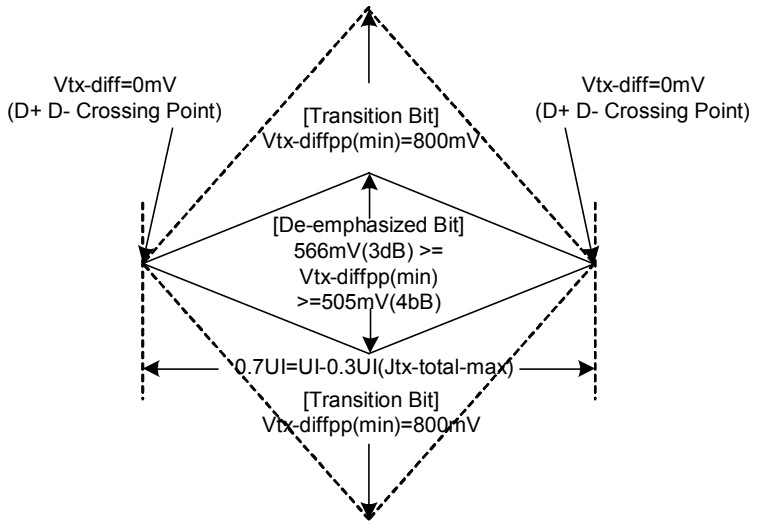


Figure 5-3 Transmitter Measurement Load

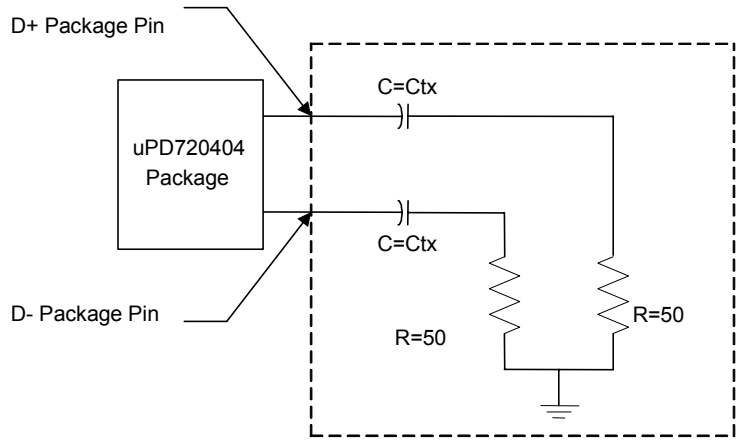


Figure 5-4 Minimum Receiver Timing and Voltage

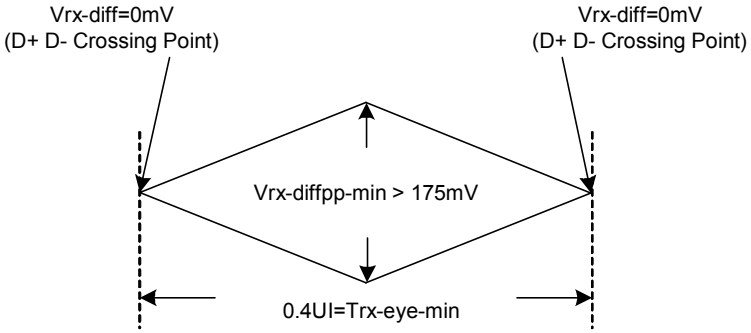


Table 5-16 AC Characteristics (SMBus Interface Block)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SMBus Operation Frequency	F_{smb}		10		400	KHz
Bus Free Time between STOP and START condition	T_{buf}		4.7			us
Hold Time after (Repeated) START condition.	$T_{hd:sta}$		4.0			us
Repeated START Condition setup time	$T_{su:sta}$		4.7			us
STOP condition setup time	$T_{su:sto}$		4.0			us
Data hold time	$T_{hd:dat}$		300			ns
Data setup time	$T_{su:dat}$		250			ns
Clock Low period	T_{low}		4.7			us
Clock High period	T_{high}		4.0		50	us
Clock/Data Fall time	T_f				300	ns
Clock/Data Rise time	T_r				1000	ns

Table 5-17 AC Characteristics (EEPROM Interface Block)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency,EPR_CLK	F_{scl}				100	KHz
Clock Pulse Width Low	T_{low}		4.7			us
Clock Pulse Width High	T_{high}		4.7			us
Clock Low to Data Out Valid	T_{aa}		2.5		2.8	us
START Hold time	$T_{hd:sta}$		4.0			us
START Setup time	$T_{su:sta}$		4.7			us
Data In Hold time	$T_{hd:dat}$		0			us
Data In Setup time	$T_{su:dat}$		0			us
Inputs Rise time	T_r				1000	ns
Inputs Fall time	T_f				300	ns
Stop Setup time	$T_{su:sto}$		4.7			ns
Data Out Hold time	T_{dh}		2.5			ns

Table 5-18 AC Characteristics (Hot-Plug External Shift-IN Register)

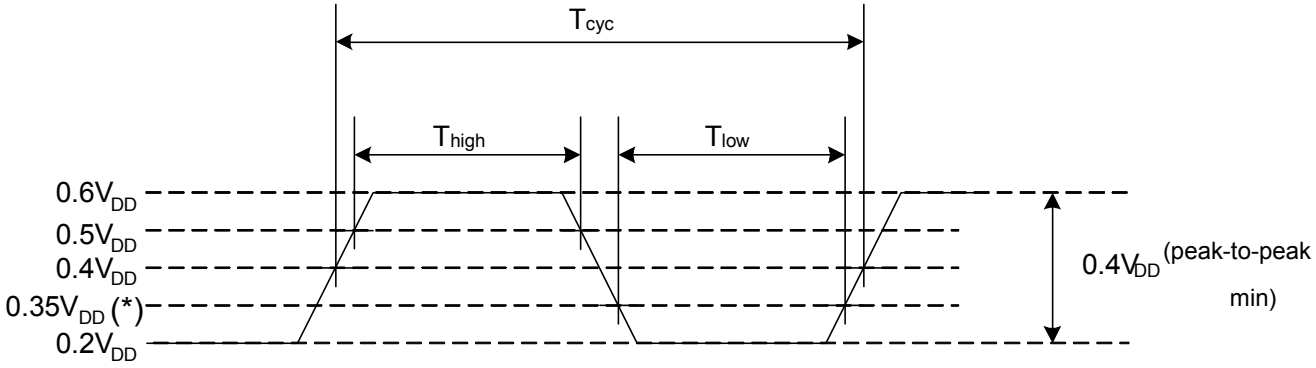
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency, S_SIC	F_{sic}				12.5	MHz
Clock Pulse Width Low	T_{low}		40			ns
Clock Pulse Width High	T_{high}		40			ns
Load Pulse Width Low	$T_{low:load}$		40			ns
Load fall to Clock rise	T_{load}		80			ns
Rise Time	T_r				10	ns
Fall Time	T_f				10	ns
Input Data Setup time	T_{su}		10			ns
Input Data Hold time	T_{hd}		0			ns

Table 5-19 AC Characteristics (Hot-Plug External Shift-OUT Register)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Frequency, S_SOC	F_{soc}				12.5	MHz
Clock Pulse Width Low	T_{low}		40			ns
Clock Pulse Width High	T_{high}		40			ns
Reset Pulse Width Low	$T_{low:rst}$		40			ns
Load Pulse Width High	$T_{high:load}$		60			ns
Clock fall to Load reset	T_{load}		80			ns
Rise Time	T_r				10	ns
Fall Time	T_f				10	ns
Clock High to Data Output	T_{do}		40		50	ns

5.10. Timing Diagram

Figure 5-5 PCI/PCI-X Clock



(*) PCI-X. $0.3V_{DD}$ for Conventional PCI.

Figure 5-6 PCI/PCI-X Output Timing Measurement Timing

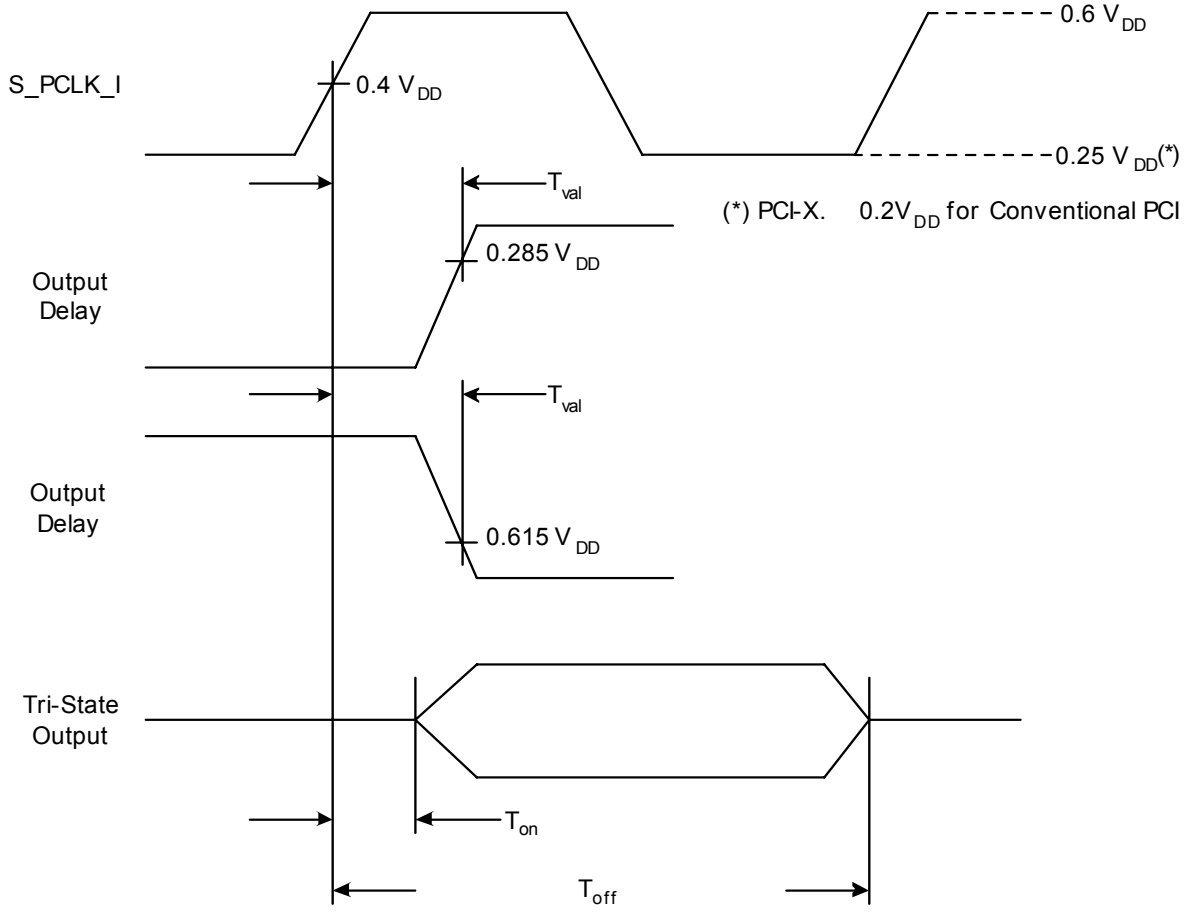


Figure 5-7 PCI/PCI-X Input Timing Measurement condition

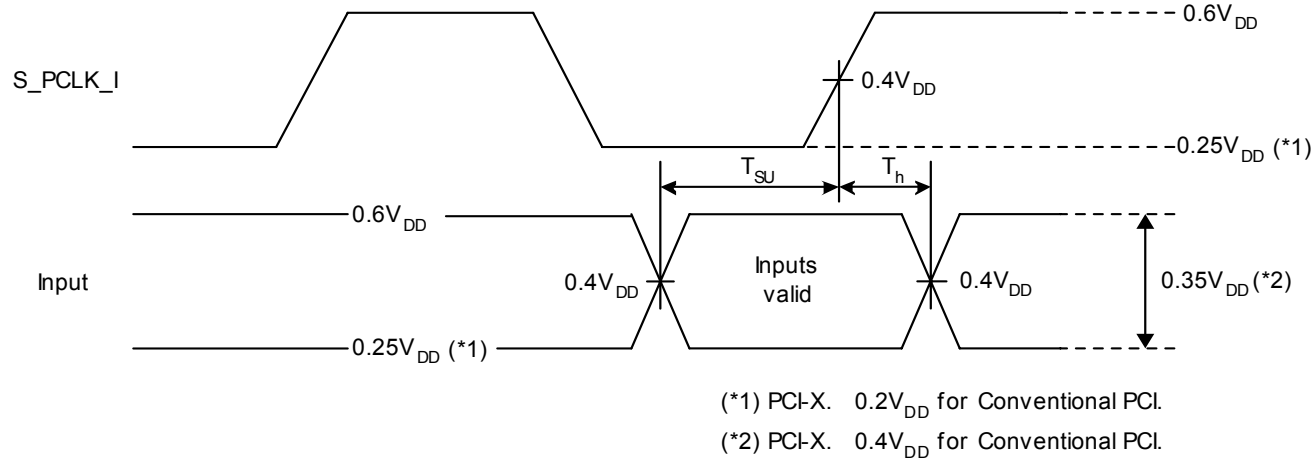


Figure 5-8 SMBus Timing

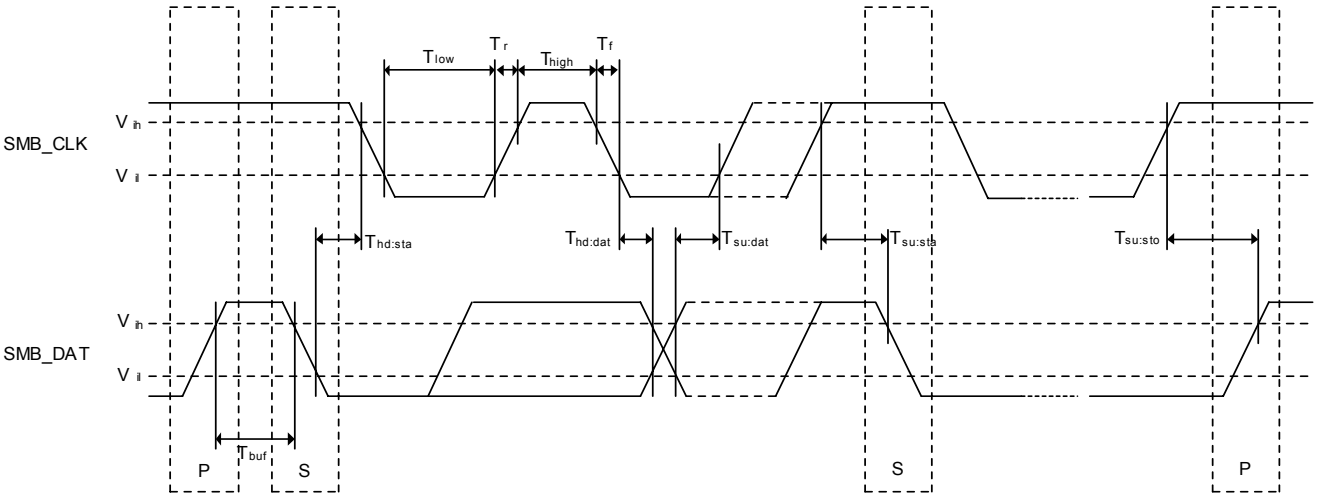


Figure 5-9 EEPROM Timing

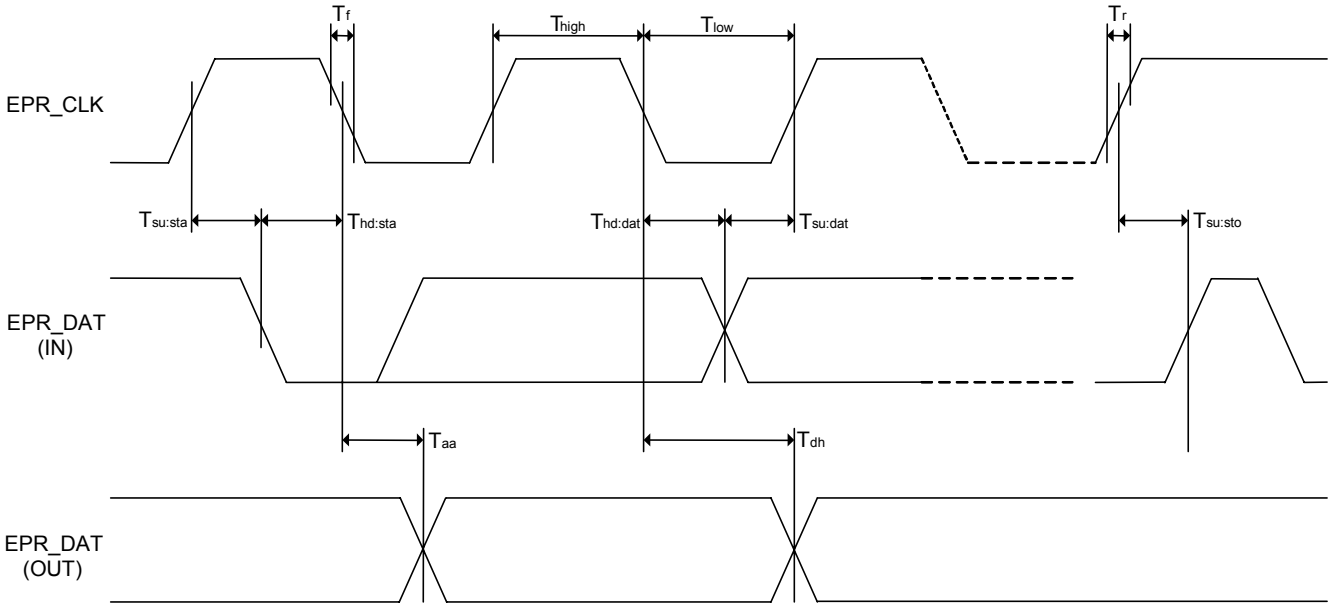


Figure 5-10 Hot-Plug SHIFT-IN Timing

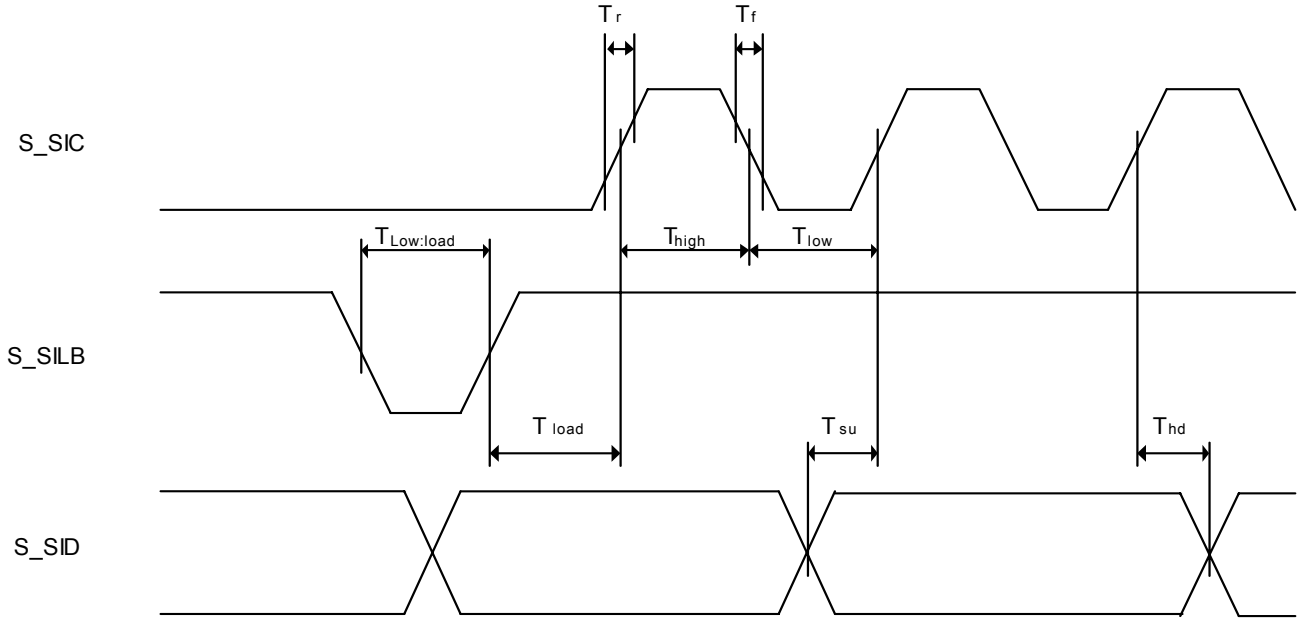


Figure 5-11 Hot-Plug SHIFT-OUT Timing