Designing the Video Section of 1600 x 1280-Pixel CRTs

National Semiconductor
Application Note 867
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DESIGN OBJECTIVES

- Design the complete video section for a 1600 x 1280 display resolution CRT monitor
- Video:
  B.W = 160 MHz
  Pixel time = 6.25 ns
  f_H = 74 kHz
  f_V = 60 Hz
  Rise/Fall time (at Cathode) < 4 ns
- Tube characteristics: 27 inch CRT with 0.37 mm dot pitch

After reading this paper, the interested reader will be able to design the complete video section of 1600 x 1280 pixel CRTs. For our design, the specified horizontal and vertical scan rates are 74 kHz and 60 Hz respectively. This gives rise to a video bandwidth of 160 MHz and 6.25 ns pixel time. Theoretically the desired rise and fall times at the cathode should be a third of the pixel time and is approximately 2 ns for a 1600 x 1280-pixel CRT.

Although achieving 2 ns rise and fall times at the cathode is not impossible, doing so may be cost prohibitive. Since full on-off pixels are very difficult to resolve with the naked eye when viewing high resolution displays, rise and fall times of one half the pixel time or slightly greater is quite acceptable. We set a goal of 4 ns or less rise and fall time at the cathode thus allowing the use of low cost commercially available ICs.

Figure 1 shows a simplified block diagram of a color CRT (Cathode Ray Tube) monitor. The entire circuitry within the monitor can be grouped into three main categories: video signal processing and amplification, horizontal/vertical deflection and synchronizing, and power supply. The subject of our discussion here is going to be on video signal processing and amplification.

The video signal is usually 1 V_{PP} and requires amplification before the signal can be applied to the CRT's cathode. The amplification of the video signal is done in two stages. A low voltage preamplifier amplifies the 1 V_{PP} signal to a 4 V_{PP}–6 V_{PP} signal. In addition to amplification, the preamplifier also provides contrast and brightness control. Many preamplifiers also provide DC restoration or black level clamping.

The CRT driver is the second stage of the video section that boosts the 4 V_{PP}–6 V_{PP} signal from the preamplifier to a 40 V_{PP}–60 V_{PP} signal that the cathode requires to energize each phosphor dot on the screen. In a color monitor, there is a trio of red, blue and green phosphor dots. Together, each triad constitutes the smallest possible picture element of the CRT. The light emitted by the phosphor dot is proportional to the number of electrons striking the phosphor. Thus by modulating the voltage of each of the three cathodes in a color monitor, the corresponding phosphor dots in a triad are energized at varying intensities, thereby producing the various shades of color. To change a pixel from black to peak white, the three CRT video amplifiers may be required to swing as much as 40 V_{PP} or more.

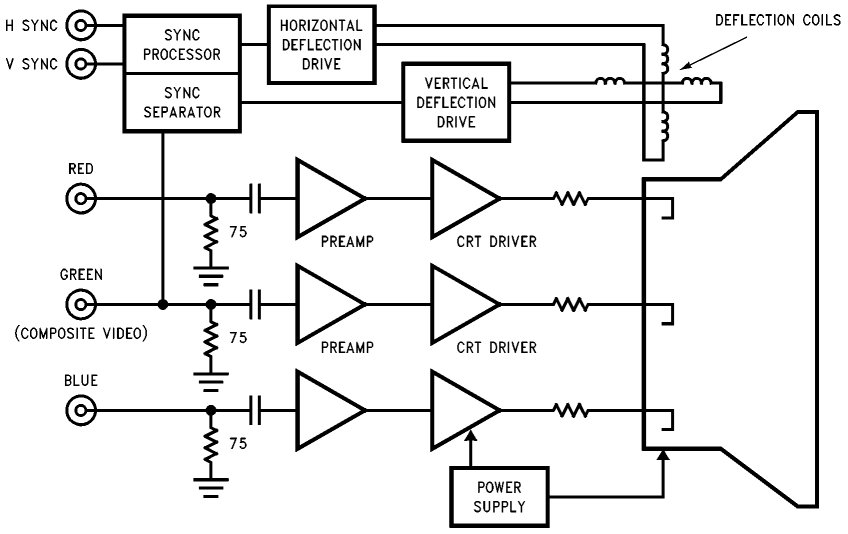

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FIGURE 1. Simplified Block Diagram of an RGB CRT Monitor

Functions Needed on a CRT Video Board

- Video signal amplification
- DC restoration
- H/V sync and/or sync on green processing
- Contrast and brightness control
- Δ gain and cutoff adjustments
- Video blanking

The CRT video board accomplishes the task of video signal processing and amplification. Video signal amplification is required to amplify the 1 V_{PP} video signal from the computer to a 40 V_{PP}–60 V_{PP} signal at the cathode. The input video signal is normally AC coupled since it is difficult to match DC references of an unknown source. Therefore DC restoration circuitry is needed to restore the DC component of each line on the screen. This is accomplished by clamping the video signal to the black level. Horizontal and vertical (H/V) sync processing circuitry is employed to generate the clamp pulse required for DC restoration.

The CRT board must also have contrast (AC gain) and brightness (DC offset) controls. These controls are usually accessible to the user so that he may adjust them. For color monitors, the board must also make provisions for Δ gain adjustment for white balance. Also, color monitors require independent cutoff adjustments to match the normally mismatched guns in a color tube.

Additional features that would be desirable are: ''Sync on Green'' and video blanking. Some computers transmit a composite video signal on the green channel. The composite video signal carries both video and sync information. A ''Sync on Green'' feature in the monitor directly extracts the necessary sync signals from the composite video signal without the need for an external H/V sync signal. During horizontal and vertical retrace, the screen is blanked to make the retrace lines invisible. Normally blanking is done by applying a large negative pulse at grid G1 during the blanking interval.

Before starting our design lets partition the system into functional blocks and create a roadmap. A system block diagram of the video section is shown in *Figure 2*. Since the required cutoff voltage at the cathodes is greater than the supply voltage of the CRT driver, the video signal is AC coupled. To restore the video signal's DC component at the cathode, a black level clamp circuit operating from +120V supply clamps the signal's black level to the desired cutoff voltage. And, to ensure that the CRT guns are completely cutoff during retrace, grid (G1) blanking is employed. The circuitry for grid blanking also provides the appropriate G1 bias and brightness control. Finally to DC restore the video signal at the preamplifier section, a back porch clamp signal is required. The back porch clamp pulse generator generates the back porch clamp signal from the externally supplied H-sync signal.

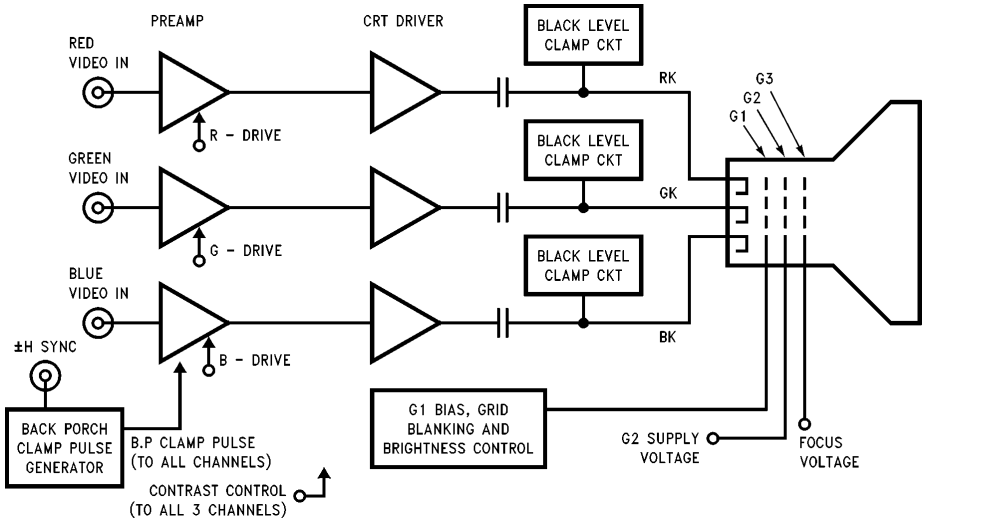

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FIGURE 2. System Block Diagram of Video Section

DESIGNING THE PREAMPLIFIER SECTION

PREAMPLIFIER SELECTION

LM1202 230 MHz VIDEO AMPLIFIER SYSTEM

- Video preamplifier for 1600 x 1200 and 2048 x 2048 display resolution
- Single channel CRT video preamplifier
- Includes DC restoration of video signal
- Includes drive adjustment for use in RGB systems
- Can parallel three LM1202s for optimum contrast tracking in RGB systems
- 0V–4V DC control of contrast, drive and brightness.

The LM1202 is a single channel high frequency video amplifier system designed for use in high resolution monochrome or RGB monitors. The device includes contrast, brightness, drive controls and DC restoration circuitry for black level clamping. All DC controls operate from 0V to 4V range for easy interface to bus controlled alignment systems. Three LM1202s can be paralled so that one IC provides master contrast control thus achieving better than 0.1 dB contrast tracking in RGB systems.

LM1202—KEY SPECIFICATIONS

- 230 MHz large signal bandwidth (at $V_O = 4\ V_{PP}$)
- 1.5 ns rise/fall times
- 26 dB gain with 0 db to 60 dB attenuation range
- ± 3 dB drive adjustment range

The LM1202 has 230 MHz bandwidth at 4 V_{PP} output voltage and is well suited for 1600 x 1280 and 2048 x 2048 display resolution CRT monitors. The device has typical rise and fall times of 1.5 ns and has a maximum tested limit of 2 ns. The LM1202 offers 26dB gain with 0 dB to 60 dB attenuation range. For achieving white balance in an RGB system, LM1202's drive adjustment allows individual gain adjustment of each channel.

A block diagram of the LM1202 video amplifier is shown in *Figure 3*. Contrast control is a DC-operated attenuator which varies the AC gain of the amplifier. Signal attenuation (contrast) is achieved by varying the base drive to a differential pair and thereby unbalancing the current through the differential pair. Pin 20 provides a 5.3V bias voltage for the positive input of the attenuator (pin 1). Pin 3 provides a control voltage for the negative input (pin 2) of the attenuator. The voltage at pin 3 varies as the voltage at the contrast control input (pin 8) varies thus providing signal attenuation. The gain is maximum (0 dB attenuation) if the voltage at pin 8 is 4V and is minimum (maximum attenuation) if the voltage at pin 8 is 0V. The 0V to 4V DC-operated drive control at pin 9 provides a 6 dB gain adjustment range. This feature is necessary for RGB applications where independant adjustment of each channel is required.

The brightness or black level clamping requires a ''sample and hold'' circuit which holds the DC bias of the video amplifier constant during the black level reference portion of the video waveform. Black level clamping, often referred to as DC restoration is accomplished by applying a back porch clamp signal to the clamp gate input pin (pin 14). The clamp comparator is enabled when the clamp signal goes low during the black level reference period. When the clamp comparator is enabled, the clamp capacitor connected to pin 12 is either charged or discharged until the voltage at the minus input of the comparator matches the voltage set at the plus input of the comparator. During the video portion of the signal, the clamp comparator is disabled and the clamp capacitor holds the proper DC bias. In a DC coupled cathode drive application, picture brightness function can be achieved by varying the voltage at the comparator's plus input. Note that the back porch clamp pulse width (t_W) must be greater than 100 ns for proper operation.

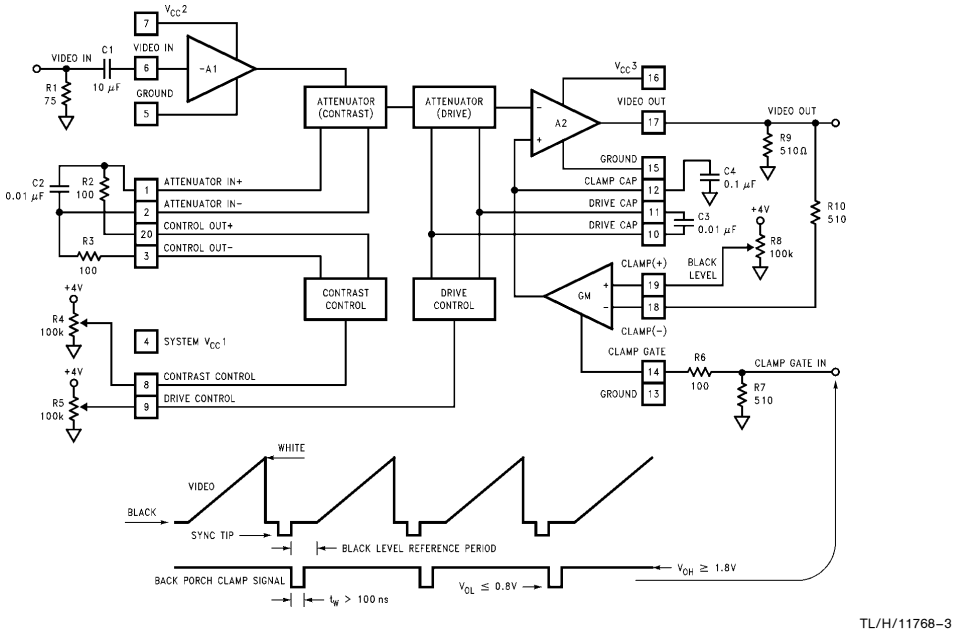

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FIGURE 3. LM1202 Block Diagram

Figure 4 shows a typical application for a single video channel. The video signal is AC coupled to pin 6. The LM1202 internally biases the video signal to 2.6 V_{DC}. Contrast control is achieved by applying a 0V to 4V DC voltage at pin 8. The amplifiers gain is minimum (i.e maximum signal attenuation) if pin 8 is at 0V and is maximum if pin 8 is at 4V. With pin 9 (drive control) at 0V, the amplifier has a maximum gain of 10.

For DC restoration, a clamp signal must be applied to the clamp gate input (pin 14). The clamp signal should be logic low (less than 0.8V) only during the back porch (black level reference period) interval. The clamp gate input is TTL compatible. Brightness control is provided by applying a 0V to 4V DC voltage at pin 19. For example, if pin 19 is biased at 1V then the video signal's black level will be clamped at 1V. A 510Ω load resistor is connected from the video output pin (pin 17) to ground. This resistor biases the emitter follower output stage of the amplifier. For power dissipation considerations, the load resistor should not be much less than 510Ω.

The complete RGB video preamplifier section is shown on in *Figure 5*. Note that pins 1 and 2 of IC1 are connected to pins 1 and 2 of IC2 and IC3 respectively. This allows IC1 to provide a master contrast control and optimum contrast tracking. Adjusting the contrast voltage at pin 8 of IC1 will vary the gain of all three video channels simultaneously. Drive control input (pin 9) of each LM1202 allows individual gain adjustment for achieving white balance.

The black level of each video channel can be individually adjusted to the desired voltage by adjusting the voltage at pin 19. In a DC coupled cathode drive application, adjusting the voltage at pin 19 of each IC will provide cutoff adjustment. In an AC coupled cathode drive application, the video signal is AC coupled and DC restored at the cathode. In such an application, the video signal's black level may be clamped to the desired level by simply biasing pin 19 using a voltage divider.

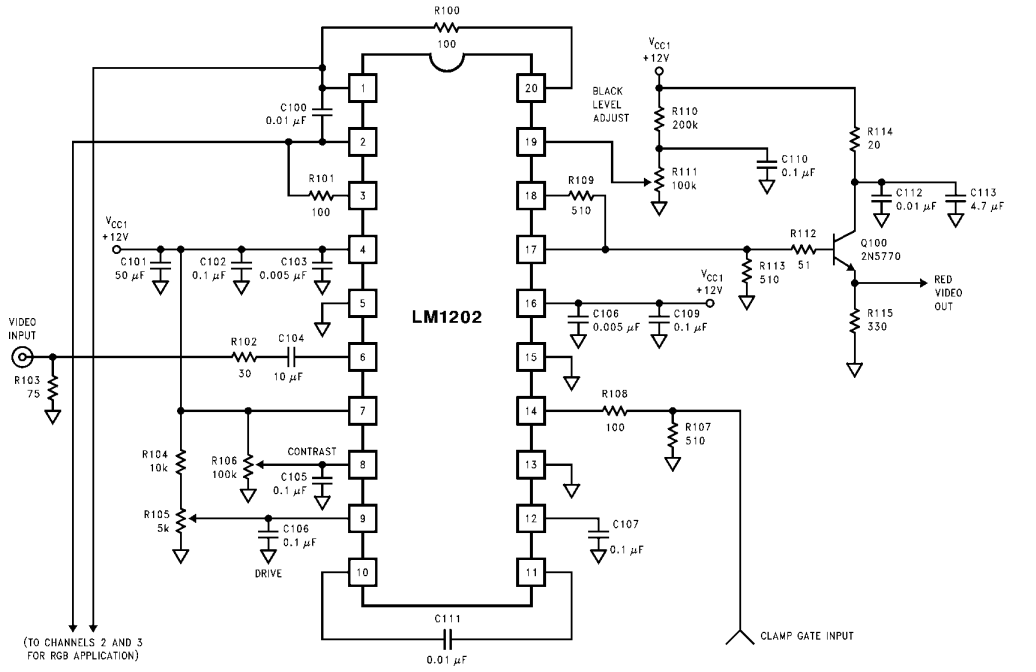

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FIGURE 4. LM1202 Connection Diagram For Single Channel Application

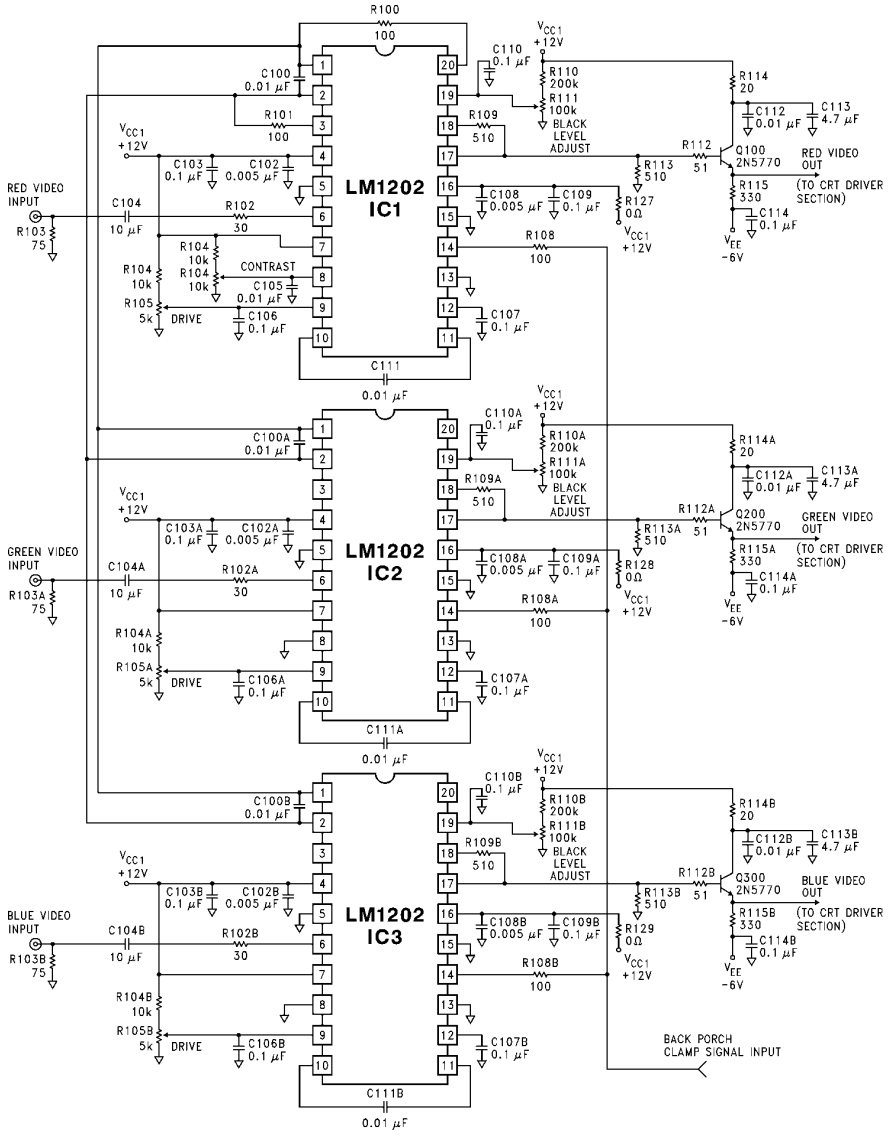

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FIGURE 5. COMPLETE PREAMPLIFIER SECTION

DESIGNING THE CRT DRIVER SECTION

CRT DRIVER SELECTION

LH2424 175 MHz CRT Driver

- CRT driver for 1600 x 1200 and 2048 x 1536 display resolution
- Single channel CRT driver
- Closed loop transimpedance amplifier
- Internal feedback resistor

Having completed the design of the preamplifier section, we can start designing the CRT driver section. The LH2424 was selected because of its 175 MHz bandwidth, low cost and ease of use. Moreover, the LH2424 is pin and function compatible with similar drivers from Motorola and Philips. The LH2424 is a transimpedance amplifier with an internal feedback resistor. One external resistor connected in series with the input accomplishes the task of voltage to voltage gain.

LH2424—KEY SPECIFICATIONS

- 175 MHz large signal bandwidth (at $V_O = 40\ V_{PP}$)
- 2 ns rise and fall times
- Voltage gain of -13
- Output can swing 50 V_{PP} (at $V+ = 60V$)

LH2424's 2 ns rise and fall times and 175 MHz bandwidth at 40 V_{PP} output voltage makes the device very suitable for our design. When coupled with the LM1202 (1.5 ns rise/fall times), the theoretical rise/fall time for the system is 2.5 ns and is well within our design objectives.

A simplified schematic of the LH2424 is shown in *Figure 6*. Resistors R1 and R2 set up the bias voltage at the base of Q1, giving rise to 1.2V drop across R3 when $V_+ = +60V$. With V_+ fixed at $+60V$, Q1 acts as a constant current source thus developing 1.2V across R5. The quiescent bias voltage at the base of Q2 is therefore approximately 1.7V, the measured value is closer to 1.6V. The 1.6V DC bias at the base of Q2 appears across R_B and causes 9.7 mA current to flow through R_F. If pin 1 is open circuit, 9.7 mA flowing through R_F causes the quiescent output voltage to be approximately 30V, thus biasing the output at one half the supply voltage. It can be easily shown that for any supply voltage the circuit output is biased at one half the supply voltage when pin 1 is open circuit.

Connecting a gain setting resistor, R_G in series with the input signal, V_{IN} and pin 1 accomplishes the task of voltage to voltage gain. If $V_{IN} = 1.6V$, the voltage across R_G is 0V and $V_{OUT} = 30V$. As the input voltage changes relative to the 1.6V DC bias, current is injected into the summing node (inverting input, pin 1) and flows entirely through the feedback resistor R_F because the current through R_B remains unchanged due to the fixed 1.6V DC bias voltage impressed across R_B. A current change of ± 6.67 mA at the summing node causes the amplifier's output to swing $\pm 20V$ from its quiescent output DC voltage of 30V. Thus when operating from $V+ = 60V$, the input signal should be referenced to 1.6V DC. The amplifier's AC gain is given by, $A_V = -R_F/R_G$.

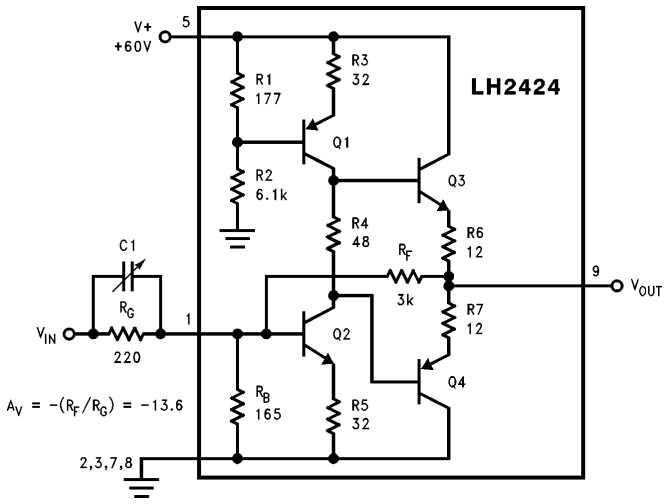

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FIGURE 6. Simplified Schematic of LH2424 CRT Driver

Figure 7 shows the schematic of the complete CRT driver section. Total series input resistance of 150Ω and LH2424's internal 3k feedback resistor configure the amplifier for a gain of −20. A peaking capacitor, for example C1 for the red video channel, is connected across the 100Ω input resistor. At high frequencies, C1 bypasses the 100Ω resistor, R2, and significantly increases the amplifier's closed loop gain thus causing high frequency peaking. Initially for prototype design, a 10 pF–120 pF variable capacitor can be selected for C1, C3 and C5. By varying the value of the peaking capacitor, the pulse response at the output of the LH2424 can be optimized for fast rise/fall time and low overshoot. Once the design is optimized, the value of the variable capacitor is measured and the capacitor is replaced with a fixed capacitor of measured value.

The LH2424's pulse response exhibits a low frequency tilt. This low frequency tilt causes picture smearing on the screen and can be observed by displaying a black box on a white background. The low frequency tilt is caused by thermal drift internal to the LH2424 and can be eliminated by feeding back a portion of the output signal back to the amplifier's input. As shown for the red video channel, R25, C7 and R26 accomplish the task of tilt compensation. One way to compensate all three channels is to display red, green and blue horizontal bars on a white background and adjust R26, R28 and R30 until picture smearing is eliminated.

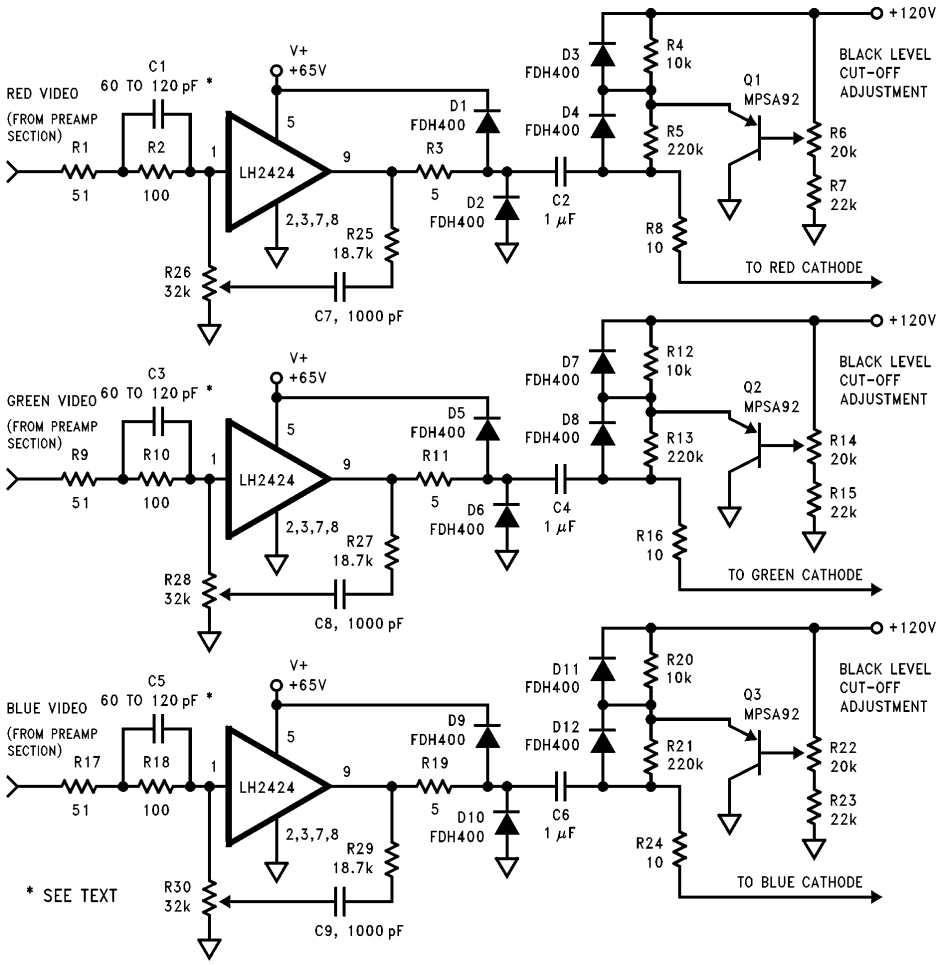

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FIGURE 7. COMPLETE CRT DRIVER SECTION

As the bandwidth of the driver amplifier is increased, it becomes more difficult to maintain high breakdown voltages. Although the video preamplifiers can provide full black level DC restoration, at high resolutions it may become more appropriate to consider AC coupling to the cathode. With AC coupling the CRT driver amplifier does not have to have a supply voltage rating high enough to accommodate the DC offsets required for individual gun matching. *Figure 8* shows the LH2424 operated from a 65V supply, whereas the AC coupled cathode is operated from a 120V supply, leaving a much larger voltage range for DC offset adjustment. A 1 μF capacitor couples the signal to the cathode. To restore the DC at the cathode, the MPSA92 high voltage transistor and the diode D4 clamp the peak signal voltage (i.e., black level or sync tip level) on the cathode side of the capacitor to 1.4V above the voltage set by the cut-off adjustment potentiometer. For arc-over protection, the second diode D3 prevents the transistor emitter from being pulled more than 0.7V above the 120V supply.

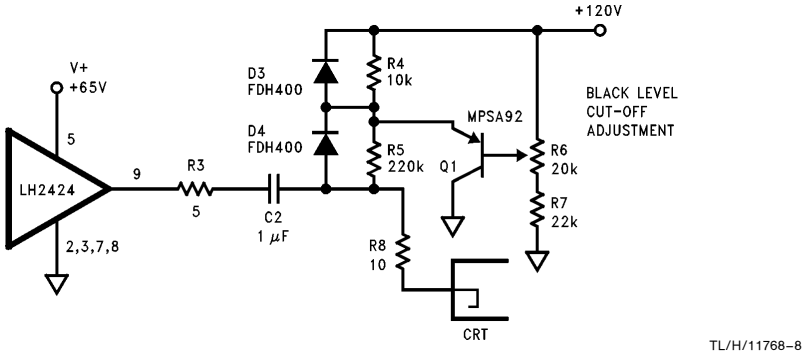

FIGURE 8. AC Cathode Drive with Black Level Clamping

The high voltage differences between the anode of the CRT and the gun grids can often lead to arc-overs or highly destructive voltages being present on circuit elements connected to the CRT. To limit the potential arc-over voltage, spark gaps are connected from the cathodes and the grids to ground (see *Figure 9*). Even with the spark gaps, the arc-over voltage may be too high for the CRT driver. For added protection, clamp diodes are added to the driver outputs. These diodes should have a high peak current capability, low series impedance and a low shunt capacitance for them to be effective. Adding the 5Ω and 10Ω series resistors will help limit the arc-over current but this extra resistance will contribute to slower rise-times. The rise time can be improved by series peaking. A small inductor in series with the cathode can improve rise times at the expense of introducing more overshoot into the signal. The actual inductor value is selected empirically to get the best compromise between overshoot and rise time, 50 nH is a good starting value. To further protect the low voltage circuitry on the video board from high arc-over current, a small isolation resistor of value 10Ω to 100Ω is used to isolate the circuit ground from the CRT/arc ground.

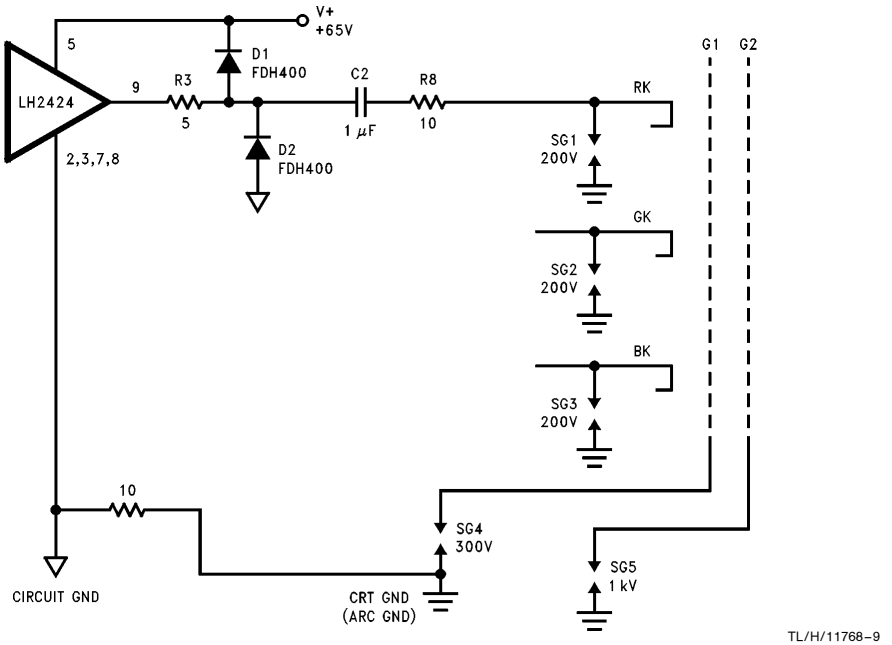

FIGURE 9. ARC Protection

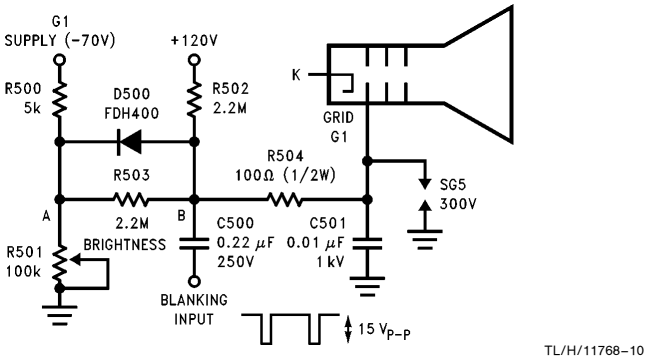

FIGURE 10. CRT Grid Blanking and Brightness Control

The circuit used to accomplish blanking is shown in *Figure 10*. A negative voltage is applied to grid G1 using the resistor divider comprised of R500 and R501. Brightness control is achieved by varying the bias at G1 using potentiometer R501. Blanking at the grid is accomplished by R502, R503, D500 and C500. Resistor R502 biases the clamp diode D500. A 15 V_{PP} blanking signal is AC coupled through C500. Since the voltage at node "B" can not go more than one diode drop above the voltage at node "A" the blanking signal at G1 is clamped at the G1 bias voltage. During the blanking portion of the video signal, the blanking signal goes low thus reverse biasing D500 and pulling G1 15V negative with respect to its normal bias voltage. This action cuts off the CRT's beam current during the blanking interval and accomplishes blanking.

A versatile back porch clamp generator circuit is shown in *Figure 11*. A quad Exclusive-OR gate (MM74HC86) is used to generate the back porch clamp signal from the composite H-sync input signal. The composite H-sync input signal may have either positive or negative polarity. The logic level at pin 11 (Flag out) indicates the polarity of the H-sync signal applied to the clamp generator. The Flag output is a logic low (less than 0.8V) if the H-sync input signal has a negative polarity and is a logic high (greater than 2.4V) if the H-sync input signal has a positive polarity.

Regardless of the H-sync input signal's polarity, a negative polarity H-sync signal is output at pin 8. Furthermore, a negative polarity back porch clamp pulse is output at pin 3. The width of the back porch clamp pulse is determined by the time constant due to R28 and C12. For fast horizontal scan rates, the back porch clamp pulse width can be made narrower by decreasing the value of R28 or C12 or both. Note that an MM74C86 Exclusive-OR gate may also be used, however, the pin out is different than that of the MM74HC86.

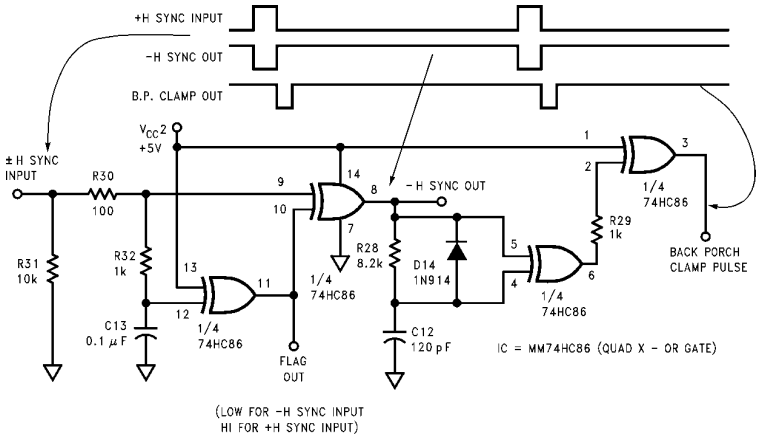

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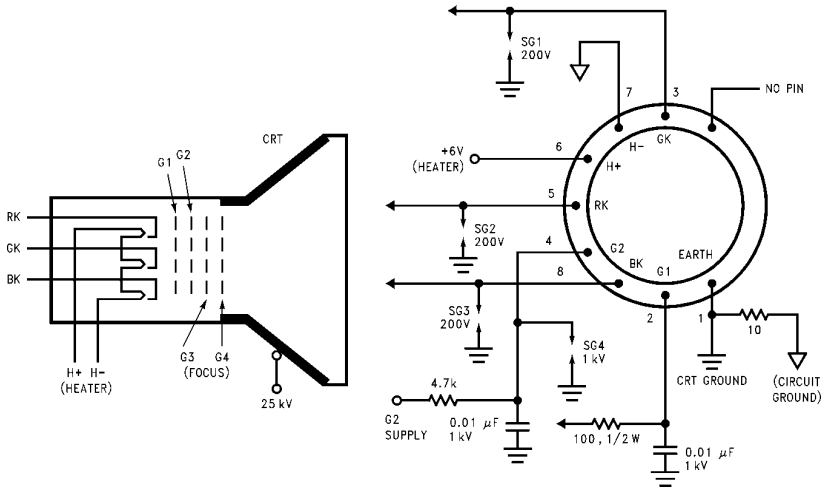
FIGURE 11. Back Porch Clamp Pulse Generator



CRT Socket: Hosiden HPS0380

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FIGURE 12. CRT Socket Connection

A typical connection diagram for the CRT socket is shown in *Figure 12*. Note that pinout for the socket may be different depending on the CRT tube used.

A photograph of the fully assembled 1600 × 1280-pixel color CRT monitor is shown in *Figure 13*. The viewable screen size is 27'' with 0.37 mm dot pitch. The horizontal and vertical scan rates are 74 kHz and 60 Hz respectively. The monitor weighs 110 lbs.

MEASURED DATA

Response at cathode:
t_R = 3.5 ns
t_F = 3.4 ns
Overshoot = 0.4V
Undershoot = 0V
Settling time (±5%) = 12 ns

Sub 3 ns rise and fall times can be achieved by including an inductor in series with the output of the CRT driver. The value of the inductor is empirically determined, 50 nH is a good starting value. The inductor will improve rise and fall times at the expense of increased overshoot.

ADDITIONAL READING:

1. Grob, Bernard, ''Basic Television and Video Systems,'' (5th edition), McGraw Hill, N.Y., 1984.
2. Rahim, Zahid, ''Understanding the operation of a CRT monitor,'' Application Note 656, National Semiconductor Corp., Nov, 1989.
3. ————, ''110 MHz CRT video amplifier fulfills demands of high resolution monitors,'' Application Note 598, National Semiconductor Corp., April, 1989.
4. ———— ''Guide to CRT video design,'' Application Note 861, National Semiconductor Corp.
5. LM1202 data sheet, National Semiconductor Corp.
6. LH2424 data sheet, National Semiconductor Corp.

ACKNOWLEDGEMENTS:

The author would like to acknowledge Ron Page (National Semiconductor Corp.) for designing the back porch clamp generator circuit shown in *Figure 11.*

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FIGURE 13. Photograph of Fully Assembled 1600 × 1280-Pixel CRT Monitor

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