Interfacing the DP8432V and the 80486

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INTRODUCTION

This application note shows how to interface the DP8432V-33 DRAM controller with Intel's 80486 microprocessor. The reader should be familiar with the 80486 and the DP8432V modes of operation. The nature of this application note is to give an idea of a possible configuration. After reading this application note, the reader must do an analysis for his/her particular application.

The design operates at 33 MHz and it supports ''Non-Burst Cache Filling'' during read cycles. This application note inserts 3 wait states during opening accesses, and 1 wait state during Non-Burst Cacheable Multiple-Cycle Sequence. The memory is interleaved every 4 double words (16 bytes) between two banks. The memory is organized in 2 Banks of 32 bits in width. Using 4M X 1 DRAMs, this arrangement gives a total memory of 32 Mb. The design uses DRAMs with output enable making transceivers in the data bus unnecessary. By having 4 Banks instead of 2 Banks, the total memory can be increased to 64 Mb. In this case, the timing calculations must be revised due to a heavier capacitive load on the output drivers.

Four timing waveforms are presented.

1. Non Delayed Back to Back Accesses to Different Banks. It shows two opening accesses, one to each bank (Memory Interleaving).
2. Delayed Back to Back Access to the Same Bank. Access-Precharge-Access.
3. Cache Filling Multiple Accesses. Fastest way of access, it transfers 16 bytes in a 5-3-3-3 fashion during the read cycle only.
4. Refresh Cycle Arbitration.

The glue logic is implemented using a 10 ns PAL and to reduce component count. This application note is applicable to the DP8431V/30V also. The logic for a second design running at 20 MHz is also presented.

DESCRIPTION

Resetting and Programming. Resetting the DP8432V is accomplished by asserting $\overline{\text{RESET}}$ for at least 16 positive edges of clock. The controller is programmed during the first memory write after a system reset. During reset $\overline{\text{ML}}$ is low. During the first memory access the 80486 starts a write cycle to a location equal to the programming selection. $\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{AREQ}}$ will assert at the beginning of the access. When $\overline{\text{AREQ}}$ goes low, the programming bits affecting the wait logic become valid, this allows $\overline{\text{DTACK}}$ to assert and the 80486 to finish the access. At the end of the access, when $\overline{\text{WR}}$ negates, $\overline{\text{ML}}$ goes high. At this time the rest of the programming bits take effect and the 60 ms initialization period begins.

Non Delayed Opening Accesses. An access begins when the 80486 places a valid address onto the address bus and asserts $\overline{\text{ADS}}$#. Due to the delay from Clock high to $\overline{\text{ADS}}$# asserted (t6 = 19 ns 80486 data sheet), it is required to latch $\overline{\text{ADS}}$# from the 80486 and assert it early enough during T2 to meet $\overline{\text{ADS}}$ asserted set up to CLK high ($400 in the DP8432V data sheet).

The DRAM controller will assert $\overline{\text{RAS}}$ from $\overline{\text{ADS}}$ asserted to latch the row address into the DRAM. The DP8432V guarantees the programmed Row Address Hold Time, t_{RAH}, before switching the internal multiplexor to place the column address onto the Q outputs. The DRAM controller guarantees the programmed Column Address Set Up time, t_{ASC}, before asserting $\overline{\text{CAS}}$ to latch the column address into the DRAM. $\overline{\text{DTACK}}$ is programmed to assert from the rising edge of T4 for a non delayed access (1T for R2 = 1, R3 = 0 plus 1T due to $\overline{\text{WAITIN}}$). RDY# will assert from the rising edge of T5. It takes 5 clock periods (~151 ns) to complete a non delayed access.

If the 80486 is to perform a single access, $\overline{\text{BLAST}}$ is asserted during T2. $\overline{\text{BLAST}}$ and $\overline{\text{RDY}}$ asserted negate $\overline{\text{AREQ}}$&$\overline{\text{ADS}}$ finishing the access.

Delayed Accesses. If the CPU requests an access in the middle of a refresh cycle, or when there are back to back accesses to the same bank, the DRAM controller will delay the second access to guarantee RAS precharge time. In this application note, the DP8432V is programmed to guarantee 3 positive edges of CLK for precharge.

During most accesses, RAS negates just before the positive edge of T2 on the second access. In these cases, **that** positive edge of CLK will count as the first positive clock of precharge.

To guarantee the precharge time, the DRAM controller will keep $\overline{\text{DTACK}}$ high during the 3 edges of precharge. After meeting precharge, $\overline{\text{RAS}}$ will assert from the 3rd positive edge of CLK, T4. to finish the access the DP8432V asserts $\overline{\text{DTACK}}$ from the positive edge of T6. The 80486 finishes the access when it samples $\overline{\text{RDY}}$ asserted at the end of T7.

If worst case timing occurs (Max PAL delay to $\overline{\text{AREQ}}$ negated, and AREQ negated to RAS negated), RAS may negate after the positive edge of T2 on the second access. In this case precharge will be longer and the complete access takes one extra clock. $\overline{\text{RAS}}$ will assert from T5, $\overline{\text{DTACK}}$ from T7 and $\overline{\text{RDY}}$ from T8. In this case the CPU will finish the access at the end of T8.

Programming 3Ts of precharge guarantees that in any case precharge will be met. If 2Ts were to be programmed, it is possible to violate the 60 ns minimum of $\overline{\text{RAS}}$ precharge when $\overline{\text{RAS}}$ negates just before the beginning of T2.

Cache Filling Multiple Accesses. Every time the 80486 addresses the DRAM array, $\overline{\text{CS}}$ asserted with $\overline{\text{ADS}}$# asserted latches a true signal into the KEN# input. The 80486 supports cache fill during read cycles only. If the 80486 is to perform a cache fill (see i486 data sheet for requirements for cacheable accesses), the CPU will not assert the $\overline{\text{BLAST}}$ output. $\overline{\text{BLAST}}$ high keeps $\overline{\text{AREQ}}$&$\overline{\text{ADS}}$ asserted, and $\overline{\text{AREQ}}$*$\overline{\text{ADS}}$ asserted keeps $\overline{\text{RAS}}$ asserted.

The opening access finishes when the DP8432V asserts $\overline{\text{DTACK}}$ from the rising clock edge of T4 to generate $\overline{\text{RDY}}$# from T5. The 80486 samples $\overline{\text{RDY}}$ asserted at the end of T5. $\overline{\text{HCAS}}$ negates from the rising clock edge after $\overline{\text{DTACK}}$ asserts (end of T5).

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To continue cache filling (2nd read), after the 80486 samples $\overline{RDY\#}$ asserted at the end of T5, (rising edge of T1 second read), it outputs a new address and asserts $\overline{ADS\#}$ for the second read. $\overline{ADS\#}$ low for the second read makes $\overline{HCAS}$ to assert from the next rising edge of clock (T2 of 2nd read). $\overline{DTACK}$ is programmed to stay low during burst accesses (R4 = 0, R5 = 0). $\overline{DTACK}$ and $\overline{HCAS}$ asserted make $\overline{RDY}$ to assert from the rising edge of T3. $\overline{RDY}$ asserted allows the i486 to latch the second piece of data. This logic allows up to 4 multiple accesses to fill the cache line. $\overline{AREQ\&ADS}$ will negate only after $\overline{BLAST}$ and $\overline{DTACK}$ assert during the last access of the cache fill.

Refresh Cycles. The DP8432V will automatically refresh a memory row every 15 μs. In cases where an access is in progress at the time of the refresh request, the DP8432V waits for the access to finish and precharge to take place before doing the refresh. In the same way, if a refresh cycle is in progress and the i486 request a memory access, the DP8432V will insert wait states into the CPU cycle to allow refresh and precharge to finish. The DP8432V can insert a refresh cycle in between two back to back accesses.

Timing Analysis. Timing parameters with a "$" refer to the DP8430/31/32V-33 data sheet. Timing parameters starting with a "#" refer to the 80486 33 MHz data sheet. The user can calculate new timings based on the equations given. This application note uses DRAMs with t_{RAC} = 70 ns, t_{CAC} = 20 ns and t_{AA} = 35 ns.

The DP8430V/31V/32V timing parameters may have changed since this application note was written. The reader should always refer to the latest data sheet.

$400b $\overline{ADS}$ Asserted Set Up to CLK High (8 ns min)

= Tcp33 – Max PAL Delay to $\overline{ADS}$ Asserted

= 30.3 – 8

= 22.3 ns

$401 $\overline{CS}$ Asserted to $\overline{ADS}$ Asserted (2 ns min)

= (Tcp + Min PAL Delay to $\overline{ADS}$ Asserted)—(#t6 CLK to Address Valid + Max Decoder Delay)

= (30.3 + 5.5) – (19 − 14)

= 35.8 – 33

= 2.8 ns

$404 Row/Bank Address Set Up to $\overline{ADS}$ Asserted (3 ns and 6 ns)

$407

= (Tcp + Min PAL Delay to $\overline{ADS}$ Asserted)—(#t6 CLK to Address Valid)

= 30.3 + 5.5 – 19

= 35.8 – 19

= 16.8 ns

#t6 $\overline{RDY}$ Set Up Time (6 ns min)

Normal Access

= 1 Tcp33 – Max PAL Delay to $\overline{RDY}$ Asserted

= 30.3 – 8

= 22.3 ns

Cache Filling Access (6 ns min)

= 1.0 Tcp33 – Max PAL Delay to $\overline{RDY}$ Asserted

= 30.30 – 8

= 22.3 ns

t_{RAC} Access Time from RAS

= 4Tpc33 – (Max PAL Delay to $\overline{ADS}$ Asserted + $402 $\overline{ADS}$ to RAS Asserted + #t22 Data Set Up Time)

= 121.2 – (8 + 20 + 5)

= 121.2 – 33

= 88.2 ns

t_{CAC} Access Time from CAS

Normal Access (20 ns min)

= 4Tpc33 – (Max PAL Delay to $\overline{ADS}$ Asserted + $403 $\overline{ADS}$ to CAS Asserted + #t22 Data Set Up Time)

= 121.2 – (8 + 70 + 5)

= 121.2 – 83

= 38.2 ns

Cache Filling Access (20 ns min)

= 2Tpc33 – (Max PAL Delay to $\overline{HCAS}$ Asserted + Max OR Gate Delay + $14 Max $\overline{ECAS}$ Asserted to $\overline{CAS}$ Asserted + #22 Data Set Up Time)

= 60.60 – (8 + 6 + 13 + 5)

= 60.60 – (32)

=28.60 ns

t_{AA} Access Time from Row Address Valid

Normal Access (40 ns min)

= 4Tpc33 – (Max PAL Delay to $\overline{ADS}$ Asserted + $417 $\overline{ADS}$ to Row Address Valid + #t22 Data Set Up Time)

= 121.2 – (8 + 63 + 5)

= 121.2 – 76

= 45.2 ns

Cache Filling Access (40 ns min)

= 3Tpc33 – (#t6 CLK High to Address Valid + $26 Address Valid to Q Valid + #t15 Data Set Up Time)

= 90.90 – (19 + 20 + 5)

= 90.90 – 44

= 46.90 ns

t_{RP} RAS Precharge (60 ns min)

RAS Negates before the Positive Edge of T2. Typical Case

= 3Tpc – (PAL Delay to $\overline{ADS}$&$\overline{AREQ}$ negated + $13 AREQ to RAS negated)

= 90.90 – (7 + 20) typical case

= 64.90 ns

RAS Negates after the Positive Edge of T2

= 4Tpc – Max (PAL Delay to $\overline{ADS}$&$\overline{AREQ}$ Negated + $13 AREQ to RAS negated)

= 121.20 – (8 + 25) worst case

= 121.20 – 33

= 88.20 ns

The controller needs to be programmed for 3 Ts of precharge. 2Ts do not provide enough precharge during cases where $\overline{RAS}$ negates just before T2.

t_{RAS} RAS Refresh

Refresh is programmed for 4Ts.

PAL EQUATIONS

A 15 ns PAL16R6 is used to meet the timing calculations. The following are the equations for the PAL.

Inputs: CLK, ADS#, RESET, BLAST#, $\overline{DTACK}$, $\overline{CS}$, RW#, MIO#.

Outputs: $\overline{AREQ}$, RDY#, $\overline{HCAS}$, KEN#, $\overline{WE}$, $\overline{ML}$.

$\overline{AREQ}$~: = $\overline{ADS}$__ * RESET__
+ $\overline{AREQ}$__ * RESET__ * DTACK__
+ $\overline{AREQ}$__ * RESET__ * BLAST__

$\overline{HCAS}$~: = $\overline{ADS}$__ * RESET__
+ $\overline{HACS}$__ * DTACK__ * RESET__

$\overline{RDY}$~: = $\overline{HCAS}$__ * $\overline{DTACK}$__

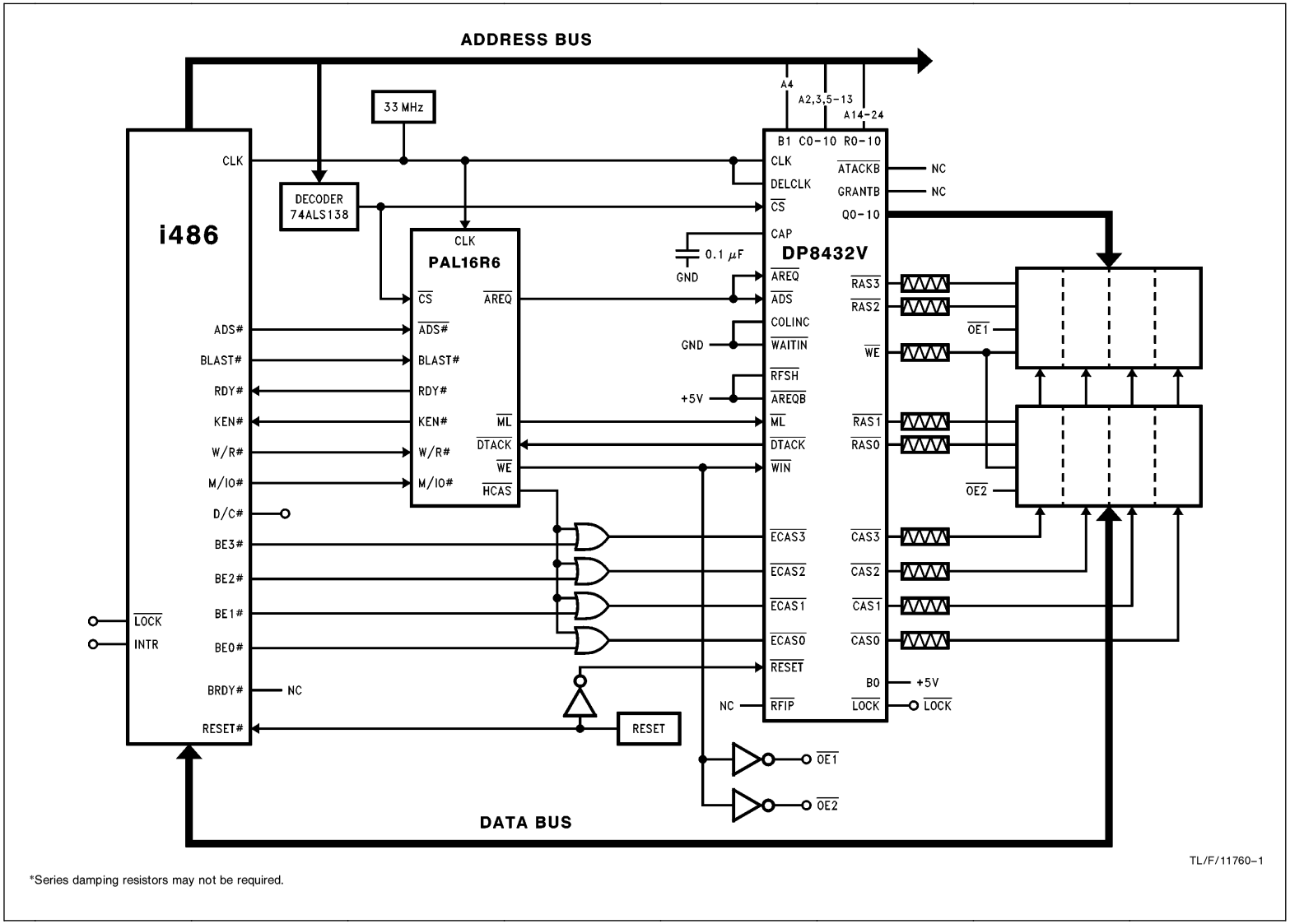
$\overline{KEN}$~: = $\overline{ADS}$__ * RESET__ * $\overline{CS}$__
+ $\overline{KEN}$__ * $\overline{AREQ}$__ * RESET__ * $\overline{CS}$__

$\overline{MW}$~: = $\overline{RW}$ * MIO

$\overline{ML}$~: = $\overline{RESET}$__
+ $\overline{ML}$__ * RESET__ * $\overline{WR}$__
+ $\overline{ML}$__ * RESET__ * ADS__

DRAM CONTROLLER PROGRAMMING BITS

$\overline{ECAS}$ = 0	C4 = 0	R6 = 0
B1 = 1	C3 = 0	R5 = 0
B2 = 1	C2 = 0	R4 = 0
C9 = 0	C1 = 1	R3 = 0
C8 = 1	C0 = 0	R2 = 1
C7 = 1	R9 = 0	R1 = 1
C6 = 1	R8 = 1	R0 = 1
C5 = 0	R7 = 1	



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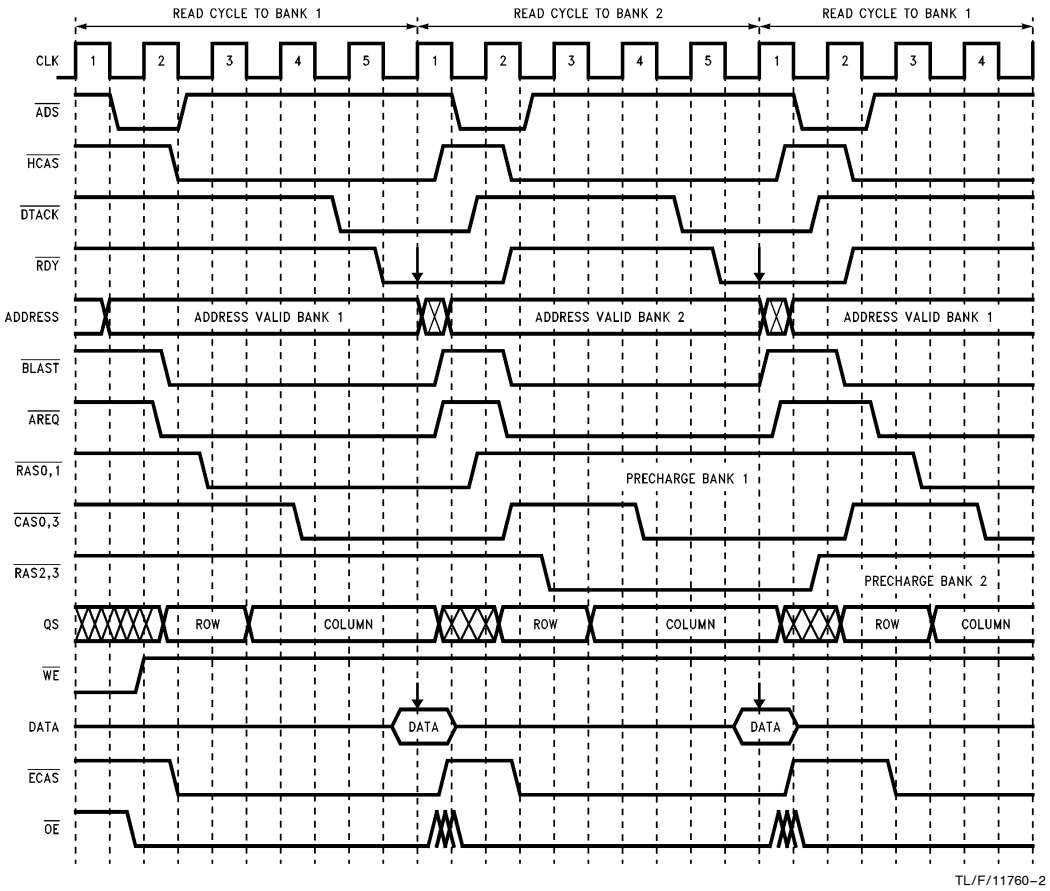
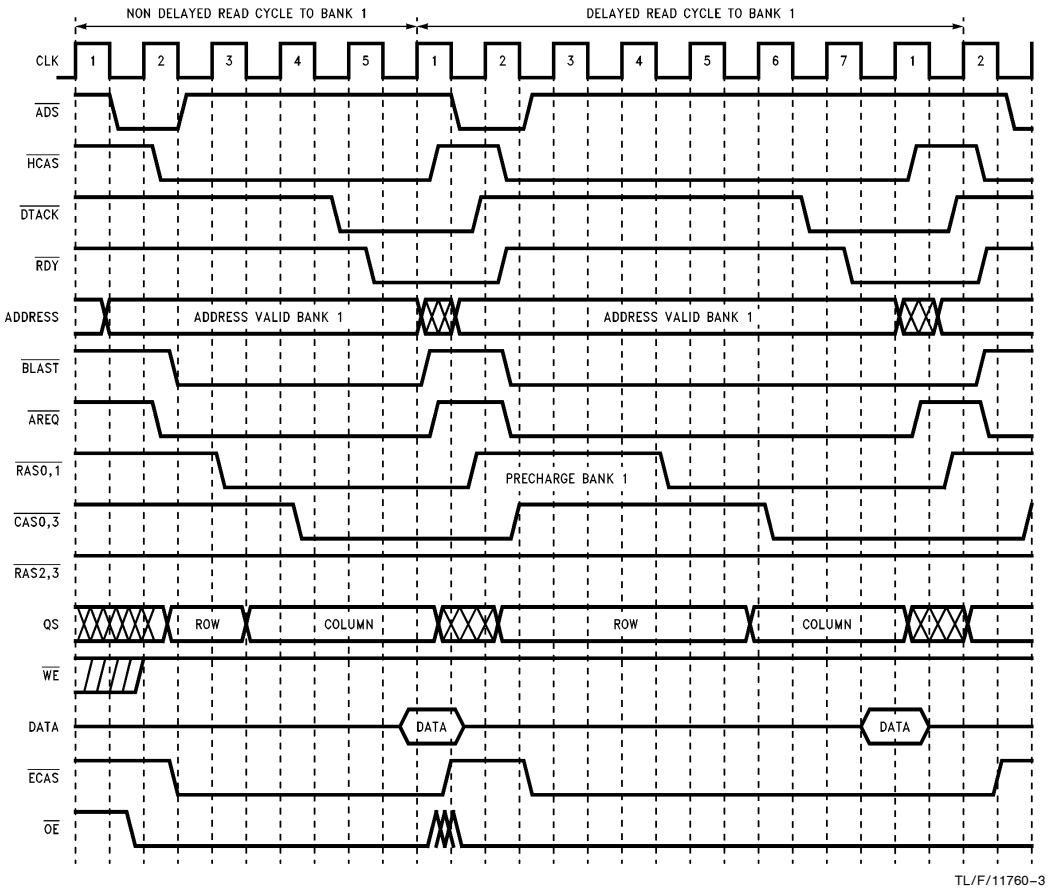
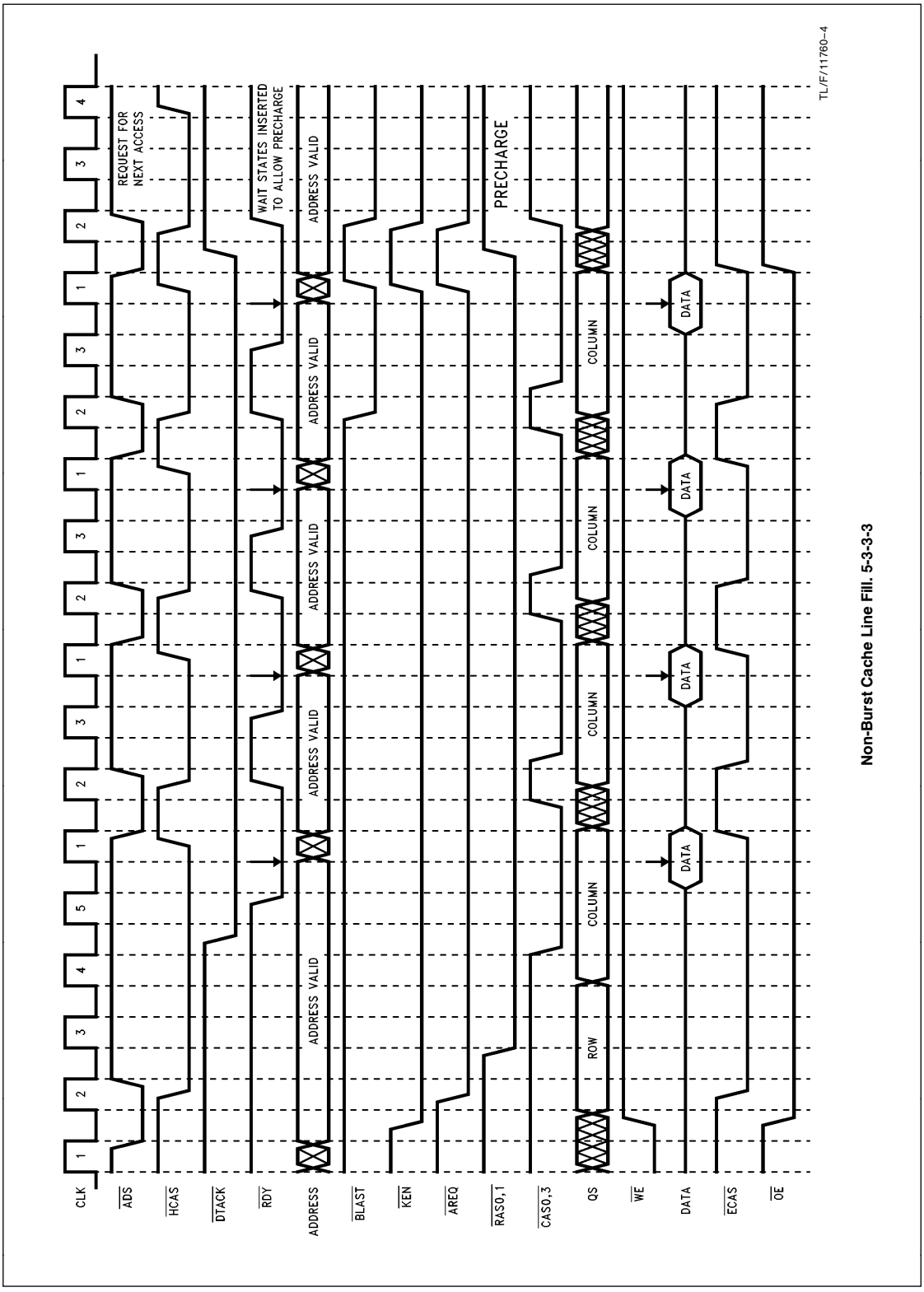
*Series damping resistors may not be required.



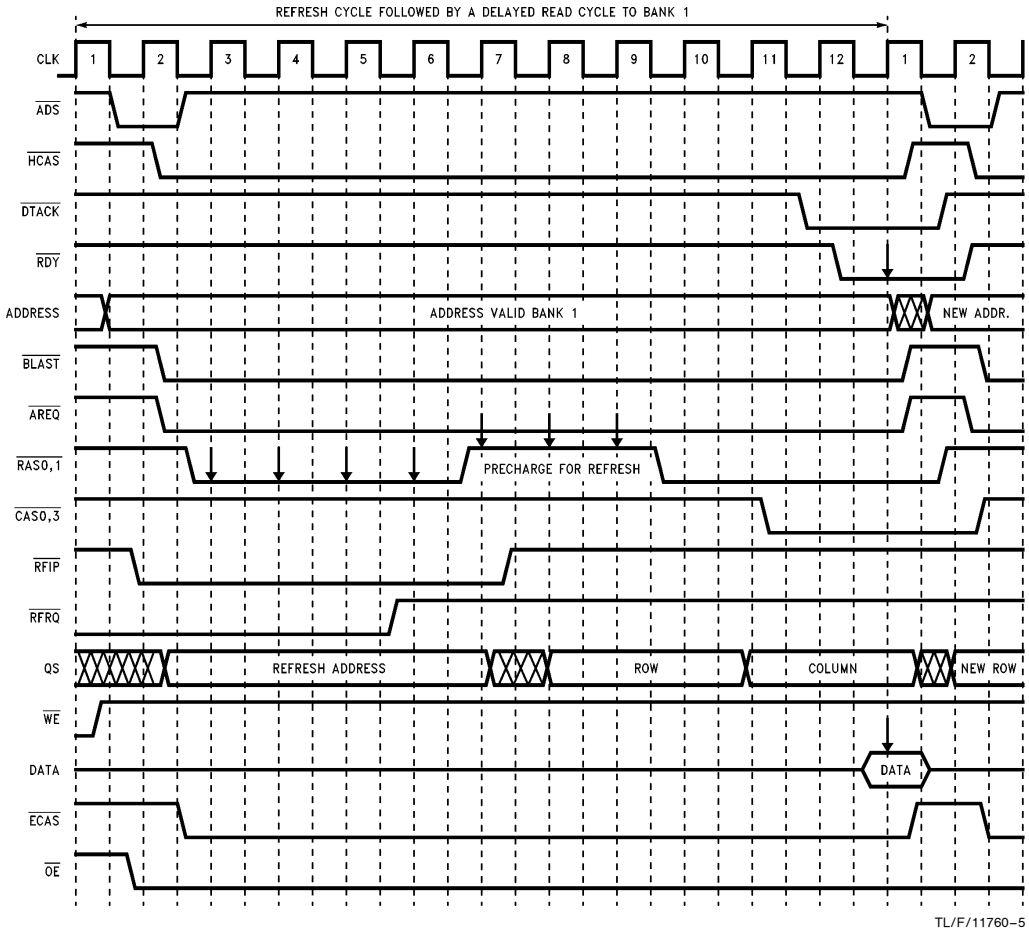
Non Delayed Back to Back Access to Different Banks



Delayed Back to Back Access to Bank 1



Non-Burst Cache Line Fill. 5-3-3-3



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Refresh Followed by an Access to Bank 1

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