8-Channel 8-Bit PWM Controller

National Semiconductor
Application Note 824
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INTRODUCTION

This application note discusses a cost effective implementation of an 8-channel DAC to replace potentiometers.

TECHNICAL OVERVIEW

The COP822C was considered for the application. At the outset since the DACs were replacing pots, speed of conversion was not an issue. The issue became in that how fast a frequency with 8-bits of resolution on eight channels could be implemented in software. This would then determine the response time and therefore the filtering components to convert the varying duty cycle squarewave to a DC voltage. A simple RC can be used or for better response a pie filter can be used. Depending on the load, buffering may be required. In preliminary testing ripple was less than 1-bit.

IMPLEMENTATION

Software was then written to determine the time required to execute one loop of the program that determined the resolution that could be achieved for 8 separate channels. The routine is basically a small loop that decrements 8 registers or counters and reloads these counters after 8-bits of resolution. It was determined that the loop could be done in 40 μs. This is the limiting factor. From this 40 μs (100 Hz instruction cycle frequency) per bit for 8 bits of resolution, the period turns out to be 10 ms. Therefore, in 10 ms all 8 channels are updated with their on/off times.

Since the outputs are constantly running, interrupts are not used so that the PWM outputs stay more stable. Also, this provides a faster throughput. Interface to the chip can be done in either a serial (MICROWIRE/PLUS™) or parallel fashion, depending on best fit for the application. For a serial implementation the Microwire busy bit can be polled each loop. If parallel interface is required, there are enough pins on the device to implement a simple handshake exchange; i.e., have 3 address lines, 4 data lines and a chip select. In either case, it requires a two byte protocol: address and data. Data is the PWM "on time" to determine duty cycle.

CONCLUSION

This low cost implementation of an 8-channel 8-bit PWM controller has multiple features. Besides a low speed DAC, PWM control in conjunction with NSC DMOS power products could also be a cost effective peripheral for power drive applications. It should be noted that using this approach, there is no CPU time for doing other tasks. One last item to note is the COP800 output structure. Depending on application the outputs (G and L) can be configured in TRI-STATE® mode, thereby putting the external filter in a holding pattern or low leakage state. In this way other small routines i.e., interface, could be accomplished.

Due to the software implementation methodology, there is flexibility, i.e., in the number of channels, resolution and the interface. Also, since it is based around a COP800 solution, packing (pins) and operating frequency including crystal options are also flexible.

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The following pages show the code used in evaluating the concept as well as the filter components. Basically, eight register with varying "on times" were loaded so that the PWM outputs could be analyzed along with software performance. The remaining code for MICROWIRE/PLUS and the exact filter components are not finalized.

```
; COP822 - 8-Channel 8-Bit PWM Output
          .CHIP        820

INIT:     LD           0EE,#00        ;clear control reg.
          LD           0EF,#00        ;clear psw, int, etc.
          LD           SP,#02F        ;TOP OF STACK ??

          LD           008,#05        ;LOAD 8 AUTO RELOAD RESCNT"ERS
          LD           009,#25        ;RAM ADDR 8 THROUGH 0FH
          LD           00A,#50        ;TEST ONLY, IN REAL LIFE THESE
          LD           00B,#90        ;GET LOADED THROUGH MICROWIRE
          LD           00C,#125
          LD           00D,#160
          LD           00E,#210
          LD           00F,#250

; PLACE TO TRANSFER RELOAD COUNTERS TO RESCNTERS

          JSR          RELOAD         ;AUTO RELOAD COUNT TO RESCNT'ERS

          LD           0D1,#0FF       ;L CONFIG. REG TO PUSH PULL ONE OUT
          LD           0D0,#0FF       ;L ports to all 1's

PERIOD:   LD           0F0,#255       ;255 * THROUGH LOOP = 8-BIT RES.
RESCNT:   LD           B.#00          ;START OF RAM MAP FOR RESCNT'ERS
          LD           A,[B]          ;DEC "ON TIME" COUNTERS
          DEC          A
          X            A,[B+]         ;PUT BACK FOR NEXT TIME
          IFEQ         A,#00          ;WHEN CNT = 0, PORT LOW
          RBIT         0,0D0          ;D0 = MEMORY MAP FOR PORT L

;2ND PWM OUTPUT
          LD           A,[B]          ;DEC "ON TIME" COUNTERS
          DEC          A
          X            A,[B+]         ;PUT BACK FOR NEXT TIME
          IFEQ         A,#00          ;WHEN CNT = 0, PORT LOW
          RBIT         1,0D0          ;D0 = MEMORY MAP FOR PORT L
;3RD PWM OUTPUT
          LD           A,[B]          ;DEC "ON TIME" COUNTERS
          DEC          A
          X            A,[B+]         ;PUT BACK FOR NEXT TIME
          IFEQ         A,#00          ;WHEN CNT = 0, PORT LOW
          RBIT         2,0D0          ;D0 = MEMORY MAP FOR PORT L
;4TH PWM OUTPUT
          LD           A,[B]          ;DEC "ON TIME" COUNTERS
          DEC          A
          X            A,[B+]         ;PUT BACK FOR NEXT TIME
          IFEQ         A,#00          ;WHEN CNT = 0, PORT LOW
          RBIT         3,0D0          ;D0 = MEMORY MAP FOR PORT L
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;5TH PWM OUTPUT
          LD          A,[B]              ;DEC "ON TIME" COUNTERS
          DEC         A
          X           A,[B+]             ;PUT BACK FOR NEXT TIME
          IFEQ        A,#00              ;WHEN CNT = 0, PORT LOW
          RBIT        4,0D0               ;D0 = MEMORY MAP FOR PORT L
;6TH PWM OUTPUT
          LD          A,[B]              ;DEC "ON TIME" COUNTERS
          DEC         A
          X           A,[B+]             ;PUT BACK FOR NEXT TIME
          IFEQ        A,#00              ;WHEN CNT = 0, PORT LOW
          RBIT        5,0D0               ;D0 = MEMORY MAP FOR PORT L
;7TH PWM OUTPUT
          LD          A,[B]              ;DEC "ON TIME" COUNTERS
          DEC         A
          X           A,[B+]             ;PUT BACK FOR NEXT TIME
          IFEQ        A,#00              ;WHEN CNT = 0, PORT LOW
          RBIT        6,0D0               ;D0 = MEMORY MAP FOR PORT L
;8TH PWM OUTPUT
          LD          A,[B]              ;DEC "ON TIME" COUNTERS
          DEC         A
          X           A,[B+]             ;PUT BACK FOR NEXT TIME
          IFEQ        A,#00              ;WHEN CNT = 0, PORT LOW
          RBIT        7,0D0               ;D0 = MEMORY MAP FOR PORT L

;  NOTE 255 TIMES IS NOW IN LOOP, SOON TO BE INTERRUPT.
          DRSZ        0F0                ;PERIOD TERMINATOR = 0F0
          JMP         RESCNT             ;FINISH 255 TIMES

;DEC 0F0 IF ZERO RESET RES COUNTERS AND PUT PORT L HI.

          LD          0D0,#0FF           ;PORT L HI
          JSR         RELOAD
                              ;This is place Microwire should be checked.
          JMP         PERIOD             ;START PERIOD OVER WITH NEW COUNTS

; RELOAD WILL PUT RAM FROM ADDR 8 TO F IN 0 TO 7.
RELOAD
          LD          X,#008             ;1ST RELOAD COUNTER
          LD          B,#00              ;ST RESCNT
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          LD          A,[X+]
          X           A,[B+]
          RET
          .END
```

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