# Interfacing the DP8420A/21A/22A to the National Semiconductor NS32532

National Semiconductor
Application Note 541
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### 1.0 INTRODUCTION

This application note describes how to interface the National Semiconductor NS32532 microprocessor to the DP8422A DRAM controller (also applicable to DP8420A/21A). It is assumed that the reader is already familiar with NS32532 and the DP8422A modes of operation.

### 2.0 DESCRIPTION OF DESIGN, ALLOWING UP TO 25 MHz OPERATION WITH 2 OR 3 WAIT STATES IN NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES

This design drives two banks of DRAM, each bank being 32 bits in width, giving a maximum memory capacity of 32 Mbytes (using 4 Mbit x 1 DRAMs). By choosing a different $\overline{RAS}$ and $\overline{CAS}$ configuration mode (see programming mode bits section of DP8422A data sheet) this application could support 4 banks of DRAM, giving a memory capacity of 64 Mbytes (using 4 Mbit x 1 DRAMs, NOTE that when driving 64 Mbytes the timing calculations will have to be adjusted to the greater capacitive load).

The memory banks are interleaved on every four word (32-bit word) boundary. This means that the address bit (A4) is tied to the bank select input of the DP8422A (B1). If the majority of accesses made by the NS32532 are sequential, the NS32532 can be doing burst accesses most of the time. Each burst of four words can alternate memory banks, allowing one memory bank to be precharging ($\overline{RAS}$ precharge) while the other bank is being accessed. This is a higher performance memory system than a non-interleaved memory system (bank select on the higher address bits). Each separate memory access to the same memory bank will generally require extra wait states to be inserted into the CPU access cycles to allow for the $\overline{RAS}$ precharge time.

This design supports the NS32532 burst access operations. To support these operations it is assumed that nibble mode DRAMs will be used. (See the timing calculations, Section IV).

The logic shown in this application note forms a complete NS32532 memory sub-system, no other logic is needed. This sub-system automatically takes care of:

A arbitration between Port A, Port B, and refreshing the DRAM;

B the insertion of wait states to the processor (Port A and Port B) when needed (i.e., if $\overline{RAS}$ precharge is needed, refresh is happening during a memory access, the other Port is currently doing an access . . . etc);

C performing byte writes and reads to the 32-bit words in memory.

The Confirm Bus Cycle ($\overline{CONF}$) signal is input to the DP8422A Chip Select ($\overline{CS}$) input. Therefore the $\overline{CONF}$ signal disables the current access, from the DP8422A, if the NS32532 has cancelled it ($\overline{CONF}$ high setup to $\overline{ADS}$ transitioning low). The PAL starts an access via the DP8422A by pulling the $\overline{ADS}$, $\overline{AREQ}$ inputs low. These inputs are brought low given that $\overline{CS}$ and Begin Memory Transaction ($\overline{BMT}$) are both low.

By making use of the enable input on the 74AS244 buffer, this application can easily be used in a dual access application. The addresses and chip select are TRI-STATE® through this buffer, the write input ($\overline{WIN}$), lock input ($\overline{LOCK}$), and $\overline{ECAS}0-3$ inputs must also be able to be TRI-STATE (another 74AS244 could be used for this purpose). By multiplexing the above inputs (through the use of the above parts and similar parts for Port B) the DP8422A can be used in a dual access application. If this design is used in a dual access application at 25 MHz the $t_{RAC}$ and $t_{CAC}$ (required $\overline{RAS}$ and $\overline{CAS}$ access time required by the DRAM) will have to be recalculated since the time to $\overline{RAS}$ and $\overline{CAS}$ is longer for the dual access application (see TIMING section of this application note).

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### 3.0 NS32532 DESIGN, UP TO 25 MHz WITH 2 OR 3 WAIT STATES DURING NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES, PROGRAMMING MODE BITS

| Programming Bits | Description |
|---|---|
| R0 = 1 | $\overline{RAS}$ low four clocks, $\overline{RAS}$ |
| R1 = 1 | precharge of three clocks. |
| R2 = 1 | $\overline{DTACK}$1 is chosen. $\overline{DTACK}$ low |
| R3 = 0 | first rising CLK edge after access $\overline{RAS}$ is low. |
| R4 = 0 | No Wait states during burst |
| R5 = 0 | accesses. |
| R6 = 0 | If $\overline{WAITIN}$ = 0, add one clock to $\overline{DTACK}$. Since we are not using the $\overline{WAITIN}$ input it should be tied high on the DP8422A. |
| R7 = 1 | Select $\overline{DTACK}$ |
| R8 = 1 | Non-Interleaved Mode |
| R9 = X | |
| C0 = X | Select based upon the input |
| C1 = X | ''DELCLK'' frequency. Example: if |
| C2 = X | the input clock frequency is 20 MHz then choose C0,1,2 = 0,0,0 (divide by ten, this will give a frequency of 2 MHz). If using the DP8422A over 20 MHz do an initial divide by two externally and then run that output into the DELCLK input and choose the correct divider. |
| C3 = X | |
| C4 = 0 | $\overline{RAS}$ groups selected by ''B1''. This |
| C5 = 0 | mode allows two $\overline{RAS}$ outputs to |
| C6 = 1 | go low during an access, and allows byte writing 32-bit words. |
| C7 = 1 | Column address setup time of 0 ns. |
| C8 = 1 | Row address hold time of 15 ns. |
| C9 = 1 | Delay $\overline{CAS}$ during write accesses to one clock after $\overline{RAS}$ transitions low. |
| B0 = 1 | Fall-thru latches |
| B1 = 1 | Access Mode 1 |
| $\overline{ECAS}$0 = 0 | $\overline{CAS}$ not extended beyond $\overline{RAS}$. |

0 = program with low voltage level

1 = program with high voltage level

X = program with either high or low voltage level (don't care condition)

### NS32532 TIMING CALCULATIONS FOR DESIGN AT 25 MHz WITH 3 WAIT STATES DURING THE NORMAL ACCESSES AND 1 WAIT STATE DURING BURST ACCESSES

1 Minimum $\overline{ADS}$ low setup time to $\overline{CLOCK}$ high for $\overline{DTACK}$ logic to work correctly (DP8422A-25 needs 25 ns):

40 ns (one clock period) − 8 ns (PAL16R4D clocked output maximum) = 32 ns

2a Minimum time to $\overline{ADS}$ low = 40 ns (one clock period) + 2 ns (minimum clocked output delay of PAL16R4D PAL) = 42 ns minimum

2b Minimum address setup time to $\overline{ADS}$ low (DP8422A-25 needs 14 ns):

42 ns (#2a above) − 8 ns (max time to address valid from BLCK high) − 6.2 ns (74AS244 buffer delay max) = 27.8 ns

3a Minimum $\overline{CS}$ setup time to CLK high (PAL16R4D needs 10 ns):

40 ns (one clock period) − 8 ns (maximum time to address valid from BCLK high) − 6.2 ns (74AS244 buffer delay maximum) − 9 ns (max 74AS138 decoder) = 16.8 ns

3b Minimum $\overline{CS}$ setup time to $\overline{ADS}$ low (DP8422A-25 needs 5 ns):

a Minimum time to $\overline{ADS}$ low (see #2a from above) = 42 ns

b Maximum time to $\overline{CONF}$ ($\overline{CONF}$ is tied to $\overline{CS}$ of the DP8422A) = 20 ns (one half clock period) + 9 ns ($\overline{CONF}$ low from falling clock edge) = 29 ns maximum

Therefore:

42 ns (minimum time to $\overline{ADS}$ low) − 29 ns (maximum time to $\overline{CONF}$ low) = 13 ns

4 Determining $t_{RAC}$ during a normal access ($\overline{RAS}$ access time needed by the DRAM):

160 ns (four clock periods to do the access) − 8 ns (PAL16R4D clocked output) − 29 ns ($\overline{ADS}$ to $\overline{RAS}$ low) − 10 ns (NS32532 data setup time) − 7 ns (74F245) = 106 ns

Therefore the $t_{RAC}$ of the DRAM must be 106 ns or less.

5 Determining $t_{CAC}$ during a normal access ($\overline{CAS}$ access time) and column address access time needed by the DRAM:

160 ns − 8 ns − 10 ns − 7 ns − 75 ns ($\overline{ADS}$ to $\overline{CAS}$ low on DP8422A-25, 50 pF spec) − 12 ns [74AS32, 6 ns, plus 6 ns extra, taken from lab data on the 74AS32, for drving a 22Ω damping resistor and 150 pF of capacitance associated with driving 16 DRAM $\overline{CAS}$ inputs (per $\overline{CAS}$ output)] = 48 ns

Therefore the $t_{CAC}$ of the DRAM must be 48 ns or less.

6 Determining the nibble mode access time needed during a burst access:

80 ns (two clock periods to do the burst) − 20 ns (one half clock period during which $\overline{CAS}$ is high from the previous access) − 10 ns (PAL16R4D combinational output from CLK input falling edge, $\overline{ENCAS}$) − 12 ns (74AS32 delay to produce $\overline{CAS}$ from the $\overline{ENCAS}$ input, see description from #5) − 10 ns (NS32532 data setup time) − 7 ns (74F245) = 21 ns

Therefore the nibble mode access time of the DRAM must be 21 ns or less.

7 Maximum time to $\overline{DTACK}$1 low (PAL16R6D needs 10 ns setup to BCLK):

40 ns (one clock) − 28 ns ($\overline{DTACK}$1 low from CLK high on DP8422A-25) = 12 ns

8 Minimum $\overline{RDY}$ setup time to BCLK (19 ns to BCLK rising edge is needed by the NS32532):

40 ns (one clock period) − 8 ns (PAL16R4D clocked output maximum) = 32 ns

**Note:** Calculations can be performed for different frequencies by substituting the appropriate values into the above equations.

**5.0 NS32532 DESIGN, PAL EQUATIONS WRITTEN IN NATIONAL SEMICONDUCTOR PLAN FORMAT**

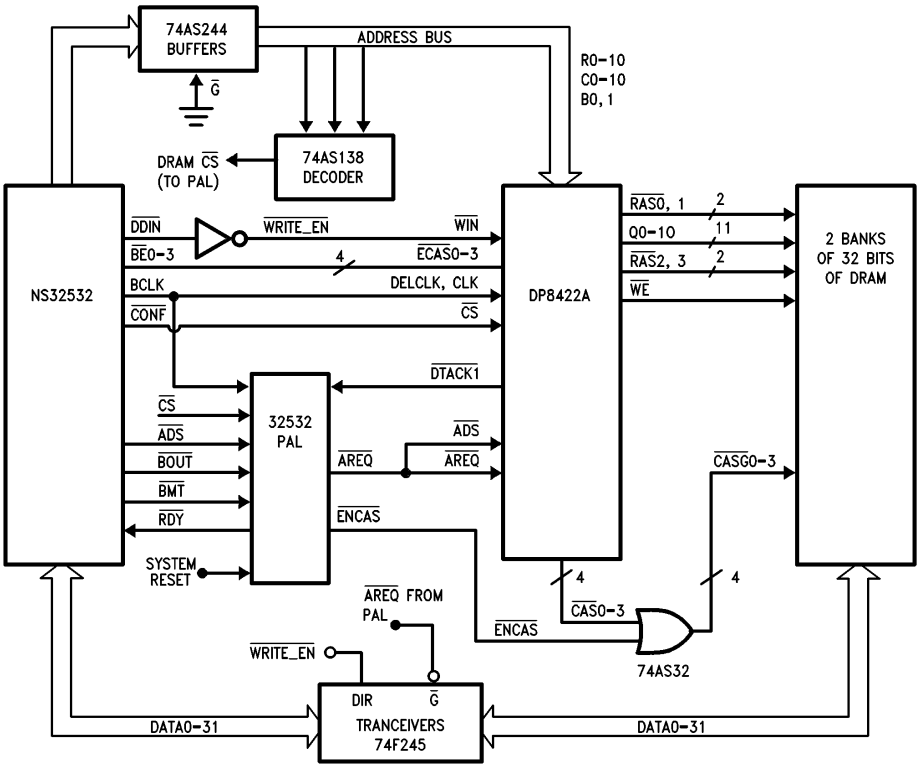
```
PAL16R4D
BCLK /CS /ADS /BOUT /DTACK /EXRDY /3W CLK /BMT GND
/OE NC1 /DB NC2 /RDY /DA /AREQ /ENCAS /ADSL VCC

IF (VCC) /ADSL = /ADS
                 +/ADSL*/CLK
                 +/ADSL*/BOUT*/CS
                 +/ADSL*RDY*/CS

IF (VCC) /ENCAS = /AREQ*/CS*DB
                  +/AREQ*/CLK*/CS

IF (VCC) /DB = /AREQ*/BOUT*/RDY*/CLK
               +/AREQ*/BOUT*/DB*CLK

/AREQ := /ADSL*/BMT*/CS
         +/ADSL*/AREQ*/CS

/DA := /ADSL*/AREQ*/DTACK*DA*/3W*/CS

/RDY := /AREQ*/DTACK*/ADSL*/DA*/CS*/3W
        +/AREQ*/DTACK*/ADSL*RDY*/CS*3W
        +/EXRDY
```

**Key: Reading PAL equations written in PLAN**

```
EXAMPLE EQUATIONS: IF (VCC) /DB = /AREQ*/BOUT*/RDY*/CLK
                                  +/AREQ*/BOUT*/DB*CLK
```

This example reads: the output ''/DB'' will transition low given that one of the following conditions are valid;
1) the output ''/AREQ'' is low AND the input ''/BOUT'' is low AND the output ''/RDY'' is low and the input ''CLK'' is low, OR
2) the output ''/AREQ'' is low AND the input ''/BOUT'' is low AND the output ''/DB'' is low and the input ''CLK'' is high.

**NS32532 Design, up to 25 MHz, with 2 or 3 Wait States in Normal Accesses and 1 Wait State in Burst Accesses**

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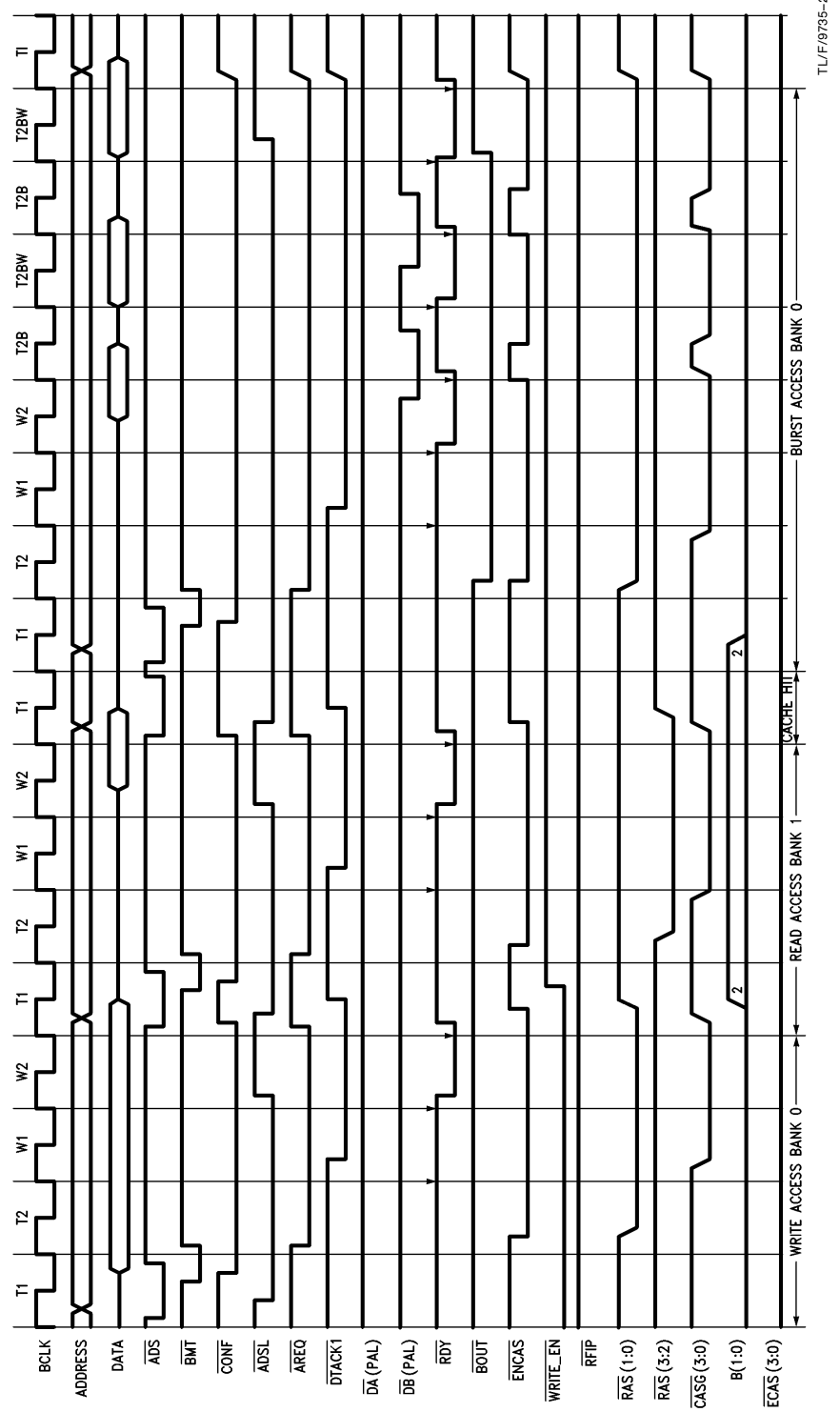
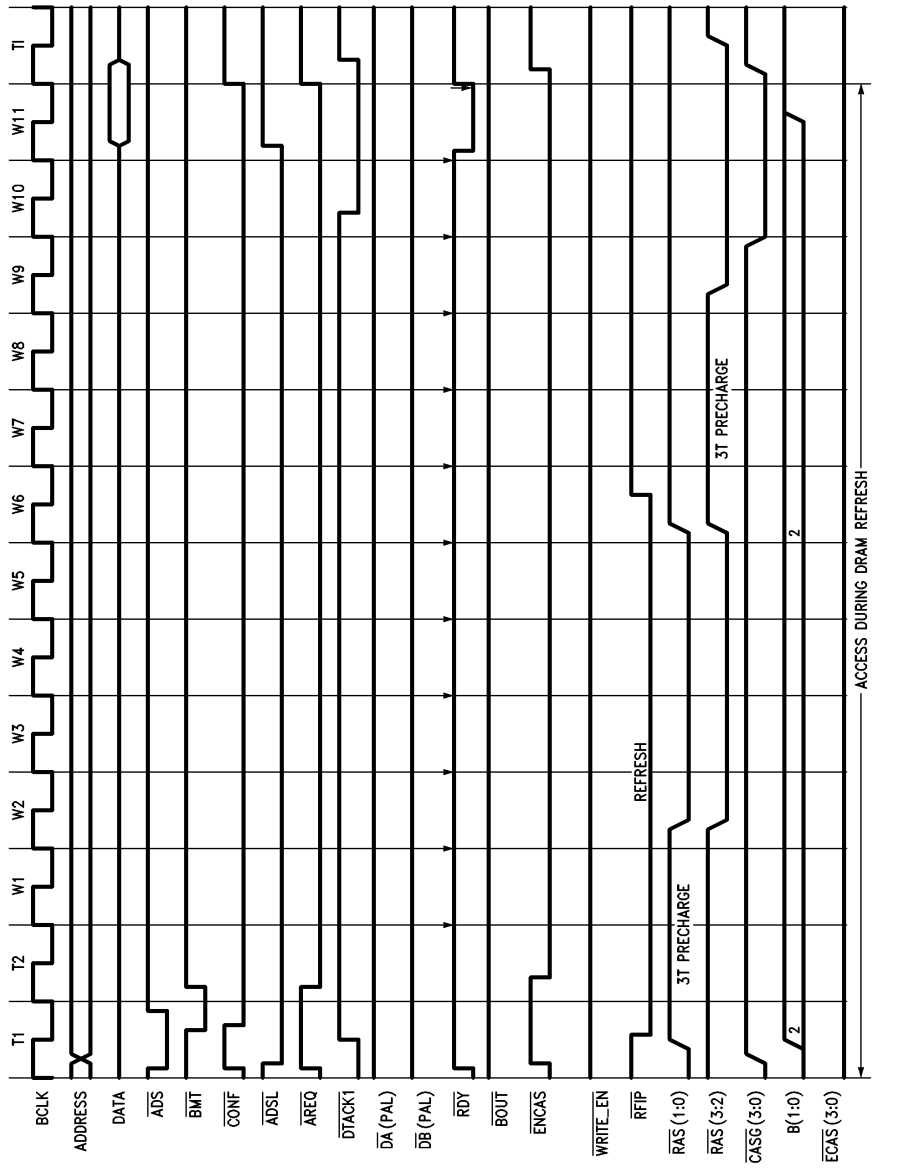
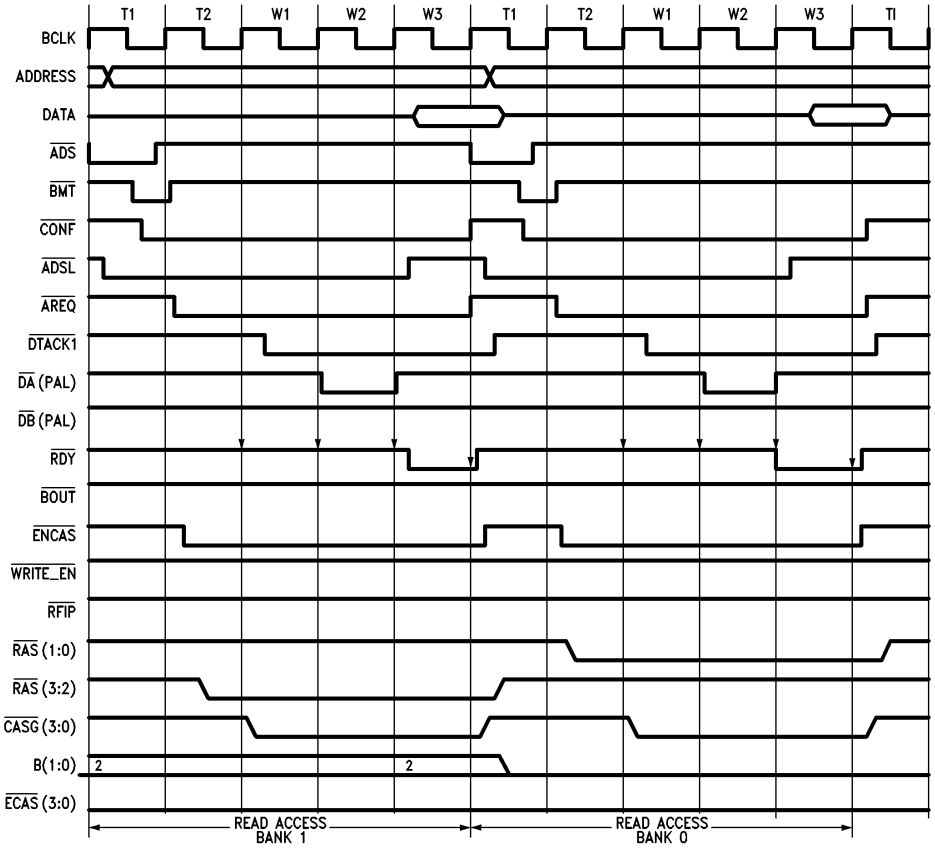
**NS32532 with 2 Wait States per Access (One Wait State during Burst Accesses), $\overline{3W}$ Input of PAL is Tied High**



**NS32532 with 2 Wait States per Access (One Wait State during Burst Accesses), $\overline{3W}$ Input of PAL is Tied High**



**NS32532 with 3 Wait States per Access (One Wait State during Burst Accesses), $\overline{3W}$ Input of PAL is Tied Low**

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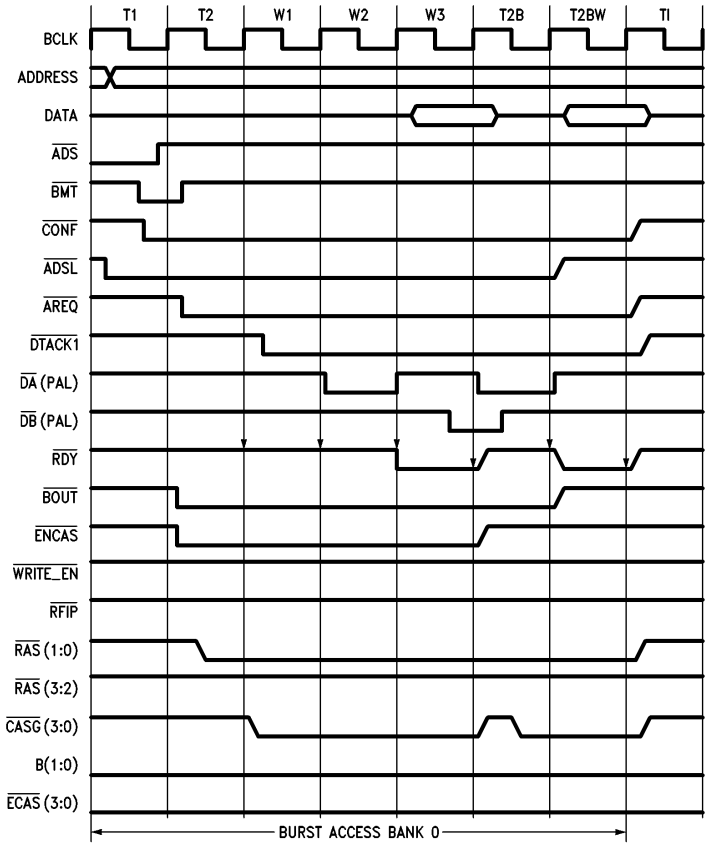
**NS32532 with 3 Wait States per Access (One Wait State during Burst Accesses), $\overline{3W}$ Input of PAL is Tied Low**

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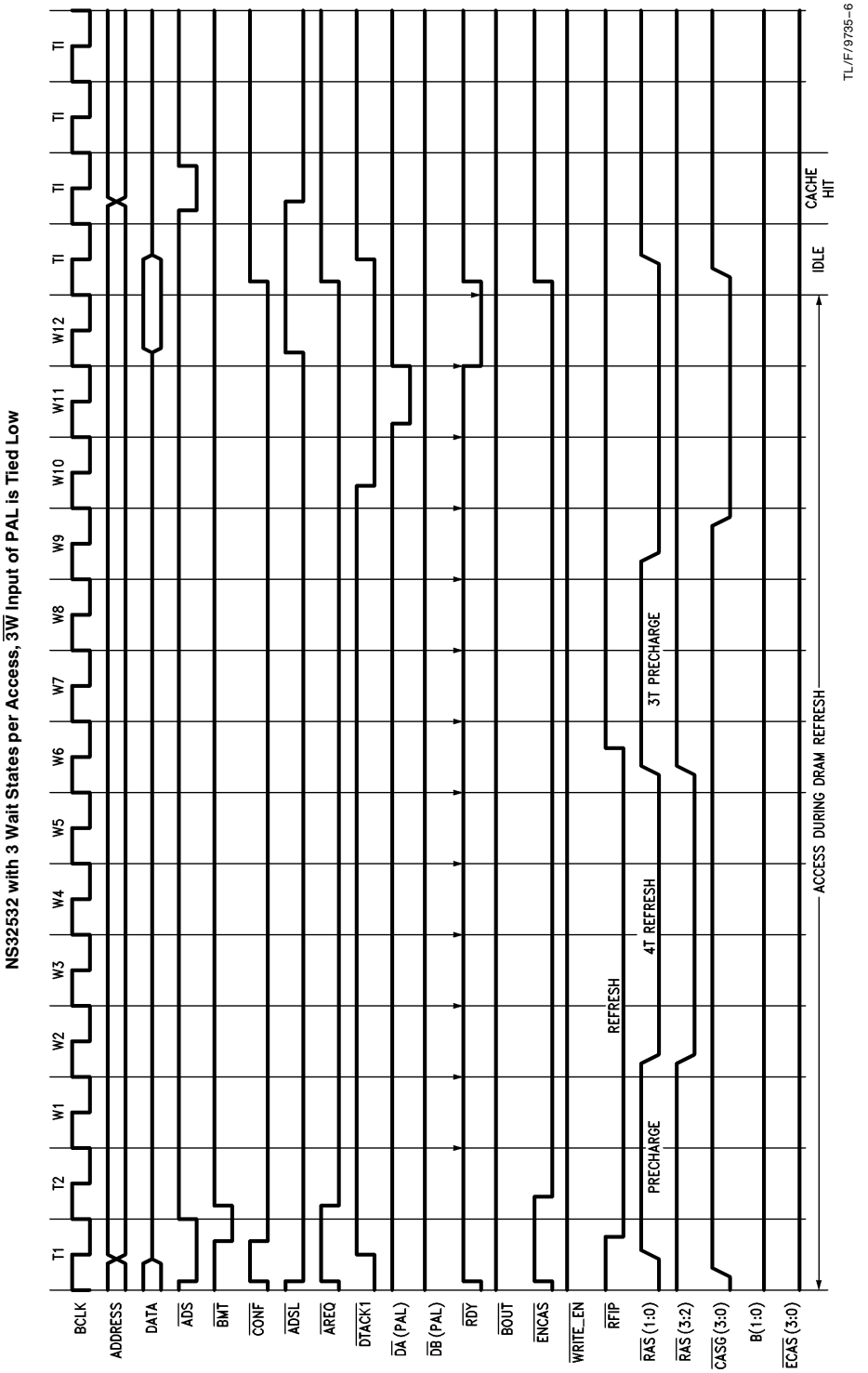
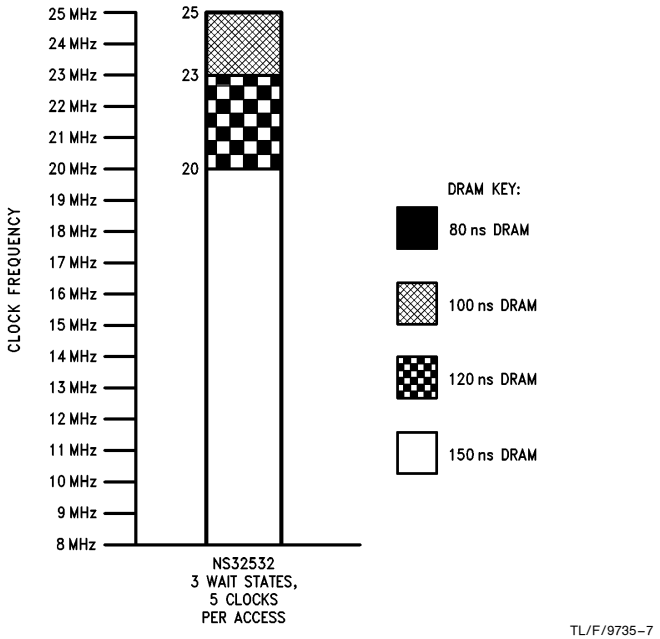
**NS32532 with 3 Wait States per Access, $\overline{3W}$ Input of PAL is Tied Low**



**DRAM Speed Vs. Processor Speed, (DRAM Speed References the RAS Access Time, $t_{RAC}$, of the DRAM, using DP8422A-25 Timing Specificatons)**

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