TP3200 MC-SLIC Application Guide

National Semiconductor
Application Note 439
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INTRODUCTION

In a Central Office or Private Branch Exchange, each subscriber's telephone line is interfaced to the switching equipment through a Subscriber Line Interface Circuit (SLIC) on the line card. To integrate the SLIC function has been a challenge for IC designers. The requirements for the SLIC function are very stringent in that they involve an environment of 48V battery feed and up to 150 Vrms of ringing voltage on the line, not to mention the ability to withstand 1500V lightning surges. Another particularly difficult problem to solve is the maintenance of a good longitudinal balance against common mode current induced by adjacent power cables.

Several implementations of an all-monolithic SLIC have been demonstrated, although they require a somewhat expensive high voltage process and involve tradeoffs in performance. A transformer-based SLIC, on the other hand, offers the most cost-effective and reliable solution for many applications.

The TP3200 and TP3204 Magnetic Compensation SLIC are intended to reduce both the size and cost of implementing the SLIC while retaining all the advantages of a transformer-based design. The MC-SLIC also provides on-chip supervision and ring trip functions together with three relay drivers with latched inputs.

This applications note provides line card designers with a thorough understanding of the device's operation as well as some application hints that are useful to the circuit designer.

Block diagrams illustrating the device architecture are shown in *Figure 1*. The TP3200 is designed with PNP relay drivers, while the TP3204 is designed with NPN relay drivers.

MAGNETIC COMPENSATION

The TP3200 family of MC-SLICs reduces the size of the line interface transformer by using a flux cancellation technique. The device senses the loop current magnitude by means of a differential amplifier A1 (see *Figure 2*) and an on-chip high precision sensing resistor bridge across the external feeding resistor pair Rs.

The output of the amplifier A1 produces a voltage proportional to the instantaneous loop current. And the low pass filter formed by R1 and external capacitor CAP1 prevents the AC component of the loop current from disturbing the

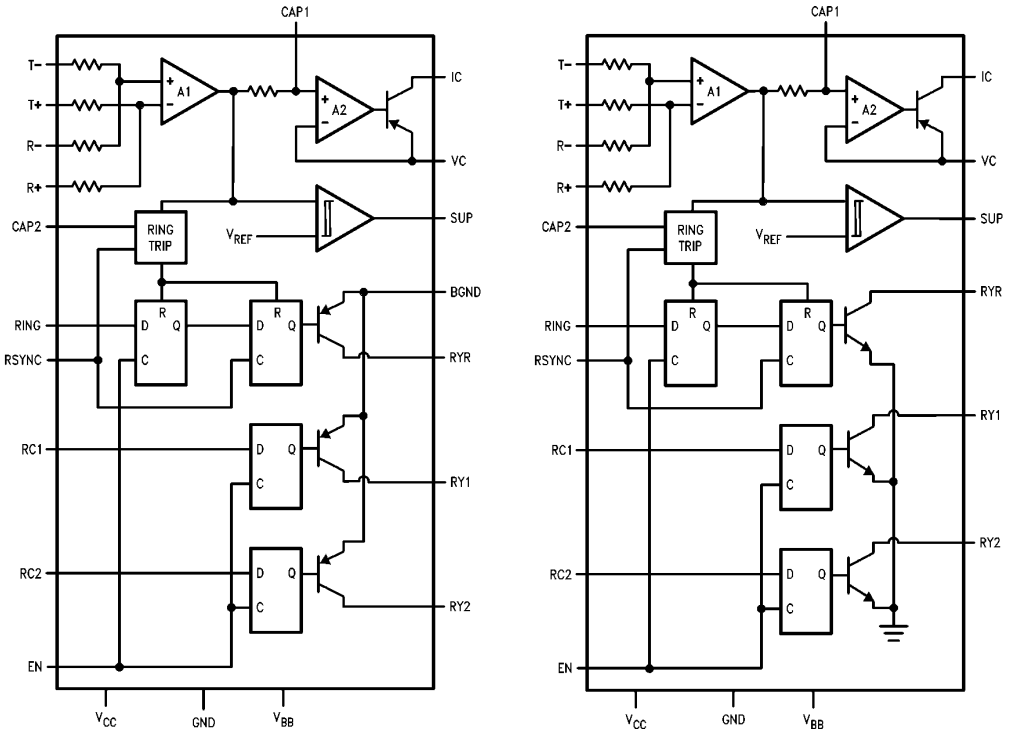

FIGURE 1. Simplified Block Diagram

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flux cancellation. For a typical CAP1 of 1 μF, the cutoff frequency is approximately 2 Hz.

The voltage follower A2 and output transistor Q1 reproduce a voltage at VC output, proportional to the average DC loop current. A resistor R_L connected from VC to GND creates a current flow from the IC pin into the compensation winding of the transformer. By proper selection of R_L and the transformer winding ratio, the flux created by the compensation current can exactly cancel the flux produced by the DC loop current. The output current source requires a high output impedance at IC (typically 5 MΩ) in order to ensure that the reflected impedance from the compensation winding to the line will not create a loading effect on the line impedance. The IC pin should be connected to the finish of the compensation winding in order to reduce the capacitive loading of the transformer, thereby, increasing the effective reflected impedance from the compensation winding. It is recommended to connect R_L and CAP1 to the same ground point in order to prevent ground noise from being injected into the subscriber loop via the compensation winding.

With the DC flux removed, the hybrid transformer can be wound on a small ferrite core without an air gap, yet can maintain a large inductance without running into magnetic saturation.

Figure 2 shows a simplified schematic of the magnetic compensation circuit and *Figure 3* is a plot of V_C versus the loop current.

Equations relating to the magnetic compensation circuit are:

$$V_C = A_V \times 2 \times R_S \times I_{LOOP} \quad (1)$$

$$I_C = V_C/R_L$$

$$= A_V \times 2 \times R_S \times I_{LOOP}/R_L \quad (2)$$

For perfect flux cancellation,

$$I_{LOOP} \times 2 \times N_P = I_C \times N_C$$

or,

$$R_L = A_V \times R_S \times N_C/N_P \quad (3)$$

The reflected impedance from the compensation winding is:

$$Z_C = R_{IC} \times (2N_P/N_C)^2$$

Where R_{IC} is the output impedance at IC.

The value of CAP1 is:

$$CAP1 = 1.6/f\ \mu F$$

Where f is the desired upper cutoff frequency.

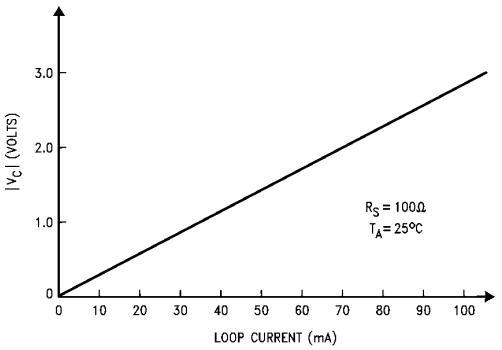

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FIGURE 3. V_C Output vs Loop Current

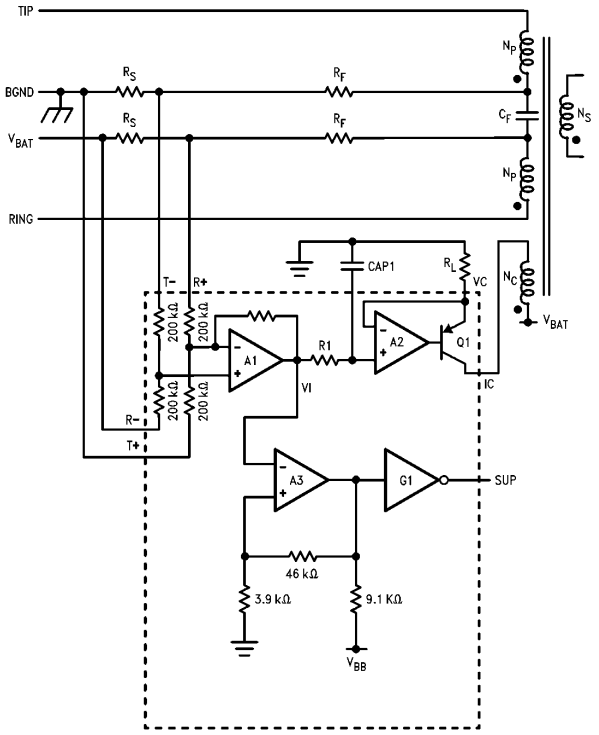

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FIGURE 2. Magnetic Compensation and Supervision Circuit

SUPERVISION

The supervision circuit of the TP3200 family consists of a loop current comparator with hysteresis. It provides status information on off-hook detection, dial pulse replication and ring-trip detection.

Referring back to *Figure 2*, the input to the comparator A3 is taken from the output of amplifier A1, which represents the instantaneous loop current. In the on-hook condition, the SUP output is at logic high. When the loop current rises above 13 mA, the SUP output switches low, indicating off-hook. When the loop current falls below approx. 11 mA, the SUP output will go high, indicating an on-hook condition. These comparator thresholds are selected so that in the extreme case of a very short loop, any possible cable leakage will not be misinterpreted as an off-hook. At the other extreme of a very long loop, there is enough safety margin for reliable detection of off-hook for very weak loop current of less than 15 mA.

During pulse dialing, the loop current changes from 0 mA during the break period and goes back to normal magnitude during the make period. The SUP output will produce a logic-replication of the dial pulses. However, under the worst case condition of a line loaded with 5 ringers, and with a cable leakage of 15 kΩ, the heavy capacitive loading of the ringers will cause excessive delay in loop current decay during break interval, creating dial pulse distortion. This results in shortening of the break period as reflected at the SUP output. *Figure 4* shows the relationship between SUP and the loop current under this condition.

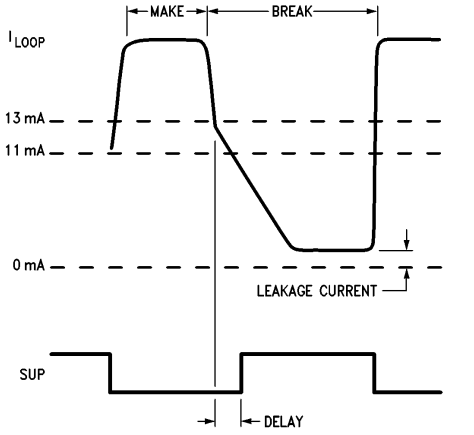

FIGURE 4. SUP Output Under 5 Ringers and 15 kΩ Cable Leakage

To repeat these dial pulses through the switching system, a software routine is recommended to be included in the call-control processor, which monitors the SUP output and reconstructs the dial pulses in the appropriate break-make ratio.

During ringing, the comparator A3 will detect the instantaneous AC ringing current through the loop and create a waveform at SUP output. During on-hook, the waveform is a square wave with a mark-to-space ratio of larger than 50%. When the telephone goes off-hook, the DC loop current superimposed on the AC ringing current will cause the comparator to generate a waveform with less than 50% duty cycle. This change in duty cycle can be easily monitored by the call-control processor as a test for ring-trip.

This is the most flexible way to detect ring-trip as it is independent of the ringing frequency. However, the CPU must be fast enough to make the detection within 200 mS.

AUTOMATIC RING-TRIP

The automatic ring-trip circuit consists of a ring-trip detection circuit and a double-latched ring relay driver. *Figure 5* shows a simplified schematic diagram.

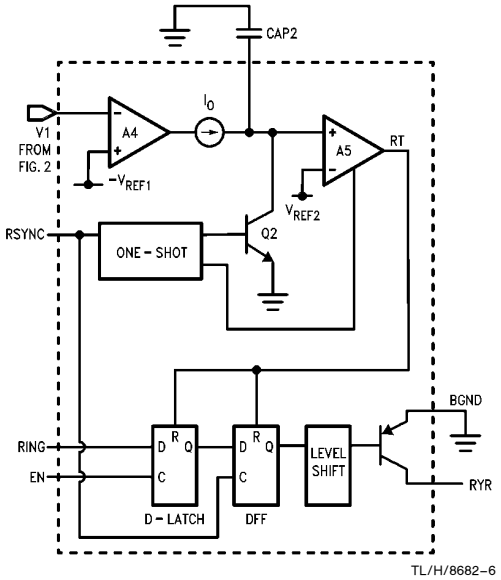

FIGURE 5. Automatic Ring-Trip Circuit

Based on the state of the RING input, the D-latch is set or reset while the strobe EN is active high, and latched on the falling edge of EN. RSYNC is the clock input to the ring flip-flop. It is driven by the output of the external zero-crossing detector of the ringing voltage on the line. Based upon the state of the output of the D-latch, the ring flip-flop is set or reset at the rising edge of RSYNC. This scheme ensures that the ring relay is turned on or off near the zero crossing of the ringing current to prevent arcing and minimize relay contact wear.

The ring-trip circuit takes its input from the output of amplifier A1, which represents the instantaneous AC ringing current superimposed on the DC off-hook loop current. The comparator A4 compares this instantaneous loop current against a threshold equivalent to approximately 12 mA. Depending upon the polarity of the comparator's output, the constant current source I_O either sources or sinks 10 μA into CAP2. This results in charging and then discharging CAP2 in each ring cycle. Depending on the duty cycle of the output from A4, this charging and discharging process creates a resultant voltage on CAP2 after one ringing cycle, which is then compared against a threshold of about 50 mV at comparator A5. When the DC loop current increases to above 12 mA, the duty cycle of the output of amplifier A4 is less than 50%. The resultant voltage at CAP2 after a

complete ring cycle then exceeds the 50 mV threshold. As a result, the A5 amplifier generates an output at the next rising edge of RSYNC, which resets the ring latches.

Each positive transition of RSYNC enables the comparator A5 for 20 μS via the one-shot circuit, after which CAP2 is discharged to GND for 100 μS via Q2 to ensure that CAP2 always charges up from 0V. The reset pulse from A5 will always appear at the rising edge of RSYNC to ensure that the ring relay is reset at the zero-crossing of the ringing current. *Figure 6* shows the timing diagram for ring-trip.

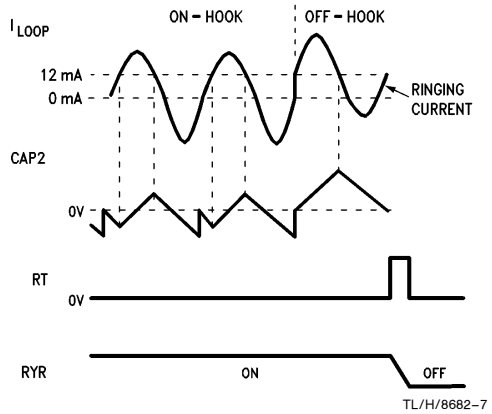

FIGURE 6. Timing Diagram for Ring-Trip

CAP2 is selected such that the constant current source I_O (approx. 10 μA) when integrated over half of one ringing cycle, will not create a charging voltage at CAP2 exceeding ±3V. A 0.1 μF is recommended for ringing frequency range of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz.

The automatic ring-trip circuit provides a reliable ring-trip detection. Normally, one ring cycle is needed for detection, and the second ring cycle to generate the reset pulse. The worst case ring-trip detection time will be within 3 ringing cycles. If the SUP output is used to detect ring-trip externally, the input at CAP2 should be grounded.

The RING or EN inputs should be kept at logic low after the ring relay is turned on in order to prevent relay chattering when the loop current is near to the 12 mA threshold. This is the condition where the automatic ring-trip tries to turn off the ring relay and the RING and EN inputs try to turn it on again. This results in relay chattering which may cause damage to the relay.

COMPENSATION ACCURACY

The accuracy of flux cancellation is one of the critical factors determining the size of the hybrid transformer. On chip Si-chrome resistors are used for the sensing resistor bridge to ensure high accuracy in loop current tracking. The offset voltage at V_C is zener trimmed to within 30 mV to further minimize the compensation error.

The tolerances of resistors R_S and R_L also contribute to compensation error. The feeding resistors R_S, however, are normally matched to each other to within ±0.1%, as are feeding resistors R_F, to ensure 60 dB longitudinal balance.

The following table shows a list of parameters that contribute to compensation errors:

Parameter	Typical	Tolerance
A_V	0.15 V/V	2%
V_{OS}	0	30 mV
R_S	100Ω	0.1%
R_L	150Ω	0.5%
N_C/N_P	10	0.05%

From Equation 2 above, the compensation error can be derived as follows:

$$\begin{aligned}\text{Compensation Error} &= I_{LOOP} - I_C \times N_C/2N_P \\ &= I_{LOOP} - (N_C/2N_P) \times (A_V \times 2R_S \times I_{LOOP} \pm V_{OS})/R_L \\ &= (1 - N_C/N_P \times A_V \times R_S/R_L) \times I_{LOOP} \pm V_{OS}/R_L \\ &= \pm(0.026 \times I_{LOOP} + 0.2)\ \text{mA} \qquad (4)\end{aligned}$$

For a maximum loop current of 100 mA for Central Office application, the worst case compensation error is ±2.8 mA. For a maximum loop current of 60 mA for PBX application, the worst case compensation error is ±1.8 mA. The ferrite material of the hybrid transformer must be able to handle this uncompensated DC current before magnetic saturation starts.

TRANSFORMER DESIGN

The size and design of the hybrid transformer is influenced by the following factors:

1. Low frequency Return Loss, which in turn determines the minimum inductance of the primary windings.
2. The worst case compensation error, which determines the ampere-turn before magnetic saturation occurs.
3. The permeability and magnetization characteristics of the ferrite material.
4. Insertion loss and frequency response.

Figure 7 shows a simplified equivalent circuit for a hybrid transformer. r_p and r_s are the coil resistance of the primary and secondary windings. R_T and C_T are the terminating impedances of the secondary winding, and L is the total primary inductance. As the compensation winding is driven by a high impedance current source, it can be ignored from the equivalent circuit.

The return loss against a reference impedance Z_O can be calculated from the equation:

$$\text{Return Loss} = 20 \log \left| \frac{Z_I + Z_O}{Z_I - Z_O} \right|$$

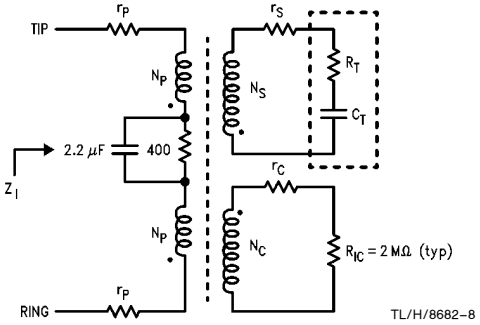

FIGURE 7. Simplified Equivalent Circuit of Hybrid Transformer

Figure 8 is a plot of return loss against a reference impedance of 600Ω + 2.16 μF. To achieve a 20 dB return loss, it can be seen from the plot that it requires a primary inductance of more than 0.8H even under the worst case compensation error of 2.8 mA. An acceptable ferrite is Siemens RM8-T35 ferrite core with a typical inductance factor of 8400 nH/T^2. Following a similar calculation, it can be found that it requires a minimum primary inductance of 1.4H in order to achieve a 20 dB return loss against a reference impedance of 900Ω + 2.16 μF. A suitable ferrite is Siemens RM10-T35 ferrite core with a typical inductance factor of 11000 nH/T^2.

To ensure a 60 dB longitudinal balance, the two primary windings must be carefully wound for symmetry. Usually this is done by winding the two primary windings with bifilar wires of the same gauge. Furthermore, to prevent heating up the ferrite core on a short loop, the primary resistance has to be kept to a minimum and is recommended to be below 30Ω.

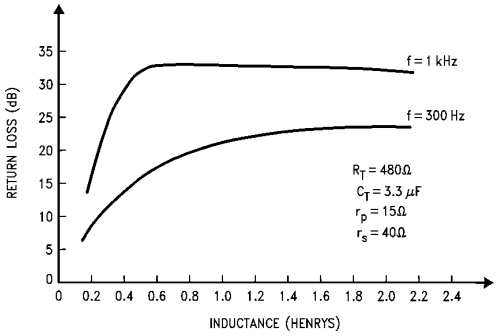

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FIGURE 8. Return Loss Against 600Ω + 2.16 μF

OUTPUT BIASING

The AC signal voltage across the subscriber loop will appear at the IC output and is amplified by the turns ratio $N_C/2N_P$. A suitable DC bias voltage must be provided for the compensation winding to ensure sufficient swing for the AC signals.

At minimum loop current (see *Figure 9a*), the DC bias at IC must be sufficiently positive with respect to the zener voltage to allow the peak negative swing without clipping. Thus:

$$I_{CMIN} \times (R_C + r_C) > N \times V_P - (V_{ZMIN} - |V_{BAT}|_{MAX})$$

or,

$$(R_C + r_C) \times I_{LOOPMIN}/N > N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX} \quad (5)$$

Where, V_{ZMIN} is the minimum zener voltage at IC

V_{BATMAX} is the maximum battery voltage

R_C is the filtering resistor for the compensation winding

r_C is the coil resistance of the compensation winding

N is the transformer turn ratio $N_C/2N_P$

V_P is the AC peak voltage swing across Tip and Ring

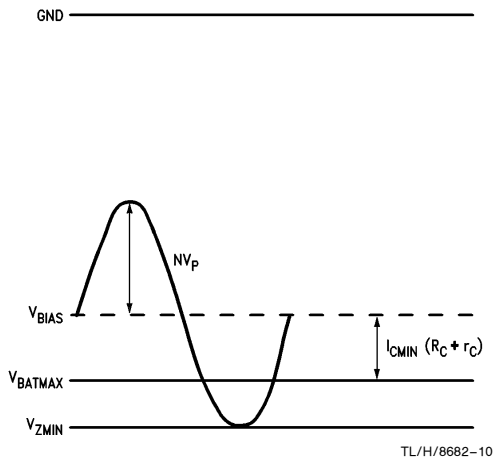

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FIGURE 9a. IC At Minimum Loop Current

At the other extreme with maximum loop current (see *Figure 9b*), the output transistor must not be saturated at the positive peak swing at IC. This requires:

$$|V_{BAT}|_{MIN} > I_{CMAX} \times (R_C + r_C) + V_{CMAX} + |V_{ICSAT}| + N \times V_P$$
$$> (R_C + r_C)\, I_{LOOPMAX}/N + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P \quad (6)$$

Substituting for (R_C + r_C) from equation 5:

$$|V_{BAT}|_{MIN} > (N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX}) \times I_{LOOPMAX}/I_{LOOPMIN} + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P$$

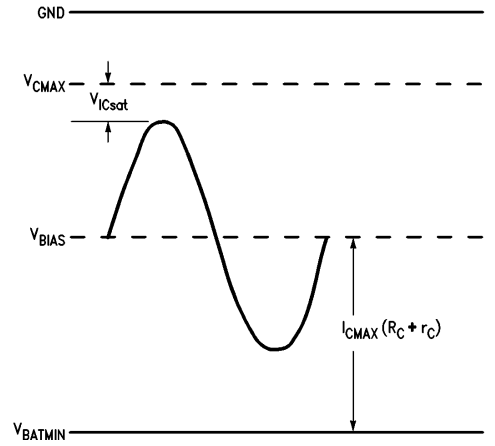

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FIGURE 9b. IC At Maximum Loop Current

The maximum current range of IC of 25 mA places a constraint on the minimum compensation to primary turn-ratio of the transformer.

$$N = N_C/2N_P$$
$$= I_{LOOP}/I_C$$

Thus,

$$N_{MIN} = I_{LOOPMAX}/25 \quad (7)$$

To allow for a +3 dBm line signal over loop current from 20 mA to 100 mA, with a zener voltage of 62V ±5%, and battery voltage of −42V to −54V, the compensation turns ratio and total resistance ($R_C + r_C$) can be calculated from the above equations and is shown in the following table:

	Line Impedance	
	600Ω	**900Ω**
Minimum N	4.0	4.0
Maximum N	6.67	5.45
Minimum ($R_C + r_C$) for N = 5	712.5Ω	1143.8Ω
Maximum ($R_C + r_C$) for N = 5	1487.5Ω	1401.3Ω

INPUT COMMON MODE RANGE

Consideration should be given to the various subscriber line voltages and currents, such that the magnetic compensation circuitry only operates within its dynamic range.

The A1 amplifier's differential input is biased using negative feedback so that it works within the range of $V_{BB} + 0.5V$ to $V_{CC} - 1V$, where $V_{CC} = +5V \pm 5\%$, and $V_{BB} = -5V \pm 5\%$. The input common mode voltage V_{IN} is given by the following expression:

$$V_{IN} = 0.0155 \times (V_{BAT} + V_R \sin wt + 2R_S \times I_{CM}) - 0.05R_S \times (I_{LOOP} + I_R \sin (wt + A)) \quad (8)$$

where, V_{BAT} is the battery voltage

I_{LOOP} is the DC loop current

V_R is the peak ringing voltage

I_R is the peak ringing current

I_{CM} is the peak longitudinal current of arbitrary phase

It should be noted that for short subscriber loops, the component of voltage at V_{IN} due to the ringing current is in antiphase to the ringing voltage. For longer loops, the phase angle A between the ringing voltage and the ringing current increases. Thus the resulting voltage for V_{IN} will be a vector summation. Under the latter condition, however, the subscriber loop resistance is greater, which will reduce I_{LOOP} and I_R, and consequently reduce their influence on V_{IN}.

As an example, consider an application with $V_{BAT} = -48V$, $V_R = 110V$ rms at 60 Hz, $I_{LOOP} = 100$ mA, $I_{CM} = 30$ mA peak, and a ringer impedance of 2 kΩ + 4.7 μF. During on-hook ringing, the voltage swing at V_{IN} can be derived from equation (8) as follows:

$$-2.93V < V_{IN} < 1.45V$$

When the telephone goes off-hook, and at the point before ring trip, the voltage swing at V_{IN} becomes :

$$-2.86V < V_{IN} < 0.38V$$

This reduction in voltage swing is due to the small phase angle A and the increase of AC ringing current.

OVER-VOLTAGE PROTECTION

The TP3200 family has been designed on a standard 70V bipolar process requiring no expensive dielectric isolation. In fact, any possible line transient voltage is scaled down through the feeding resistors R_S and R_F, insuring that the device will never see more than one half of the line transient. However, to prevent excessively high transient voltage induced by lightning or from nearby power cables, it is essential to provide some protective device across Tip and Ring. It is recommended to put a 10Ω current-limit resistor and a 300V peak transient suppressor from Tip to GND and from Ring to GND.

Moreover, any transient voltage on the line will also be reflected into the compensation winding as well as the secondary winding. Such a transient in the compensation winding is especially significant as it is boosted up by the turns ratio $N_C/2N_P$. A fast acting 62V zener diode is necessary to connect from IC output to GND for protection. On the secondary winding, two 3.9V zener diodes connected back-to-back will insure the COMBO will never see any transient voltage exceeding its supply voltages.

The on-chip relay driver has been designed to sink 30 mA for TP3200 and 80 mA for TP3204. When the relay is turned off, the back emf in the coil winding may possibly cause damage to the output driver. Each relay driver should be protected by a rectifier diode connected close to the relay coil in order to dissipate the stored energy in the coil.

A TYPICAL LINE CIRCUIT APPLICATION

Figure 10 shows a typical line circuit design using a TP3071 COMBO II™ device to perform the CODEC and filtering functions. To provide a +3.17 dBm overload level on the telephone line (0TLP) from the VF_RO receive output, a transformer with 600Ω secondary winding is used along with a series 600Ω terminating resistor. The COMBO II device has an internal programmable hybrid balance network for cancelling the echo. No external balance network components are needed. The SLIC control inputs (EN, RC2, RC1 and RING) are handled via the COMBO II Interface I/O latches, as is the line supervision output. These latches are individually programmable as inputs or outputs. Programming of the COMBO II I/O latches, hybrid balance network, transmit and receive gains, etc. is accomplished via a three pin serial microcomputer bus. The Control Clock (CCLK) and Control Input/Output (CI/O) pins are bussed to all COMBO II devices on the line card. A separate Chip Select ($\overline{CS}$) line is used for each COMBO II.

Ring voltage is applied to the line by breaking the battery feed path and superimposing the AC ring voltage via a 4-pole relay driven from the SLIC RYR output. Normally open contacts short the transformer primary windings when the ring voltage is applied to prevent attenuation and distortion of the ring signal and generation of large transients in the secondary and magnetic compensation windings due to core saturation by the 20 Hz ring current. Also a normally closed contact, in series with 2.2 μF capicator, opens when ringing is applied to prevent shunting the ring current. The two SLIC general purpose relay driver outputs, RY1 and RY2, are used to drive 2-pole battery reversal and test relays.

For additional information on design of a suitable zero crossing detector, see NATIONAL semiconductor Linear Application Note AN-74.

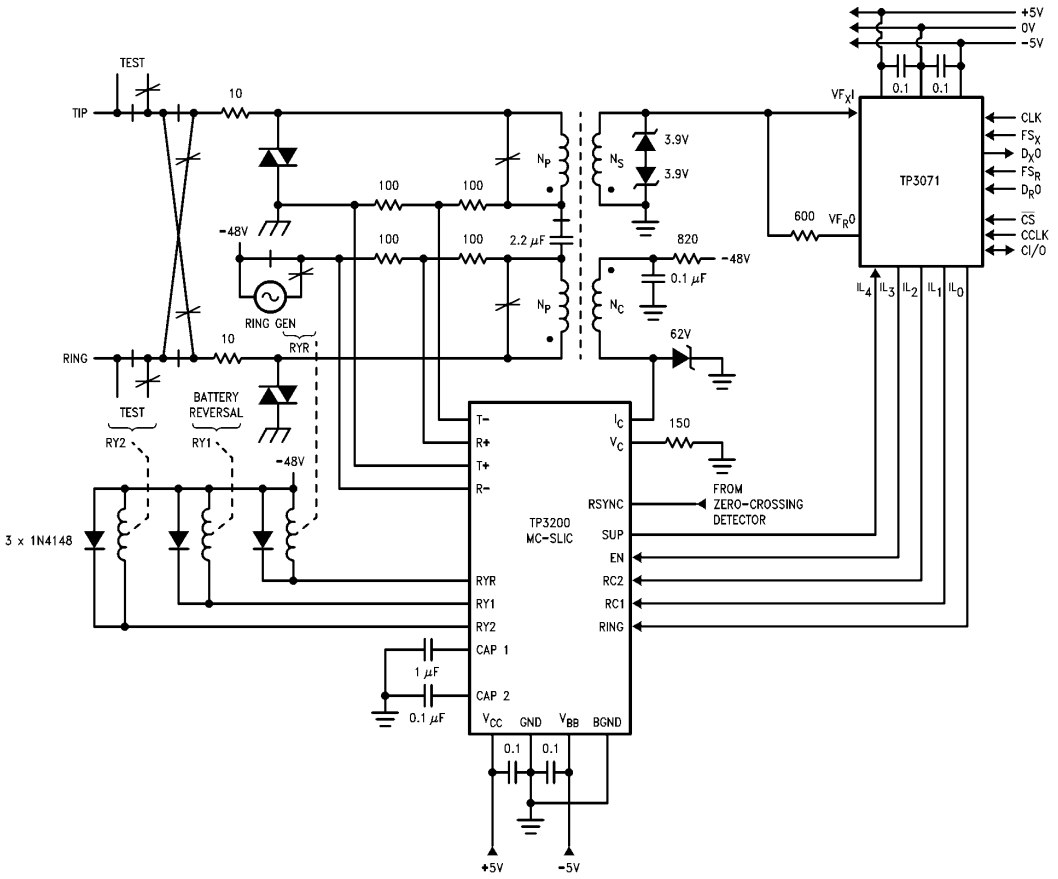

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FIGURE 10. A Typical Line Circuit Application

APPENDIX A: Transformer Specification for 600Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	210 T,	AWG #36
Np2:	Start 12,	end 1,	210 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2100T,	AWG #42

2. Ferrite Core

   Siemens RM8-T35 or equivalent

   AL = 8400 nH/T^2 +30/−20%

3. DC Resistance

   Np1: 15Ω max

   Np2: 15Ω max

   Ns : 45Ω max

   Nc : 650Ω max

4. Inductance

   (total primary inductance with Np1 and Np2 in series aiding)

   1.5 H typical at 0 mA primary current

   0.7 H min at 3 mA DC primary current

5. Impedance: 600Ω to 600Ω

6. Frequency response

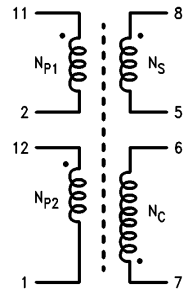
   ±0.5 dB reference to 1 kHz, 300–3500 Hz

7. Longitudinal Balance

   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded

8. Dielectric

   1500 Vrms from primary to any other conductors



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APPENDIX B: Transformer Specification for 900Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	255 T,	AWG #36
Np2:	Start 12,	end 1,	255 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2550T,	AWG #41

2. Ferrite Core

   Siemens RM10-T35 or equivalent

   AL = 11000 nH/T^2 +30/−20%

3. DC Resistance

   Np1 : 20Ω max

   Np2 : 20Ω max

   Ns : 55Ω max

   Nc : 800Ω max

4. Inductance

   (total primary inductance with Np1 and Np2 in series aiding)

   2.5 H typical at 0 mA DC primary current

   1.3 H min at 3 mA DC primary current

5. Impedance: 900Ω to 600Ω

6. Frequency response

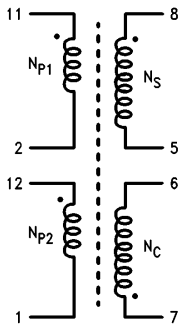
   ±0.5 dB reference to 1 kHz, 300–3500 Hz

7. Longitudinal Balance

   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded

8. Dielectric

   1500 Vrms from primary to any other conductors



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APPENDIX C: Transformer Specification for a Center Tap Transformer

1. Turns Ratio

Np1:	Start 1,	End 4,	175 T
Np2:	Start 3,	End 6,	175 T
Ns1:	Start 12,	End 11,	175 T
Ns2:	Start 11,	End 9,	175 T
Nc :	Start 10,	End 7,	1750T

2. Wire Gauge

   Np1, Np2 wound by Bifilar wires, 0.125 mm
   Ns1, Ns2 wound by Bifilar wires, 0.125 mm
   Nc wound by 0.06 mm wires

3. Ferrite Core

   Siemens RM8-T38 or equivalent,
   $A_L = 12500\ nH/T^2\ +30/-40\%$

4. Resistance matching of coils

   Np1 to Np2: 1% max
   Ns1 to Ns2: 1% max

5. Inductance

   (total primary inductance with Np1 and Np2 in series aiding)
   0.8H min at 3 mA DC primary current. f = 300 Hz.

6. High Voltage Isolation

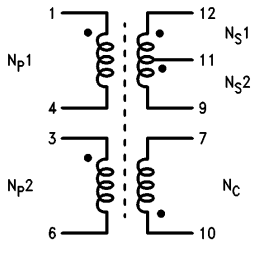
   1500V between all coils

7. Suggested Vendors

   Ferroglen Research Ltd.
   20 Tanfield Road
   Croyden Surrey
   CRO 1 AL

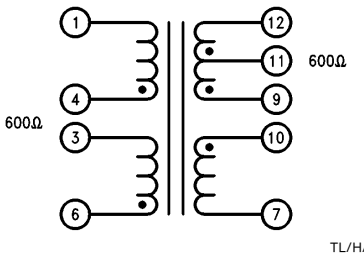
   or

   Gardners Transformers Ltd.
   Christchurch
   Dorset
   BH23 3PN



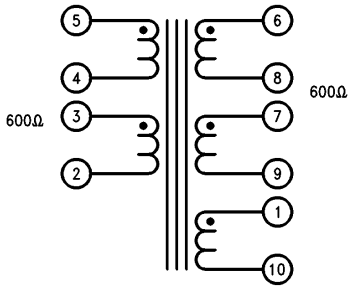
TL/H/8682–17

APPENDIX D: Other Transformers Available with Magnetic Compensation Winding



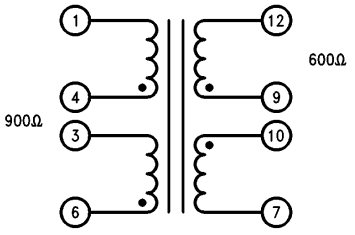
TL/H/8682–18

P/N 671-8500
Ferrite Core



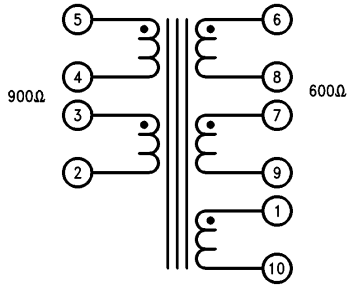
TL/H/8682–19

P/N 671-8501
Laminated Core



TL/H/8682–20

P/N 671-8503
Ferrite Core



TL/H/8682–21

P/N 671-8504
Laminated Core

For Complete Specifications, Contact:
MIDCOM, INC.
P.O. Box 1330
121 Airport Drive
Watertown, SD 57201-6330
Phone (605) 886-4385
Fax (605) 886-4486
Hotline 1-800-MIDCOM1

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