Read Data Processor

GENERAL DESCRIPTION

The ML541 is a monolithic bipolar integrated circuit for use in a disk drive system to detect analog pulse peaks generated by the recording head during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator for further processing. It contains both analog and digital circuitry and supports the reading of MFM and RLL encoded data at rates up to 15 megabits/second.

The primary functional blocks within the device include an AGC amplifier, a level detector, a slope detector, and output logic. Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's ouput during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

By using both level and slope detection, accurate pulse validation and peak time detection is acheived. The ML541 performance can be adjusted to fit particular needs through external component selection.

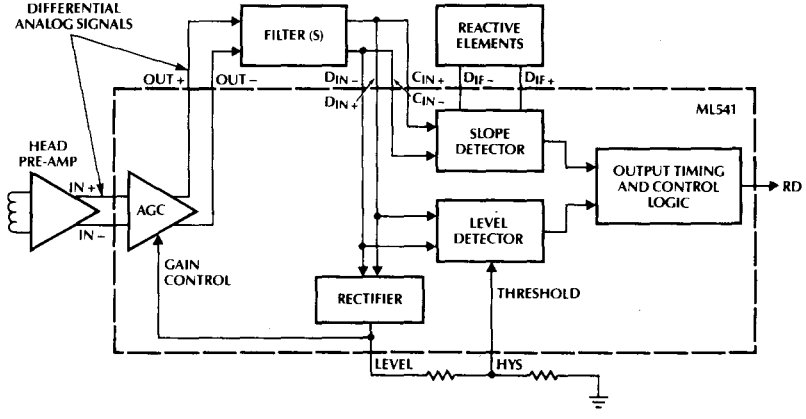
The ML541 is available both in a 24-pin PDIP and 28-pin PCC.

FEATURES

- Second source for SSI 541
- Data rates up to 15 megabits/second
- Supports MFM and RLL encoded read data
- 25MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- Write to read transient suppression
- Supports embedded servo decoding
- +5V, +12V power supplies

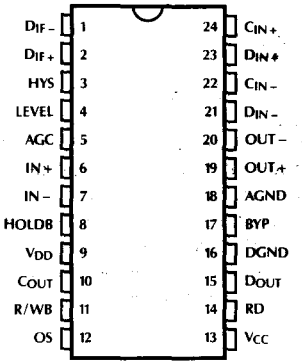
5

SIMPLIFIED BLOCK DIAGRAM



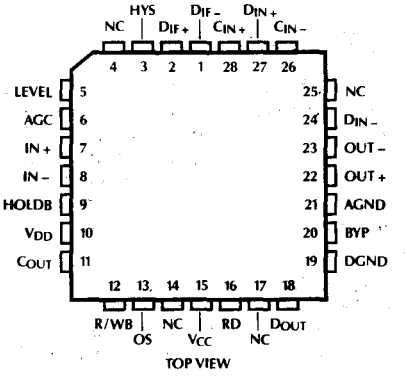
PIN CONNECTIONS

24-Pin DIP and SOIC Package



TOP VIEW

28-Pin PCC Package



TOP VIEW

PIN DESCRIPTION

NAME	FUNCTION
V_{CC}	+5V
V_{DD}	+12V
AGND	Analog Ground.
DGND	Digital Ground.
R/WB	TTL compatible Read/Write Control pin.
IN+, IN–	Analog Signal Input pins
OUT+, OUT–	AGC Amplifier Output pins
BYP	The AGC timing capacitor C_{AGC} is tied between this pin and AGND.
HOLDB	TTL compatible pin that holds the AGC gain when pulled low.
AGC	Reference input voltage level for the AGC circuit.
D_{IN+}, D_{IN-}	Analog input to the hysteresis comparator.

NAME	FUNCTION
HYS	Input for setting hysteresis level of the hysteresis comparator.
LEVEL	Provides rectified signal level for input to the hysteresis comparator.
D_{OUT}	Buffered test point for monitoring D input of the flip-flop.
C_{IN+}, C_{IN-}	Analog input to the differentiator.
D_{IF+}, D_{IF-}	External differentiating network connection pins.
C_{OUT}	Buffered test point for monitoring the clock input to the flip-flop.
OS	Connection for read output pulse width setting capacitor C_{OS}.
RD	TTL compatible read output.

TABLE 1 MODE SELECT

R/WB	HOLDB	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low
1 = Logic level high
X = Don't care

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Power Supply Voltage Range
- V_{CC} ..... −0.3 to 6 V_{DC}
- V_{DD} ..... −0.3 to 14 V_{DC}

Terminal Voltage Range
- R/WB, IN+, IN−, HOLDB ..... −0.3 V to V_{CC} +0.3 V
- RD ..... −0.3 V to V_{CC} +0.3 V or +12 mA
- All others ..... −0.3 V to V_{DD} +0.3 V

Storage Temperature Range ..... −65°C to +150°C
Junction Temperature (T_J) ..... +135°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

OPERATING CONDITIONS

Supply Voltage
- V_{CC} ..... 5 V ± 10%
- V_{DD} ..... 12 V ± 10%

$V_{(C_{IN+}-C_{IN-})}$, $V_{(D_{IN+}-D_{IN-})}$ ..... $1V_{P-P}$
V_{HYS} ..... 1.0 V
C_{OS} ..... 50 to 200 pF

Typical Component Values (Refer to Typical Applications)
- C_{IN} ..... 0.001 µF
- C_S ..... 0.01 µF
- C_{OUT} ..... 0.0047 µF
- R_{OUT} ..... 400 Ω
- C_{AGC1} ..... 220 pF
- C_{AGC2} ..... 2000 pF
- R_{AGC} ..... 2.21 kΩ
- C_{LEVEL} ..... 150 pF
- R_{LEVEL1} ..... 1.54 kΩ
- R_{LEVEL2} ..... 6.49 kΩ
- C_{OS} ..... 50 pF

ELECTRICAL CHARACTERISTICS

The following specifications apply over the recommended operating conditions of V_{CC} = 5 V ± 10%, V_{DD} = 12 V ± 10%, 0°C < T_A < 70°C and external components as specified under recommended operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
DC Characteristics						
I_{CC}	V_{CC} Supply Current	Outputs unloaded			14	mA
I_{DD}	V_{DD} Supply Current	Outputs unloaded			70	mA
P_D	Power Dissipation	Outputs unloaded, T_A = 70°C			930	mW
Digital Inputs Characteristics (HOLDB, R/WB)						
V_{IH}	High Voltage		2			V
V_{IL}	Low Voltage				0.8	V
I_{IH}	High Current	V_{IH} = 2.4 V			100	µA
I_{IL}	Low Current	V_{IL} = 0.4 V	−0.4			mA
Digital Outputs Characteristics (C_{OUT}, RD)						
V_{OL}	Output Low Voltage	I_{OL} = 4 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 400 µA	2.4			V
WRITE AND HOLD MODE CHARACTERISTICS						
Mode Control						
t_{RW}	Read to Write Transition Time				1	µs
t_{WR}	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	µs
t_{RH}	Read to Hold Transition Time				1	µs
Write Mode						
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
READ MODE CHARACTERISICS						
AGC Amplifier						
R_{ID}	Differential Input Resistance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz		5		kΩ
C_{ID}	Differential Input Capacitance	$V_{(IN+-IN-)} = 100mV_{P-P}$ @ 2.5MHz			10	pF
Z_{IC}	Common Mode Input Impedance (both sides)	R/WB pin high		1.8		kΩ
		R/WB pin low		0.25		kΩ
A_{VR}	Gain Range	$1V_{P-P} \leq V_{OUT\ diff} < 2.5V_{P-P}$	4		83	V/V
e_N	Input Noise Voltage	Gain set to maximum			30	nV/ $\sqrt{Hz}$
BW	Bandwidth	Gain set to maximum, −3dB point	25			MHz
V_{OP}	Maximum Output Voltage Swing	Set by V_{AGC}	3			V_{P-P}
I_{OD}	OUT+ to OUT− Pin Current	No DC path to GND, See Note 3	±3.2			mA
R_O	Output Resistance			20	30	Ω
C_O	Output Capacitance			12		pF
V_{IP} V_{AGC}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing VS AGC Input Level	$30mV_{P-P} \leq V_{(IN+-IN-)} \leq 550mV_{P-P}$, $1.5V \leq V_{AGC} \leq 3.75V$		0.48		V_{P-P}/V
V_{IP}	$(D_{IN+} - D_{IN-})$ Input Voltage Swing Variation	$30mV_{P-P} < V_{(IN+-IN-)} < 550mV_{P-P}$, AGC Fixed, over supply and temp.			+8	%
t_D	Gain Decay Time	See Figure 1a; $V_{IN} = 300mV_{P-P}$ then $>150mV_{P-P}$ at 2.5MHz, V_{OUT} to 90% of final value.		50		µs
t_A	Gain Attack Time	See Figure 1b; from Write to Read transition to V_{OUT} at 110% of final value, $V_{IN} = 400mV_{P-P}$ @ 2.5MHz		4		µs
I_{AGCfc}	Fast AGC Capacitor Charge Current	$V_{(D_{IN+} - D_{IN-})} = 1.6V$, $V_{AGC} = 3.0V$		1.5		mA
I_{AGCsc}	Slow AGC Capacitor Charge Current	$V_{(D_{IN+} - D_{IN-})} = 1.6V$, Vary V_{AGC} until slow discharge begins		0.17		mA
	Fast to Slow Attack Switchover Point	$V_{(D_{IN+} - D_{IN-})}$		1.25		-
		$V_{(D_{IN+} - D_{IN-})}$ Final				
I_{AGCD}	AGC Capacitor Discharge Current	$V_{(D_{IN+} - D_{IN-})} = 0.0V$ Read Mode		4.5		µA
		Hold Mode	−0.2		+0.2	µA
CMRR	CMRR (Input Referred)	$V_{IN+} = V_{IN-} = 100mV_{P-P}$ @ 5MHz, gain at max.	40			dB
PSRR	PSRR (Input Referred)	V_{CC} or $V_{DD} = 100mV_{P-P}$ @ 5MHz, gain at max.	30			dB
Hysteresis Comparator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(D_{IN+} - D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(D_{IN+} - D_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6.0	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
V_{IO}	Comparator Offset Voltage	HYS pin at −0.5V, ≤1.5kΩ across D_{IN+}, D_{IN-}		5		mV

ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, IN+ and IN− AC coupled, OUT+ and OUT− differentially loaded with >600Ω and each side loaded with <10pF to GND, $C_{BYP} = 2000pF$, OUT+ and OUT− AC coupled to D_{IN+} and D_{IN-} respectively, $V_{AGC} = 2.2V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
READ MODE CHARACTERISICS (Continued)						
Hysteresis Comparator (Continued)						
V_{HYSP} V_{HYS}	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V < V_{HYS} < 3V$		0.21		V/V
I_I	HYS Pin Input Current	$1V < V_{HYS} < 3V$	0		−20	µA
I_O	LEVEL Pin Max Output Current		3			mA
R_O	LEVEL Pin Output Resistance	$I_{LEVEL} = 0.5mA$		180		Ω
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A = 70°C$	$V_{DD}-4.0$		$V_{DD}-2.5$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A = 70°C$	$V_{DD}-2.2$		$V_{DD}-1.5$	V
V_{OL}	D_{OUT} Pin Output Low Voltage	$T_A = 25°C$	$V_{DD}-4.0$		$V_{DD}-2.8$	V
V_{OH}	D_{OUT} Pin Output High Voltage	$T_A = 25°C$	$V_{DD}-2.5$		$V_{DD}-1.6$	V
Active Differentiator						
V_{IP}	Input Signal Range				1.5	V_{P-P}
R_{ID}	Differential Input Resistance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz	5		15	kΩ
C_{ID}	Differential Input Capacitance	$V_{(C_{IN+}-C_{IN-})} = 100mV_{P-P}$ @ 2.5MHz			6	pF
Z_{IC}	Common Mode Input Impedance	(both sides)		2.0		kΩ
I_{OD}	D_{IF+} to D_{IF-} Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	±1.3			mA
V_{IO}	Comparator Offset Voltage	D_{IF+}, D_{IF-} AC Coupled		5		mV
V_{OL}	C_{OUT} Pin Output Low Voltage	$0 \leq I_{OH} \leq 0.5mA$		$V_{DD}-3$		V
V_{PO}	C_{OUT} Pin Output Pulse Voltage	$0 \leq I_{OH} \leq 0.5mA$		0.4		V
PW_0	C_{OUT} Pin Output Pulse Width	$0 \leq I_{OH} \leq 0.5mA$		30		ns

The following specifications apply over the recommended operating conditions of $V_{CC} = 5V \pm 10\%$, $V_{DD} = 12V \pm 10\%$, $0°C \leq T_A \leq 70°C$, $V_{(C_{IN+}-C_{IN-})} = V_{(D_{IN+}-D_{IN-})} = 1.0V_{P-P}$ AC coupled sine wave at 2.5MHz, $R_{D_{IF}} = 100Ω$, $C_{D_{IF}} = 65pF$, $V_{HYS} = 1.8V$, $C_{OS} = 60pF$, 4kΩ to V_{CC} and 10pF to GND on pin RD unless otherwise specified.

Output Data Characteristics (Refer to Figure 2)						
t_{D1}	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+}-D_{IN-})}$ exceeding threshold to $V_{(D_{IF+}-D_{IF-})}$ reaching a peak	0			ns
t_{D3}	Propagation Delay				110	ns
t_{D5}	Output Data Pulse Width	$T_A = 25°C$, $V_{CC} = 5V$, $V_{DD} = 12V$		±15%		
t_{D5}	Output Data Pulse Width Variation	$C_{OS} = 60pF$, See Note 4	30		80	ns
t_{D3}-t_{D4}	Logic Skew (Pulse Pairing)				3	ns
t_R	Output Rise Time	$V_{OH} = 2.4V$			18	ns
t_F	Output Fall Time	$V_{OL} = 0.4V$			14	ns

Note 1: Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

Note 2: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 3: AGC amplifier output current may be increased as in Figure 4.

Note 4: $t_{D5} \cong 770\ (C_{OS})$, $50pF < C_{OS} < 150pF$.

Note 5: Typicals are parametric norm at 25°C

FUNCTIONAL DESCRIPTION

Operating Modes

The ML541 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins HOLDB and R/WB as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level V_{OUT} from the AGC amp is determined by voltage V_{AGC} present at pin AGC. V_{OUT} is full wave rectified and compared against V_{AGC} to create charge/discharge current for capacitor C_{BYP} connected at pin BYP. Voltage V_{BYP} across C_{BYP} controls the gain in the AGC amplifier.

Two distinct values of I_{BYP} are possible which determine a fast and slow AGC gain response attack rate. When V_{OUT} is more than 125% of the set level a high value of I_{BYP} is sourced which provides a fast AGC attack rate. When V_{OUT} is within 100% to 125% of the set level a reduced value of I_{BYP} is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range. V_{AGC} should be set so that the differential input voltage V_{DIN} into the level comparator is $1V_{P-P}$ at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where: A_{V1}, A_{V2} are initial and final amplifier gain values corresponding to initial and final V_{BYP} values.

$V_T = (KT)/Q = 26\,mV$ at room temperature.

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

AGC Amp During Write Mode — When the ML541 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

AGC Amp During Hold Mode — During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor C_{AGC} will then hold the present gain setting. The amplitude of V_{OUT} will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents loosing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs D_{IF-} and D_{IF+}, as shown in the typical application.

External Filter Network

Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

Level Detector

The full wave rectified V_{OUT} is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage V_{LEVEL} output from pin LEVEL. Using V_{LEVEL} provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

Slope Detector

The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

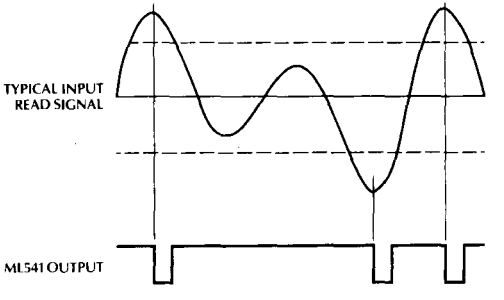
An external reactive network, shown in the Typical Application, is used between the D_{IF+} and D_{IF-} pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = External capacitor (20 pF to 150 pF)
L = External inductor
R = External resistor
$s = j\omega = j2\pi f$

Output Logic

The output logic provides a negative TTL pulse at pin RD which begins at the peak of a valid read pulse, as shown below.

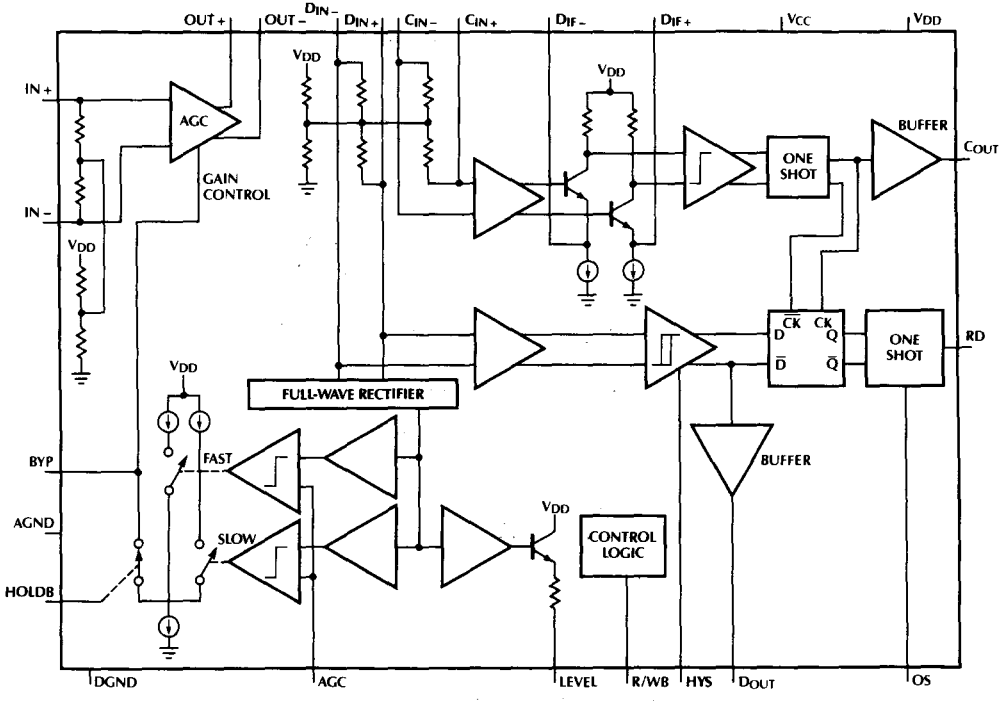


Pin R/WB must be high for the output logic to be active. The key element in the output logic is the D flip-flop. The flip-flop is clocked by the slope detector at the time of a zero crossing, which loads data from level detector. The flip-flop inputs only change state when the level detector detects a peak amplitude of a polarity opposite to the previous valid peak. Thus, through the output logic the slope detector determines output timing and the level detector determines pulse validity.

Layout Considerations

As with any high gain, wide bandwidth analog circuitry, care needs to be exercised in PC layout. Power supply and ground lines should be bypassed and well isolated from other circuitry. A ground plane is recommended, as is keeping analog lines short and well balanced to prevent interaction with nearby circuitry in the disk drive.

BLOCK DIAGRAM



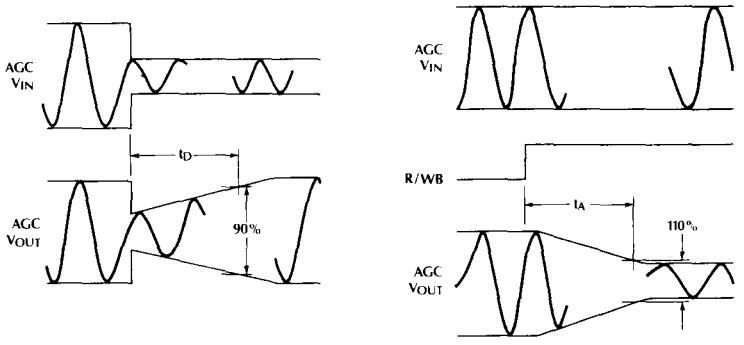


Figure 1. AGC Timing Diagram

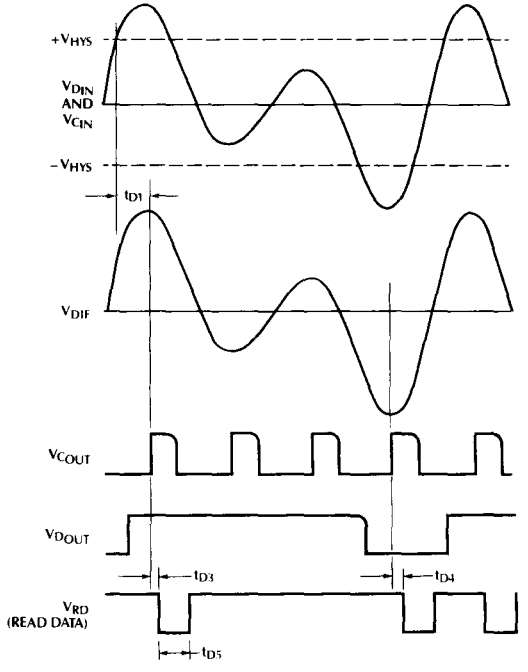


Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

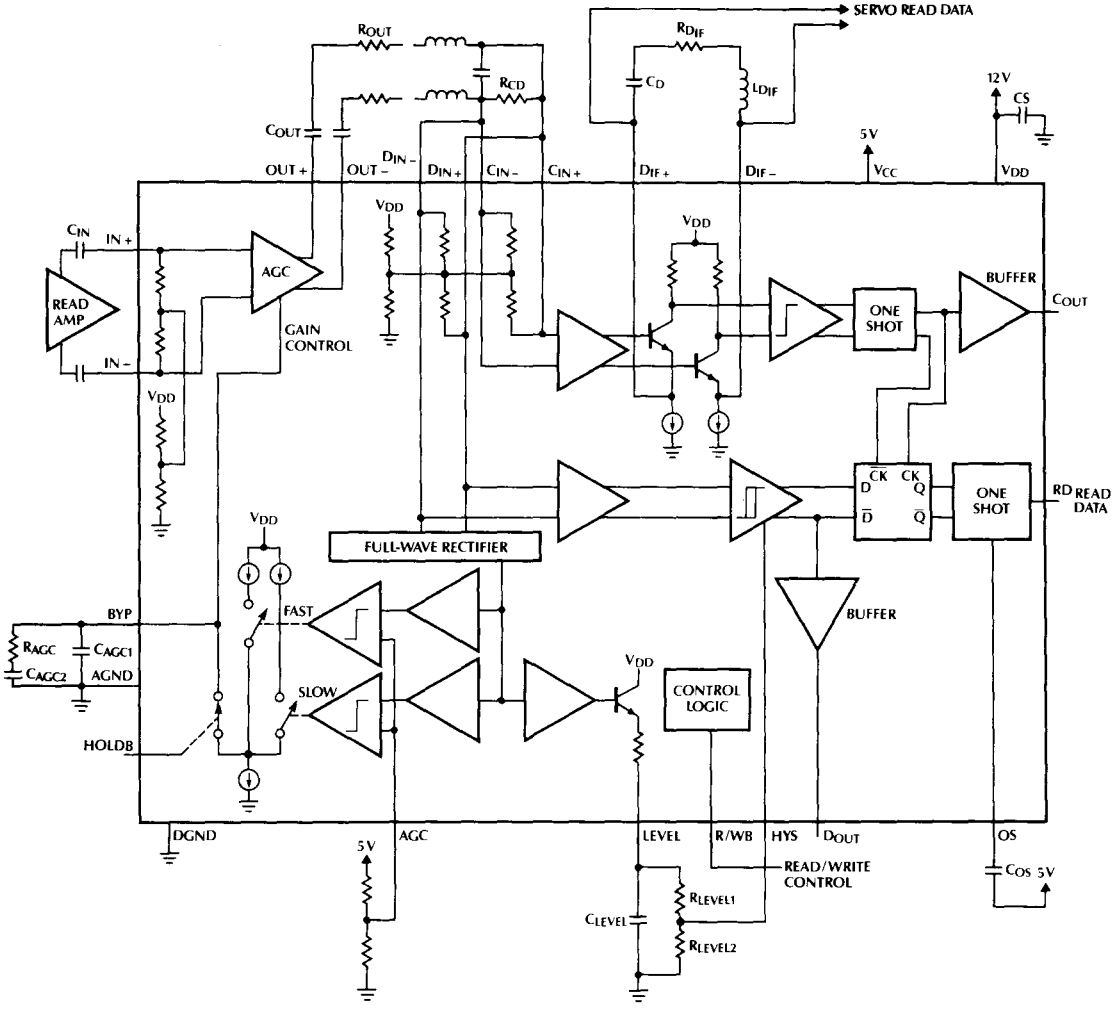


Figure 3. Typical Application Diagram

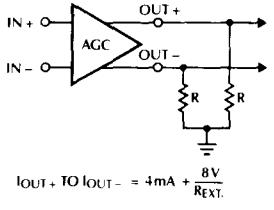


Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	PACKAGE
ML541CP	0°C to +70°C	MOLDED DIP (P24)
ML541CJ	0°C to +70°C	HERMETIC DIP (J24)
ML541CQ	0°C to +70°C	MOLDED PCC (Q28)
ML541CS	0°C to +70°C	MOLDED SOIC (S24)