

LXT970 NIC Demo Board

with DEC 21143 Controller

General Description

The LXT970 NIC Demo Board provides a complete working platform for evaluation of the LXT970 Fast Ethernet Transceiver interfacing with the DEC 21143 LAN Controller in a 10BASE-T and/or 100BASE-TX environment.

The NIC Demo Board can be configured to operate in 10/100Mbps (4B) Nibble Mode or (5B) Symbol Mode. This document describes typical Demo Board setup procedures for a 100BASE-TX environment. The NIC Demo board is designed to plug directly into a PC and includes the driver software required for the controller interface. LXT970 NIC Demo Board is operated with a single 5V power supply.

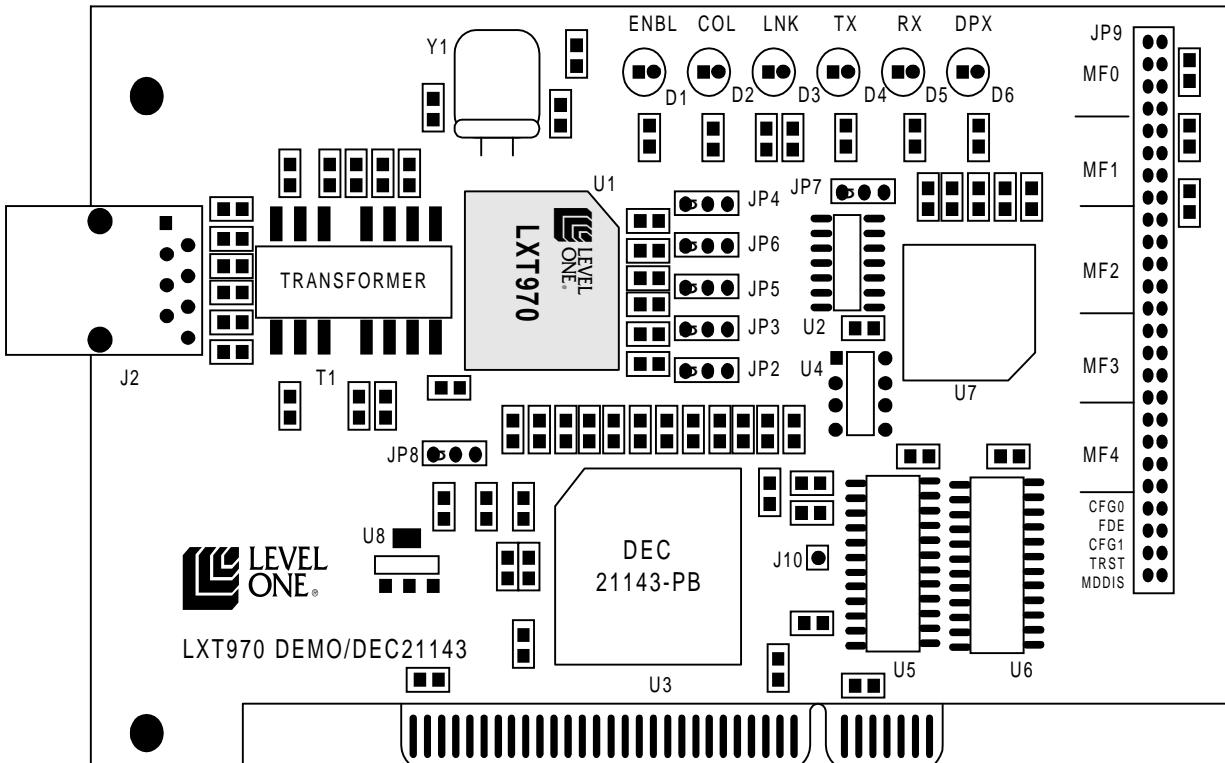
A complete Bill of Materials and schematics are included for reference.

Before using the NIC Demo Board, review the latest LXT970 Fast Ethernet Transceiver data sheet for the most current information.

Features

- Quick setup and ease of use for complete system demonstration
- LXT970 Fast Ethernet Transceiver
- DEC 21143-PB LAN Controller
- Netware Driver software included
- Configurable for:
10Mbps / 100Mbps operation
(4B)Nibble Mode / (5B)Symbol Mode operation
- Single RJ45 connection
- LED indicators for major functions
- Standard half duplex or full duplex operation at 10 or 100Mbps

LXT970 NIC Demo Board



EQUIPMENT SETUP

Equipment Requirements

The LXT970 NIC Demo Board includes all the components needed for successful evaluation. However, the following additional equipment is recommended:

- PC with PCI bus
- Category 5 Unshielded Twisted-Pair (UTP) cable

The LXT970 NIC Demo Board is designed with a DEC 21143 PCI/CardBus 10/100Mbps Ethernet LAN Controller. DEC 21143 Driver software must be installed to operate the Controller. For more information on the 21143 Controller refer to Digital Semiconductor 21143 Data Sheet.

Power Supply

The LXT970 NIC Demo Board is operated with a single 5V supply. The voltage is stepped down to 3.3V via a voltage converter (U8) to operate the DEC 21143 Controller and the LXT970 MII.

Software Installation

Important: This installation procedure is valid for users of *Novell Personal Netware* software **only**.

DEC 21143 Driver Software is included in the LXT970 NIC Demo Board Kit. DC21X4.COM is the driver for the DEC 21143 Controller. This file must be installed on a PC to operate the Demo Board.

Installation of this software will overwrite all critical files in the current configuration. Before installing driver software make provisions to restore your computer to “before installation” configuration by backing up all the files found on the 21143 Driver Software Disk.

Files included on the disk are:

- DC21X4.cli
- DC21X4.com
- DC21X4.hdi
- DC21X4.ins
- IPXODI.com
- LSL.com
- NET.cfg
- Startnet.bat
- Vtm.exe
- Readme.txt

The software disk was shipped with write protection engaged. Ensure the write protection of the disk is engaged by verifying the two square holes at the top of the disk are exposed. You can write protect the file by sliding the tab up manually on the left side at the rear of the disk jacket.

The following steps are recommended for installation of DEC 21143 Driver Software:

1. Make a copy of the files on the 21143 Driver Software Disk for safe keeping.
2. Install the disk containing the 21143 Driver Software in the Floppy (A:) Drive.
3. After boot-up, use DOS “CD” command, and change the directory to C:\NWCLIENT.
Type: (*cd c:\nwclient*)
4. Move to floppy disk (A:) drive.
Type: (*A:*)
5. Using DOS “CD” command, change directory to A:\NOVELL.
Type: (*cd a:\novell*)
6. Using DOS “COPY” command, copy the files necessary to get the system running into the C:\NWCLIENT directory.
7. Observe status messages from computer to insure there are no copy errors, and that all files are copied.
8. Restart the computer. Your card should load automatically during re-boot.
9. You may now edit your NET.CFG file to customize your network environment. Additional commands and explanations are included in the NET.CFG file itself. From the NWCLIENT directory (step 3):
Type: (*edit net.cfg*)
The editor will open with NET.CFG loaded. Make your edits and save the changes.

Hardware Setup

The LXT970 NIC Demo Board can be configured for (4-bit) Nibble Mode (Normal MII operation) or (5-bit) Symbol Mode operation. Set jumpers (JP2 - JP9) for the desired operating mode as shown in Table 1.

Table 1: LXT970 NIC Jumper Setup

Mode Selection	Jumpers	Jumper Pin Placement
Nibble Mode (Normal MII Operation) (4-bit)	JP2	Pins 2 and 3
	JP3	
	JP4	
	JP5	
	JP6	
	JP7	
	JP8	
	JP9	Pins 5 and 6
		Pins 15 and 16
		Pins 23 and 24
	Pins 31 and 32	
	Pins 37 and 38	
Symbol Mode (5-bit)	JP2	Pins 1 and 2
	JP3	
	JP4	
	JP5	
	JP6	
	JP7	
	JP8	Pins 2 and 3
	JP9	Pins 7 and 8
		Pins 15 and 16
		Pins 29 and 30
	Pins 39 and 40	

Hardware Installation

The LXT970 NIC Demo Board is designed to plug directly into any PC. Basic instructions for installation and network connection are as follows:

- Take the cover off the PC chassis.
- Install the LXT970 NIC Demo Board into an empty PCI slot (Note: The PC must be turned **OFF** when installing or removing the LXT970 NIC Demo Board).
- Connect the LXT970 NIC Demo Board to the Novell Network using CAT 5 Ethernet cable via the RJ45 connector.
- Connect the metal shield of the RJ45 connector to chassis ground. (This is required for ESD or EMI testing).
- Turn **ON** the PC and verify the drivers are loaded properly (If a problem occurs check the jumper settings and the “Starnet.bat” and “net.cfg” files).

LED Indicators

There are 6 status LEDs on the LXT970 NIC Demo Board. Refer to Table 2 for LED descriptions.

Table 2: LED Descriptions

Label	Ref Des	Description
ENBL	D1	Line Speed. Indicates 100Mbps operation
COL	D2	Collision. Indicates collision
LNK	D3	Link. Indicates connection
TX	D4	Transmit Data. Indicates data being transmitted
RX	D5	Receive Data. Indicates data being received
DPX	D6	Duplex. Indicates Half Duplex operation.

HARDWARE CONTROL INTERFACE

Multi-Function Pins

The Hardware Control Interface (JP9) provides access to the Multi-Function (MF) pins which decode 4-level supply voltages to establish two independent settings per pin. The first setting determines chip address. The second setting determines configuration of the LXT970.

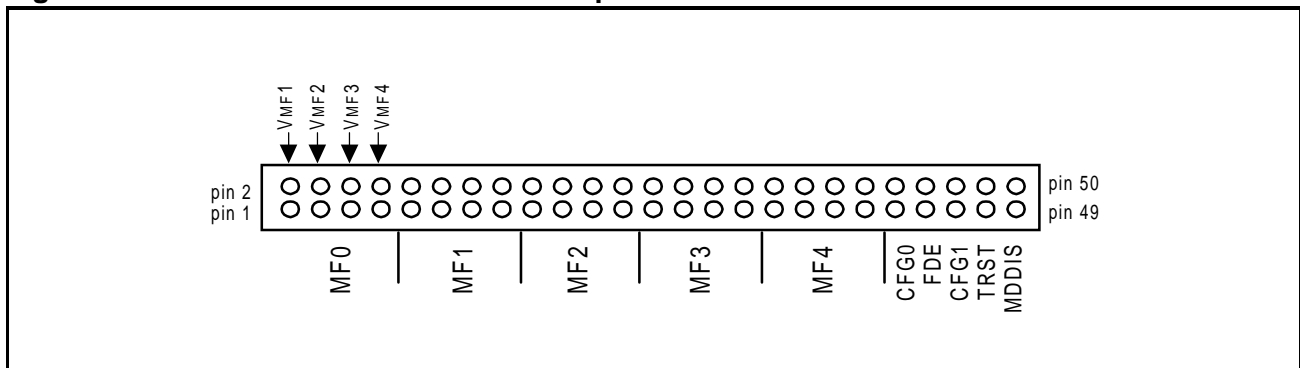
Input Voltage Levels

The 4-level inputs referred to as VMF1, VMF2, VMF3 and VMF4 are shown in Table 3. To select an Input Level place a jumper on the appropriate pins as shown in Figure 1. The 4-level input pins (VMF1, VMF2, VMF3 and VMF4) are identical for each Multi-Function (MF) section.

Table 3: MF Pins Input Voltage Levels

Parameter	Symbol	Min	Max	Units
Input Voltage Level 1	VMF1	$V_{cc} - 0.5$	-	V
Input Voltage Level 2	VMF2	$(V_{cc}/2) + 0.5$	$V_{cc} - 1.2$	V
Input Voltage Level 3	VMF3	1.2	$V_{cc}/2 - 0.5$	V
Input Voltage Level 4	VMF4	-	0.5	V

Figure 1: Hardware Control Interface Jumper Placement



Function / Address Settings

The multi-function pins allow the user to enable or disable the applicable functions and determine chip address according to the input level selected. Table 4 shows the status of the function according to the (VMF) selection.

Table 4: Hardware Control Interface (JP1) Functions

Pin	Address	Input Voltage Levels			
	Function	VMF1	VMF2	VMF3	VMF4
MF0	Address Bit 0	1	1	0	0
	Auto-Negotiation Sets the initial value of bit 0.12	Disabled (0.12 = 0)	Enabled (0.12 = 1)	Enabled (0.12 = 1)	Disabled (0.12 = 0)
MF1	Address Bit 1	1	1	0	0
	Repeater / DTE Mode Sets the initial value of bit 19.13	DTE (19.13 = 0)	Repeater (19.13 = 1)	Repeater (19.13 = 1)	DTE (19.13 = 0)
MF2	Address Bit 2	1	1	0	0
	Nibble (4B) / Symbol (5B) Mode Sets the initial value of bit 19.4	Nibble (4B) (19.4 = 0)	Symbol (5B) (19.4 = 1)	Symbol (5B) (19.4 = 1)	Nibble (4B) (19.4 = 0)
MF3	Address Bit 3	1	1	0	0
	Scrambler Operation Sets the initial value of bit 19.3	Enabled (19.3 = 0)	Bypassed (19.3 = 1)	Bypassed (19.3 = 1)	Enabled (19.3 = 0)
MF4	Address Bit 4	1	1	0	0
	If Auto-Negotiate Enabled via MF0, MF4 works in combination with CFG1 to control operating speed advertisement capabilities. See Table 5 for details.				
	If Auto-Negotiate Disabled Then TX/F Mode Sets the initial value of bit 19.2	100TX (19.2 = 0)	100FX (19.2 = 1)	100FX (19.2 = 1)	100TX (19.2 = 0)

Table 5: Operating Speed Advertisement Settings

MF4 Input Voltage Levels	CFG1	Function
If Auto-Negotiate Enabled via MF0		
VMF1, VMF4	Jumper Not Installed	Advertise all capabilities, Ignore FDE
VMF1, VMF4	Jumper Installed	Advertise 10 Mbps only, Follow FDE
VMF2, VMF3	Jumper Not Installed	Advertise 100 Mbps only, Follow FDE
VMF2, VMF3	Jumper Installed	Advertise 10/100 Mbps, Follow FDE

Additional Hardware Control Functions

In addition to the MF pins, there are ten pins (#41 - 50) labeled as CFG0, FDE, CFG1, TRST and MDDIS. These pins control the status of the applicable function by installing or removing a jumper. Table 6 shows these jumpers and their functions.

Table 6: Additional Hardware Control Interface Functions

Jumper Label	Function	Status	Jumper Installed	Jumper Not Installed
CFG0	Restart Negotiation (when Auto-Neg enabled) ¹	Enable		X
		Disable	X	
	Speed Select (when Auto-Neg disabled) ¹	10Mbps		X
		100Mbps	X	
FDE	Full Duplex	Enable	X	
		Disable		X
CFG1	Speed Advertisement Capabilities (when Auto-Neg enabled) ¹	When Auto-Neg enabled, CFG1 works in combination with MF4 to control operating speed advertising capabilities. See Table 5 for details		
	Link Test (when Auto-Neg disabled) ¹	Enable		X
		Disable	X	
TRSTE	Tristate (MDC and MDIO are not affected)	Tristates MII Data Interface	X	
		Normal Operation		X
MDDIS	MDIO Port	Enable		X
		Disable	X	

1. Auto-negotiation is set via MF0.

BILL OF MATERIALS AND BOARD SCHEMATICS

Table 7: LXD970 NIC Demo BOM

Item	Qty	Reference	Description
1	16	C1, C2, C15, C16, C17, C29, C30, C31, C32, C34, C35, C37, C38, C39, C41	.1 μ f/50V 10% 1206 SMD
2	5	C3, C4, C0, C42, C43	10 μ f/6.3V SMD
3	4	C5, C33, C40, C44	22 μ f/6.3V SMD TANT.CAPEIA B
4	2	C6, C7	18pf/50 5% .0805
5	3	C8, C9, C10	.01 μ f/50V 10% .0805 SMD
6	1	C28	22 μ f/50V .0805 SMD
7	3	D1, D2, D5	Red LED DIFF
8	2	D3, D6	Green LED DIFF
9	1	D4	Yellow LED DIFF
10	7	JP2, JP3, JP4, JP5, JP6, JP7, JP8	3-pin Gold Straight Header
11	1	J2	RJ45 1 Position Jack Shielded PC Grade
12	1	J10	Miniature Test Point
13	2	L5, L6, L7, L8	Ferrite SMD Bead P9812
14	1	JP9	25-pin Dual Row Header
15	6	R1, R2, R3, R4, R5, R59	332 Ω 1% Metal SMD Resistor
16	8	R10, R11, R14, R15, R17, R18, R19, R20	49.9 Ω 1% Metal SMD Resistor
17	2	R12, R13	75 Ω 1% Metal SMD Resistor
18	2	R57, R16	100 Ω 1% Metal SMD Resistor
19	7	R21 R22, R23, R24, R25, R62, R63	4.75k Ω 1% Metal SMD Resistor
20	18	R27, R28, R29, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41, R54, R55, R60, R74	54.9 Ω 1% Metal SMD Resistor
21	1	R30	22k Ω 1% Metal SMD Resistor
22	1	R56	2.43k 1% Metal SMD Resistor
23	8	R61, R64, R65, R66, R67, R68, R72, R73	10k 1% Metal SMD Resistor
24	3	R69, R70, R71	1k 1% Metal SMD Resistor
25	1	T1	10/100 MB Transformer HALO TG22-S010ND
26	1	T1	10/100 MB Transformer Pulse PE-68517
27	1	U1	LXT970
28	1	U2	HEX inverter SMD SO-14 Package

Table 7: LXD970 NIC Demo BOM – continued

Item	Qty	Reference	Description
29	1	U3	DEC 21143 LAN Controller 144-pin PQFP
30	1	U4	1k bit 5V EEPROM 8 DIP Pkg
31	1	U7	Surface Mount PLCC Pkg - 90ns
32	1	U8	3.3V Low Dropout Reg SOT-223 Pkg
33	1	Y1	25MHz Crystal HC49 Case
34	1	IC Socket for U7	32-pin Solder Trail PLCC Socket
35	1	IC Socket for U1	64-pin QFP Surface Mount IC Socket
36	1	IC Socket for U4	8-pin Solder Tail (Gold) DIP Socket

Figure 2: LXT970 NIC DEC 21143 Interface

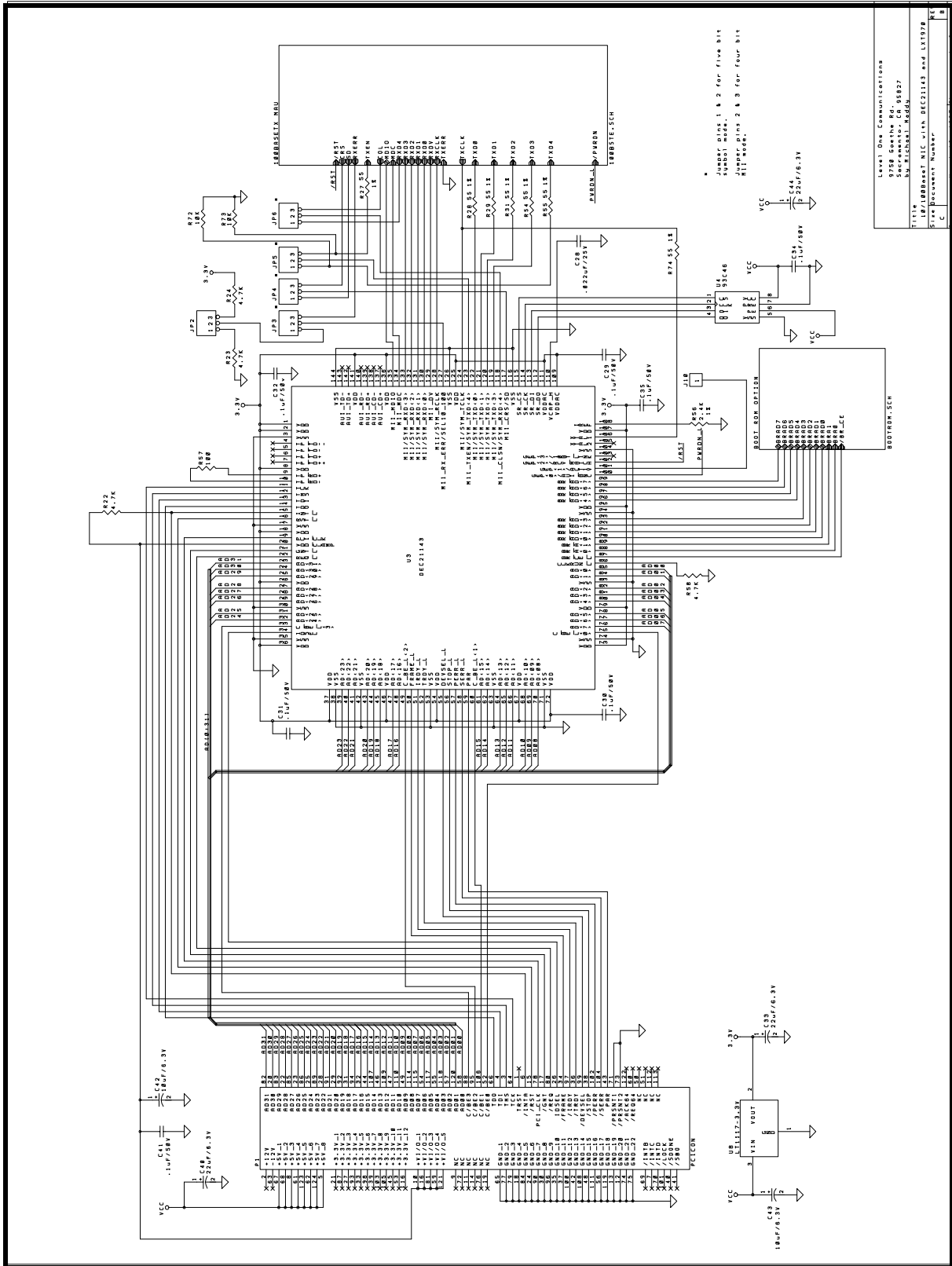
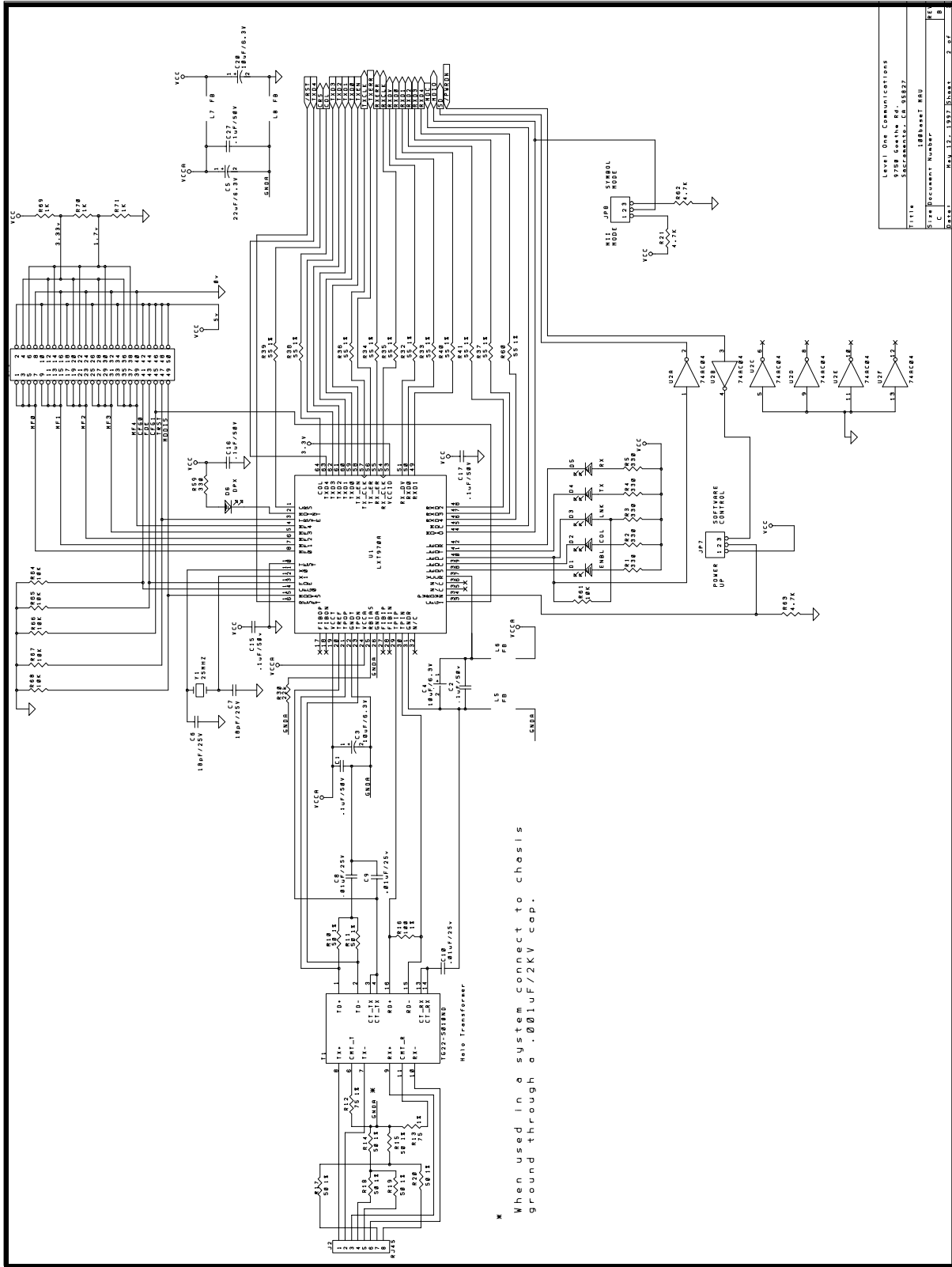
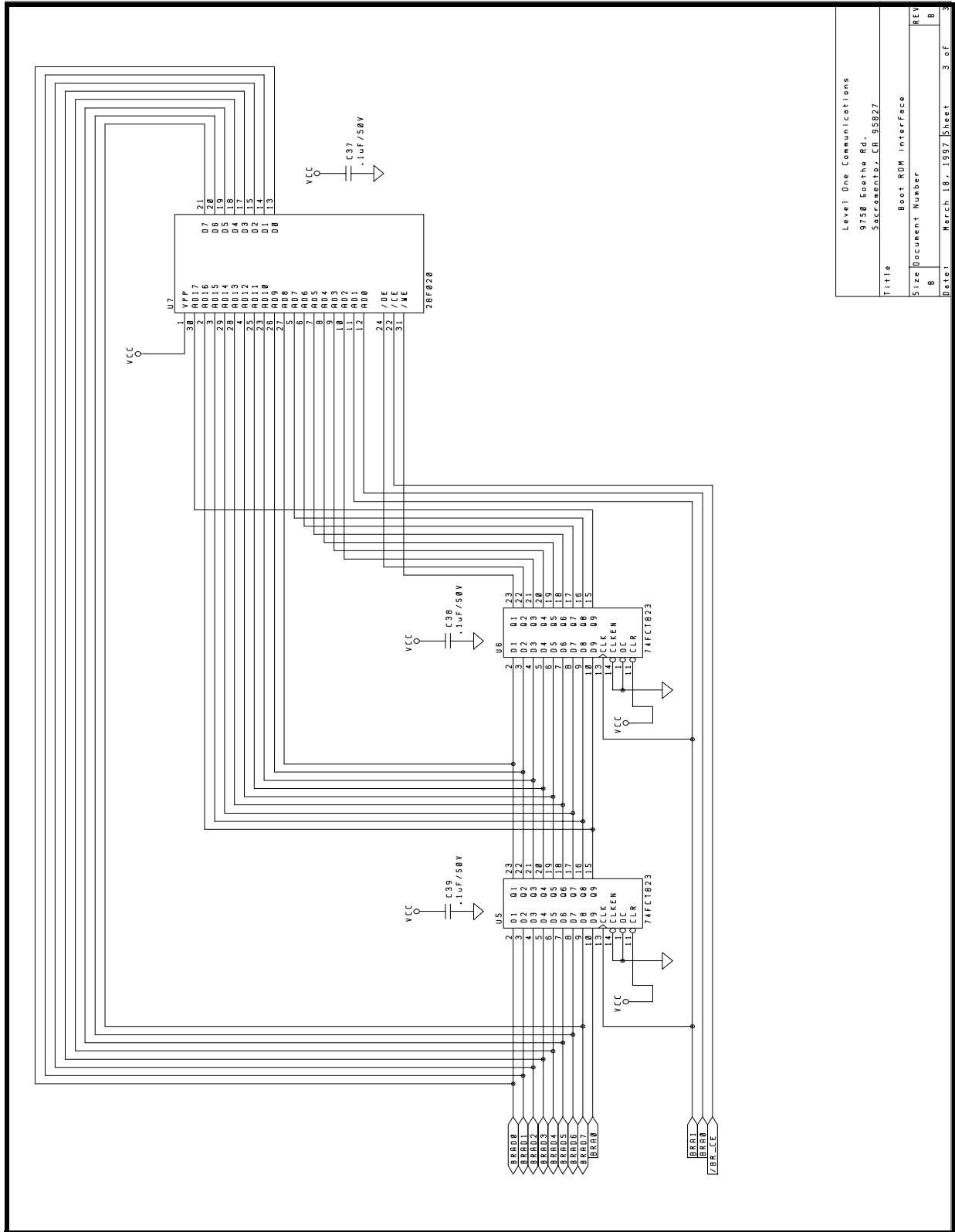


Figure 3: LXT970 NIC LXT970QC Interface



Level One Communications	REV
9758 Goethe Rd.	1
Sacramento, CA 95837	2
Site Document Number	3
1888sheet.HW	4
DATE: MON 12 1997 5:00am	5
	6

Figure 4: LXT970 NIC ROM Interface



Level One Communications 9758 Soerke Rd. Sacramento, CA 95827	
Title Boot ROM Interface	
Size	Document Number
B	REV
Date:	March 18, 1997
Sheet	3 of 3

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Revision Date Status

1.3	12/97	Revise note 6 of the Software Installation procedure and delete note 7.
1.2	10/97	Rewrite DEC 21143 driver software installation procedure and various editorial updates.
1.1	08/97	Revise software installation procedure.

This product is covered by one or more of the following patents. Additional patents pending.
2002382-1; 5,008,637; 5,028,888; 5,057,794; 5,059,924; 5,068,628; 5,077,529; 5,084,866; 5,148,427; 5,153,875; 5,157,690; 5,159,291; 5,162,746;
5,166,635; 5,181,228; 5,204,880; 5,249,183; 5,257,286; 5,267,269; 5,267,746; 5,461,661; 5,493,243; 5,534,863; 5,574,726; 5,581,585; 5,608,341