PowerPC® 405EP
Evaluation Board Manual

SA14-2686-03

Fourth Edition (11/26/02)

This edition of the *IBM PPC405EP Evaluation Board Manual* applies to the IBM PPC405EP 32-bit embedded controller, until otherwise indicated in new versions or application notes.

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law: INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS MANUAL "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions; therefore, this statement may not apply to you.

IBM does not warrant that the products in this publication, whether individually or as one or more groups, will meet your requirements or that the publication or the accompanying product descriptions are error-free.

This publication could contain technical inaccuracies or typographical errors. Changes are periodically made to the information herein; these changes will be incorporated in new editions of the publication. IBM may make improvements and/or changes in the product(s) and/or program(s) described in this publication at any time.

It is possible that this publication may contain references to, or information about, IBM products (machines and programs), programming, or services that are not announced in your country. Such references or information must not be construed to mean that IBM intends to announce such IBM products, programming, or services in your country. Any reference to an IBM licensed program in this publication is not intended to state or imply that you can use only IBM's licensed program. You can use any functionally equivalent program instead.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

No part of this publication may be reproduced or distributed in any form or by any means, or stored in a data base or retrieval system, without the written permission of IBM.

Requests for copies of this publication and for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

Address technical queries about this product to ppcsupp@us.ibm.com

Address comments about this publication to:

IBM Corporation
Department YM5A
P.O. Box 12195
Research Triangle Park, NC 27709

IBM may use or distribute whatever information you supply in any way it believes appropriate without incurring any obligation to you.

Notice to U.S. Government Users – Documentation Related to Restricted Rights – Use, duplication, or disclosure is subject to restrictions set forth in GSA ADP Schedule Contract with IBM Corporation.

Patents and Trademarks

IBM may have patents or pending patent applications covering the subject matter in this publication. The furnishing of this publication does not give you any license to these patents. You can send license inquiries, in writing, to the IBM Director of Licensing, IBM Corporation, 208 Harbor Drive, Stamford, CT 06904, United States of America.

The following terms are trademarks of the IBM Corporation:

IBM
IBM logo
PowerPC
PowerPC Architecture
PowerPC Embedded Controllers
PowerPC logo
PPC405EP
RISCTrace
RISCWatch

Other terms which are trademarks are the property of their respective owners.

Contents

Tables

Figures

About This Book

This manual describes the PPC405EP™ evaluation board, an evaluation platform for the PPC405EP chip.

Who Should Use This Book

This book is written to aid programmers and other technical personnel in the use of the PPC405EP evaluation board. In order to use the board and this document, the reader should have familiarity with the following:

- PowerPC Architecture™
- PCI bus
- Embedded microprocessor hardware
- IBM RISCWatch™ debugger

How to Use This Book

This book describes the features and interfaces of the PPC405EP evaluation board and contains the following chapters:

- Chapter 1, “Overview of the PPC405EP”, provides a brief overview of the processor chip. Some chip aspects important to understanding the board design are discussed in greater detail.
- Chapter 2, “Board Design”, describes the architecture of the evaluation board.
- Chapter 3, “Memory Map”, describes the address space usage of the board. Tables are provided which define the access methods for all memory-mapped registers on the board. Some of these registers are simple memory-mapped registers, while others are accessed by indirect addressing.
- Chapter 4, “Programming the PPC405EP Memory Controller”, outlines the required programming to configure the PPC405EP for the board memory and peripherals.
- Chapter 5, “Reset and Interrupts”, lists the sources of resets and interrupts on the board, and provides information required to program the PPC405EP interrupt controller.
- Chapter 6, “Switches”, describes all switches on the board, and includes the factory settings for the switches.
- Chapter 7, “Fuses, Batteries, and Regulators”, describes all fuses on the board.
- Chapter 8, “Displays”, describes all displays on the board.
- Chapter 9, “Jumpers”, describes all jumpers on the board, and includes the factory settings for the jumpers.
- Chapter 10, “Connectors”, describes the location, physical description, and pin usage of all connectors on the board.
- Chapter 11, “FPGA Programming”, describes the source code and timing information for the FPGAs on the board.
- Chapter 12, “Bill of Materials”, provides the list of components for the board, and provides lists of auxiliary components which might be used with the board.

Related Publications

The following publications contain related information:

- *PPC405EP Evaluation Board Schematic*
- *PowerPC Architecture*
- *PowerPC Microprocessor Family: The Programming Environments*, MPRPPCFPE-01
- *PowerPC Embedded Processor Solutions*, SC09-3032; a CDROM which includes the *RISCWatch Debugger User's Guide*

Chapter 1. Overview of the PPC405EP

The PPC405EP processor is designed specifically to address embedded applications and provides a high-performance, low-power solution which is able to interface to a wide range of peripherals. With on-chip power management features and intrinsically lower power dissipation requirements, this controller is the right choice for embedded applications. This chip contains a high-performance RISC processor core, on-chip memory, SDRAM controller, PCI bus interface, two Ethernet interfaces, control for external ROM and peripherals, DMA with scatter-gather support, two serial ports, an IIC interface, general purpose timers, and general purpose I/O. A block diagram of the PPC405EP is shown in Figure 1-1.

- PowerPC 405 core operating at up to 266 MHz
- 4 KB of on-chip memory (OCM)
- PC-100 synchronous DRAM interface operating at up to 133 MHz
  - 32-bit interface for non-ECC applications
- External peripheral bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, or 16-bit SRAM or external peripherals.
- DMA support for peripherals attached to the on-chip bus (OPB)
  - Scatter-gather chaining supported
- PCI Revision 2.2 compitible interface (32 bits, up to 66 MHz)
  - PCI bus interface is configured to operate asynchronously to the processor bus
  - Internal PCI bus arbiter which may be disabled for use with an external arbiter
- Two Ethernet 10/100 Mbps (full-duplex) ports
- Programmable interrupt controller supports seven external and 23 internal edge triggered or level-sensitive interrupts
- Programmable timers
- Two serial ports (16750 compatible UART)
- One IIC interface
- General purpose I/Os available
- General purpose timers available
- Supports JTAG for board level testing
- Supports PowerPC processor boot from PCI memory

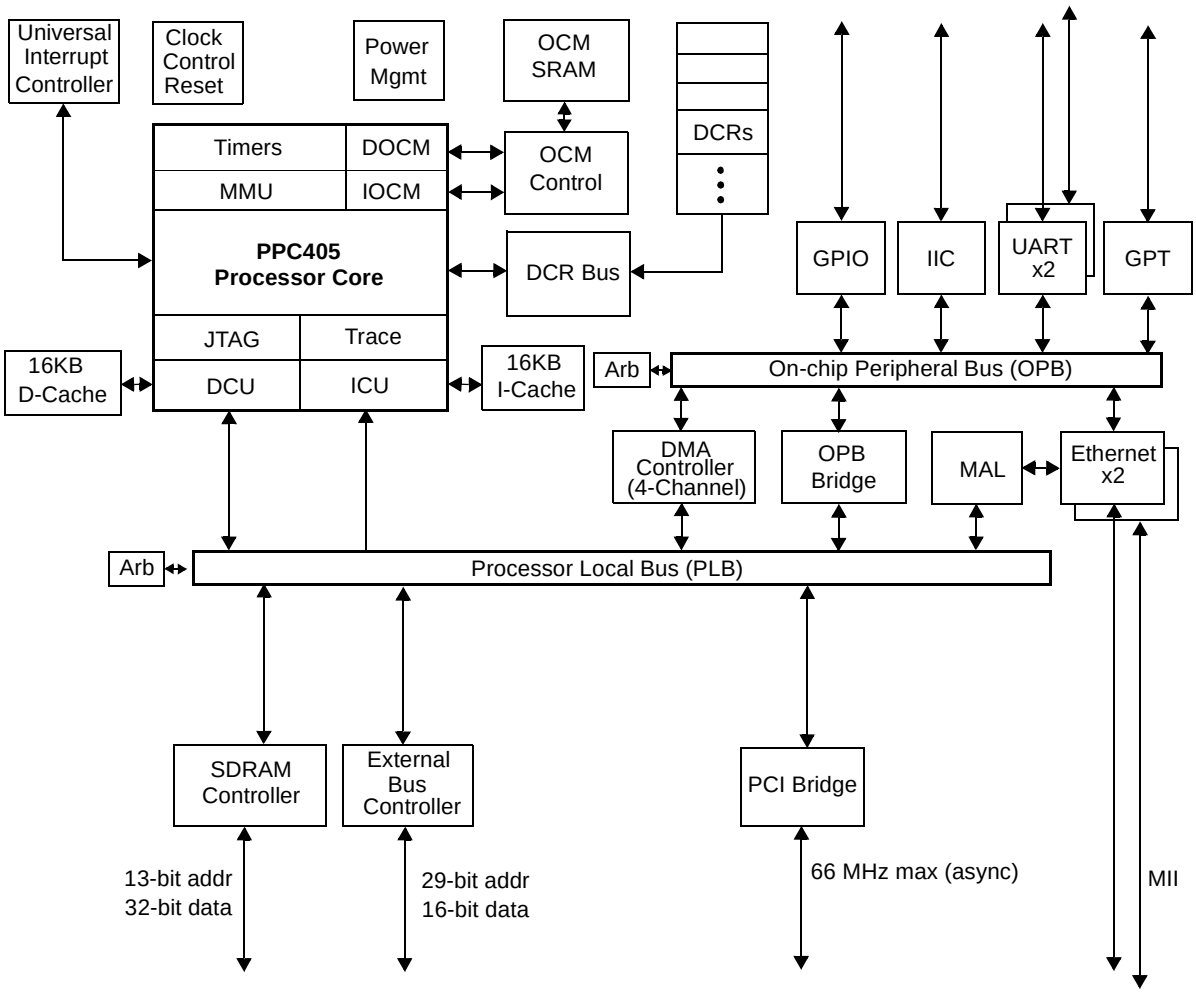


Figure 1-1. PPC405EP Block Diagram

1.1 PPC405EP and External PCI Arbiters

The PPC405EP chip contains an internal PCI arbiter, as well as support for an external arbiter. This board design provides an external arbiter to allow experimentation with that mode of operation. The external arbiter has the following features:

- The arbiter requires no programming support.
- The arbiter uses rotating priority, with all masters on the same level.
- With no requests present, the bus will park at the last-used master.
- The arbiter detects but does not report “broken masters” ($\overline{\text{Req}}$ and $\overline{\text{Gnt}}$ asserted, but $\overline{\text{Frame}}$ is not asserted within 16 clocks). The arbiter is not blocked by broken masters.
- All re-arbitration occurs while $\overline{\text{Frame}}$ is deasserted.

The board is equipped with FET switches to multiplex the internal and external arbiter lines. The FET switches for arbiter selection are intended solely to enable a user of the evaluation board to experiment with either arbiter mode. A typical board design would be hard-wired for one mode or the other, and the FET switches would not be present.

Note: If PCI mastering devices are plugged into all four PCI slots, use of the external abiter is required. The internal PCI arbiter in the PPC405EP supports only three external PCI mastering devices. Slot 3 (J35) is available only for a PCI slave device when using the internal arbiter.

Chapter 2. Board Design

The PPC405EP processor is a variation of the PPC405GP processor.

Figure 2-1 illustrates the architecture of the PPC405EP evaluation board. Subsequent paragraphs discuss aspects of the diagram in more detail.

Note: All of the information in the following sections, unless otherwise noted, applies to the PPC405EP processor. To see corresponding specifications for the PPC405GP processor please refer to the *PPC405GP Reference Board Manual*.

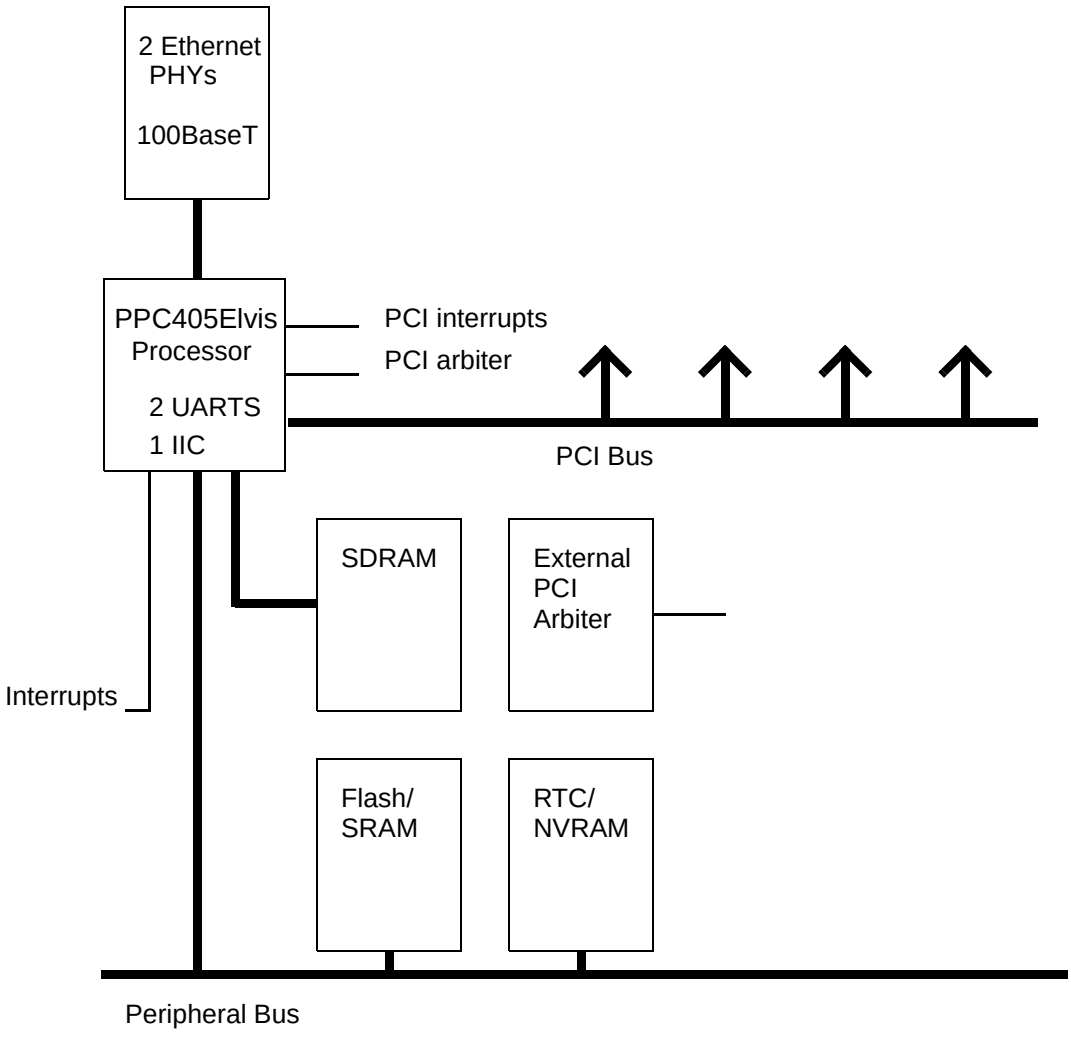


Figure 2-1. PPC405EP Evaluation Board Architecture

2.1 Processor

The PPC405EP evaluation board allows evaluation of designs using the PPC405EP processor. This chip utilizes an IBM PPC 405 32-bit, RISC processor core.

2.2 PPC405EP Internal Clocking

PPC405EP is highly configurable, and supports a wide range of clock ratios on its internal and external buses.

The following diagram indicates the major buses which exist in the PPC405EP chip. A single PLL is used as the source for the CPU clock. All generated clocks are integer ratios of this CPU clock. The clock architecture within the PPC405EP chip is illustrated in Figure 2-2.

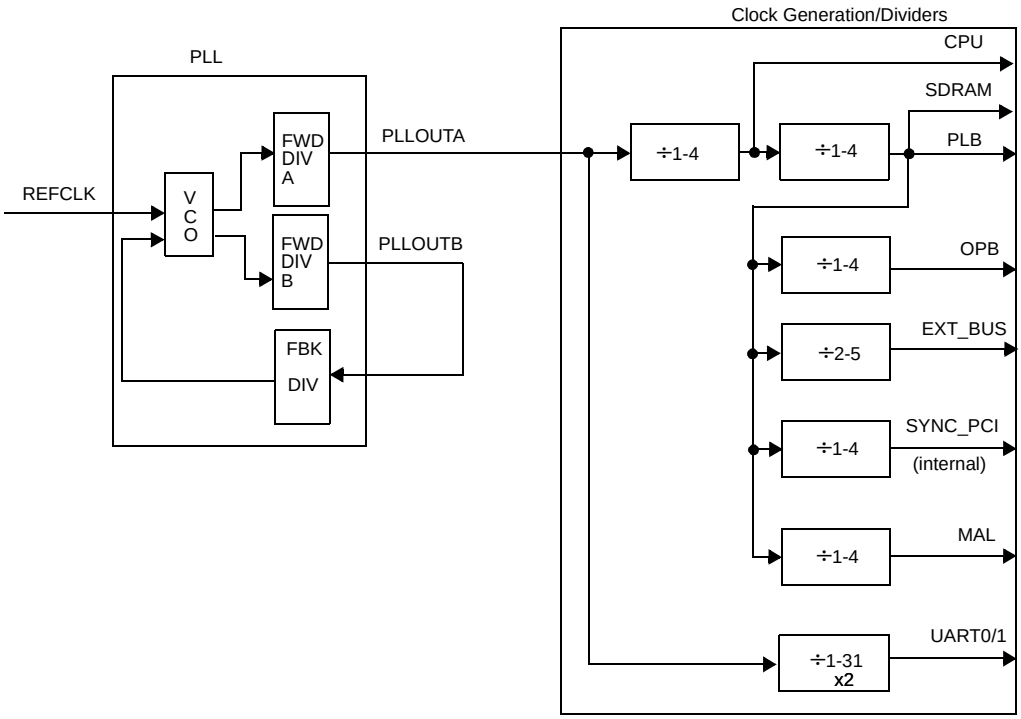


Figure 2-2. Clock Architecture of PPC405EP Chip

2.2.1 Strapping Options

The PPC405EP processor configures itself at reset based on strapping options. On the PPC405EP evaluation board, these options can be selected using board switch S4. See Figure 6-1 on page 6-2 for the location of the switch on the board.

The strapping options for the PPC405EP are shown in Table 2-1. Table 2-1 shows the switch settings for each option and the corresponding bits in the internal chip register (CPC0_BOOT) that are affected by the switch settings.

Table 2-1. PPC405EP Strapping Options

Switch (position)	CPC0_BOOT Bits (Name)	Option	Comments
S4(1)	30 (SEPROMPresent)	Enable/Disable Configuration SEPROM 0 Disable (factory setting) 1 Enable	0 = closed = on
S4(2:3)	28:29 (ebcBootWidth)	If S4(1) = 0 this is the Boot ROM width: 00 8 bits (factory setting) 01 16 bits 10 Reserved 11 Reserved	0 = closed = on
	25:26 (SEPROM BaseAddress)	If S4(1) = 1, these bits define the offset from the SEPROM base address (0xA0) on the IIC interface where the configuration record starts. 00 0x00 01 0x40 10 0x80 11 0xC0	0 = closed = on

2.3 Board Clocking

The clock architecture of the PPC405EP evaluation board is illustrated in Figure 2-3. Note that the clock generator is reset only at board power-on, not by any other reset source.

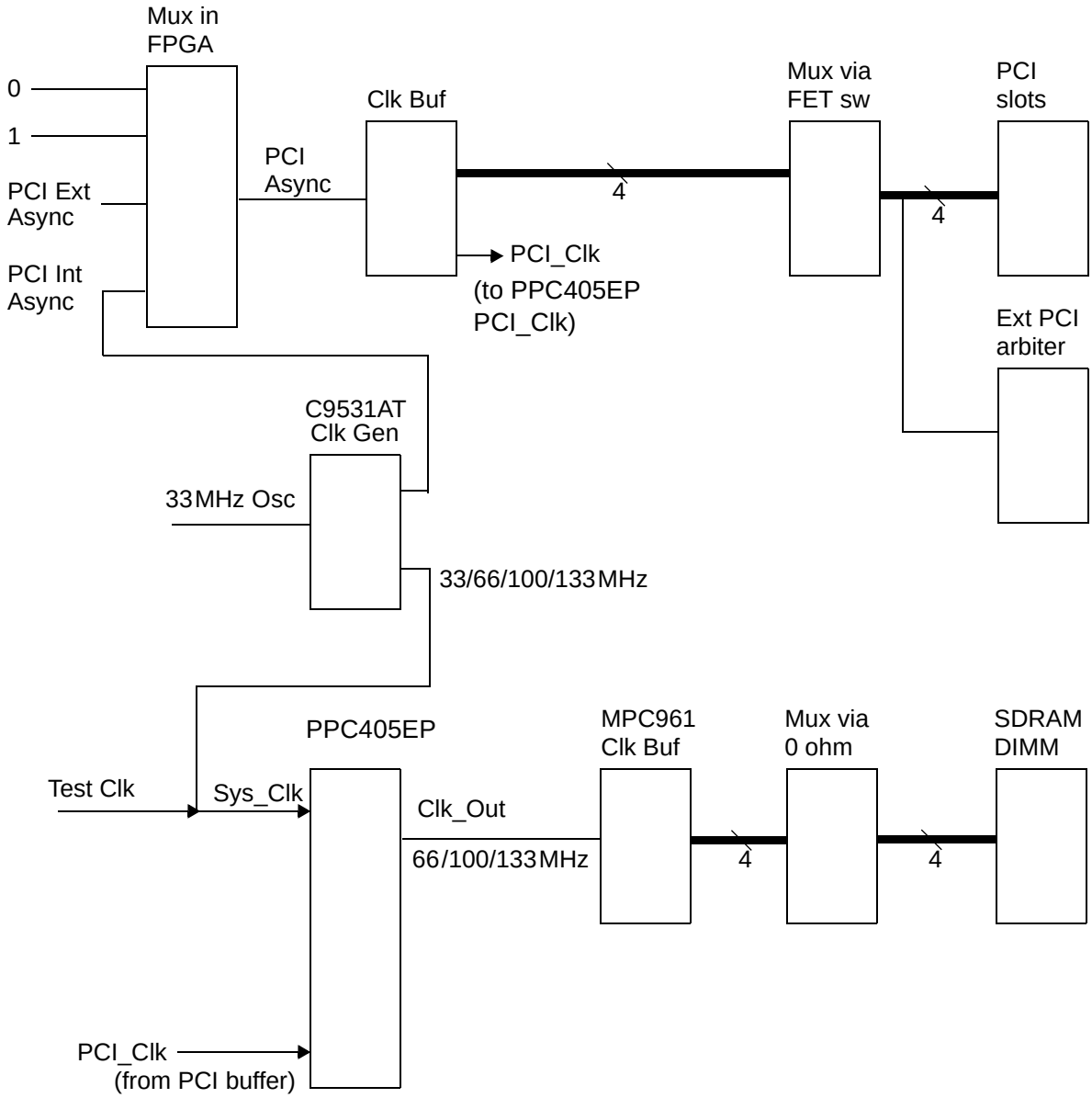


Figure 2-3. Clock Architecture of PPC405EP Board

See “PCI Bus” on page 2-8 for more information relating to Sys_Clk and PCI_Clk. The PCI_Clk input to the PPC405EP is selectable using the indicated jumpers and switch shown in Table 2-2.

Table 2-2. Sys_Clk and PCI_Clk Selection

MASTER_SEL_1 (J22)	MASTER_SEL_0 (J24)	PCI_FREQ_SEL (S4 Pos 4)	Sys_Clk (MHz)	PCI_Clk (MHz)
0	0	x	33.33	33.33
0	1	0	66.66	33.33
0	1	1	66.66	66.66
1	0	0	100	25
1	0	1	100	50
1	1	0	133.33	33.33
1	1	1	133.33	66.66

Note: 0 = jumper installed or switch closed
1 = jumper open or switch open
x = don't care

2.4 SDRAM Design

The PPC405EP chip supports 32-bit non-error correcting operation.

2.4.1 Supported Memory

On this board, SDRAM is provided by one 168-pin DIMM populated with 64-bit memory. DIMMs allow 64-bit memory to be configured as blocks of 32-bit memory, and that usage is applied to this board. The ECC bits on the 72-bit DIMMs are not used by this board.

The PPC405EP chip supports non-registered, non-buffered SDRAM at the processor local bus speed (up to 133 MHz). To achieve this bus speed and a CAS latency of 3 or less, it is required to use -75 or faster SDRAM. This corresponds to the normal PC-133 chip requirement for all SDRAM controllers. Non-buffered SDRAM DIMMs have four clock inputs, each of which may have multiple loads. Each clock input is separately driven.

The board supports the following 64-bit memory sizes:

- 2M x 64, 16MB
- 4M x 64, 32MB
- 8M x 64, 64MB
- 16M x 64, 128MB
- 32M x 64, 256MB

Note: Due to market conditions and availability, the SDRAM module shipped with the evaluation board may vary in size and type.

The structure of SDRAM DIMMs is analogous to DRAM SIMMs. There exist single-sided versions which are addressed by two chip selects (in 32-bit mode). See Figure 2-4 on page 2-4 for reference. See Section 2.4.2 on page 2-6 for detailed 32-bit wiring.

SDRAM uses IIC compatible Serial Presence Detect EEPROM. One PPC405EP IIC port is applied to that function. See “SDRAM Banks 0-1” on page 4-1 for more detail.

See Table 2-3 on page 2-7 for wiring.

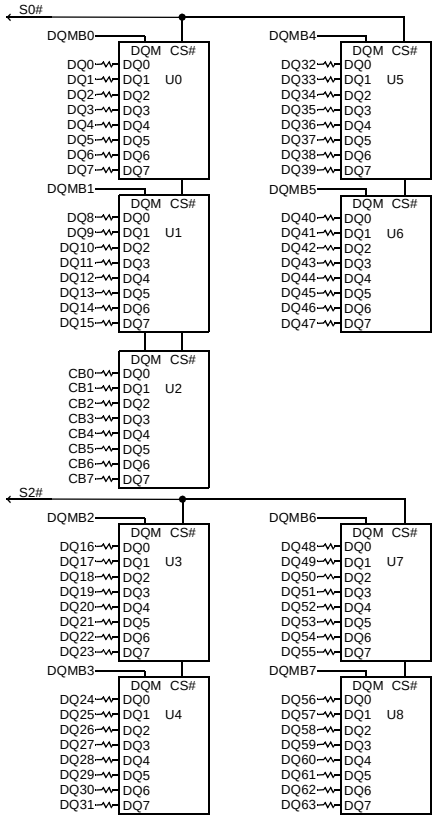


Figure 2-4. Single-sided DIMMs

2.4.2 DIMM Wiring Details

DIMMs with 168-pins were primarily designed for 64- or 72-bit systems. Because the DIMMs present a chip select for every 32-bit block, they may also be used in 32-bit mode. However, the DIMM pin naming, designed for 64-bit usage, makes 32-bit wiring somewhat confusing. On this board, the DIMM is connected to the PPC405EP according to Table 2-3.

Table 2-3. 32/40-bit Wiring of 64/72-bit DIMM

DIMM Pins	PPC405EP Pins	Comments
S0_N S2_N	BANK_SEL_0_N BANK_SEL_2_N	Chip selects for DIMM front side.
DQMB0 and DQMB2 DQMB1 and DQMB3 DQMB4 and DQMB6 DQMB5 and DQMB7	DQM_0 DQM_1 DQM_2 DQM_3	All four PPC405EP DQM pins are used regardless of ECC mode.
DQ0 and DQ16 DQ1 and DQ17 DQ2 and DQ18 DQ3 and DQ19 DQ4 and DQ20 DQ5 and DQ21 DQ6 and DQ22 DQ7 and DQ23	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	Byte lane 0
DQ8 and DQ24 DQ9 and DQ25 DQ10 and DQ26 DQ11 and DQ27 DQ12 and DQ28 DQ13 and DQ29 DQ14 and DQ30 DQ15 and DQ31	DATA8 DATA9 DATA10 DATA11 DATA12 DATA13 DATA14 DATA15	Byte lane 1
DQ32 and DQ48 DQ33 and DQ49 DQ34 and DQ50 DQ35 and DQ51 DQ36 and DQ52 DQ37 and DQ53 DQ38 and DQ54 DQ39 and DQ55	DATA16 DATA17 DATA18 DATA19 DATA20 DATA21 DATA22 DATA23	Byte lane 2
DQ40 and DQ56 DQ41 and DQ57 DQ42 and DQ58 DQ43 and DQ59 DQ44 and DQ60 DQ46 and DQ61 DQ46 and DQ62 DQ47 and DQ63	DATA24 DATA25 DATA26 DATA27 DATA28 DATA29 DATA30 DATA31	Byte lane 3

2.5 PCI Bus

The PPC405EP chip supports an asynchronous 3.3V PCI bus at either 33.33MHz or 66.66MHz, or a 5V PCI bus at 33.33MHz. The board is provided with a non-standard PCI connector footprint to allow any of these modes to be used. See “PCI Connectors” on page 10-24 for more details.

PCI at 66.66 MHz is available only in PCI slot 0 (J42).

The PPC405EP PCI frequency range can be altered only at reset. It is set based upon the capability of the installed card.

A separate PCI_Clk input is also provided to PPC405EP. PCI bus frequencies up to 66.66MHz are supported.

On this board, PCI_Clk input is selectable. See Table 2-2, “Sys_Clk and PCI_Clk Selection,” on page 2-5.

Normally, the PCI interface defaults to 66.66MHz if there are no PCI cards installed. Since the maximum PCI bus speed is 33.33MHz in a 5V PCI system, a switch is provided that can be used to force the PCI interface to run at 33.33MHz. This feature is useful for testing purposes. It also saves the user from having to modify the PCI divider switch settings when a PCI card is not installed.

2.5.1 Adapter-Mode Verification

The PPC405EP chip may be employed as either a PCI host or as a PCI adapter. This board demonstrates the host mode. The external PCI_Clk input allows testing of the chip in asynchronous mode with a truly asynchronous clock.

2.5.2 Booting the PPC405EP from PCI

A strapping option allows the PPC405EP to boot from the PCI bus instead of booting from Flash. The intent of this option is to allow many adapter cards without Flash to be hosted by a PCI system which contains the boot images for the adapter cards. The host system would hold each adapter card reset until the host was prepared to supply the boot images. This procedure eliminates the expense of the Flash and simplifies the problem of upgrading Flash images over time, as adapter software evolves.

2.6 Ethernet Design

The board provides two 100Base-T Ethernet ports, with auto negotiation to 10Base-T when connected to networks not capable of 100Mbps operation.

Ethernet support through the Media Access Control (MAC) layer is provided in the PPC405EP chip. The Physical Layer Device (PHY) and the Physical Medium Dependent sublayer and interface (PMD) are provided on the board. The connections between the MAC and the PHY conform to the Medium Independent Interface (MII) specification.

The PHY and PMD sublayer are provided by a National Semiconductor DP83843. There are two PHYs, PHY0 and PHY1, provided. PHY0 is connected with address PHYAD=0b00001, and PHY1 is connected with address PHYAD=0b00010. There are jumpers provided for both PHYs to allow address changes to avoid PHY address conflicts or to disable the PHY (see “PHY Address Selection” on page 9-4). Address strapping takes effect at reset of the PHY chip.

The supported media is Category 5 Unshielded Twisted Pair cable (UTP), accessed by means of RJ-45 connectors on the board. For details on the connector usage, see Section “Ethernet TWP Connectors” on page 10-4.

2.7 Flash Memory

Flash memory can be present in two ways. Flash memory is provided on the board. Additional Flash memory can be provided by means of an expansion card installed in the Expansion Interface connector.

2.7.1 Flash on the PPC405EP Board

Eight-bit Flash memory is used on the PPC405EP board. No benchmarking impact is expected from the use of a narrow rather than a wide Flash array. For performance work, the user should be prepared to replace the initial firmware support provided in the Flash with optimized routines residing in DRAM.

A socketed 0.5 MB Flash is installed at the top of the address space. Immediately below that Flash in the address space is 0.5 MB of SRAM. Position 8 on switch S4 allows the exchange of the two 0.5 MB blocks in the address space. The intent of this SRAM is to aid in the debug of ROM boot code, not for speed enhancement. Flash contents can be copied to SRAM, then SRAM can be placed at the top of the address space. ROM code can then be debugged from SRAM, allowing the placement of unlimited software breakpoints.

Both memory devices are accessed by peripheral bank 0, chip select P_CS0. Position 7 on switch S4 allows the chip select to be withheld from both these memories, so that a boot device may be placed on the Expansion interface without conflict.

2.7.2 Flash on an Expansion Card

To allow PPC405EP to boot from an Expansion card connected to the Expansion interface, an Expansion card Flash can be accessed by peripheral bank 0, chip select P_CS0. Position 7 on switch S4 also allows the Flash to be accessed by a spare peripheral chip select present on the Expansion interface. In this mode, PPC405EP boots from the Flash on the main board, and the Expansion card Flash may be placed elsewhere in the address space by appropriate PPC405EP bank register programming.

The purpose of supporting a Flash Expansion card is to support activities such as Windows CE certification which mandate large Flash, without impacting customers who have no need for such large amounts.

2.8 Real-Time Clock/NVRAM

The Real-Time Clock (RTC) used on the PPC405EP board is the Dallas Semiconductor DS1743P (5V part). The clock is Y2K compliant. The chip contains a directly-accessed 8 KB non-volatile RAM. The required crystal and lithium battery are contained in a Dallas Semiconductor DS9034PCX PowerCap which snaps over the clock module.

2.9 IIC Port

The PPC405EP chip provides one IIC port. This port is used for SDRAM Serial Presence Detect. The port is also terminated on the Expansion connector for connection to customer IIC devices.

2.10 Serial Ports

Two serial ports, software compatible with 16750, are included in the PPC405EP chip.

UART 0 provides a full set of modem control lines. Some of these lines are multiplexed with GPIO signals.

UART 1 provides only Tx and Rx.

The UART clock is generated in the PPC405EP chip. There is no provision for the use of an external UART clock.

2.11 Expansion Interface Support

A connector is provided to facilitate the attachment of customer prototyping logic. All lines of the External Peripheral interface are presented (only those chip selects which are not used elsewhere on the board are presented). All unused interrupt lines are presented. All signals presented on the Expansion connector are also presented on Mictor logic analyzer connectors.

The Expansion Interface connector is located and Expansion Interface daughter cards are sized such that the system chassis may be closed while the daughter cards are installed.

2.12 Logic Analyzer Connections

The peripheral bus is equipped with Mictor logic analyzer connectors. See “Logic Analyzer Connectors” on page 10-13 for details.

HP Logic analyzer connection to the SDRAM bus is accomplished using a FuturePlus SDRAM DIMM Bus Probe/Extender Card, vendor part number FS2320. The customer may purchase this probe from the manufacturer. Probe hardware does not ship with the board.

HP Logic analyzer connection to the PCI bus is accomplished using a FuturePlus PCI Local Bus Passive Analysis Probe, vendor part number FS2005. The customer may purchase this probe from the manufacturer. Probe hardware does not ship with the board.

2.13 Duplicated Controls

The board is equipped with connectors which allow the use of power and reset push button switches and of a power-good LED on a chassis (remote from the board). The board is also equipped with power and reset push buttons and with a power-good LED on the board, so that the remote connections are not required when the chassis is not in use.

2.14 Form Factor and Case

The PPC405EP board is designed to the ATX form factor. This choice allows use in a case and with power supplies that are currently widely available, and which are expected to remain available for several years. The ATX form factor was introduced as a modification of the Baby AT form factor, to provide improved user access to the motherboard and to reduce manufacturing costs. At this time, the use of the ATX form factor in the market is increasing, and it is expected to become the dominant form factor within the next year. Figure 2-5 illustrates the general layout within an ATX chassis.

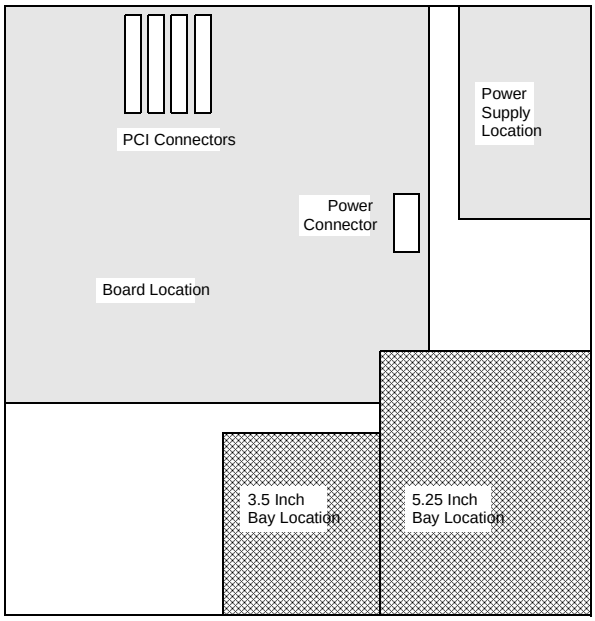


Figure 2-5. Locations Within ATX Chassis

The ATX form factor allows for 7 expansion slots, ISA and PCI in any combination. For the PPC405EP board, there are four PCI slots and no ISA slots.

Board dimensions and mounting hole locations comply with Figure 2-6.

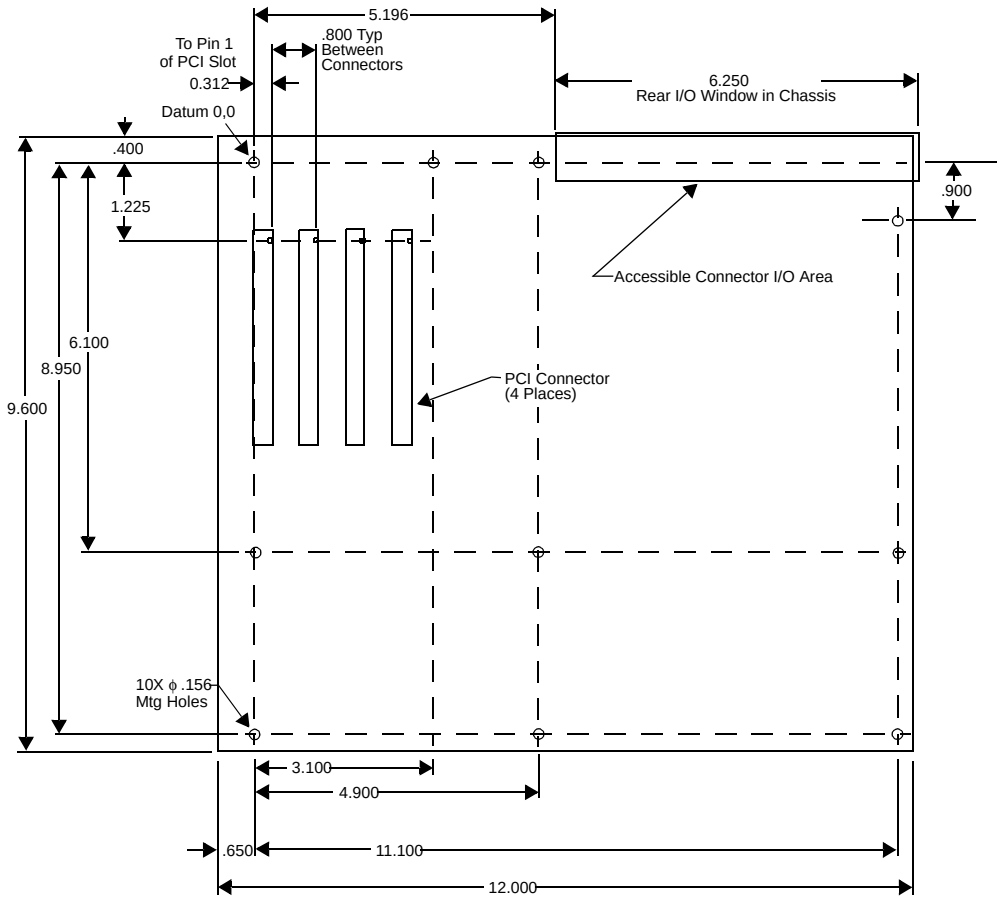


Figure 2-6. Board Dimensions and Hole Locations

To insure that the populated board fits in any standard ATX chassis and to insure that no interference occurs with full-length PCI adapter cards, components on the board must comply with height restrictions. Those restrictions are specified in Figure 2-7.

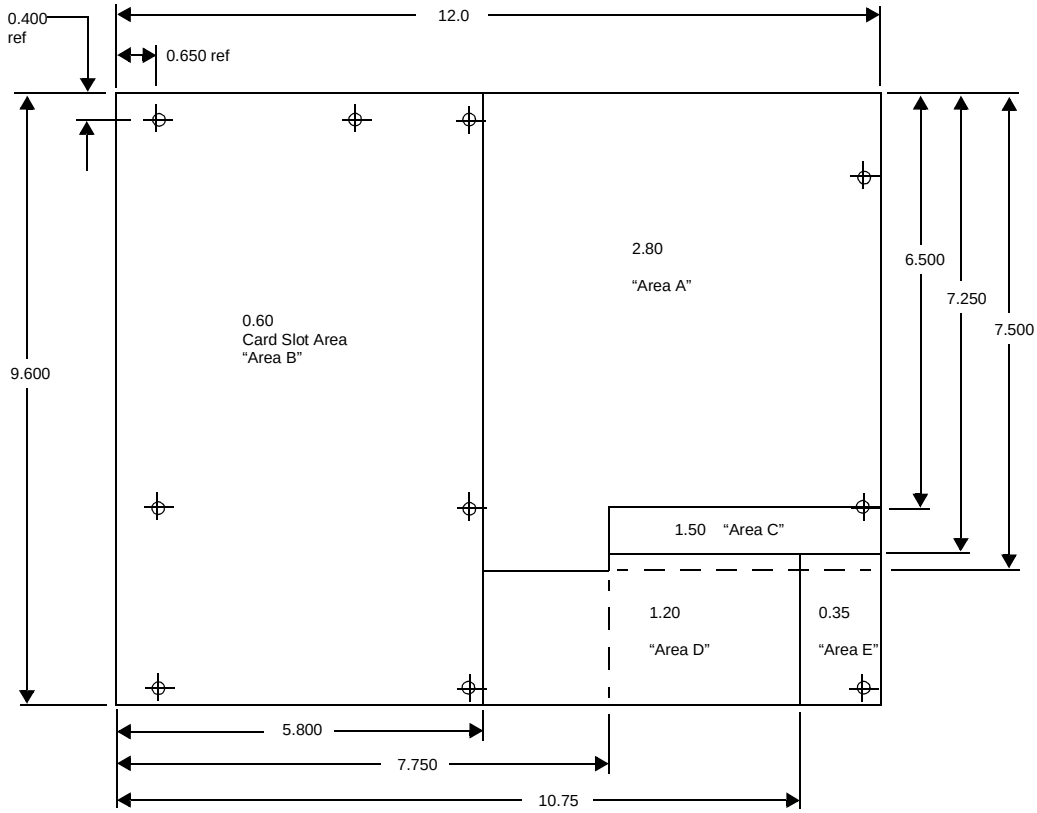


Figure 2-7. Component Height Restrictions

The ATX form factor defines a back panel area for motherboard I/O connectors. The PPC405EP board will mount two serial port connectors, a keyboard connector, a mouse connector, an Ethernet connector, and IR port optics in that area. (A reset push button will be present on the chassis front panel, not in the back panel connector area.) I/O Connector placement must comply with Figure 2-8.

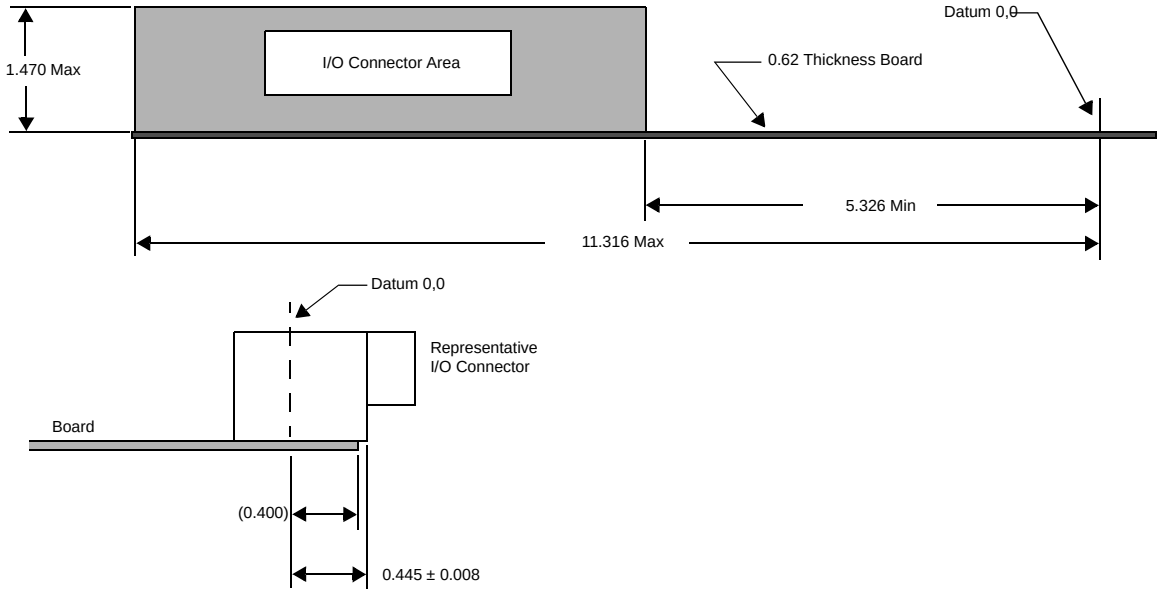


Figure 2-8. I/O Connector Placement

2.15 Power Supply

The ATX specification also covers the case and the power supply, so that a matched system is assured. The ATX supply is intended to provide a source of processor cooling air, to eliminate the need for auxiliary fans. The board-mounted power connector is a Molex 39-29-9202 or equivalent. The connector pinout is described in "Power Connector" on page 10-23.

2.16 PPC405EP Processor Power

The PPC405EP chip requires two voltages, +1.8V and +3.3V. In this board design, both voltages are derived from the standard +5V input. There are separate adjustable voltage regulators for each voltage. Individual adjustable regulators are provided to facilitate experimentation with speed sorts which might have optimal supply voltages other than the nominal values. The +3.3V adjustment is located at RV1. The +1.8V adjustment is located at RV2. A jumper at J30 must be installed for the adjustments to be functional. Current measurement test points are provided for both voltages. Zero-ohm resistors must be removed from the board to use these measurement points.

Chapter 3. Memory Map

Table 3-1 summarizes address space usage relating to the control registers on the board.

Table 3-1. PPC405EP Address Space Usage

Function	Start Address	End Address	Size
NVRAM/RTC Registers (See Table 3-2 on page 3-1)	0xF0000000	0xF0001FFF	8KB
FPGA_REG_0 (See Table 3-3 on page 3-2 and Table 3-4 on page 3-3)	0xF0300000	0xF0300000	1B
FPGA_REG_1 (See Table 3-3 on page 3-2 and Table 3-5 on page 3-4)	0xF0300001	0xF0300001	1B
ROM	0xFFF00000	0xFFFFFFFF	1MB
Socketed Flash	0xFFF8_0000	0xFFFFFFFF	512KB (socketed Flash and SRAM can be exchanged in the address space by a switch)
SRAM	0xFFF00000	0xFFF7FFFF	512KB (socketed Flash and SRAM can be exchanged in the address space by a switch)

3.1 Registers Indirectly Accessed Via Memory

Table 3-2. NVRAM/RTC Registers

Register	Address	R/W	Description
NVRAM	0xF0000000–0xF0001FF7	R/W	Non-volatile memory
RTC_CONTROL	0xF0001FF8	R/W	RTC Century Register
RTC_SECONDS	0xF0001FF9	R/W	RTC Seconds Register
RTC_MINUTES	0xF0001FFA	R/W	RTC Minutes Register
RTC_HOUR	0xF0001FFB	R/W	RTC Hour Register
RTC_DAY	0xF0001FFC	R/W	RTC Day Register

Table 3-2. NVRAM/RTC Registers (cont.)

Register	Address	R/W	Description
RTC_DATE	0xF0001FFD	R/W	RTC Date Register
RTC_MONTH	0xF0001FFE	R/W	RTC Month Register
RTC_YEAR	0xF0001FFF	R/W	RTC Year Register

Table 3-3. FPGA Registers

Register	Address	R/W	Description
FPGA_REG_0	0xF0300000	R	Interrupt status. (See Table 3-4 on page 3.)
FPGA_REG_1	0xF0300001	R/W	Interrupt enable. (See Table 3-5 on page 4.)

Table 3-4. FPGA_REG_0

Bit	Name	Description
0 (msb)	F_RANGE	1 = 50–100 MHz 0 = 100–200 MHz (default)
1		Spare
2		1 = Disable external interface 0 = Enable external interface
3		Spare
4		Spare
5		LED0 Indicator: 1 = on, 0 = off
6		LED1 Indicator: 1 = on, 0 = off
7 (lsb)		LED2 Indicator: 1 = on, 0 = off

Table 3-5. FPGA_REG_1

Bit	Name	Description (0 = closed, 1 = open)
0 (msb)	SPREAD_SPECTRUM_SEL	Spread spectrum clocking 0 = Enable 1 = Disable
1		PCI Clock Select 0 = On board 1 = External
2 3	MASTER_CLK_SEL1 MASTER_CLK_SEL0	Master clock select SEL1 SEL0 0 0 = 33MHz 0 1 = 66MHz 1 0 = 100MHz 1 1 = 133MHz
4		PCI arbiter select 0 = FPGA external 1 = PPC405EP internal
5		PCI frequency select 0 = Force PCI 33.33MHz 1 = Allow PCI 66.66MHz
6		On-board Flash 0 =Enabled) 1 =Disabled
7 (lsb)		Flash/SRAM address select 0 =High address 1 =Low address

Chapter 4. Programming the PPC405EP Memory Controller

This chapter provides guidance on programming the PPC405EP memory controller to work with the board design.

4.1 SDRAM Banks 0-1

In general, the controller settings for SDRAM are determined after reading the characteristics of the installed DIMM by reading the Serial Presence Detect EEPROM on the DIMM using the IIC interface. The following DIMM is the part which will ship with the product. Market conditions may necessitate the need to ship a compatible DIMM replacement in the future.

- Generic 168 pin, PC-100 compatible SDRAM DIMM (16M x 64, 128 MB)

The Serial Presence Detect EEPROM used on the above DIMMs is the Microchip 24LCS52 or a similar IIC EEPROM device. The IIC addresses used to access the EEPROM are as follows:

Table 4-1. Serial Presence Detect EEPROM Addresses

Description	Write	Read
Normal read and write operations	0xAA	0xAB
Software write protect register	0x60	not defined

The sequence of IIC transactions required to read the first 128 bytes from the SPD EEPROM is presented in Table 4-2.

Table 4-2. IIC Procedure to Read SPD Information

Step	Action
1	Issue IIC START.
2	Issue IIC address of 0xA0.
3	Write the EEPROM starting address of 0.
4	Issue IIC START.
5	Issue IIC address of 0xA1.
6-132	Read 127 bytes from EEPROM with IIC ACK.
133	Read 1 byte from EEPROM without IIC ACK.
134	Issue IIC STOP.

The 128 bytes returned from the Serial Presence Detect EEPROM for the Micron (16M x 64) part are covered by Table 4-4. Note in particular Byte 5 in the table. This indicates whether the DIMM is single-sided (requiring only PPC405EP SDRAM banks 0 and 2) or double-sided (requiring all PPC405EP SDRAM banks 0 through 3). The shipping memory is single-sided, so that SDRAM banks 1 and 3 will be disabled when that DIMM is used. Byte 31 of Table 4-4 on page 4-3 indicates

the number of bytes per side, where byte 31 = 0x10 for 64 MB per side and byte 31 = 0x20 for 128 MB per side.

4.1.1 SDRAM Addressing Modes

There is potential for confusion in Byte 17 of Table 4-4 on page 4-3. Individual SDRAM chips contain “banks” that are used to improve throughput. There are typically either 2 or 4 of these banks; the number is indicated by Byte 17. This number is used to set the SDRAM mode in the PPC405EP SDRAM0_BxCR registers. This number does not indicate the number of PPC405EP memory banks which must be configured for this SDRAM.

The SDRAM mode must be set for each SDRAM bank in PPC405EP register fields SDRAM0_BxCR[AM]. The mode is obtained from the SPD output by finding the number or Rows (byte 3), the number of Columns (byte 4), and the number of SDRAM Internal Banks (byte 17), and then referring to Table 4-3.

Table 4-3. Mode Definitions for Register DAM

Mode	SDRAM Configuration from SPD EEPROM — Rows x Columns (Internal Banks) — SPD byte 3 x byte 4 (byte 17)
1	11 x 9 (2) 11 x 10 (2)
2	12 x 9 (4) 12 x 10 (4)
3	13 x 9 (4) 13 x 10 (4) 13 x 11 (4)
4	12 x 8 (2) 12 x 8 (4)
5	11 x 8 (2) 11 x 8 (4)
6	13 x 8 (2) 13 x 8 (4)
7	13 x 9 (2) 13 x 10 (2)

Table 4-4. Serial Presence-Detect Matrix

Byte	Description	Entry (Version)	Symbol	Hex
0	NUMBER OF BYTES USED BY MICRON	128		80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		08
2	MEMORY TYPE	SDRAM		04
3	NUMBER OF ROW ADDRESSES	12		0C
4	NUMBER OF COLUMN ADDRESSES	10		0A
5	NUMBER OF BANKS	1 or 2		02
6	MODULE DATA WIDTH	64		40
7	MODULE DATA WIDTH (continued)	0		00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		01
9	SDRAM CYCLE TIME (CAS LATENCY = 3)	7 (-13E) 7.5 (-133) 8 (-10E)	tCK	70 75 80
10	SDRAM ACCESS FROM CLOCK (CAS LATENCY = 3)	5.4 (-13E/-133) 6 (-10E)	tAC	54 60
11	MODULE CONFIGURATION TYPE	NONPARITY		00
12	REFRESH RATE/TYPE	15.6µs/SELF		80
13	SDRAM WIDTH (PRIMARY SDRAM)	8		08
14	ERROR-CHECKING SDRAM DATA WIDTH	NONE		00
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	tCCD	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4		04
18	CAS LATENCIES SUPPORTED	2, 3		06
19	CS# LATENCY	0		01
20	WE# LATENCY	0		01
21	SDRAM MODULE ATTRIBUTES	NONBUFFERED		00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0E
23	SDRAM CYCLE TIME (CAS LATENCY = 2)	7.5 (-13E) 10 (-133/-10E)	tCK	75 A0
24	SDRAM ACCESS FROM CLK (CAS LATENCY = 2)	54 (-13E) 6 (-133/-10E)	tAC	54 60
25	SDRAM CYCLE TIME (CAS LATENCY = 1)		tCK	00

Table 4-4. Serial Presence-Detect Matrix (cont.)

Byte	Description	Entry (Version)	Symbol	Hex
26	SDRAM ACCESS FROM CLK (CAS LATENCY = 1)		tAC	00
27	MINIMUM ROW PRECHARGE TIME	15 (-13E) 20 (-133/-10E)	tRP	0F 14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	14 (-13E) 15 (-133) 20 (-10E)	tRRD	0E 0F 14
29	MINIMUM RAS# TO CAS# DELAY	15 (-13E) 20 (-133/-10E)	tRCD	0F 14
30	MINIMUM RAS# PULSE WIDTH	45 (-13E) 44 (-133) 50 (-10E)	tRAS	2D 2C 32
31	MODULE BANK DENSITY	128MB		20
32	COMMAND AND ADDRESS SETUP TIME	1.5 (-13E/-133) 2 (-10E)	tAS, tCMS	15 20
33	COMMAND AND ADDRESS HOLD TIME	0.8 (-13E/-133) 1 (-10E)	tAH, tCMH	08 10
34	DATA SIGNAL INPUT SETUP TIME	1.5 (-13E/-133) 2 (-10E)	tDS	15 20
35	DATA SIGNAL INPUT HOLD TIME	0.8 (-13E/-133) 1 (-10E)	tDH	08 10
36-61	RESERVED			00
62	SPD REVISION	REV. 1.2		12
63	CHECKSUM FOR BYTES 0-62	-13E -133 -10E		68/69 AE/AF F6/F7
64	MANUFACTURER'S JEDEC ID CODE	MICRON		2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)			FF
72	MANUFACTURING LOCATION			01 02 03 04 05 06
73-90	MODULE PART NUMBER (ASCII)			xx
91	PCB IDENTIFICATION CODE			01 02 03 04

Table 4-4. Serial Presence-Detect Matrix (cont.)

Byte	Description	Entry (Version)	Symbol	Hex
92	IDENTIFICATION CODE (CONT.)	0		00
93	YEAR OF MANUFACTURE IN BCD			xx
94	WEEK OF MANUFACTURE IN BCD			xx
95-98	MODULE SERIAL NUMBER			xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)			
126	SYSTEM FREQUENCY	100 MHz (-13E/-133/ -10E)		64
127	SDRAM COMPONENT AND CLOCK DETAIL			AF/FF

4.1.2 SDRAM Controller Initialization

Initialize the SDRAM controller as follows:

- Program SDRAM timings in register SDRAM0_TR as shown in Table 4-5 on page 4-7 (the table assumes the shipping DIMM, generic PC133 128M single-sided).
- Program SDRAM bank 0 using register SDRAM0_B0CR as shown in Table 4-6 on page 4-8. The table is shown for the shipping DIMM. For other parts, bank size is half of SPD byte 5 * decoded value of byte 31, where byte 31 = 0x10 for 64 MB per side and 0x20 for 128 MB per side.
- If DIMM is single-sided, program register SDRAM0_B2CR like SDRAM0_B0CR, but with the proper base address (for general DIMMs, base address from SDRAM0_B0CR plus bank size determines SDRAM0_B2CR base address). Program SDRAM0_B1CR[BE] = 0 and SDRAM0_B3CR[BE] = 0 to disable those banks.
- Program register SDRAM0_RTR (hi-order halfword including field IV) with 0x07F0 if SDRAM clock frequency (PLB clock frequency) is 133MHz. Program with 0x05F0 if the frequency is 100 MHz.
- Program the FPGA_BRDC SDRAM Frequency Range Select bit to 0b1 if the SDRAM clock frequency is less than 100 MHz.
- Insure that at least 200µs have elapsed since reset.
- Enable SDRAM in register SDRAM0_CFG as shown in Table 4-7 on page 4-8.

Table 4-5. Settings for Register SDRAM0_TR

Field	Value (bin)	Comment
CASL	01 (2 clks) 10 (3 clks)	CAS_ Latency 00=reserved 01=2 clocks 10=3 clocks 11=4 clocks
PTA	01 (100MHz) 10 (133MHz)	Precharge to Active (tRP) 00=reserved 01=2 clocks 10=3 clocks 11=4 clocks
CTP	10 (100MHz) 11 (133MHz)	Read/Write to Pre-charge (tRC-tRP-tRCD) 00=reserved 01=2 clocks 10=3 clocks 11=4 clocks
LDF	01	Command Leadoff 00=reserved 01=2 clocks 10=3 clocks 11=4 clocks
RFTA	011 (100MHz) 101 (133MHz)	Refresh to Activate (tRC) 000=4 clocks 001=5 clocks 010=6 clocks 011=7 clocks 100=8 clocks 101=9 clocks 110=10 clocks 111=reserved
RCD	01 (100MHz) 01 (133MHz)	Activate to Read/Write Command (tRCD) 00=reserved 01=2 clocks 10=3 clocks 11=4 clocks

Table 4-6. Settings for Register SDRAM0_B0CR

Field	Value (bin)	Comment
BA	0000 0000 00	base address
SZ	100 (64MB)	bank size
AM	001 (mode 2)	addressing mode. See discussion in Section 4.1.1 on page 4-2.
BE	1	bank enabled

Table 4-7. Settings for Register SDRAM0_CFG

Field	Value (bin)	Comment
DCE	1	Setting DCE causes the hardware initialization sequence to be sent to the SDRAM. The sequence is documented in Table 4-8 on page 4-9. SDRAM requires a hardware initialization sequence after reset. SDRAM vendors specify a time (typically 100-200µs) after reset before the sequence may be performed. The DCE bit must remain clear for at least that time. All other SDRAM configuration registers may be setup during the wait.
SRE	0	self-refresh mode disabled
PME	0	power management disabled
DRW	00	32-bit SDRAM width
BRPF	01	burst read/prefetch granularity

Table 4-8. SDRAM Hardware Initialization Sequence

Step	Action
1	Issue Precharge command to all banks
2	Wait minimum defined by PTA
3	Perform 8 CBR refresh cycles (each separated by RFTA clock cycles)
4	Issue Mode Register Write Command
5	Perform 8 CBR refresh cycles (each separated by RFTA clock cycles)
6	Wait RFTA clock cycles
7	SDRAM available for access

4.2 Peripheral Bus Timings

Program register bit EBCR[ATC] = 1. This causes the peripheral address bus to hold its last used value active when the bus is idle. This setting applies to all peripheral banks.

The following timings all assume that the peripheral bus frequency is 66 MHz. At lower bus frequencies, these timings should still work, though with sub-optimum throughput.

4.2.1 Peripheral Bank 0, Flash, and SRAM

Initialize Peripheral Bank 0, Flash, and SRAM as follows:

- Program timings in register EBC0_B0AP as shown in Table 4-9. Since Flash and SRAM are sharing the same bank, all timings are the slowest required by either memory.
- Set the base address and enable the bank by programming register EBC0_B0CR as shown in Table 4-10.

Table 4-9. Settings for Register EBC0_B0AP, Flash and SRAM

Field	Value (bin)	Comment
BME	0 (disable)	Burst mode enable
TWT	0x08	Transfer wait
CSN	00	Chip select on
OEN	00	Output enable on
WBN	01	Write byte enable on
WBF	10	Write byte enable off
TH	000	Transfer hold
RE	0 (disabled)	Ready enable
SOR	0	Sample on ready
BEM	0 (write)	Byte enable mode
PEN	0 (disable)	Parity enable

Table 4-10. Settings for Register EBC0_B0CR, Flash and SRAM

Field	Value (bin)	Comment
BAS	0xFFF	Base address
BS	000 (1MB)	Bank size
BU	11 (R/W)	Bus usage
BW	00 (8-bit)	Bus width

4.2.2 Peripheral Bank 1, NVRAM/RTC

Initialize Peripheral Bank 1 and NVRAM/RTC as follows:

- Program timings in register EBC0_B1AP as shown in Table 4-11.
- Set the base address and enable the bank by programming register EBC0_B1CR as shown in Table 4-12.

Table 4-11. Settings for Register EBC0_B1AP, NVRAM/RTC

Field	Value (bin)	Comment
BME	0 (disable)	Burst mode enable
TWT	0x08	Transfer wait
CSN	01	Chip select on
OEN	00	Output enable on
WBN	00	Write byte enable on
WBF	01	Write byte enable off
TH	000	Transfer hold
RE	0 (disabled)	Ready enable
SOR	0	Sample on ready
BEM	0 (write)	Byte enable mode
PEN	0 (disable)	Parity enable

Table 4-12. Settings for Register EBC0_B1CR, NVRAM/RTC

Field	Value (bin)	Comment
BAS	0xF00	Base address
BS	000 (1MB)	Bank size
BU	11 (R/W)	Bus usage
BW	00 (8-bit)	Bus width

4.2.3 Peripheral Bank 4, FPGA Registers

Initialize Peripheral Bank 4 and the FPGA registers as follows:

- Program timings in register EBC0_B4AP as shown in Table 4-13.
- Set the base address and enable the bank by programming register EBC0_B4CR as shown in Table 4-14.

Table 4-13. Settings for Register EBC0_B4AP, FPGA Registers

Field	Value (bin)	Comment
BME	0 (disable)	Burst mode enable
TWT	0x03	Transfer wait
CSN	00	Chip select on
OEN	01	Output enable on
WBN	01	Write byte enable on
WBF	01	Write byte enable off
TH	000	Transfer hold
RE	0 (disabled)	Ready enable
SOR	0	Sample on ready
BEM	0 (write)	Byte enable mode
PEN	0 (disable)	Parity enable

Table 4-14. Settings for Register EBC0_B4CR, FPGA Registers

Field	Value (bin)	Comment
BAS	0xF03	Base address
BS	000 (1MB)	Bank size
BU	11 (R/W)	Bus usage
BW	00 (8-bit)	Bus width

4.2.4 Peripheral Banks 2-3, Spares

Initialize Peripheral Banks 2-3 and the Spares as follows:

- Disable the banks by programming registers EBC0_B2CR and EBC0_B3CR as shown in Table 4-15.

Table 4-15. Settings for Registers EBC0_B2CR-EBC0_B3CR, Spares

Field	Value (bin)	Comment
BAS	0x000	base address
BS	000 (1MB)	bank size
BU	00 (disabled)	bus usage
BW	00 (8-bit)	bus width

Chapter 5. Reset and Interrupts

Reset is generated at power-on, by the reset pushbutton, by system-reset from the PPC405EP (usually in response to a command from the RICWatch debugger), or by undervoltage on either the +5V or +3.3V supplies.

The are 7 external interrupt inputs to the PPC405EP. A critical interrupt pushbutton is routed through the FPGA to IRQ1, which should be programmed as critical within the PPC405EP. IRQ0 is a spare. IRQ3–IRQ6 are connected to PCI card slots. More detail about these interrupts is given in Table 5-1.

Table 5-1. Interrupts

PPC405EP Signal	PPC405EP UIC Bit	Description
IRQ0	25	Spare
IRQ1	26	Generated by the FPGA in response to Expansion Interface interrupts. IRQ1 is active-high from FPGA to PPC405EP. Expansion Interface is active-low, edge-triggered from board to FPGA.
IRQ2	27	Generated by the FPGA in response to the critical interrupt signal SW_SMI_N from a board pushbutton. IRQ2 is active-high from FPGA to PPC405EP. SW_SMI_N is active-low, edge-triggered from board to FPGA.
IRQ3	28	Generated by any interrupt A-D from PCI slot 3. IRQ3 is negative level sensitive.
IRQ4	29	Generated by any interrupt A-D from PCI slot 2. IRQ4 is negative level sensitive.
IRQ5	30	Generated by any interrupt A-D from PCI slot 1. IRQ5 is negative level sensitive.
IRQ6	31	Generated by any interrupt A-D from PCI slot 0. IRQ6 is negative level sensitive.

Chapter 6. Switches

The board contains power, reset, and SMI pushbutton switches. Additionally, the board contains an octal bit switch for setting the configuration of the PPC405EP chip and certain board functions. Figure 6-1 shows the location of each switch.

Table 6-1. Switch List

Loc	Function	Page
S1	Power Pushbutton Switch	6-3
S2	Reset Pushbutton Switch	6-3
S3	SMI Pushbutton Switch	6-3
S4	PPC405EP Strapping Switches	6-4
	Board Strapping Switches	6-4

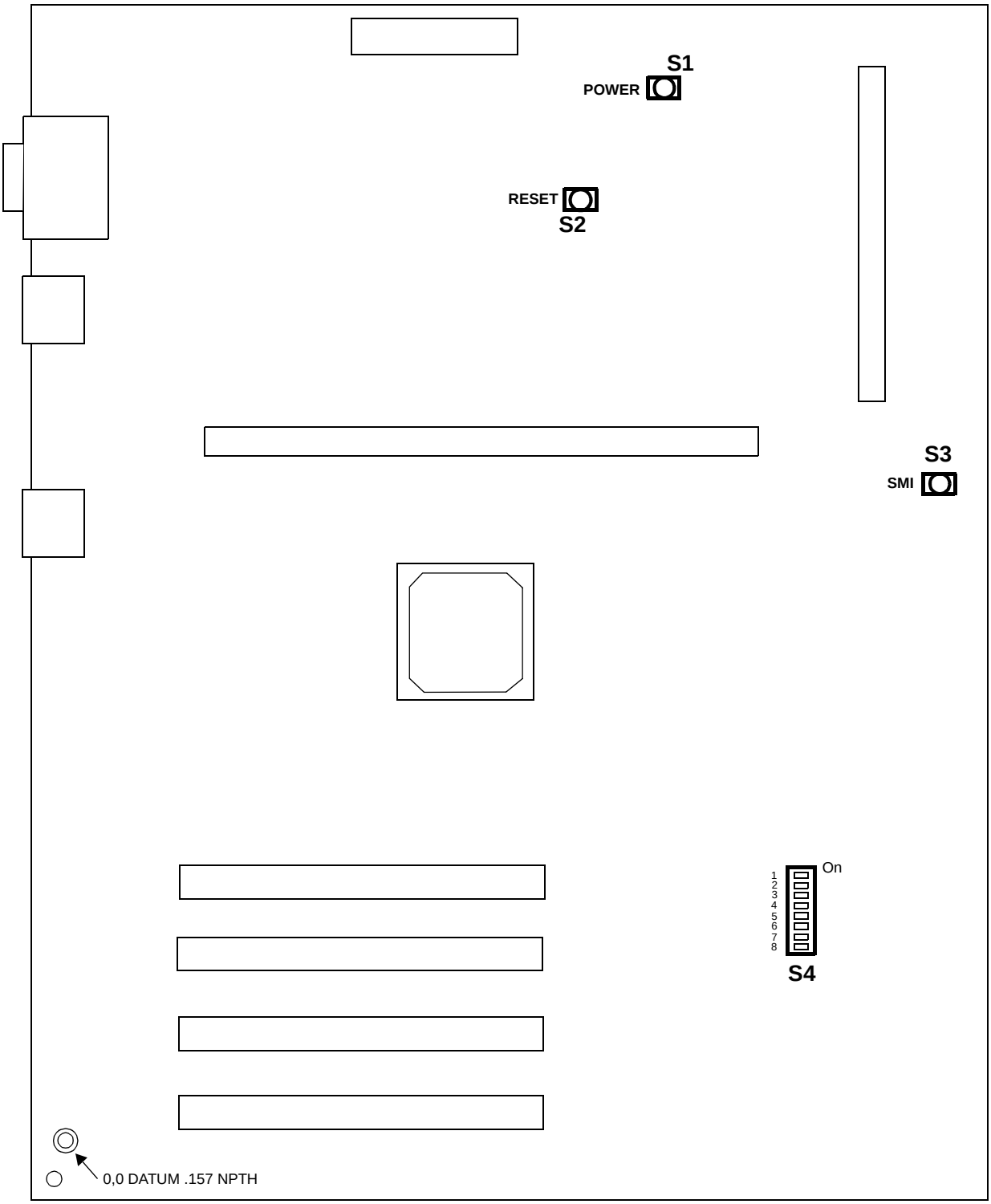


Figure 6-1. Switch Location Diagram

6.1 Power Pushbutton Switch

The power pushbutton turns power on and off. A chassis mounted power switch can be connected in parallel with the board mounted switch through the connector at J6.

Table 6-2. Power Pushbutton—S1

Signal	Description (0 = switch on)
Generates PS_ON.	Active low signal that turns on +3.3V, +5V, -5V, +12V, and -12V. (POR state is high. Toggles when the switch is pressed.)

6.2 Reset Pushbutton Switch

The reset pushbutton initiates a general reset of the board and the processor. The reset occurs when the switch is pressed. A chassis mounted reset switch can be connected in parallel with the board mounted switch through the connector at J9.

Table 6-3. Reset Pushbutton—S2

Signal	Description (0 = switch on)
Generates RESET_N	Main board reset.

6.3 SMI Pushbutton Switch

The SMI switch initiates a system maintenance interrupt to the processor. The interrupt is level sensitive and occurs when the switch is released.

Table 6-4. SMI Pushbutton—S3

Signal	Description (0 = switch on)
SW_SMI_N	System Maintenance Interrupt to processor

6.4 PPC405EP Strapping Switches

Positions 1–3 of the 8-position DIP switch at S4 are read by the PPC405EP at reset to determine the chip's configuration. A detailed description of the setting of these switches is found in "Strapping Options" on page 2-2.

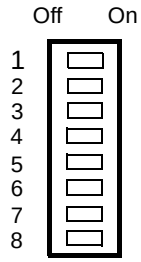


Figure 6-2. Strapping Switch

Settings for positions 4–8 of S4 are described in "Board Strapping Switches" below.

6.5 Board Strapping Switches

Positions 4–8 of the 8-position DIP switch at S4 allows selection of various clock sources and memory mappings. See "Strapping Options" on page 2-2 for the settings for positions 1–3.

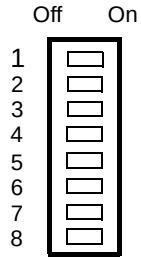


Figure 6-3. Strapping Switch

Table 6-5. Board Strapping Switches—S4

Switch Position	Signal	Description (0 = switch on)
4	PCI_FREQ_SEL	PCI Frequency Select. See Table 2-2, “Sys_Clk and PCI_Clk Selection,” on page 2-5 0 = Enable (factory setting) 1 = Disable
5	EXT_ARB_N	PCI Arbiter Select 0 = Internal arbiter (factory setting) 1 = External arbiter
6	PCI_CLK_SEL	PCI Clock Source Select 0 = External clock 1 = On-board clock (factory setting)
7	FLASH_ONBD_N	Boot Flash On-Board Switch 0 = P_CS0_N is delivered to on-board Flash and SRAM (factory setting) 1 = P_CS0_N is blocked from on-board Flash and SRAM. This signal is delivered to the Expansion Interface, so a boot device may be located there.
8	FLASH/SRAM_SEL	FLASH/SRAM Mapping Switch 0 = Flash mapped to 0xFFF8 0000 – 0xFFFF FFFF (boot) SRAM mapped to 0xFFF0 0000 – 0xFFF7 FFFF (factory setting) 1 = SRAM mapped to 0xFFF8 0000 – 0xFFFF FFFF (boot) Flash mapped to 0xFFF0 0000 – 0xFFF7 FFFF For ease in debugging Flash code by using software breakpoints, Flash may be copied to SRAM and the mapping reversed to put the SRAM in the boot location.

Chapter 7. Fuses, Batteries, and Regulators

The following sections contain detailed information on the fuses, batteries, and voltage regulator adjustments provided on the board.

7.1 Fuses

The fuses on the board are described in Table 7-1 and shown in Figure 7-2.

Table 7-1. Fuses — Board Mounted

Location	Size	Description
F1	4 A	Socketed fuse for +3.3V
F2	1 A	Socketed fuse for -12V
F3	4 A	Socketed fuse for +5V
F4	1 A	Socketed fuse for -5V
F5	1 A	Socketed fuse for +12V
C23	7 A	Surface mount fuse for PCI +5V
C19	7 A	Surface mount fuse for PCI +3.3V

7.2 PowerCap Battery

Power for the NVRAM and RTC is provided by a PowerCap module that is installed on top of the NVRAM/RTC module located at U17. The PowerCap module contains a lithium battery. To remove the battery from the board, remove the PowerCap as shown in Figure 7-1. The removal procedure is as follows:

1. Vertically insert the tip of a small screw driver into the slot at the edge of the PowerCap.
2. Slowly pull the screw driver handle back toward the opposite edge of the housing until the catch in the slot slot releases, allowing that edge of the PowerCap to lift up and away from the module base.
3. Continue lifting the PowerCap until the flange at the edge of the cap opposite from the slot disengages, allowing the cap to be completely removed from the module.

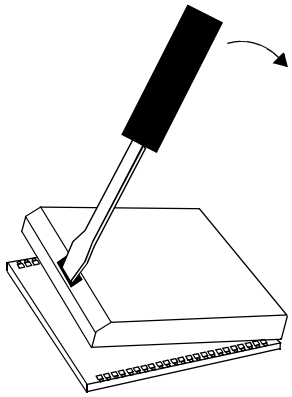


Figure 7-1. PowerCap Removal

7.3 Regulator Adjustments

Figure 7-2 shows the location of the +3.3V (RV1) and +1.8V (RV2) regulator adjustments and the jumper that enables them.

Table 7-2. Regulator Adjustments

Location	Voltage	Description
RV1	+3.3V	Regulator adjustment Adjustment range is +3.45V to +3.08V
RV2	+1.8V	Regulator adjustment Adjustment range is +1.89V to +1.67V
J30	Both	The jumper at this location must be installed for the regulator adjustments to be functional.

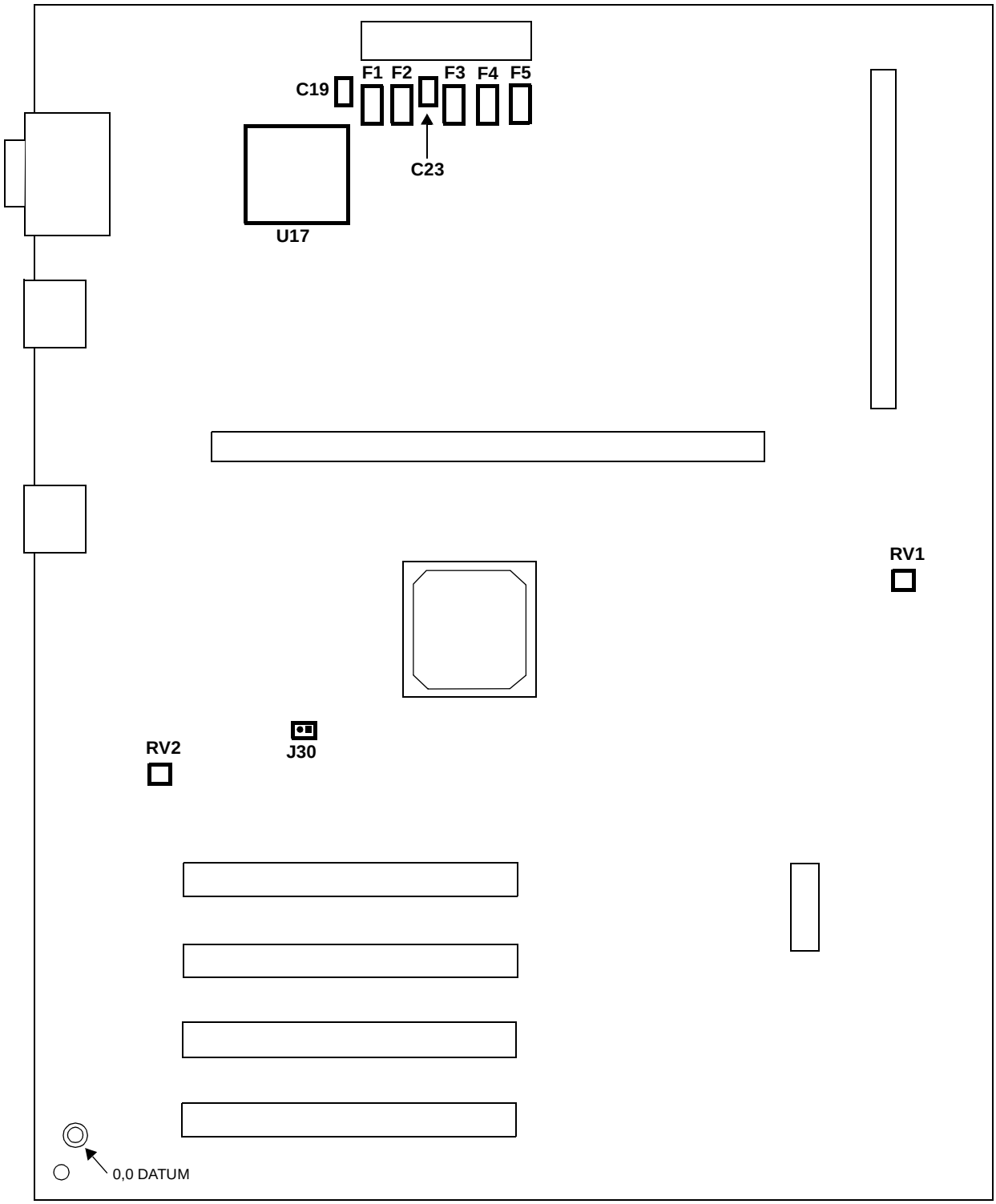


Figure 7-2. Fuse, Battery, and Regulator Location Diagram

Chapter 8. Displays

The LED displays provided on the board are described in Table 8-1 and shown in Figure 8-1.

Table 8-1. Displays

Name	Location	Color	Description
Power Good	DS1	Green	Lights when ATX power supply PWR_OK is asserted.
COL	DS2	Red	Lights when PHY1 Ethernet collision activity is detected (in half-duplex mode only).
100Mbps	DS3	Green	Lights when Ethernet PHY1 detects 100Mbps mode.
FDPOL	DS4	Amber	Lights to indicate PHY1 Full Duplex mode for Ethernet. (The PHY may be reconfigured by software to change this indicator to indicate 10Mbps link polarity inversion.)
FDPOL	DS5	Amber	Lights to indicate PHY0 Full Duplex mode for Ethernet. (The PHY may be reconfigured by software to change this indicator to indicate 10Mbps link polarity inversion.)
100Mbps	DS6	Green	Lights when Ethernet PHY0 detects 100Mbps mode.
COL	DS7	Red	Lights when PHY0 Ethernet collision activity is detected (in half-duplex mode only).
Machine Check	DS8	Red	Lights when the PPC405EP SYS_ERROR signal is asserted.
LED1	DS9	Green	Diagnostic LEDs These LEDs are wired to bits in FPGA register REG0. They give a visual indication of the state of the bit. The register bits can be set on or off as desired by the code running on the board. LED0 - bit 5 (FPGA_REG_05) LED1 - bit 6 (FPGA_REG_06) LED2 - bit 7 (FPGA_REG_07)
LED0	DS10	Green	
LED2	DS11	Green	
Ethernet PHY1 Status	J13	Yellow– Tx/Rx Activity Green– Link Status	Dual LEDs, part of the RJ-45 PHY1 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.
Ethernet PHY0 Status	J18	Yellow– Tx/Rx Activity Green– Link Status	Dual LEDs, part of the RJ-45 PHY0 Ethernet connector assembly, indicating Tx/Rx Activity and Link Status.

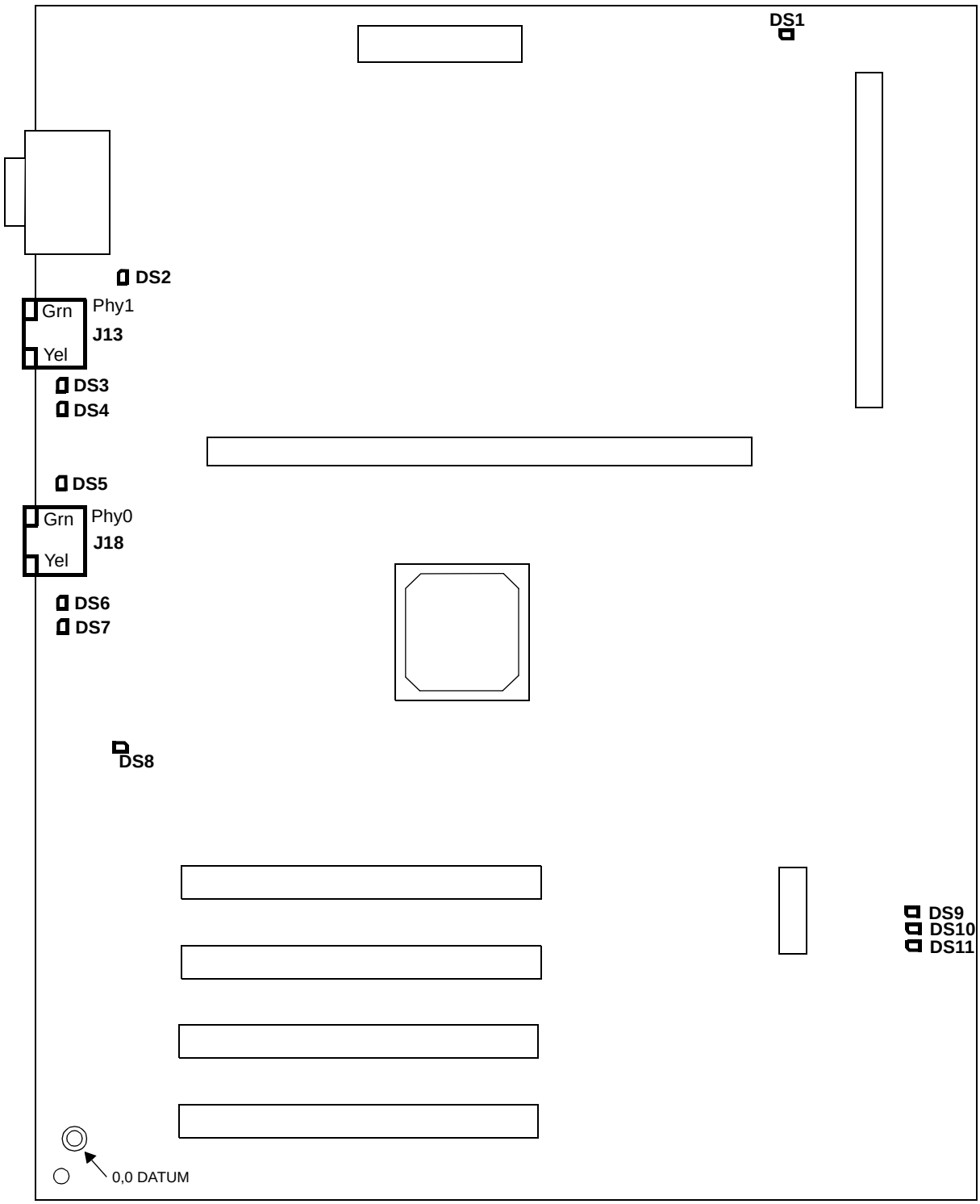


Figure 8-1. Display Connector Location Diagram

Chapter 9. Jumpers

The jumpers provided on the board are described in the following sections. The location and orientation of all jumpers are shown in Figure 9-1and Figure 9-2.

Table 9-1. Jumper List

Location	Description	Page
J11	Block Flash Writes	9-4
J14, J15, J25, J26	PHY Address Selection	9-4
J21	Clock Selection	9-5
J22, J24	System Clock Frequency	9-5
J30	Enable regulator adjustments	9-6
J41	PCI Target Mode Enable	9-6
R423, R424, R425, R426, R435, R436, R438, R439, R451, R452, R453, R454, R464, R465, R466, R467	PCI Socket Orientation	9-7
R275, R335, R352, R359, R365, R374, R494	+3.3V Current Measurements	9-7
R63, R67, R364, and R373	+1.8V Current Measurements	9-7

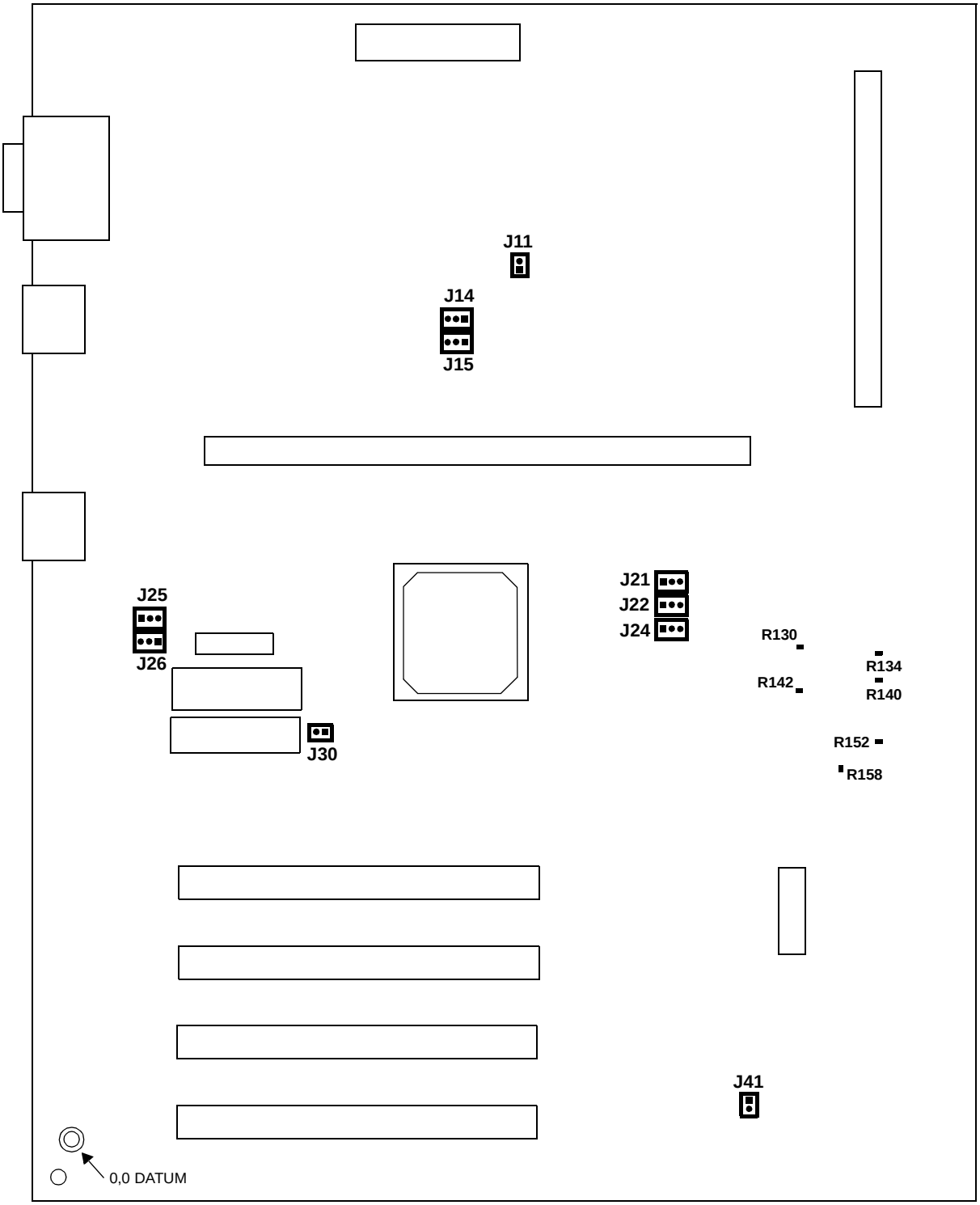


Figure 9-1. Jumper Locations—Top View

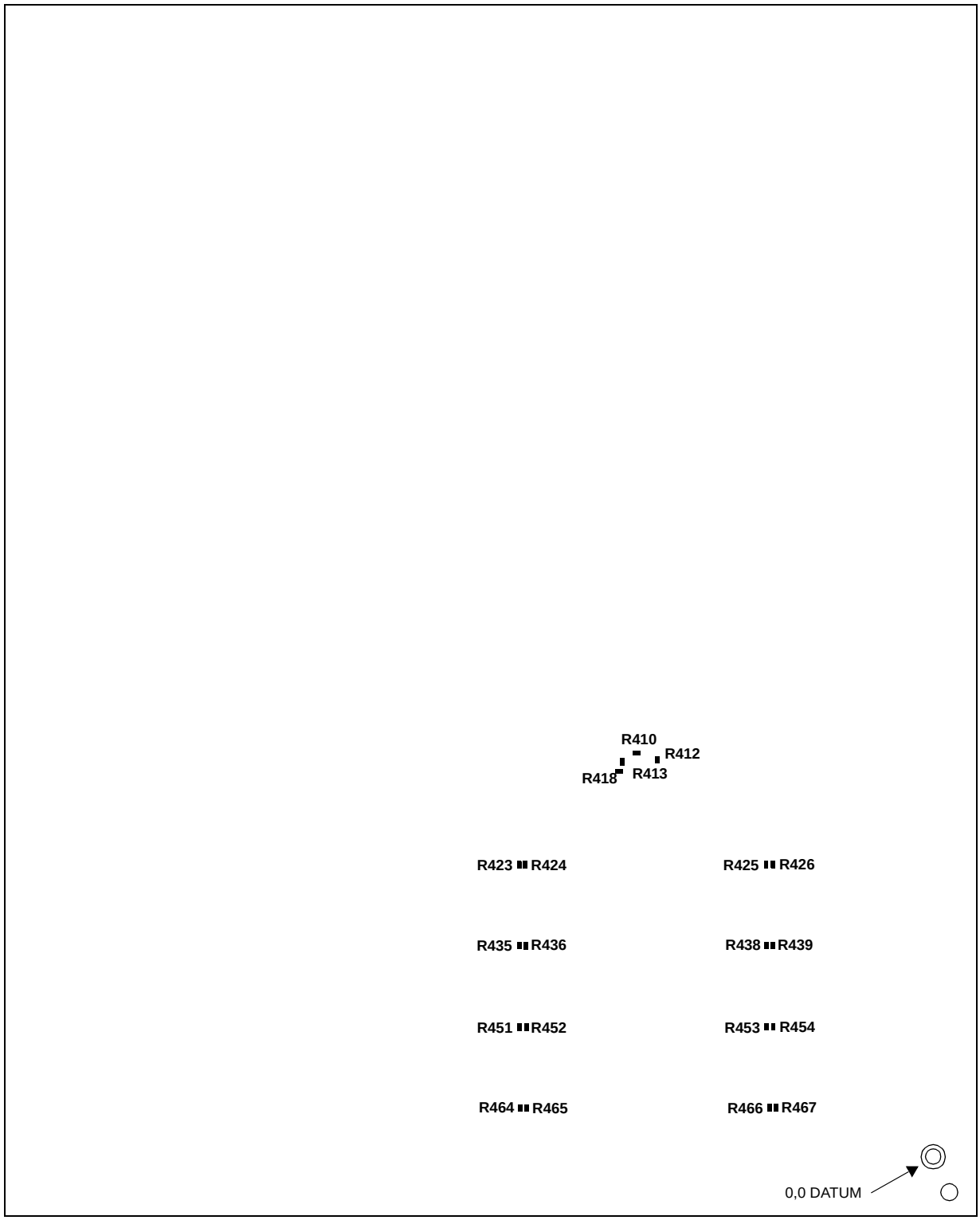


Figure 9-2. Jumper Locations—Bottom View

9.1 Block Flash Writes

Installing the jumper at J11 blocks write operations to the Flash memory.

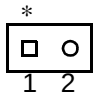


Figure 9-3. Block Flash Writes Jumper

Table 9-2. Block Flash Writes—J11

J11	Description	Factory Setting
1-2	Force PCI to run at 33.33 MHz	not installed

9.2 PHY Address Selection

The board contains two Ethernet PHYs—PHY0 and PHY1. The 5-bit address of the on-board Ethernet PHY is 0b000xx, where the two low order bits are set by jumpers PHYADD_Px(1) (J25 and J14) and PHYYADD_Px(0) (J26 and J15). If necessary, these jumpers may be changed to avoid PHY address conflicts. A PHY address of 0b00000 will isolate the local PHY. This is a 1x3 Berg type connector.

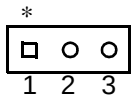


Figure 9-4. PHY Address Selection Jumpers

Table 9-3. PHY0 Address Selection Jumpers — J25, J26

J25, J26	Address	Factory Setting
2-3, 2-3	0b00000	
2-3, 1-2	0b00001	x
1-2, 2-3	0b00010	
1-2, 1-2	0b00011	

Table 9-4. PHY1 Address Selection Jumpers — J14, J15

J14, J15	Address	Factory Setting
2-3, 2-3	0b00000	
2-3, 1-2	0b00001	
1-2, 2-3	0b00010	x
1-2, 1-2	0b00011	

9.3 Clock Selection

If this jumper is installed, spread spectrum clocking can be used.

Figure 9-5. Clock Selection Jumper

Table 9-5. Clock Selection—J21

J21	Description	Factory Setting
1-2	Spread spectrum clocking	not installed

9.4 System Clock Frequency

Jumpers are installed at J22 and J24 as indicated in Table 9-6 to selected the system clock frequency. See Table 2-2, “Sys_Clk and PCI_Clk Selection,” on page 2-5.

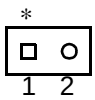


Figure 9-6. System Clock Frequency Jumper

Table 9-6. System Clock Frequency—J22, J24

J22, J24	Description	Factory Setting
1-2, 1-2	33.33 MHz	x
1-2, open	66.66 MHz	
open, 1-2	100.00 MHz	
open, open	133.33 MHz	

9.5 Voltage Regulator Adjustments

The +3.3V and +1.8V voltage regulators can be adjusted when this jumper is installed. See “Regulator Adjustments” on page 7-2.

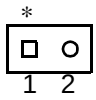


Figure 9-7. +1.8V Voltage Regulator Adjustment Jumper

Table 9-7. +1.8V Voltage Regulator Adjustment Jumper—J30

J30	Description	Factory Setting
1-2	Enables +3.3V and +1.8V voltage regulator adjustments	not installed

9.6 PCI Target Mode Enable

When this jumper is installed, the PCI interface functions as an adapter rather than a host.

Figure 9-8. PCI Target Mode Enable Jumper

Table 9-8. PCI Target Mode Enable Jumper—J41

J41	Description	Factory Setting
1-2	Enables PCI target mode	not installed

9.7 PCI Socket Orientation

The PCI sockets are installed into a non-standard board footprint which allows the orientation of the socket to be reversed. If the orientation is reversed, 3.3V PCI cards can be used. The normal shipping mode of the card has the sockets oriented to accept 5V, 33MHz PCI cards.

In order to change the orientation of the sockets, jumpers must be moved. These jumpers are zero-ohm resistors which set the VIO pins of the PCI socket to either 5V or 3.3V, matching the orientation. The correct population of these resistors is defined for 5V orientation by Table 9-9, and for 3.3V orientation by Table 9-10. The resistors are physically located on the bottom of the board. The sockets are on the top of the board.

Table 9-9. VIO Programming Resistors for 5V PCI Sockets

	PCI Slot 0 J42	PCI Slot 1 J38	PCI Slot 2 J36	PCI Slot 3 J35
Installed	R465 R466	R453 R452	R436 R438	R425 R424
Not installed	R467 R464	R454 R451	R435 R439	R426 R423

Table 9-10. VIO Programming Resistors for 3.3V PCI Sockets

	PCI Slot 0 J42	PCI Slot 1 J38	PCI Slot 2 J36	PCI Slot 3 J35
Installed	R467 R464	R454 R451	R435 R439	R426 R423
Not installed	R465 R466	R453 R452	R436 R438	R425 R424

9.8 Current Measurements

The following jumpers (zero-ohm resistors) must be removed from the board in order to use the current measurement connectors at J28 and J33.

Table 9-11. Current Measurement Resistor Removal

Location	Supply	Remove Resistors
J28	+3.3V	R130, R134, R140, R142, R152, and R158 (all on the top of the board)
J33	+1.8V	R410, R412, R413, and R418 (all on the bottom of the board)

Chapter 10. Connectors

The connector types and pin usage for board connectors are described in the following sections. The location and orientation of each connector on the board is shown in Figure 10-1.

Table 10-1. Connectors List

Location	Description	Page
J1, J3, J23, J34, J40, J43	Ground Connectors	10-9
J2	Power Good LED Connector	10-6
J4	Power Connector	10-23
J6	Power Pushbutton Connector	10-5
J7	Serial Port Connectors	10-3
J8, J12, J29	Logic Analyzer Connectors	10-13
J9	Reset Pushbutton Connector	10-5
J10	Expansion Interface Connector	10-19
J13, J18	Ethernet TWP Connectors	10-4
J16	SDRAM Connector	10-28
J17	IIC Connector	10-30
J20	External Clock Input Connector	10-7
J28, J33	Current Measurement Connectors	10-6
J27	RISCWatch JTAG Debugger Connector	10-10
J31	RISCTrace Connector	10-11
J35, J36, J38, J42	PCI Connectors	10-24
J37	FPGA JTAG Connector	10-12
J39	External PCI Clock Input Connector	10-8
TP1–TP100	Test Access	10-30
U14, U26, U28, U31, U33, U41, U47	Scope Connectors	10-31

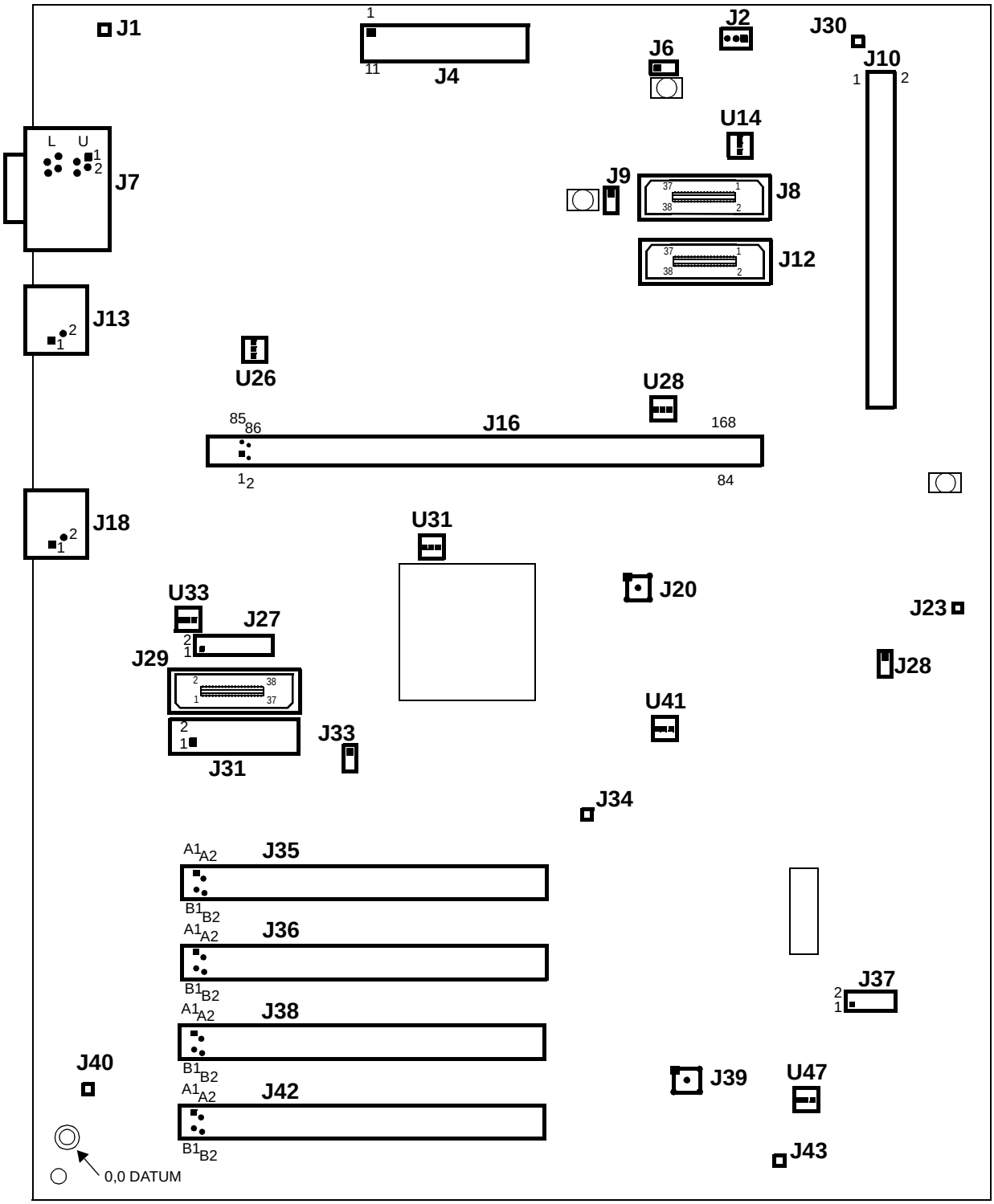


Figure 10-1. Connector Location Diagram

10.1 Serial Port Connectors

Serial Port 0 (J7 Lower) and Serial Port 1 (J7 Upper) are provided with standard nine-pin male D-shell connectors, as shown in Figure 10-2. Serial port 0 is driven by PPC405EP UART0, which provides a full set of modem control lines. Serial Port 1 is driven by PPC405EP UART1, which provides only Tx and Rx .

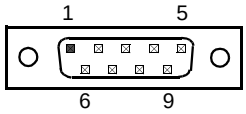


Figure 10-2. Nine-Pin Serial Port Connector

Table 10-2 describes the pin assignments for Serial Ports 0 and 1:

Table 10-2. Serial Port Connectors—J7 Lower, J7 Upper

Pin	Signal Name
1	DCD. Present on Serial Port 0 (lower) only.
2	RX
3	TX
4	DTR. Present on Serial Port 0 (lower) only.
5	GND
6	DSR. Present on Serial Port 0 (lower) only.
7	RTS. Present on Serial Port 0 (lower) only.
8	CTS. Present on Serial Port 0 (lower). only
9	RI. Present on Serial Port 0 (lower) only.

10.2 Ethernet TWP Connectors

This board provides 10BaseT and 100BaseTX Ethernet connections via Category 5 Unshielded Twisted Pair (UTP) cable using RJ-45 connectors.

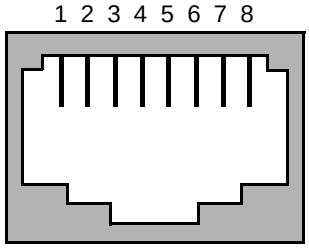


Figure 10-3. Ethernet UTP Connector

Table 10-3. Ethernet UTP Connector—J13, J18

Pin	Signal	Description
1	TxD+	Transmit Data +
2	TxD--	Transmit Data –
3	RxD+	Receive Data +
4	NC	No connection
5	NC	No connection
6	RxD--	Receive Data –
7	NC	No connection
8	NC	No connection

10.3 Reset Pushbutton Connector

The chassis-mounted Reset pushbutton connects to the board via this connector. This is a 1x2 Berg type connector.

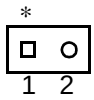


Figure 10-4. Reset Connector

Table 10-4. Reset Connector—J9

Pin	Signal Name
1	-RESET from chassis-mounted pushbutton
2	Ground

10.4 Power Pushbutton Connector

The chassis-mounted Power pushbutton connects to the board via this connector. The power supply on/off state toggles each time the Power Pushbutton is pressed. This is a 1x2 Berg type connector.

Figure 10-5. Power Pushbutton Connector

Table 10-5. Power Pushbutton Connector—J6

Pin	Signal Name
1	-TOGGLE_POWER from chassis-mounted pushbutton
2	Ground

10.5 Power Good LED Connector

This is a 1x3 Berg type connector.

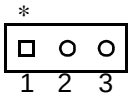


Figure 10-6. Power Good LED Connector

Table 10-6. Power Good LED Connector—J2

Pin	Signal Name
1	+5V thru pullup
2	Unused
3	Buffered PWR_OK

10.6 Current Measurement Connectors

There are current measurement points for +3.3V at J28 and +1.8V at J33. These are 1x2 Berg type connectors.

Note: Use of these connectors require the removal of zero-ohm jumpers (resistors). See “Current Measurements” on page 9-7.

Figure 10-7. Current Measurement Connector

Table 10-7. Current Measurement Connector—J28 and J33

Pin	Signal Name
1	Current –
2	Current +

10.7 External Clock Input Connector

The PPC405EP may be tested in a PLL bypass mode in which arbitrary clocks not available on the board may be required. These clocks may be provided by an external oscillator connected to this board-mounted SMA connector. The oscillator output should have 3.3V logic levels. The input impedance to this connector is approximately 50Ω.

.

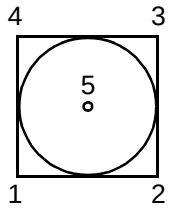


Figure 10-8. External Clock Input Connector

Table 10-8. External Clock Input Connector—J20

Pin	Signal Name
1	Ground
2	Ground
3	Ground
4	Ground
5	SYS_CLK

10.8 External PCI Clock Input Connector

The board PCI clock may be provided by an external oscillator connected to this board-mounted SMA connector. The oscillator output should have 3.3V logic levels. The oscillator will be loaded with approximately 50 Ohms by the board.

.

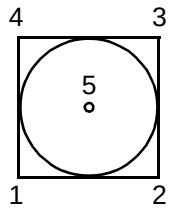


Figure 10-9. External Clock Input Connector

Table 10-9. External PCI Clock Input Connector—J39

Pin	Signal Name
1	Ground
2	Ground
3	Ground
4	Ground
5	PCI_EXT_ASYNC_CLK

10.9 Ground Connectors

Test points for grounding logic analyzers and other test equipment are available on these connectors. These are 1x1 Berg type connectors.

Figure 10-10. Ground Connectors

Table 10-10. Ground Connectors—J1, J3, J23, J34, J40, J43

Pin	Signal Name
1	GND

10.10 RISCWatch JTAG Debugger Connector

The RISCWatch JTAG debugger connects to the board through a 2x8-pin header at J27. This header is shown in Figure 10-11.

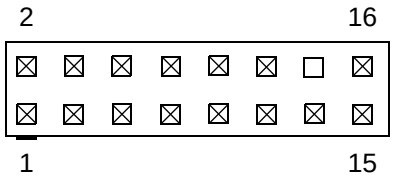


Figure 10-11. RISCWatch JTAG Connector

Pin usage is described in Table 10-11.

Table 10-11. RISCWatch Connector—J27

Pin	Signal Name
1	TDO
2	Unused
3	TDI
4	–TRST. From RISCWatch.
5	Unused
6	+POWER. This is a status signal, not a power source.
7	TCK
8	Unused
9	TMS
10	Unused
11	–HALT. From RISCWatch.
12	Unused
13	Unused
14	KEY. Pin in this location is removed.
15	Unused
16	GND

10.11 RISCTrace Connector

The RISCTrace feature connects to the board through a 2x10-pin header at J31. This header is shown in Figure 10-12.

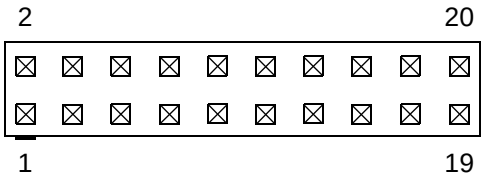


Figure 10-12. RISCTrace Connector

Pin usage is described in Table 10-12.

Table 10-12. RISCTrace Connector—J31

Pin	Signal Name
1	reserved
2	reserved
3	TRCCLK
4	reserved
5	reserved
6	reserved
7	reserved
8	reserved
9	reserved
10	reserved
11	reserved
12	TS1O
13	TS2O
14	TS1E
15	TS2E
16	TS3
17	TS4
18	TS5
19	TS6
20	GND

10.12 FPGA JTAG Connector

The FPGAs may be programmed in place on the board via this JTAG connector and appropriate downloading software. This is a 2x5 Berg type connector.

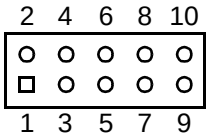


Figure 10-13. FPGA JTAG Connector

Table 10-13. FPGA JTAG Connector—J37

Pin	Signal Name
1	ISP_TCK
2	GND
3	ISP_TDO
4	+5V
5	ISP_TMS
6	unused
7	unused
8	unused
9	ISP_TDI
10	GND

10.13 Logic Analyzer Connectors

Connection to HP logic analyzers via HP E5346A High Density Probe Adapters is provided by the following board mounted Mictor connectors.

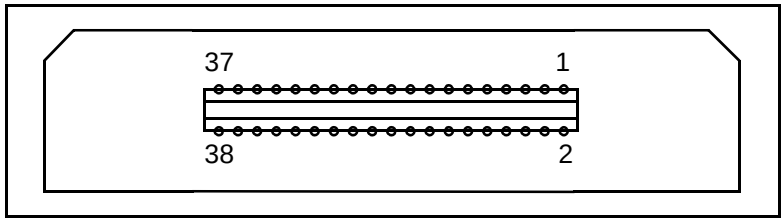


Figure 10-14. Logic Analyzer Connectors

Table 10-14. Logic Analyzer Connector, Peripheral Bus Data—J12

Pin	Analyzer	Signal Name
1	data_pod0 – +5VDC	unused
2	data_pod1 – SCL	unused
3	data_pod0 – GND DC	GND
4	data_pod1 – SDA	unused
5	data_pod0 – CLK	unused
6	data_pod1 – CLK	SYS_ERROR
7	data_pod0 – D15	P_DATA(0)
8	data_pod1 – D15	P_WBE_N(0)
9	data_pod0 – D14	P_DATA(1)
10	data_pod1 – D14	P_WBE_N(1)
11	data_pod0 – D13	P_DATA(2)
12	data_pod1 – D13	P_READY
13	data_pod0 – D12	P_DATA(3)
14	data_pod1 – D12	unused
15	data_pod0 – D11	P_DATA(4)
16	data_pod1 – D11	P_OE_N
17	data_pod0 – D10	P_DATA(5)
18	data_pod1 – D10	P_WE_N
19	data_pod0 – D9	P_DATA(6)
20	data_pod1 – D9	P_RNW

Table 10-14. Logic Analyzer Connector, Peripheral Bus Data—J12 (cont.)

Pin	Analyzer	Signal Name
21	data_pod0 – D8	P_DATA(7)
22	data_pod1 – D8	P_BLAST_N
23	data_pod0 – D7	P_DATA(8)
24	data_pod1 – D7	P_CS_N(0)
25	data_pod0 – D6	P_DATA(9)
26	data_pod1 – D6	P_CS_N(1)
27	data_pod0 – D5	P_DATA(10)
28	data_pod1 – D5	P_CS_N(2)
29	data_pod0 – D4	P_DATA(11)
30	data_pod1 – D4	P_CS_N(3)
31	data_pod0 – D3	P_DATA(12)
32	data_pod1 – D3	P_CS_N(4)
33	data_pod0 – D2	P_DATA(13)
34	data_pod1 – D2	unused
35	data_pod0 – D1	P_DATA(14)
36	data_pod1 – D1	unused
37	data_pod0 – D0	P_DATA(15)
38	data_pod1 – D0	unused

Table 10-15. Logic Analyzer Connector, Peripheral Bus Address—J8

Pin	Analyzer	Signal Name
1	addr_pod0 – +5VDC	unused
2	addr_pod1 – SCL	unused
3	addr_pod0 – GND DC	GND
4	addr_pod1 – SDA	unused
5	addr_pod0 – CLK	unused
6	addr_pod1 – CLK	P_CLK4
7	addr_pod0 – D15	unused
8	addr_pod1 – D15	P_ADDR(16)
9	addr_pod0 – D14	unused
10	addr_pod1 – D14	P_ADDR(17)
11	addr_pod0 – D13	unused
12	addr_pod1 – D13	P_ADDR(18)
13	addr_pod0 – D12	P_ADDR(3)
14	addr_pod1 – D12	P_ADDR(19)
15	addr_pod0 – D11	P_ADDR(4)
16	addr_pod1 – D11	P_ADDR(20)
17	addr_pod0 – D10	P_ADDR(5)
18	addr_pod1 – D10	P_ADDR(21)
19	addr_pod0 – D9	P_ADDR(6)
20	addr_pod1 – D9	P_ADDR(22)
21	addr_pod0 – D8	P_ADDR(7)
22	addr_pod1 – D8	P_ADDR(23)
23	addr_pod0 – D7	P_ADDR(8)
24	addr_pod1 – D7	P_ADDR(24)
25	addr_pod0 – D6	P_ADDR(9)
26	addr_pod1 – D6	P_ADDR(25)
27	addr_pod0 – D5	P_ADDR(10)
28	addr_pod1 – D5	P_ADDR(26)
29	addr_pod0 – D4	P_ADDR(11)
30	addr_pod1 – D4	P_ADDR(27)

Table 10-15. Logic Analyzer Connector, Peripheral Bus Address—J8 (cont.)

Pin	Analyzer	Signal Name
31	addr_pod0 – D3	P_ADDR(12)
32	addr_pod1 – D3	P_ADDR(28)
33	addr_pod0 – D2	P_ADDR(13)
34	addr_pod1 – D2	P_ADDR(29)
35	addr_pod0 – D1	P_ADDR(14)
36	addr_pod1 – D1	P_ADDR(30)
37	addr_pod0 – D0	P_ADDR(15)
38	addr_pod1 – D0	P_ADDR(31)

Table 10-16. Logic Analyzer Connector, Miscellaneous Signals—J29

Pin	Analyzer	Signal Name
1	misc_pod0 – +5VDC	C377 (filter cap to gnd)
2	misc_pod1 – SCL	unused
3	misc_pod0 – GND DC	GND
4	misc_pod1 – SDA	unused
5	misc_pod0 – CLK	unused
6	misc_pod1 – CLK	TRCCLK
7	misc_pod0 – D15	SYS_HALT_N
8	misc_pod1 – D15	unused
9	misc_pod0 – D14	unused
10	misc_pod1 – D14	unused
11	misc_pod0 – D13	TDO
12	misc_pod1 – D13	JTAG_VREF
13	misc_pod0 – D12	unused
14	misc_pod1 – D12	unused
15	misc_pod0 – D11	TCK
16	misc_pod1 – D11	unused
17	misc_pod0 – D10	TMS
18	misc_pod1 – D10	unused
19	misc_pod0 – D9	TDI
20	misc_pod1 – D9	unused
21	misc_pod0 – D8	TRST_N
22	misc_pod1 – D8	unused
23	misc_pod0 – D7	unused
24	misc_pod1 – D7	TS1O
25	misc_pod0 – D6	unused
26	misc_pod1 – D6	TS2O
27	misc_pod0 – D5	unused
28	misc_pod1 – D5	TS1E
29	misc_pod0 – D4	unused
30	misc_pod1 – D4	TS2E

Table 10-16. Logic Analyzer Connector, Miscellaneous Signals—J29 (cont.)

Pin	Analyzer	Signal Name
31	misc_pod0 – D3	unused
32	misc_pod1 – D3	TS3
33	misc_pod0 – D2	unused
34	misc_pod1 – D2	TS4
35	misc_pod0 – D1	unused
36	misc_pod1 – D1	TS5
37	misc_pod0 – D0	unused
38	misc_pod1 – D0	TS6

10.14 Expansion Interface Connector

User logic may be placed on a daughter card attached to the Expansion Interface connector. The pin usage of the connector is described in Table 10-17. Refer to the board schematic for the definitions of each of the signal names in the table.

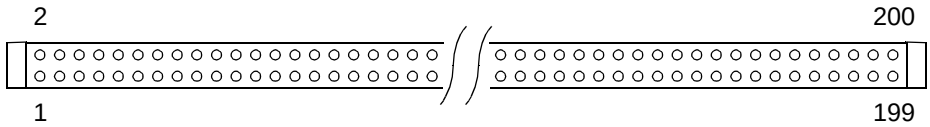


Figure 10-15. Expansion Interface Connector

Table 10-17. Expansion Interface Connector—J10

Pin	Signal Name	Pin	Signal Name
1	unused	2	AUX_DATA(0) — msb
3	unused	4	AUX_DATA(1)
5	unused	6	AUX_DATA(2)
7	AUX_ADDR(3)	8	AUX_DATA(3)
9	AUX_ADDR(4)	10	AUX_DATA(4)
11	AUX_ADDR(5)	12	AUX_DATA(5)
13	AUX_ADDR(6)	14	AUX_DATA(6)
15	AUX_ADDR(7)	16	AUX_DATA(7)
17	+5V	18	+5V
19	GND	20	GND
21	AUX_ADDR(8)	22	AUX_DATA(8)
23	AUX_ADDR(9)	24	AUX_DATA(9)
25	AUX_ADDR(10)	26	AUX_DATA(10)
27	AUX_ADDR(11)	28	AUX_DATA(11)
29	AUX_ADDR(12)	30	AUX_DATA(12)
31	AUX_ADDR(13)	32	AUX_DATA(13)
33	AUX_ADDR(14)	34	AUX_DATA(14)
35	AUX_ADDR(15)	36	AUX_DATA(15)
37	+3.3V	38	+3.3V
39	GND	40	GND
41	AUX_ADDR(16)	42	unused
43	AUX_ADDR(17)	44	unused

Table 10-17. Expansion Interface Connector—J10 (cont.)

Pin	Signal Name	Pin	Signal Name
45	AUX_ADDR(18)	46	unused
47	AUX_ADDR(19)	48	unused
49	AUX_ADDR(20)	50	unused
51	AUX_ADDR(21)	52	unused
53	AUX_ADDR(22)	54	unused
55	AUX_ADDR(23)	56	unused
57	+5V	58	+5V
59	GND	60	GND
61	AUX_ADDR(24)	62	unused
63	AUX_ADDR(25)	64	unused
65	AUX_ADDR(26)	66	unused
67	AUX_ADDR(27)	68	unused
69	AUX_ADDR(28)	70	unused
71	AUX_ADDR(29)	72	unused
73	AUX_ADDR(30)	74	unused
75	AUX_ADDR(31) — lsb	76	unused
77	+3.3V	78	+3.3V
79	GND	80	GND
81	unused	82	unused
83	unused	84	unused
85	unused	86	unused
87	AUX_P_CLK	88	unused
89	unused	90	unused
91	unused	92	unused
93	unused	94	IIC0_SCL
95	unused	96	IIC0_SDA
97	unused	98	+5V
99	unused	100	GND
101	AUX_P_RESET_N	102	unused
103	unused	104	unused
105	unused	106	TP3

Table 10-17. Expansion Interface Connector—J10 (cont.)

Pin	Signal Name	Pin	Signal Name
107	unused	108	unused
109	unused	110	GND
111	unused	112	+12V
113	unused	114	GND
115	unused	116	unused
117	+5V	118	+5V
119	GND	120	GND
121	unused	122	unused
123	unused	124	unused
125	AUX_WBE_N(1)	126	TP4
127	AUX_WBE_N(0)	128	GND
129	AUX_OE_N	130	–5V
131	AUX_WE_N	132	GND
133	AUX_RNW	134	unused
135	AUX_BLAST_N	136	unused
137	+3.3V	138	+3.3V
139	GND	140	GND
141	unused	142	TP5
143	unused	144	unused
145	unused	146	GND
147	unused	148	–12V
149	AUX_CS_N(3)	150	GND
151	AUX_CS_N(2)	152	unused
153	unused	154	unused
155	AUX_CS_N(0)	156	TP6
157	+5V	158	+5V
159	GND	160	GND
161	unused	162	unused
163	unused	164	TP7
165	unused	166	unused
167	unused	168	unused

Table 10-17. Expansion Interface Connector—J10 (cont.)

Pin	Signal Name	Pin	Signal Name
169	unused	170	unused
171	unused	172	unused
173	unused	174	unused
175	unused	176	unused
177	+3.3V	178	+3.3V
179	GND	180	GND
181	AUX_CLK	182	unused
183	GND	184	unused
185	unused	186	unused
187	unused	188	unused
189	unused	190	AUX_P_READY
191	unused	192	unused
193	unused	194	unused
195	unused	196	AUX_IRQ
197	+5V	198	+5V
199	GND	200	GND

10.15 Power Connector

The board is equipped with a standard ATX power connector for connection to an ATX power supply. This board-mounted header is a Molex 39-29-9202 or equivalent. Table 10-18 describes the pin usage in the power connector.

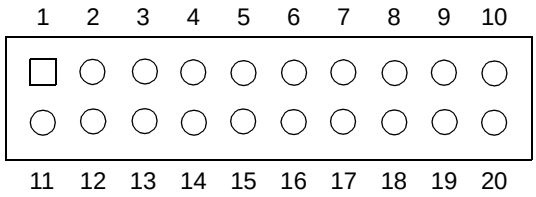


Figure 10-16. ATX Power Supply Connector

Table 10-18. Power Connector—J4

Pin	Name	Comment
1	+3.3V	Tolerance ± 4%
2	+3.3V	Tolerance ± 4%
3	GND	
4	+5V	Tolerance ± 5%
5	GND	
6	+5V	Tolerance ± 5%
7	GND	
8	PWR_OK	Active high indicator that +5V and +3.3V are above their undervoltage thresholds
9	+5V SB	Standby power, at least 10 mA, tolerance ± 5%
10	+12V	Tolerance ± 5%
11	+3.3V	Tolerance ± 4%
12	-12V	Tolerance ± 5%
13	GND	
14	PS_ON	Active low signal that turns on +3.3V, +5V, -5V, +12V, and -12V.
15	GND	
16	GND	
17	GND	
18	-5V	Tolerance ± 5%
19	+5V	Tolerance ± 5%

Table 10-18. Power Connector—J4 (cont.)

Pin	Name	Comment
20	+5V	Tolerance ± 5%

10.16 PCI Connectors

Four PCI connectors are provided for 33MHz PCI operation. PCI slot 0 is located at J42, slot 1 is at J38, slot 2 is at J36, and slot 3 is at J35. Figure 10-17 on page 10-25 shows a top view of these connectors. Pin usage for these connectors is given by Table 10-20 on page 10-25.

If PCI is used at 66MHz, only PCI slot 0 may be used. In 66MHz mode, the other three PCI slots must be unused (no adapter cards installed in those slots).

For the initialization of PCI adapter cards using PCI Configuration Cycles, the IDSEL inputs to the adapter cards are driven by bits from the PCI address bus. The slot addresses for use during configuration are given in Table 10-19.

Table 10-19. PCI Slot Configuration Addresses

PCI Slot 0 J42	PCI Slot 1 J38	PCI Slot 2 J36	PCI Slot 3 J35
0x4000	0x2000	0x1000	0x0800

The PCI connectors are installed into a non-standard board footprint which allows the orientation of the connector to be reversed. The normal shipping mode of the card has the connectors oriented to accept 5V, 33MHz PCI cards. If the orientation is reversed, 3.3V PCI cards may be supported. The 3.3V orientation is required for 66MHz operation.

While it is physically possible to, simultaneously, have some of the PCI connectors installed in 5V orientation and others installed in 3.3V orientation, this arrangement is not recommended, since a 5V adapter card might damage a 3.3V adapter card. If the orientation of the connectors is changed, jumpers must be moved. See “PCI Socket Orientation” on page 9-7.

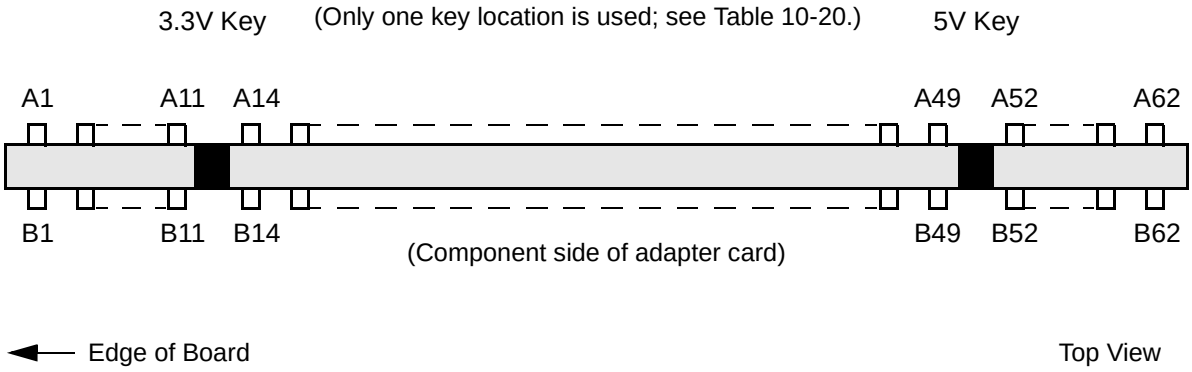


Figure 10-17. Socket for PCI Adapter Card

Table 10-20. PCI Connectors—J42, J38, J36, J35

Pin (comp. side)	Signal	Pin	Signal
B1	-12V	A1	TRST#
B2	TCK	A2	+12V
B3	GND	A3	TMS
B4	TDO	A4	TDI
B5	+5V	A5	+5V
B6	+5V	A6	INTA#
B7	INTB#	A7	INTC#
B8	INTD#	A8	+5V
B9	PRSNT1#	A9	reserved
B10	reserved	A10	+3.3V (I/O)
B11	PRSNT2#	A11	reserved
B12	GND (for 5V PCI)	A12	no-connect (for 5V PCI)
	connector key (for 3.3V PCI)		connector key (for 3.3V PCI)
B13	no-connect (for 5V PCI)	A13	GND (for 5V PCI)
	connector key (for 3.3V PCI)		connector key (for 3.3V PCI)
B14	reserved	A14	reserved
B15	GND	A15	RST#
B16	CLK	A16	+3.3V (I/O)
B17	GND	A17	GNT#

Table 10-20. PCI Connectors—J42, J38, J36, J35 (cont.)

Pin (comp. side)	Signal	Pin	Signal
B18	REQ#	A18	GND
B19	+3.3V (I/O)	A19	reserved
B20	AD31	A20	AD30
B21	AD29	A21	+3.3V
B22	GND	A22	AD28
B23	AD27	A23	AD26
B24	AD25	A24	GND
B25	+3.3V	A25	AD24
B26	C/BE3#	A26	IDSEL
B27	AD23	A27	+3.3V
B28	GND	A28	AD22
B29	AD21	A29	AD20
B30	AD19	A30	GND
B31	+3.3V	A31	AD18
B32	AD17	A32	AD16
B33	C/BE2#	A33	+3.3V
B34	GND	A34	FRAME#
B35	IRDY#	A35	GND
B36	+3.3V	A36	TRDY#
B37	DEVSEL#	A37	GND
B38	GND	A38	STOP#
B39	LOCK#	A39	+3.3V
B40	PERR#	A40	SDONE
B41	+3.3V	A41	SBO#
B42	SERR#	A42	GND
B43	+3.3V	A43	PAR
B44	C/BE1#	A44	AD15
B45	AD14	A45	+3.3V
B46	GND	A46	AD13
B47	AD12	A47	AD11

Table 10-20. PCI Connectors—J42, J38, J36, J35 (cont.)

Pin (comp. side)	Signal	Pin	Signal
B48	AD10	A48	GND
B49	M66EN/GND	A49	AD9
B50	connector key (for 5V PCI)	A50	connector key (for 5V PCI)
	GND (for 3.3V PCI)		no-connect (for 3.3V PCI)
B51	connector key (for 5V PCI)	A51	connector key (for 5V PCI)
	no-connect (for 3.3V PCI)		GND (for 3.3V PCI)
B52	AD8	A52	C/BE0#
B53	AD7	A53	+3.3V
B54	+3.3V	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	GND
B57	GND	A57	AD2
B58	AD1	A58	AD0
B59	+3.3V (I/O)	A59	+3.3V (I/O)
B60	ACK64#	A60	REQ64#
B61	+5V	A61	+5V
B62	+5V	A62	+5V

10.17 SDRAM Connector

The SDRAM connector is a 2x84 pin DIMM type connector with 50 mil pin spacing. Figure 10-18 shows a top view of the connector. Table 10-21 shows the connector pin assignments.

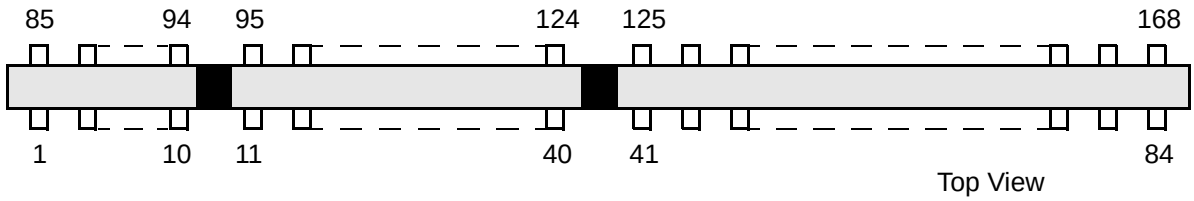


Figure 10-18. Socket for SDRAM DIMM

Table 10-21. SDRAM Connector—J16

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#*
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	Vcc	48	DU	90	Vcc	132	RFU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC

Table 10-21. SDRAM Connector—J16 (cont.)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#*	156	DQ59
31	DU	73	Vcc	115	RAS#	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	NC	123	A11	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	CK1	167	SA2
42	CK0	84	Vcc	126	A12	168	Vcc

10.18 IIC Connector

The IIC interface connects to J17.This is a 1x3 header connector.

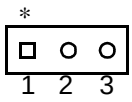


Figure 10-19. IIC Connector—J17

Table 10-22. IIC Connector Pin Assignment—J17

Pin	Signal Name
1	IIC0_SDA
2	Ground
3	IIC_SCL

10.18.1 Test Access

Access to selected pins and other test points is provided. In many cases the test points are provided at a via on the board. There are 100 test point vias numbered TP1 through TP100. These vias are documented in the schematics . To determine the signal to which the via connects, refer to the schematic.

10.19 Scope Connectors

The ScopeJack (Johnson 129-0701-201) provides a convenient means of connecting an oscilloscope to a critical net. There are seven locations on the board where a ScopeJack connector can be installed. Figure 10-20 shows the layout of the pins provided on the board for installation of this type of connector. In every case, pins 1 and 3 are ground and pin 2 carries the signal.

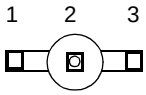


Figure 10-20. Scope Connector Jacks

Table 10-23. Scope Connectors—U14, U26, U28, U31, U33, U41, U47

Location	Signal Name (on pin 2)
U14	TP1 (spare)
U26	TP8 (spare)
U28	TP9 (spare)
U31	SYS_CLK
U33	TP34 (spare)
U41	TP80 (spare)
U47	TP100 (spare)

Chapter 11. FPGA Programming

11.1 Control Functions and Registers

The following sections contain the FPGA code listing and the related timing information for the board registers and control functions.

11.1.1 Register FPGA Code

```
%************************************************************************%
% FPGA for the 38P1861 Board                    22AUG02                  %
%************************************************************************%
%************ PERIPHERAL CHIP SELECT, CONTROL SIGNALS AND PCI ARBITER ************%
%************************************************************************%
INCLUDE "74169";

SUBDESIGN ELVIS1
(

%************************************************************************%
            %********************* Required JTAG Programming Pins
**********************%

%************************************************************************%
            % TCK:           INPUT;                location in device is fixed %
            % TMS:           INPUT;                location in device is fixed %
            % TDI:           INPUT;                location in device is fixed %
            % TDO:           OUTPUT;               location in device is fixed %


%************************************************************************%
            %*************************  INPUT SIGNALS
*******************************%

%************************************************************************%
            P_CLK:                    INPUT;   % FPGA internal clock
%
            P_RESET_N:                INPUT;   % FPGA reset
%

            P_ADDR31:                                          INPUT;   % P_ADDR
bit 31 (LSB)                                       %

            P_OE_N:                   INPUT;   % Output enable from 405EP
%
            P_WBE_N0:                 INPUT;   % Write enable from 405EP
%
            P_RNW:                    INPUT;   % P_RNW/EXT_RNW from 405EP
%

            P_CS_N0:                  INPUT;   % Chip select 0 from 405EP
%
```

```
            P_CS_N1:                    INPUT;   % Chip select 1 from 4405EP
%
            P_CS_N2:                    INPUT;   % Chip select 2 from 405EP
%
            P_CS_N3:                    INPUT;   % Chip select 3 from 405EP
%
            P_CS_N4:                    INPUT;   % Chip select 4 from 405EP
            %

            PCI_FREQ_SEL:               INPUT;   % Switch from the 38P1861 board
            %
            PCI_CLK_SEL:                             INPUT;   % Switch from the
38P1861 board        %
            FLASH/SRAM_SEL:             INPUT;   % Switch from the 38P1861 board
%
            FLASH_ONBD_N:               INPUT;   % Switch from the 38P1861 board
%
            MASTER_CLK_SEL[1..0]:INPUT;   % Switch from the 38P1861 board  %

            PCI_EXT_CLK:                             INPUT; % Offboard oscillator for
the PCI_CLK    %
            PCI_ONBD_CLK:                            INPUT; % PCI_CLK sourced from the
C9531                       %
            SPREAD_SPECTRUM_SEL:INPUT; % C9531 Operation mode                 %

            EXT_IRQ:                                                 INPUT;       %
Interrupt from expansion area                        %
            SW_SMI_N:                                                INPUT;       % SMI
pushbutton                                                                        %


%*************************************************************************%
            %********************** INPUT SIGNALS for PCI
*****************************%

%*************************************************************************%
            CLK:              INPUT;    % PCI clock                            %
            RST_N:            INPUT;    % PCI reset                            %
            FRAME_N:          INPUT;    % PCI transaction start line           %
            IRDY_N:           INPUT;    % PCI initiator ready line             %
            EXT_ARB_N:       INPUT;     % PCI arbiter control.                 %
                              %   1=405EP  internal arbiter selected  %
                              %   0=external arbiter selected         %
            REQ_N[4..0]:      INPUT;    % PCI REQ# inputs from masters         %
                              % REQ_N4 is from 405EP               %
                              % REQ_N[3..0] are from PCI slots 3..0 %
                              % respectively.                      %
            TARGET_MODE_EN:     INPUT;  % PCI target mode selected               %


%*************************************************************************%
            %************************** OUTPUT SIGNALS
*******************************%

%*************************************************************************%
            AUX_DIR_DATA:      OUTPUT;  % External connector data direction    %
            AUX_ENABLE_CNTL_N:OUTPUT;  % External connector enable address    %
            AUX_ENABLE_DATA_N:OUTPUT;  % External connector enable data       %
```

```
            PCI_CLK:                                OUTPUT;      % Carries the PCI
Async clock                             %
            F_RANGE:                                OUTPUT;      % SDRAM PLL freq
range select                                        %
            IRQ1:                                                OUTPUT;      %
Interrupt to the 405EP                                           %
            IRQ2:                                                OUTPUT;      %
Interrupt to the 405EP                                           %
            LED0:                                                OUTPUT;       % LED
0 indicator                                                      %
            LED1:                                                OUTPUT;       % LED
1 indicator                                                      %
            LED2:                                                OUTPUT;       % LED
2 indicator                                                      %


%************************************************************************%
            %*********************** OUTPUT SIGNALS for PCI
**************************%

%************************************************************************%
            GNT_N[4..0]:     OUTPUT;   % PCI GNT# outputs to masters            %
                                                                                 %
GNT_N4 is to 405EP                  %
                              %    GNT_N[3..0] are to PCI slots 3..0    %
                              %       respectively.                     %
            EXT_PCI_ARB_N:   OUTPUT;   % External PCI arbiter select        %
            INT_PCI_ARB_N:   OUTPUT;   % Internal PCI arbiter select        %
            TARGET_MODE:                OUTPUT;      % PCI Target mode select
%
            TARGET_MODE_N:              OUTPUT;      % PCI Target mode select
%


%************************************************************************%
            %*********************** BIDIRECTIONAL SIGNALS
**************************%

%************************************************************************%
            P_DATA[7..0]:    BIDIR;    % P_DATA 0-7 (MSByte), 405EP  data bus   %

)

VARIABLE
            FPGA_REG_0[7..0]:  DFF;                 % Control regisiter
            %
            FPGA_REG_1[7..0]:  DFF;    % Control regisiter
            %

            FPGA_REG_0_CS:    NODE;    % Select for intenal register 0        %
            FPGA_REG_1_CS:    NODE;    % Select for intenal register 1        %

            T_DATA[7..0]:     TRI_STATE_NODE;  % Node to allow multiple       %
                             % internal connections to the data bus  %

            P_CS_EXTDEV_N:    NODE;                 % Chip select for an external
device                     %
```

```
            PCI_INT_CLK1:             TFF;                       % PCI divide by 2
clock                                                                          %
            PCI_INT_CLK2:             TFF;                       % PCI divide by 4
clock                                                                          %

            REQ_B[4..0]:     DFF;      % the REQ_N inputs are registered       %
                           % to the PCI clock in REQ_B, to         %
                           % improve setup times                   %
            CNT:             74169;    % timer to abort a grant to a broken    %
                           % master (defined by the PCI spec as    %
                           % a master which  asserts REQ#,         %
                           % receives GNT#, and  does not assert   %
                           % FRAME# within 16 clocks)                          %
            IDLE:            NODE;     % hi if PCI bus is Idle                 %

            ARB:             MACHINE   % PCI Arbiter State Machine             %
                  OF BITS (GNT_N[4..0])
                  WITH STATES (ARB00 = B"11111", % grant none     %
                               ARB02 = B"11111", % grant none      %
                               ARB03 = B"11110", % grant slot 0    %
                               ARB04 = B"11110", % grant slot 0    %
                               ARB05 = B"11110", % grant slot 0    %
                               ARB12 = B"11111", % grant none      %
                               ARB13 = B"11101", % grant slot 1    %
                               ARB14 = B"11101", % grant slot 1    %
                               ARB15 = B"11101", % grant slot 1    %
                               ARB22 = B"11111", % grant none      %
                               ARB23 = B"11011", % grant slot 2    %
                               ARB24 = B"11011", % grant slot 2    %
                               ARB25 = B"11011", % grant slot 2    %
                               ARB32 = B"11111", % grant none      %
                               ARB33 = B"10111", % grant slot 3    %
                               ARB34 = B"10111", % grant slot 3    %
                               ARB35 = B"10111", % grant slot 3    %
                               ARB42 = B"11111", % grant none      %
                               ARB43 = B"01111", % grant 405EP     %
                               ARB44 = B"01111", % grant 405EP     %
                               ARB45 = B"01111"  % grant 405EP     %
                                                                              );

BEGIN

            % Register the REQ_N inputs in REQ_B.                             %
            % Setup time for REQ_N to GNT_N without registering the           %
            % inputs is 10.8 nsec.  PCI spec requires 5 nsec or less.         %
            REQ_B[].CLK   = GLOBAL(CLK);
            REQ_B[].PRN   = GLOBAL(RST_N);
            REQ_B[].CLRN  = VCC;
            REQ_B[].D     = REQ_N[];

            % Function prototype for 74169 counter.                             %
            % (q[3..0], tcn) = 74169 (ldn, entn, enpn, u/dn, clk, d[3..0]);     %

            CNT.LDN      = !((ARB == ARB03) # (ARB == ARB13) # (ARB == ARB23) #
                  (ARB == ARB33) # (ARB == ARB43));
            CNT.ENTN     = GND;
            CNT.ENPN     = GND;
            CNT.U/DN     = GND;
            CNT.CLK      = GLOBAL(CLK);
```

```
     CNT.D[3..0]  = VCC;

     % IDLE.                                                          %
     % Node which is high when the PCI bus is Idle.                   %

     IDLE       = FRAME_N & IRDY_N;

     % ARB.                                                           %
     % PCI arbiter state machine.                                     %
     %                                                               %
     % 1) This arbiter uses rotating priority, with all              %
     %    masters on the same level.                                 %
     % 2) With no requests present, the bus will park at the         %
     %    last-used master.                                          %
     % 3) The arbiter detects but does not report "broken            %
     %    masters" (REQ# and GNT# asserted, but FRAME# is not         %
     %    asserted within 16 clocks).  The arbiter is not            %
     %    blocked by broken masters.                                 %
     % 4) All re-arbitration occurs while FRAME# is                  %
     %    deasserted.                                                %

     ARB.clk   =  GLOBAL(CLK);
     ARB.reset = !GLOBAL(RST_N) # GLOBAL(EXT_ARB_N);

     TABLE
         ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;

     % Reset state, no grants asserted.                               %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;               %
ARB00, B"11111", x,    x,       x       => ARB00;
ARB00, B"xxxx0", x,    x,       x       => ARB03; % grant to 0 %
ARB00, B"xxx01", x,    x,       x       => ARB13; % grant to 1 %
ARB00, B"xx011", x,    x,       x       => ARB23; % grant to 2 %
ARB00, B"x0111", x,    x,       x       => ARB33; % grant to 3 %
ARB00, B"01111", x,    x,       x       => ARB43; % grant to 405EP  %

     % Insert one clock with no grants.                               %
     % The following state will grant to 0.                          %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;               %
ARB02, B"xxxxx", x,    x,       x       => ARB03;

     % Grant to slot 0.                                               %
     % Counter loads here.                                            %
     % Earliest possible assertion of FRAME_N is here.                %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;               %
ARB03, B"xxxxx", x,    x,       x       => ARB04;

     % Grant to slot 0.                                               %
     % Wait up to 16 clocks for master to accept grant.               %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;               %
ARB04, B"xxxxx", x,    1,       1      => ARB04;
ARB04, B"xxxxx", x,    1,       0      => ARB05; % broken master %
ARB04, B"xxxxx", x,    0,       0      => ARB05;
ARB04, B"xxxxx", x,    0,       1      => ARB05;
```

```
     % Grant to slot 0.                                                  %
     % When FRAME# is deasserted, arbitrate for new master.              %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                  %
ARB05, B"xxxxx", x,    0,       x       => ARB05;
ARB05, B"11111", 1,    1,       x       => ARB05; % park %
ARB05, B"11111", 0,    1,       x       => ARB05;
ARB05, B"11110", x,    1,       x       => ARB05;
ARB05, B"xxx0x", 0,    1,       x       => ARB13;
ARB05, B"xxx0x", 1,    1,       x       => ARB12;
ARB05, B"xx01x", 0,    1,       x       => ARB23;
ARB05, B"xx01x", 1,    1,       x       => ARB22;
ARB05, B"x011x", 0,    1,       x       => ARB33;
ARB05, B"x011x", 1,    1,       x       => ARB32;
ARB05, B"0111x", 0,    1,       x       => ARB43;
ARB05, B"0111x", 1,    1,       x       => ARB42;

     % Insert one clock with no grants.                                  %
     % The following state will grant to 1.                             %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                  %
ARB12, B"xxxxx", x,    x,       x       => ARB13;

     % Grant to slot 1.                                                  %
     % Counter loads here.                                               %
     % Earliest possible assertion of FRAME_N is here.                   %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                  %
ARB13, B"xxxxx", x,    x,       x       => ARB14;

                % Grant to slot 1.                                       %
     % Wait up to 16 clocks for master to accept grant.                  %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                  %
ARB14, B"xxxxx", x,    1,       1       => ARB14;
ARB14, B"xxxxx", x,    1,       0       => ARB15; % broken master %
ARB14, B"xxxxx", x,    0,       0       => ARB15;
ARB14, B"xxxxx", x,    0,       1       => ARB15;

     % Grant to slot 1.                                                  %
     % When FRAME# is deasserted, arbitrate for new master.              %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                  %
ARB15, B"xxxxx", x,    0,       x       => ARB15;
ARB15, B"11111", 1,    1,       x       => ARB15; % park %
ARB15, B"11111", 0,    1,       x       => ARB15;
ARB15, B"11101", x,    1,       x       => ARB15;
ARB15, B"xx0xx", 0,    1,       x       => ARB23;
ARB15, B"xx0xx", 1,    1,       x       => ARB22;
ARB15, B"x01xx", 0,    1,       x       => ARB33;
ARB15, B"x01xx", 1,    1,       x       => ARB32;
ARB15, B"011xx", 0,    1,       x       => ARB43;
ARB15, B"011xx", 1,    1,       x       => ARB42;
ARB15, B"111x0", 0,    1,       x       => ARB03;
ARB15, B"111x0", 1,    1,       x       => ARB02;

     % Insert one clock with no grants.                                  %
     % The following state will grant to 2.                             %
```

```
     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB22, B"xxxxx", x,    x,       x       => ARB23;

     % Grant to slot 2.                                                 %
     % Counter loads here.                                              %
     % Earliest possible assertion of FRAME_N is here.                  %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB23, B"xxxxx", x,    x,       x       => ARB24;

     % Grant to slot 2.                                                 %
     % Wait up to 16 clocks for master to accept grant.                 %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB24, B"xxxxx", x,    1,       1       => ARB24;
ARB24, B"xxxxx", x,    1,       0       => ARB25; % broken master %
ARB24, B"xxxxx", x,    0,       0       => ARB25;
ARB24, B"xxxxx", x,    0,       1       => ARB25;

     % Grant to slot 2.                                                 %
     % When FRAME# is deasserted, arbitrate for new master.            %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB25, B"xxxxx", x,    0,       x       => ARB25;
ARB25, B"11111", 1,    1,       x       => ARB25; % park %
ARB25, B"11111", 0,    1,       x       => ARB25;
ARB25, B"11011", x,    1,       x       => ARB25;
ARB25, B"x0xxx", 0,    1,       x       => ARB33;
ARB25, B"x0xxx", 1,    1,       x       => ARB32;
ARB25, B"01xxx", 0,    1,       x       => ARB43;
ARB25, B"01xxx", 1,    1,       x       => ARB42;
ARB25, B"11xx0", 0,    1,       x       => ARB03;
ARB25, B"11xx0", 1,    1,       x       => ARB02;
ARB25, B"11x01", 0,    1,       x       => ARB13;
ARB25, B"11x01", 1,    1,       x       => ARB12;

     % Insert one clock with no grants.                                 %
     % The following state will grant to 3.                            %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB32, B"xxxxx", x,    x,       x       => ARB33;

     % Grant to slot 3.                                                 %
     % Counter loads here.                                              %
     % Earliest possible assertion of FRAME_N is here.                  %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB33, B"xxxxx", x,    x,       x       => ARB34;

     % Grant to slot 3.                                                 %
     % Wait up to 16 clocks for master to accept grant.                 %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB34, B"xxxxx", x,    1,       1       => ARB34;
ARB34, B"xxxxx", x,    1,       0       => ARB35; % broken master %
ARB34, B"xxxxx", x,    0,       0       => ARB35;
ARB34, B"xxxxx", x,    0,       1       => ARB35;

     % Grant to slot 3.                                                 %
```

```
     % When FRAME# is deasserted, arbitrate for new master.            %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB35, B"xxxxx", x,    0,       x       => ARB35;
ARB35, B"11111", 1,    1,       x       => ARB35; % park %
ARB35, B"11111", 0,    1,       x       => ARB35;
ARB35, B"10111", x,    1,       x       => ARB35;
ARB35, B"0xxxx", 0,    1,       x       => ARB43;
ARB35, B"0xxxx", 1,    1,       x       => ARB42;
ARB35, B"1xxx0", 0,    1,       x       => ARB03;
ARB35, B"1xxx0", 1,    1,       x       => ARB02;
ARB35, B"1xx01", 0,    1,       x       => ARB13;
ARB35, B"1xx01", 1,    1,       x       => ARB12;
ARB35, B"1x011", 0,    1,       x       => ARB23;
ARB35, B"1x011", 1,    1,       x       => ARB22;

     % Insert one clock with no grants.                                %
     % The following state will grant to 4.                           %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB42, B"xxxxx", x,    x,       x       => ARB43;

     % Grant to 405GP .                                               %
     % Counter loads here.                                            %
     % Earliest possible assertion of FRAME_N is here.                %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB43, B"xxxxx", x,    x,       x       => ARB44;

     % Grant to 405GP .                                               %
     % Wait up to 16 clocks for master to accept grant.               %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB44, B"xxxxx", x,    1,       1       => ARB44;
ARB44, B"xxxxx", x,    1,       0       => ARB45; % broken master %
ARB44, B"xxxxx", x,    0,       0       => ARB45;
ARB44, B"xxxxx", x,    0,       1       => ARB45;

     % Grant to 405GP .                                               %
     % When FRAME# is deasserted, arbitrate for new master.           %

     % ARB,   REQ_B[],  IDLE, FRAME_N, CNT.TCN => ARB;                 %
ARB45, B"xxxxx", x,    0,       x       => ARB45;
ARB45, B"11111", 1,    1,       x       => ARB45; % park %
ARB45, B"11111", 0,    1,       x       => ARB45;
ARB45, B"01111", x,    1,       x       => ARB45;
ARB45, B"xxxx0", 0,    1,       x       => ARB03;
ARB45, B"xxxx0", 1,    1,       x       => ARB02;
ARB45, B"xxx01", 0,    1,       x       => ARB13;
ARB45, B"xxx01", 1,    1,       x       => ARB12;
ARB45, B"xx011", 0,    1,       x       => ARB23;
ARB45, B"xx011", 1,    1,       x       => ARB22;
ARB45, B"x0111", 0,    1,       x       => ARB33;
ARB45, B"x0111", 1,    1,       x       => ARB32;

     END TABLE;

%*************************************************************************%
```

```
            %*********************** Register Section
**********************************%

%*************************************************************************%
            % The external data bus is driven by the internal tri_state_node    %
            % which internally ties separate users of the bus.                   %
            P_DATA[] = T_DATA[];

            % Register selects %
            FPGA_REG_0_CS = (P_ADDR31 == B"0") & !P_CS_N4;
    FPGA_REG_1_CS = (P_ADDR31 == B"1") & !P_CS_N4;

            % FPGA_REG_0 bits
                        %
            % Bit 0 : F_RANGE, SDRAM PLL freq range                            %
            %                                        0 = 100mhz - 200mhz (default)  %
            %                                        1 = 50mhz - 100mhz           %
            % Bit 1 : 0 (spare bit)                                            %
            % Bit 2 : disable external interface, 1 = disabled                 %
            % Bit 3 : 0 (spare bit)                                            %
            % Bit 4 : 0 (spare bit)                                            %
            % Bit 5 : LED1 indictor                                            %
            % Bit 6 : LED0 indictor                                            %
            % Bit 7 : LED2 indictor                                            %

            % FPGA_REG_0 read %
            T_DATA0 = TRI(FPGA_REG_00, FPGA_REG_0_CS & !P_OE_N);
            T_DATA1 = TRI(FPGA_REG_01, FPGA_REG_0_CS & !P_OE_N);
            T_DATA2 = TRI(FPGA_REG_02, FPGA_REG_0_CS & !P_OE_N);
            T_DATA3 = TRI(FPGA_REG_03, FPGA_REG_0_CS & !P_OE_N);
            T_DATA4 = TRI(FPGA_REG_04, FPGA_REG_0_CS & !P_OE_N);
            T_DATA5 = TRI(FPGA_REG_05, FPGA_REG_0_CS & !P_OE_N);
            T_DATA6 = TRI(FPGA_REG_06, FPGA_REG_0_CS & !P_OE_N);
            T_DATA7 = TRI(FPGA_REG_07, FPGA_REG_0_CS & !P_OE_N);

            % FPGA_REG_0 write %
            FPGA_REG_0[].CLRN = P_RESET_N;
            FPGA_REG_0[].PRN  = VCC;
            FPGA_REG_0[].CLK  = !(FPGA_REG_0_CS & !P_WBE_N0);
            FPGA_REG_0[].D    = P_DATA[];

            % FPGA_REG_1 bits
%
            % Bit 0 : SPREAD_SPECTRUM_SEL                                      %
            %                            0 = SPREAD_SPECTRUM_SEL = Enable SS clocking
%
            %                            1 = SPREAD_SPECTRUM_SEL = Disable SS
clocking                                                                     %
            % Bit 1 : PCI_CLK_SEL                                              %
            %                            0 = PCI_CLK_SEL = PCI onboard clock selected
%
            %                            1 = PCI_CLK_SEL = PCI offboard clock
selected                                                                     %
            % Bit 2 : MASTER_CLK_SEL1                                          %
            % Bit 3 : MASTER_CLK_SEL0                                          %
            %                                       SEL1,SEL0
                                                             %
            %                                       0   ,0 = MASTER_CLK = 33Mhz
                                      %
```

```
            %           0   ,1 = MASTER_CLK = 66Mhz                          %
            %           1   ,0 = MASTER_CLK = 100Mhz                         %
            %           1   ,1 = MASTER_CLK = 133Mhz                         %
            %           Function implemented by the FPGA.                  %
            % Bit 4 : PCI_ARB_SEL switch                                     %
            %         0 = Use external arbiter (switch closed)             %
            %             EXT_ARB = low                                      %
            %         1 = Use 405EP internal arbiter (switch opened)     %
            %             EXT_ARB = high                                     %
            %         Function implemented by the FPGA.                  %
            % Bit 5 : PCI_FREQ_SEL switch                                    %
            %         0 = Force PCI Bus speed to be 33Mhz or 25Mhz       %
            %         1 = Allow 66Mhz PCI if available                     %
            %         Function implemented in hardware.                  %
            % Bit 6 : FLASH_ONBD_N switch                                    %
            %         0 = On board FLASH enabled  (switch closed)        %
            %         1 = On board FLASH disabled (switch opened)        %
            %         Function implemented in hardware.                  %
            % Bit 7 : FLASH/SRAM SEL switch                                  %
            %         0 = FLASH high addr (switch closed)                  %
            %         1 = FLASH low addr  (switch opened)                  %
            %         Function implemented in hardware.                  %

            % FPGA_REG_1 read %
            T_DATA0 = TRI(FPGA_REG_10, FPGA_REG_1_CS & !P_OE_N);
            T_DATA1 = TRI(FPGA_REG_11, FPGA_REG_1_CS & !P_OE_N);
            T_DATA2 = TRI(FPGA_REG_12, FPGA_REG_1_CS & !P_OE_N);
            T_DATA3 = TRI(FPGA_REG_13, FPGA_REG_1_CS & !P_OE_N);
            T_DATA4 = TRI(FPGA_REG_14, FPGA_REG_1_CS & !P_OE_N);
            T_DATA5 = TRI(FPGA_REG_15, FPGA_REG_1_CS & !P_OE_N);
            T_DATA6 = TRI(FPGA_REG_16, FPGA_REG_1_CS & !P_OE_N);
            T_DATA7 = TRI(FPGA_REG_17, FPGA_REG_1_CS & !P_OE_N);

            % FPGA_REG_1 write        %
            % Read only register %

            EXT_PCI_ARB_N = EXT_ARB_N # !TARGET_MODE_EN;
            INT_PCI_ARB_N = !EXT_ARB_N # !TARGET_MODE_EN;
            TARGET_MODE = !TARGET_MODE_EN;
            TARGET_MODE_N = TARGET_MODE_EN;


%*************************************************************************%
            %********************** External Connector Section
************************%

%*************************************************************************%
            % Chip select for an external device                           %
            % Will be low if any is low, otherwise high                    %
            IF (FPGA_REG_16 == B"1") THEN
                        % Onboard FLASH is disabled, P_CS_N0 is used externally %
            % !P_CS_EXTDEV_N = !P_CS_N0 # !P_CS_N2 # !P_CS_N3;             %
            P_CS_EXTDEV_N = P_CS_N0 & P_CS_N2 & P_CS_N3;
            ELSE
            % Onboard FLASH is enabled, P_CS_N0 is used on 38P1861 board%
            % !P_CS_EXTDEV_N = !P_CS_N4 # !P_CS_N5 # !P_CS_N6;             %
            P_CS_EXTDEV_N = P_CS_N2 & P_CS_N3;
            END IF;
```

```
            % Enable the interface all the time unless disabled by the user %
            % Register bit is low by default, i.e interface enabled         %
            IF (FPGA_REG_02 == B"1") THEN
            AUX_ENABLE_CNTL_N = B"1";% Disable address and control             %
            AUX_ENABLE_DATA_N = B"1";% Disable data                            %

            ELSE
            % Enable address and controls                                      %
            AUX_ENABLE_CNTL_N = B"0";
                                        IF (P_CS_EXTDEV_N == B"0") THEN% External
device chip select        %
                                                    IF (P_RNW == B"1") THEN% 405EP
read                                                                        %
                                                                AUX_DIR_DATA = B"0";
% Direction BtoA, external -> 38P1861 %
                        AUX_ENABLE_DATA_N = P_OE_N;% Enable when P_OE goes low    %
            ELSE
                        AUX_DIR_DATA = B"1";   % 405EP write                  %
                                                                AUX_ENABLE_DATA_N =
P_WBE_N0; % Enable DATA                                 %
            END IF;
            ELSE
           % Allow data to flow away from 405EP to external connector%
            AUX_DIR_DATA = B"1";     % Direction AtoB, 38P1861 -> external %
            AUX_ENABLE_DATA_N = B"0";% Enable right away                       %
            END IF;
            END IF;


%*************************************************************************%
            %********************** Clocking Section
**********************************%

%*************************************************************************%

            % Set SDRAM PLL freq range                                        %

            F_RANGE = FPGA_REG_00;


            % PCI clock selects                                               %

            PCI_INT_CLK1.PRN = VCC;
            PCI_INT_CLK1.CLRN = VCC;
            PCI_INT_CLK1.CLK = PCI_ONBD_CLK;
            PCI_INT_CLK1.T = VCC;

            PCI_INT_CLK2.PRN = VCC;
            PCI_INT_CLK2.CLRN = VCC;
            PCI_INT_CLK2.CLK = PCI_INT_CLK1;
            PCI_INT_CLK2.T = VCC;

            IF    (PCI_CLK_SEL == B"1") THEN
      PCI_CLK = PCI_EXT_CLK;% PCI_CLK sourced from externalgenerator %
            ELSE
                        IF (PCI_FREQ_SEL == B"0") THEN  % Limit PCI freq to 33.33Mhz
or less      %
                                    CASE MASTER_CLK_SEL[] IS
```

```
                                                    WHEN 0 => PCI_CLK = PCI_ONBD_CLK;
% PCI_CLK = 33.33Mhz       %
                                                    WHEN 1 => PCI_CLK = PCI_INT_CLK1;
% PCI_CLK = 33.33Mhz       %
                                                    WHEN 2 => PCI_CLK = PCI_INT_CLK2;
% PCI_CLK = 25.00Mhz       %
                                                    WHEN 3 => PCI_CLK = PCI_INT_CLK2;
% PCI_CLK = 33.33Mhz       %
                                        END CASE;
                            ELSE
                                        CASE MASTER_CLK_SEL[] IS% Allow 66.66Mhz PCI
operation                               %
                                                    WHEN 0 => PCI_CLK = PCI_ONBD_CLK;
% PCI_CLK = 33.33Mhz       %
                                                    WHEN 1 => PCI_CLK = PCI_ONBD_CLK;
% PCI_CLK = 66.67Mhz       %
                                                    WHEN 2 => PCI_CLK = PCI_INT_CLK1;
% PCI_CLK = 50.00Mhz       %
                                                    WHEN 3 => PCI_CLK = PCI_INT_CLK1;
% PCI_CLK = 66.67Mhz       %
                                        END CASE;
                            END IF;
              END IF;

%*************************************************************************%
              %************************** Misc Section
*********************************%

%*************************************************************************%


              IRQ1 = EXT_IRQ;
              IRQ2 = !SW_SMI_N;
              LED0 = FPGA_REG_06;
              LED1 = FPGA_REG_05;
              LED2 = FPGA_REG_07;



%*************************************************************************%
              %************************** Strapping Section
*****************************%

%*************************************************************************%
              FPGA_REG_10.CLRN = VCC;
              FPGA_REG_10.PRN  = VCC;
              FPGA_REG_10.CLK  = P_CLK;
              FPGA_REG_10.D    = SPREAD_SPECTRUM_SEL;

              FPGA_REG_11.CLRN = VCC;
              FPGA_REG_11.PRN  = VCC;
              FPGA_REG_11.CLK  = P_CLK;
              FPGA_REG_11.D    = PCI_CLK_SEL;

              FPGA_REG_12.CLRN = VCC;
              FPGA_REG_12.PRN  = VCC;
              FPGA_REG_12.CLK  = P_CLK;
```

```
                FPGA_REG_12.D    = MASTER_CLK_SEL1;

                FPGA_REG_13.CLRN = VCC;
                FPGA_REG_13.PRN  = VCC;
                FPGA_REG_13.CLK  = P_CLK;
                FPGA_REG_13.D    = MASTER_CLK_SEL0;

                FPGA_REG_14.CLRN = VCC;
                FPGA_REG_14.PRN  = VCC;
                FPGA_REG_14.CLK  = P_CLK;
                FPGA_REG_14.D    = EXT_ARB_N;

                FPGA_REG_15.CLRN = VCC;
                FPGA_REG_15.PRN  = VCC;
                FPGA_REG_15.CLK  = P_CLK;
                FPGA_REG_15.D    = PCI_FREQ_SEL;

                FPGA_REG_16.CLRN = VCC;
                FPGA_REG_16.PRN  = VCC;
                FPGA_REG_16.CLK  = P_CLK;
                FPGA_REG_16.D    = FLASH_ONBD_N;

                FPGA_REG_17.CLRN = VCC;
                FPGA_REG_17.PRN  = VCC;
                FPGA_REG_17.CLK  = P_CLK;
                FPGA_REG_17.D    = FLASH/SRAM_SEL;
END;
```

11.1.2 Register Timing

The timing data which follows is based on simulation.

Table 11-1. Register Performance

Clock	Source	Destination	Period (ns)	Frequency (MHz)
clk	|74169:CNT|Q3~fit~in1	ARB~1.Q	17.7	56.49
clk	|74169:CNT|Q1~fit~in1	ARB~1.Q	17.7	56.49
clk	|74169:CNT|Q1~fit~in1	|74169:CNT|Q3~fit~in1	16.0	62.50
clk	|74169:CNT|Q1~fit~in1	|74169:CNT|Q2.Q	16.0	62.50
clk	GNT_N4~.Q	GNT_N4~.Q	12.6	79.36
clk	GNT_N4~.Q	GNT_N3~.Q	12.6	79.36
clk	GNT_N4~.Q	GNT_N2~.Q	12.6	79.36
clk	GNT_N4~.Q	GNT_N1~.Q	12.6	79.36
clk	GNT_N4~.Q	GNT_N0~.Q	12.6	79.36
clk	GNT_N4~.Q	ARB~3.Q	12.6	79.36
PCI_INT_CLK1.Q	PCI_INT_CLK2.Q	PCI_INT_CLK2.Q	6.8	147.05
PCI_ONBD_CLK	PCI_INT_CLK1.Q	PCI_INT_CLK1.Q	6.8	147.05

Table 11-2. Setup/Hold Time Analysis

Register	Input	Clock	Setup (ns)	Hol (ns)
ARB~1.Q	FRAME_N	clk	9.1ns	0.0ns
ARB~1.Q	IRDY_N	clk	9.1ns	0.0ns
ARB~2.Q	FRAME_N	clk	9.1ns	0.0ns
ARB~2.Q	IRDY_N	clk	9.1ns	0.0ns
ARB~3.Q	FRAME_N	clk	9.1ns	0.0ns
ARB~3.Q	IRDY_N	clk	9.1ns	0.0ns
GNT_N0~.Q	FRAME_N	clk	9.1ns	0.0ns
GNT_N0~.Q	IRDY_N	clk	9.1ns	0.0ns
GNT_N1~.Q	FRAME_N	clk	9.1ns	0.0ns
GNT_N1~.Q	IRDY_N	clk	9.1ns	0.0ns
GNT_N2~.Q	FRAME_N	clk	9.1ns	0.0ns
GNT_N2~.Q	IRDY_N	clk	9.1ns	0.0ns
GNT_N3~.Q	FRAME_N	clk	9.1ns	0.0ns
GNT_N3~.Q	IRDY_N	clk	9.1ns	0.0ns
GNT_N4~.Q	FRAME_N	clk	9.1ns	0.0ns
GNT_N4~.Q	IRDY_N	clk	9.1ns	0.0ns
REQ_B0.Q	REQ_N0	clk	3.4ns	0.0ns
REQ_B1.Q	REQ_N1	clk	3.4ns	0.0ns
REQ_B2.Q	REQ_N2	clk	3.4ns	0.0ns
REQ_B3.Q	REQ_N3	clk	3.4ns	0.0ns
REQ_B4.Q	REQ_N4	clk	3.4ns	0.0ns
FPGA_REG_00.Q	P_DATA0	P_ADDR31	0.0ns	5.6ns
FPGA_REG_01.Q	P_DATA1	P_ADDR31	0.0ns	5.6ns
FPGA_REG_02.Q	P_DATA2	P_ADDR31	0.0ns	5.6ns
FPGA_REG_03.Q	P_DATA3	P_ADDR31	0.0ns	5.6ns
FPGA_REG_04.Q	P_DATA4	P_ADDR31	0.0ns	5.6ns
FPGA_REG_05.Q	P_DATA5	P_ADDR31	0.0ns	5.6ns
FPGA_REG_06.Q	P_DATA6	P_ADDR31	0.0ns	5.6ns
FPGA_REG_07.Q	P_DATA7	P_ADDR31	0.0ns	5.6ns
FPGA_REG_00.Q	P_DATA0	P_CS_N4	0.0ns	5.6ns

Table 11-2. Setup/Hold Time Analysis (cont.)

Register	Input	Clock	Setup (ns)	Hol (ns)
FPGA_REG_01.Q	P_DATA1	P_CS_N4	0.0ns	5.6ns
FPGA_REG_02.Q	P_DATA2	P_CS_N4	0.0ns	5.6ns
FPGA_REG_03.Q	P_DATA3	P_CS_N4	0.0ns	5.6ns
FPGA_REG_04.Q	P_DATA4	P_CS_N4	0.0ns	5.6ns
FPGA_REG_05.Q	P_DATA5	P_CS_N4	0.0ns	5.6ns
FPGA_REG_06.Q	P_DATA6	P_CS_N4	0.0ns	5.6ns
FPGA_REG_07.Q	P_DATA7	P_CS_N4	0.0ns	5.6ns
FPGA_REG_00.Q	P_DATA0	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_01.Q	P_DATA1	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_02.Q	P_DATA2	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_03.Q	P_DATA3	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_04.Q	P_DATA4	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_05.Q	P_DATA5	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_06.Q	P_DATA6	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_07.Q	P_DATA7	P_WBE_N0	0.0ns	5.5ns
FPGA_REG_10.Q	SPREAD_SPECTRUM_SEL	P_CLK	3.4ns	0.0ns
FPGA_REG_11.Q	PCI_CLK_SEL	P_CLK	3.5ns	0.0ns
FPGA_REG_12.Q	MASTER_CLK_SEL1	P_CLK	3.4ns	0.0ns
FPGA_REG_13.Q	MASTER_CLK_SEL0	P_CLK	3.4ns	0.0ns
FPGA_REG_14.Q	EXT_ARB_N	P_CLK	3.7ns	0.0ns
FPGA_REG_15.Q	PCI_FREQ_SEL	P_CLK	3.4ns	0.0ns
FPGA_REG_16.Q	FLASH_ONBD_N	P_CLK	3.4ns	0.0ns
FPGA_REG_17.Q	FLASH/SRAM_SEL	P_CLK	3.4ns	0.0ns

Table 11-3. Delay Matrix

Source	Destination	Min Path (ns)	Max Path (ns)
P_ADDR31	AUX_DIR_DATA	-	15.8
P_CLK	AUX_DIR_DATA	-	9.5
P_CS_N0	AUX_DIR_DATA	-	6.0
P_CS_N2	AUX_DIR_DATA	-	6.0
P_CS_N3	AUX_DIR_DATA	-	6.0
P_CS_N4	AUX_DIR_DATA	-	15.8
P_RNW	AUX_DIR_DATA	-	6.0
P_WBE_N0	AUX_DIR_DATA	-	15.7
P_ADDR31	AUX_ENABLE_CNTL_N	-	10.3
P_CS_N4	AUX_ENABLE_CNTL_N	-	10.3
P_WBE_N0	AUX_ENABLE_CNTL_N	-	10.2
P_ADDR31	AUX_ENABLE_DATA_N	-	15.8
P_CLK	AUX_ENABLE_DATA_N	-	9.5
P_CS_N0	AUX_ENABLE_DATA_N	-	6.0
P_CS_N2	AUX_ENABLE_DATA_N	-	6.0
P_CS_N3	AUX_ENABLE_DATA_N	-	6.0
P_CS_N4	AUX_ENABLE_DATA_N	-	15.8
P_OE_N	AUX_ENABLE_DATA_N	-	6.1
P_RNW	AUX_ENABLE_DATA_N	-	6.0
P_WBE_N0	AUX_ENABLE_DATA_N	6.0	15.7
EXT_ARB_N	EXT_PCI_ARB_N	-	6.3
TARGET_MODE_EN	EXT_PCI_ARB_N	-	6.1
P_ADDR31	F_RANGE	-	15.3
P_CS_N4	F_RANGE	-	15.3
P_WBE_N0	F_RANGE	-	15.2
clk	GNT_N0	-	4.0
clk	GNT_N1	-	4.0
clk	GNT_N2	-	4.0
clk	GNT_N3	-	4.0
clk	GNT_N4	-	4.0

Table 11-3. Delay Matrix (cont.)

Source	Destination	Min Path (ns)	Max Path (ns)
EXT_ARB_N	INT_PCI_ARB_N	-	6.3
TARGET_MODE_EN	INT_PCI_ARB_N	-	6.1
EXT_IRQ	IRQ1	-	6.0
SW_SMI_N	IRQ2	-	6.0
P_ADDR31	LED0	-	15.3
P_CS_N4	LED0	-	15.3
P_WBE_N0	LED0	-	15.2
P_ADDR31	LED1	-	15.3
P_CS_N4	LED1	-	15.3
P_WBE_N0	LED1	-	15.2
P_ADDR31	LED2	-	15.3
P_CS_N4	LED2	-	15.3
P_WBE_N0	LED2	-	15.2
MASTER_CLK_SEL0	PCI_CLK	6.0	9.7
MASTER_CLK_SEL1	PCI_CLK	-	6.0
PCI_CLK_SEL	PCI_CLK	-	6.1
PCI_EXT_CLK	PCI_CLK	-	6.0
PCI_FREQ_SEL	PCI_CLK	6.0	9.7
PCI_ONBD_CLK	PCI_CLK	6.0	17.8
P_ADDR31	P_DATA0	6.1	15.7
P_CLK	P_DATA0	-	9.4
P_CS_N4	P_DATA0	6.1	15.7
P_OE_N	P_DATA0	6.1	11.8
P_WBE_N0	P_DATA0	-	15.6
P_ADDR31	P_DATA1	6.1	15.7
P_CLK	P_DATA1	-	9.4
P_CS_N4	P_DATA1	6.1	15.7
P_OE_N	P_DATA1	6.1	11.8
P_WBE_N0	P_DATA1	-	15.6
P_ADDR31	P_DATA2	6.1	15.8
P_CLK	P_DATA2	-	9.4

Table 11-3. Delay Matrix (cont.)

Source	Destination	Min Path (ns)	Max Path (ns)
P_CS_N4	P_DATA2	6.1	15.8
P_OE_N	P_DATA2	6.1	11.8
P_WBE_N0	P_DATA2	-	15.7
P_ADDR31	P_DATA3	6.1	15.7
P_CLK	P_DATA3	-	9.4
P_CS_N4	P_DATA3	6.1	15.7
P_OE_N	P_DATA3	6.1	11.8
P_WBE_N0	P_DATA3	-	15.6
P_ADDR31	P_DATA4	6.1	15.7
P_CLK	P_DATA4	-	9.4
P_CS_N4	P_DATA4	6.1	15.7
P_OE_N	P_DATA4	6.1	11.8
P_WBE_N0	P_DATA4	-	15.6
P_ADDR31	P_DATA5	6.1	15.7
P_CLK	P_DATA5	-	9.4
P_CS_N4	P_DATA5	6.1	15.7
P_OE_N	P_DATA5	6.1	11.8
P_WBE_N0	P_DATA5	-	15.6
P_ADDR31	P_DATA6	6.1	15.7
P_CLK	P_DATA6	-	9.5
P_CS_N4	P_DATA6	6.1	15.7
P_OE_N	P_DATA6	6.1	11.8
P_WBE_N0	P_DATA6	-	15.6
P_ADDR31	P_DATA7	6.1	15.7
P_CLK	P_DATA7	-	9.4
P_CS_N4	P_DATA7	6.1	15.7
P_OE_N	P_DATA7	6.1	11.8
P_WBE_N0	P_DATA7	-	15.6
TARGET_MODE_EN	TARGET_MODE	-	6.1
TARGET_MODE_EN	TARGET_MODE_N	-	6.1

Chapter 12. Bill of Materials

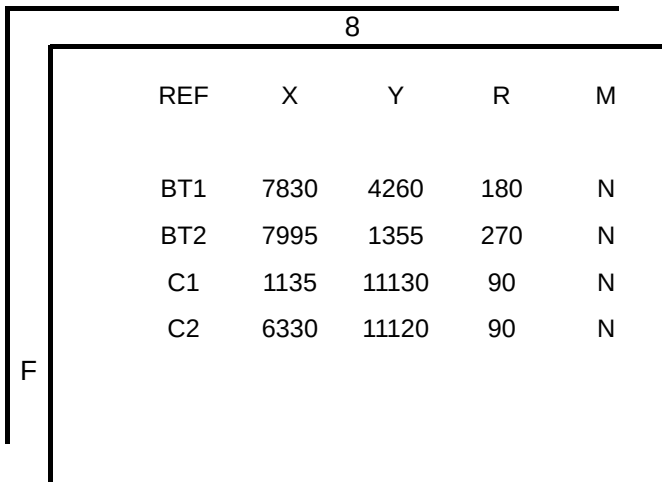
Table 12-5, “Evaluation Board Bill of Materials,” on page 12-8 identifies all parts that can possibly be assembled on the board. Those parts that are not assembled on the board, as it ships from the factory, are labeled DNP (do not populate). In some cases installation of DNP parts requires the removal of installed parts and constitutes a change in the design of the board. IBM does not support boards that have been modified by removing normally installed parts.

Materials provided with the board but that are not a part of board assembly are detailed in Table 12-2, “Auxiliary Materials in Kit,” on page 12-5 on.

12.1 Component Location

The location of any component on the board can be identified by using the coordinate grid that appears along the outside edges of the board. An example of this grid, as it appears on the top side of the board is shown in Figure 12-2. The X-coordinate scale is along the short edge of the board and the Y-coordinate scale is along the long edge of the board.

The coordinates of each component are provided in a table that appears in the schematic diagrams. The schematic pages that contain this table are titled Component Placement. Figure 12-1 shows an example of the table as it appears on the schematic page.



REF	X	Y	R	M
BT1	7830	4260	180	N
BT2	7995	1355	270	N
C1	1135	11130	90	N
C2	6330	11120	90	N

Figure 12-1. Example of a Component Placement List in the Schematics

The information provided in each column of the component placement table is described in Table 12-1:

Table 12-1. Component Placement Data Description

Column Heading[1]	Description
REF	Reference designator as it appears in the BOM and the schematics
X	X-coordinate of the component location
Y	Y-coordinate of the component location
R	Rotation of the component in degrees
M	Shows which side of the board the component is on: N = top side Y = bottom side
Note 1: The column headings shown are representative only. The actual column headings will vary from schematic to schematic. However, the information provided is the same in all cases.	

All of the coordinates are referenced to the 0,0 datum point which is at the center of the mounting hole in the bottom left corner of the board as viewed from the top side. The coordinate values in the table and the labels on the board are given in thousandths of inches. For example, an X-coordinate value of 7995 indicates that the component has an X-coordinate that is 7.995 inches from the 0,0 datum. Note that it is possible for components to have negative coordinate values.

The normal procedure to locate a component is to look up the coordinates in the Component Placement table in the schematic diagram, then use the X and Y scales on the edge of the board to get to the approximate location of the component on the board. The reference designator that is silk-screened on the board is then use to locate the component precisely. The location of component BT1 at coordinates X = 7830 and Y = 4260 from the example table is shown in Figure 12-2.

Note: The appearance of the scales as shown in the example figure is representative only. The actual appearance will vary from board to board due to constraints imposed by available board space and component placement. However, the basic format is the same in all cases with a reference mark appearing, whenever possible, every inch.

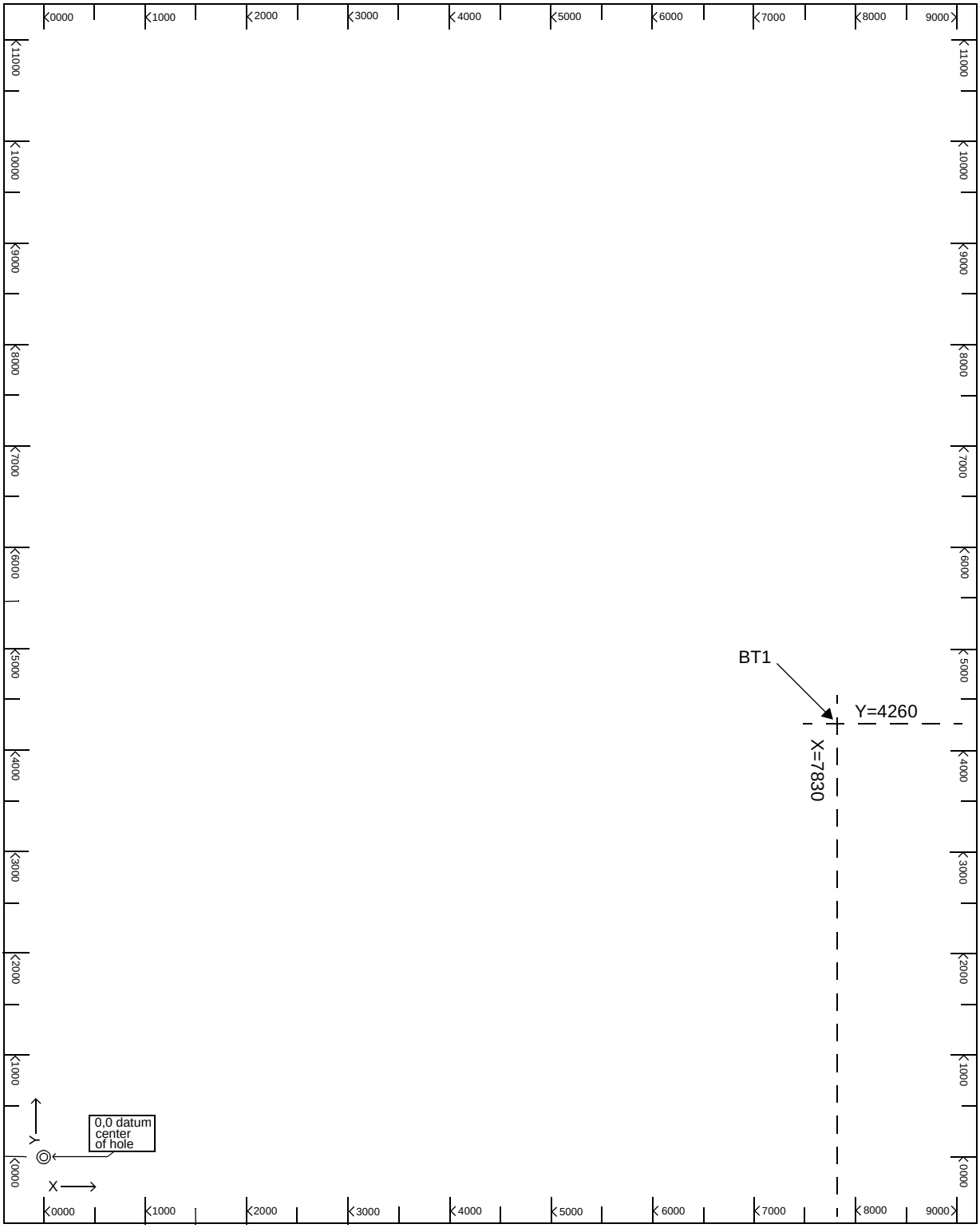


Figure 12-2. Board Location Grid—Top View

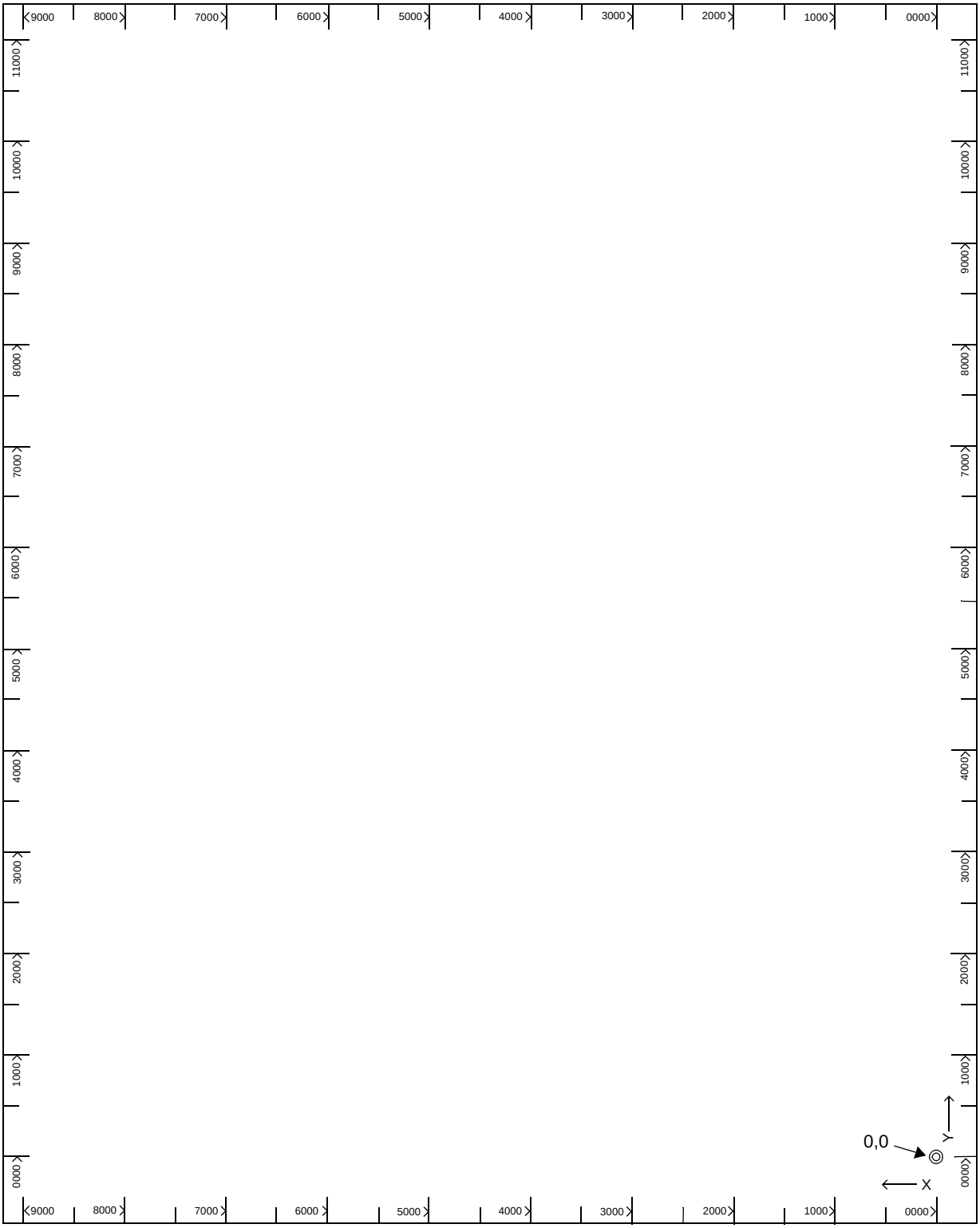


Figure 12-3. Board Location Grid—Bottom View

12.2 Bills of Materials

The following tables identify all of the components and tools that are associated with the board.

Table 12-2. Auxiliary Materials in Kit

Schematic P/N	Qty Supplied	Description	Details
na	1	PC-133 SDRAM module	Package: 168-pin DIMM Vendor: Generic Vendor P/N:
na	1	ATX power supply	Package: ATX power supply Vendor: Avance Vendor P/N: IBM-150PFC
04H5457	1	AMD Flash EPROM 128KX8 120ns	Package: PLCCE32 Vendor: AMD Vendor P/N: AM29F040B-120JC V
na	1	Power Cap for timer module (Battery and crystal case is applied over U17)	Package: Vendor: Dallas Semiconductor Vendor P/N: DS9034PCX
na	6	Standard shunt, 2.54mm	Package: Vendor: AMP/Tyco Vendor P/N: 1-382811-6
na	9	Locking card support on base	Package: Vendor: Richo Vendor P/N: LCBCB-8-01
	1	IIC Serial PROM	Package: Vendor: SGA-Thomson Vendor P/N: M24C02 WBN6

Table 12-3. SDRAM Options

Qty Supplied	Description
1	16M x 64, 133MHz Package: 168-pin DIMM Vendor 1: Any generic PC-133 compatible SDRAM with an addressing mode supported by the PPC405EP Vendor 1 P/N: Vendor 2: Vendor 2 P/N: Location:

Table 12-4. Debugging Tools

Qty Supplied	Description
0	168-pin DIMM analysis probe Vendor 1: FuturePlus, Inc. Vendor 1 P/N: FS2320 Location:
0	64-bit PCI analysis probe (passive) Vendor 1: FuturePlus, Inc. Vendor 1 P/N: FS2005 Location:
0	High-density termination adapter Vendor 1: Hewlett-Packard Vendor 1 P/N: E5346A Location:

Table 12-5. Evaluation Board Bill of Materials

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
	0.1U	318	C4, C8, C14, C15, C17, C18, C20-C22, C24-C28, C31, C32, C34, C35, C39, C41, C45, C46, C50, C56, C58, C60, C62, C63, C65, C66, C69-C71, C73, C77-C79, C82-C89, C91, C92, C94, C99-C103, C106-C110, C112-C119, C121, C122, C125, C130, C131, C133-C136, C138, C140, C142, C144, C145, C148, C149, C152, C153, C155-C158, C161, C162, C164, C176-C178, C180, C182, C183, C187, C189, C197, C198, C204, C205, C209, C210, C213, C214, C216-C219, C224-C226, C228, C230, C232, C237, C242, C243, C245, C248-C252, C254-C260, C265, C268, C281, C284-C286, C288-C291, C293-C304, C306-C308, C310, C313, C314, C316, C317, C319-C324, C326, C328-C337, C339, C341-C365, C367-C374, C376, C377, C379-C480	SMEC0603	KEMET	C0603C104Z3VAC	TDK	C1608Y5V1E104ZT	AVX	06033G104ZAT2A
	33U	56	C3, C5, C16, C29, C30, C33, C36, C37, C43, C47, C61, C64, C75, C96-C98, C111, C124, C126-C128, C132, C141, C147, C150, C154, C166, C175, C179, C186, C188, C190, C193-C196, C199-C203, C206-C208, C212, C215, C220-C223, C229, C231, C235, C236, C238, C246	SMEC2816R	SPRAGUE	293D336X0020D2T	NEC	NRD336M20RBM	AVX	TAJD336M020R
	100P	2	C67, C120	SMC2225_100	AVX	2225HA101JATRE	-	-	-	-
	100P	2	C72, C123	SMEC1206R	AVX	12061A101KAT2A	MURATA	GRM426C0G101K100AD	TDK	C3216C0G2A101KT
	0.0033U	6	C68, C74, C81, C129, C137, C143	SMEC0805R	AVX	08055C332KAT2A	KEMET	C0805C332K5RAC	TDK	C2012X7R1H332KT
	1K@100Mhz	16	C6, C7, C13, C38, C40, C42, C44, C48, C49, C51-C53, C55, C57, C59, C253	SMEC0603	FAIR-RITE CORP	2506031027Y0	VISHAY	ILBB-0603-1000	-	-
	0U	3	C139, C163, C375	SMC1206R	MURATA	BLM31A700S	-	-	-	-
	0.001U	4	C90, C146, C287, C309	SMEC0603	AVX	06035C102JAT2A	KEMET	C0603C102J5RAC	MURATA	GRM39X7R102J050AD
	33P	2	C171, C181	SMEC0805R	AVX	08055A330JAT2A	KEMET	C0805C330J5GAC	MURATA	GRM40C0G330J050AD
		2	C19, C23	SMEC2816R	DIGIKEY	283-2438-1-ND	Cooper-Bussmann	SFT-7	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
	100P	22	C9, C54, C261-C264, C266, C267, C269-C280, C282, C283	SMEC0603	PANASONIC	ECU-V1H101JCV	-	-	-	-
	10P	6	C76, C93, C292, C305, C315, C325	SMEC0603	AVX	06035A100JAT2A	KEMET	C0603C100J5GAC	MURATA	GRM39C0G100J050AD
	47P	1	C312	SMEC0805R	AVX	08055A470JAT2A	KEMET	C0805C470J5GAC	MURATA	GRM40C0G470J050AD
		6	DS1, DS3, DS6, DS9-DS11	SMC_LED3	PANASONIC	LN1351C	-	-	-	-
		3	DS2, DS7, DS8	SMC_LED3	PANASONIC	LN1251C	-	-	-	-
		2	DS4, DS5	SMC_LED3	PANASONIC	LN1451C	-	-	-	-
		2	F1, F3	FUSEBLK_2	DIGIKEY	F1227TR-ND	LITTLEFUSE	154004	-	-
		3	F2, F4, F5	FUSEBLK_2	DIGIKEY	F1222TR-ND	LITTLEFUSE	154001	-	-
		10	FL1-FL10	FILTER3216	TDK	HF70ACB-321611T	-	-	-	-
		6	J1, J3, J23, J34, J40, J43	BERG1X1	MOLEX	22-28-4010	-	-	-	-
		1	J10	CONN2X100_SMRECP_461	BERGSTAK	61082-202000	-	-	-	-
		10	J6, J9, J11, J21, J22, J24, J28, J30, J33, J41	BERG2X1	AMP	104350-1	-	-	-	-
		3	J8, J12, J29	CONN_MICTOR38	AMP	2-767004-2	-	-	-	-
		2	J13, J18	RJ45_L1X1_LED2	AMP	406549-4	-	-	-	-
		6	J2, J14, J15, J17, J25, J26	HDR1X3_MTA100	AMP	640452-3	-	-	-	-
		1	J16	DIMM_SOCKET_168_GENERIC	MOLEX	71251-0012	-	-	-	-
		2	J20, J39	SMA	AMP	221789-1	-	-	-	-
		1	J27	HDRM2X8_JTAGCLIP	THOMAS & BETTS	PS-16DS-WXA	-	-	-	-
		1	J31	VHEADER_2X10	3M	2520-6003-UB	-	-	-	-
		4	J35, J36, J38, J42	CEE2X60SV3_SPECIAL	AMP	145154-4	-	-	-	-
		1	J37	HDR2X5A	AMP	104352-5	-	-	-	-
		1	J4	CONN2X10_VHDR_PEGS	MOLEX	39-29-9202	-	-	-	-
		1	J7	DCONN9X2P_318	AMP	787920-1	-	-	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
		3	Q1-Q3	SOT23	ON SEMICONDUCTOR	BAS16LT1	ROHM	BAS16 SOT-23	-	-
		8	Q4-Q11	SOT23	SEMTECH	SLVU2.8TC	-	-	-	-
		4	Q12-Q15	SOT23	International Rectifier	IRLML6401	-	-	-	-
	10K	30	R9, R10, R18, R26, R31-R34, R45, R46, R57, R129, R131, R135, R183-R185, R215, R216, R221, R226, R240, R245, R258, R260, R296, R298, R338, R352, R382	SMER0805R	PANASONIC	ERJ6GEYJ103V	ROHM	MCR10EZHJ103	PHILIPS	232273061103
	1K	46	R6, R7, R11, R21, R40-R43, R47-R49, R54, R93, R94, R97, R99-R102, R163-R168, R206-R208, R211-R214, R219, R222, R223, R228, R241, R244, R246, R303, R311, R351, R364, R383, R409, R468	SMER0805R	ROHM	MCR10EZHJ102	PANASONIC	ERJ6GEYJ102V	PHILIPS	232273061102
	1.0K	4	R103, R104, R319, R328	SMER0603	PANASONIC	ERJ3GEYJ102V	-	-	-	-
	56	16	R39, R50, R52, R56, R105, R113, R116, R123, R145, R146, R151, R153, R154, R187, R346, R403	SMER0805R	PHILIPS	232273061560	PANASONIC	ERJ6GEYJ560V	ROHM	MCR10EZHJ560
	100	20	R12-R15, R22, R44, R75, R76, R106, R144, R209, R217, R218, R224, R225, R238, R239, R387, R395, R408	SMER0805R	PANASONIC	ERJ6ENF1000V	ROHM	MCR10EZHF1000	PHILIPS	232273461001
	205	2	R107, R156	SMER0805R	PANASONIC	ERJ6ENF2050V	-	-	-	-
	0	32	R108, R130, R134, R140, R142, R152, R155, R158, R322, R324, R327, R396, R405-R407, R410, R412-R418, R424, R425, R436, R438, R446, R452, R453, R465, R466	SMER0603	ROHM	MCR03EZHJ000	PHILIPS	232270296001	PANASONIC	ERJ3GEYOR00V
	10K	30	R110, R112, R117, R127, R334, R337, R341, R345, R348, R350, R354, R358-R361, R366, R367, R370, R372, R374, R376, R378, R384, R389, R390, R392, R398-R400, R402	SMER0402	PANASONIC	ERJ2GEJ103X	PHYCOMP	9C1A04021002JLHF3	-	-
	31.6	10	R111, R115, R118, R124, R128, R343, R347, R353, R357, R388	SMER0603	PANASONIC	ERJ3EKF31R6V	PHYCOMP	9C06031A31R6FKHFT	-	-
	392	1	R114	SMER0805R	PANASONIC	ERJ6ENF3920V	-	-	-	-
	127	1	R125	SMER0805R	PANASONIC	ERJ6ENF1270V	-	-	-	-
	232	1	R126	SMER0805R	PANASONIC	ERJ6ENF2320V	-	-	-	-
	10K	15	R137, R171-R176, R178, R180, R249, R250, R362, R379-R381	SMER0603	PANASONIC	ERJ3GEYJ103V	-	-	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
	48.70	5	R143, R147-R150	SMER0805R	PHILIPS	232273464879	PANASONIC	ERJ6ENF48R7V	ROHM	MCR10EZHF48R7
	62	3	R157, R182, R186	SMER0805R	PANASONIC	ERJ6GEYJ620V	ROHM	MCR10EZHJ620	PHILIPS	232273061629
	78.7	1	R159	SMER0805R	PANASONIC	ERJ6ENF78R7V	PHYCOMP	9C08052A78R7FKHFT	-	-
	100	12	R16, R17, R19, R20, R23-R25, R27-R29, R160, R161	SMER0603	PANASONIC	ERJ3GEYJ101V	-	-	-	-
	5.1K	17	R162, R197, R419-R421, R429, R432-R434, R441, R448-R450, R455, R460-R462	SMER0805R	PHILIPS	232273061512	PANASONIC	ERJ6GEYJ512V	ROHM	MCR10EZHJ512
	0.0	22	R169, R333, R336, R344, R349, R356, R363, R365, R368, R369, R371, R373, R375, R377, R385, R386, R391, R393, R394, R397, R401, R404	SMER0402	PANASONIC	ERJ2GE0R00X	PHYCOMP	9C1A04020R00JLHF3	-	-
	200	15	R177, R179, R181, R220, R227, R233, R247, R248, R251, R277, R314, R340, R342, R355, R411	SMER0805R	PANASONIC	ERJ6GEYJ201V	PHILIPS	232273061201	ROHM	MCR10EZHJ201
	8.2K	25	R192-R196, R198-R201, R204, R205, R422, R428, R430, R431, R440, R442-R444, R447, R456-R458, R463, R469	SMER0805R	PANASONIC	ERJ6GEYJ822V	ROHM	MCR10EZHJ822	PHILIPS	232273061822
	49.90	16	R229-R232, R236, R237, R242, R243, R305-R307, R318, R326, R330-R332	SMER0805R	PANASONIC	ERJ6ENF49R9V	ROHM	MCR10EZHF49R9	PHILIPS	232273464999
	75	8	R234, R235, R316, R317, R427, R437, R445, R459	SMER0805R	PANASONIC	ERJ6ENF75R0V	ROHM	MCR10EZHF75R0	PHILIPS	232273467509
	24.90	64	R58-R67, R69-R74, R77-R92, R261-R276, R278-R293	SMER0603	PANASONIC	ERJ3EKF24R9V	PHILIPS	232270462499	ROHM	MCR03EZPFX24R9
	0U	1	R30	SMC1210	TDK	HF50ACB-322513-T	-	-	-	-
	6.8	5	R309, R310, R312, R313, R315	SMER0805R	PANASONIC	ERJ6GEYJ6R8V	PHYCOMP	9C08052A6R80JLHFT	-	-
	31.60	1	R339	SMER0805R	PANASONIC	ERJ6ENF31R6V	ROHM	MCR10EZHF31R6	PHILIPS	232273463169
	69.8K	2	R35, R96	SMER1206R	PHILIPS	232272466983	ROHM	MCR18EZHF6982	PANASONIC	ERJ8ENF6982V
	4.87K	2	R36, R98	SMER1206R	PHILIPS	232272464872	PANASONIC	ERJ8ENF4871V	ROHM	MCR18EZHF4871
	3.3M	2	R37, R95	A155N1100P2	DALE ELECTRONICS	RNX-3/4 3300KJM	-	-	-	-
	1.5K	1	R38	SMER1206R	PANASONIC	ERJ8ENF1501V	ROHM	MCR18EZHF1501	PHILIPS	232272461502
		2	RN1, RN2	SOE14RN_330	DALE ELECTRONICS	SOMC1401103G	CTS	768141103G	-	-
	100	2	RV1, RV2	SM_POT	BOURNS	3214W-1-101W	-	-	-	-
		3	S1-S3	SPDTF	APEM	A2216	-	-	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
		1	S4	DIP_SMCSWITCH8	GRAYHILL	90HBW08PR	-	-	-	-
		2	T1, T2	SOG16T_540_H235	PULSE	PE-H1086	-	-	-	-
		92	TP1, TP8, TP9, TP11-TP16, TP18-TP100	TP	DO NOT ORDER	DO NOT ORDER	-	-	-	-
		8	TP2-TP7, TP10, TP17	EHOLE	DO NOT ORDER	DO NOT ORDER	-	-	-	-
		1	U1	SOE14_280R	FAIRCHILD	MM74HC74AMX	MOTOROLA	MC74HC74AD	-	-
		2	U10, U43	SOE14_280R	FAIRCHILD	74LCX125M	-	-	-	-
		2	U5, U11	SSOP28P65_212	TI	SN75LV4737A	-	-	-	-
		1	U12	SOT223A	DALLAS SEMI	DS1233DZ-10 SOT-223	-	-	-	-
		1	U13	SOT223A	DALLAS SEMICONDUCTOR	DS1233AZ-10	-	-	-	-
		1	U15	TSSOP48P5	TEXAS INSTRUMENTS	SN74LVCH16245ADGGR	-	-	-	-
		4	U16, U25, U27, U36	SOE14_280R	PHILIPS	N74F125D-T	TEXAS INSTRUMENTS	SN74F125DR	FAIRCHILD	MM74F125MX
		1	U17	SOG34_PWRCAP	DALLAS	DS1743P	-	-	-	-
		1	U18	PLCCE32	AMP	3-822498-1	-	-	-	-
		1	U19	TSOP2_32	HITACHI	HM628512BLTT	-	-	-	-
		2	U2, U23	SOE14_280R	MOTOROLA	MC74LVX14D	-	-	-	-
		1	U20	SSOPE20P65	TI	74LVCH244ADB	-	-	-	-
		2	U7, U21	TSSOP14P65	PHILIPS	74LVC32APW-T	TEXAS INSTRUMENTS	SN74LVC32APWR	-	-
		1	U22	TSSOP14P65	NATIONAL	74LCX86MTC	-	-	-	-
		2	U24, U32	QFPE80P65	NATIONAL	DP83843VJE	-	-	-	-
		2	U29, U39	SOE14_280R	PHILIPS	N74F06D-T	-	-	-	-
		1	U3	SOE14_280R	TEXAS INSTRUMENTS	SN74ALS04BDR	-	-	-	-
		1	U30	TQFP32P8	MOTOROLA	MPC961CFA	-	-	-	-
	C9531AT	1	U34	TSSOP28_P65	IMI	C9531AT				
		1	U35	EPBGA23X23_385	IBM	405D4	-	-	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
	CY2305	1	U37	SOE08_280R	CYPRESS	CY2305SC-1H	CYPRESS	CY2305SI-1H	-	-
		1	U38	SOE16_280R	CYPRESS	CY2309NZSC-1H	-	-	-	-
		1	U4	SOE14_280R	TEXAS INSTRUMENTS	SN74F86DR	FAIRCHILD	74F86SCX	-	-
		2	U40, U49	TSSOP14P65	FAIRCHILD	FST3125MTC	-	-	-	-
		1	U42	TSSOP14P65	TEXAS INSTRUMENTS	74LVC08APWR	-	-	-	-
		3	U44, U45, U48	SOG24_400	FAIRCHILD	FST3384WM	-	-	-	-
		1	U46	QFPE100RP65	ALTERA	EPM7128SQC100-7	-	-	-	-
		2	U6, U8	TSSOP48P5	FAIRCHILD	74LCX16244MTD	TI	74LVC16244ADGGR	-	-
		1	U9	SOE14_280R	PHILIPS	74HC14D-T	FAIRCHILD	MM74HC14MX	-	-
		2	VR1, VR2	D2_PAK	LINEAR TECHNOLOGY	LT1085CM	-	-	-	-
	I2CPROMSOCKET	1	X1	DIP_SOCKET_8	AMP	2-382462-1	-	-	-	-
		1	Y1	SG636	EPSON	SG-636PCE-25.000MC0	-	-	-	-
	MA-306-33.3333M-C	1	Y2	MA306	EPSON	MA-306-33.3333M-C	-	-	-	-
TRUE	0.1U	18	C1, C2, C10-C12, C159, C160, C165, C167-C169, C233, C234, C239-C241, C244, C247	SMEC0603	KEMET	C0603C104Z3VAC	TDK	C1608Y5V1E104ZT	AVX	06033G104ZAT2A
TRUE	100P	22	C80, C95, C104, C105, C151, C170, C172-C174, C184, C185, C191, C192, C211, C227, C311, C318, C327, C338, C340, C366, C378	SMEC0603	PANASONIC	ECU-V1H101JCV	-	-	-	-
TRUE	50	10	FID1-FID10	CARDFID						
TRUE	0U	9	R1, R3, R4, R136, R138, R141, R189, R202, R203	SMC1210	TDK	HF50ACB-322513-T	-	-	-	-
TRUE	0	34	R2, R5, R8, R68, R109, R132, R133, R139, R188, R190, R191, R210, R252-R255, R297, R299-R302, R304, R308, R321, R323, R325, R423, R426, R435, R439, R451, R454, R464, R467	SMER0603	ROHM	MCR03EZHJ000	PHILIPS	232270296001	PANASONIC	ERJ3GEYOR00V
TRUE	10K	9	R119-R122, R256, R257, R259, R294, R295	SMER0805R	PANASONIC	ERJ6GEYJ103V	ROHM	MCR10EZHJ103	PHILIPS	232273061103
TRUE	0.0	1	R170	SMER0402	PANASONIC	ERJ2GE0R00X	PHYCOMP	9C1A04020R00JLHF3	-	-

Table 12-5. Evaluation Board Bill of Materials (cont.)

DNP	Value	Qty	Ref Des	JEDEC Type	Vendor	Vendor PN	ALT1 Vendor	ALT1 Vendor PN	ALT2 Vendor	ALT2 Vendor PN
TRUE	10K	2	R320, R329	SMER0402	PANASONIC	ERJ2GEJ103X	PHYCOMP	9C1A04021002JLHF3	-	-
TRUE	49.90	1	R335	SMER0805R	PANASONIC	ERJ6ENF49R9V	ROHM	MCR10EZHF49R9	PHILIPS	232273464999
TRUE	1K	3	R51, R53, R55	SMER0805R	ROHM	MCR10EZHJ102	PANASONIC	ERJ6GEYJ102V	PHILIPS	232273061102
TRUE		7	U14, U26, U28, U31, U33, U41, U47	SCOPEJACK	JOHNSON	129-0701-201	-	-	-	-
TOTAL		1204								

Index

Inside of back cover

©International Business Machines Corporation 2000, 2002

Printed in the United States of America 11/26/02

All Rights Reserved

The information contained in this document is subject to change without notice. The products described in this document are NOT intended for use in applications such as implantation, life support, or other hazardous uses where malfunction could result in death, bodily injury, or catastrophic property damage. The information contained in this document does not affect or change IBM's product specifications or warranties. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. All information contained in this document was obtained in specific environments, and is presented as illustration. The results obtained in other operating environments may vary.

While the information contained herein is believed to be accurate, such information is preliminary, and should not be relied upon for accuracy or completeness, and no representations or warranties of accuracy or completeness are made.

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROVIDED ON AN "AS IS" BASIS. In no event will IBM be liable for any damages arising directly or indirectly from any use of the information contained in this document.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6531

The IBM home page can be found at **http://www.ibm.com**

The IBM Microelectronics Division home page can be found at **http://www.chips.ibm.com**

Address technical questions about this product to **ppcsupp@us.ibm.com**

Document Number: SA14-2686-03